DS87C530
EPROM Micro with Real-Time Clock

REVISION A4 ERRATA

The errata listed below describe situations where DS87C530 revision A4 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS87C530 revision A4 components. Revision A4 components are branded on the topside of the package with a six-digit code in the form yywwA4, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS87C530 die revision, visit our website at www.maxim-ic.com/errata.

1. $\overline{\text{PSEN}}$ PIN TOGGLES CONTINUOUSLY

Description:
The $\overline{\text{PSEN}}$ pin toggles regardless of whether internal or external program memory is used. The function description of this pin indicates that it should be inactive during internal program execution.

Work Around:
None.

2. WRITES TO SCONx REGISTER CAN CORRUPT SERIAL OPERATION IN PROGRESS

Description:
SPTA0 and SPRA0 bits may not show the correct state if a write to SCON0 is performed during reception or transmission of a character on serial port 0. Also, SPTA1 and SPRA1 bits may not show the correct state if a write to SCON1 is performed during reception or transmission of character on serial port 1.

Work Around:
Prior to writing to either SCON, verify that there is no activity on the serial port by reading the appropriate SPTA and SPRA bits.

3. SERIAL PORTS EXHIBIT VOLTAGE SENSITIVITY

Description:
At voltages below 4.25V, serial ports 0 and 1 operating in modes 1, 2, or 3 may not properly detect a false start bit, causing the device to erroneously detect the start of a serial reception.

Work Around:
Operate the device V_{CC} as close as possible to 5.0V.

4. SERIAL PORTS MAY VIOLATE t_{QVXL} SPECIFICATION

Description:
The serial port operating in mode 0 may violate the t_{QVXL} spec when the external crystal speed is above 25MHz.

Work Around:
Use only the rising edge of the clock to latch output data if the external crystal speed is above 25MHz.

5. IN-SYSTEM DISABLE (ISD) MODE MAY ACCIDENTALLY SET EPROM LOCK BITS

Description:
The device may erroneously set one or more EPROM lock bits when exiting In-System Disable (ISD) mode. This could cause a device with an unlocked EPROM to become locked.

Work Around:
None.

6. ALE, $\overline{\text{PSEN}}$ SIGNALS DRIVEN LOW IN IN-SYSTEM DISABLE (ISD) MODE

Description:
In In-System Disable (ISD) mode, ALE and $\overline{\text{PSEN}}$ are pulled low. The functional description of these pins in this mode states they should be held weakly high.

Work Around:
None.

7. WRITES TO CKCON SFR CAN CORRUPT WATCHDOG TIMER COUNT

Description:
Modifying the Clock Control Register (CKCON; 8Eh) while the watchdog timer is enabled can advance the watchdog time count by a random amount. This could result in an inaccurate watchdog timer period. This will not occur if the current watchdog time-out period is already set to its maximum count (WD1:0=11; CKCON7:6).

Work Around:
If the watchdog timer is enabled, reset the watchdog timer via the RWT bit (WDCON.0) before accessing the CKCON register. This will prevent an unexpected early time-out of the watchdog timer.

8. SHORT RESET DURING MOVX INSTRUCTION CAUSES INITIAL WEAK ALE SIGNAL

Description:
When a short reset stimulus occurs during the execution of an extended MOVX data memory access, the ALE signal may not be driven with the strong transition drivers (V_{OH2} test levels) on the first instruction fetch following reset. This reduced drive current may not allow the ALE signal to rise to a logic high level before the first instruction fetch at location 0000h, possibly latching an incorrect address. This situation will only occur during a watchdog timer reset (the timer generates a momentary pulse to the internal reset circuitry) or when an external reset pulse of less than 2μs is asserted. This erratum does not affect a power-on reset as the internal crystal warm-up period counter provides a reset pulse of greater than 2μs.

Work Around:
If the watchdog timer reset function is employed, use the watchdog timer interrupt to ensure that the device will not be executing MOVX instructions when the watchdog timer reset occurs. If an external reset stimulus is used, be sure that it is at least 2μs in duration.

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