DS89C420
Ultra-High-Speed Microcontroller

REVISION A2 ERRATA

The errata listed below describe situations where DS89C420 revision A2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS89C420 revision A2 components. Revision A2 components are branded on the top side of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS89C420 die revision, visit the website at www.maxim-ic.com/errata.

1. P3.7 MUST BE HIGH WHEN ENTERING OR EXITING LOADER MODE

Description:
To enter loader mode, port pin P3.7 must be pulled high when the pin combination of RST = 1, $\overline{PSEN}$ = $\overline{EA}$ = 0 is applied. When exiting loader mode, port pin P3.7 must be pulled high before the pin combination of RST = 1, $\overline{PSEN}$ = $\overline{EA}$ = 0 is released.

Work Around:
None

2. MOVC INSTRUCTIONS IN INTERNAL SRAM FAIL IF PRAME = 1

Description:
MOVC instructions executed from internal SRAM (locations 0400h–07FFh) when the internal SRAM is configured as program memory (PRAME = 1) do not execute correctly.

Work Around:
None

3. WRITES TO PARALLEL I/O PORTS MAY BE DELAYED 1 CLOCK CYCLE

Description:
Under some circumstances, writes to parallel I/O ports can be delayed 1 clock cycle. In most cases, this has no effect on system operation. If the immediately following instruction reads that modified port, however, the read instruction may read the port before its output value has changed. This behavior would differ from that of the traditional 8051.

Work Around:
In most cases, none is necessary. If the application software incorporates the unlikely occurrence of a port write immediately followed by a read of that port, an NOP can be inserted between the two

instructions to incorporate sufficient delay to obviate the problem. This erratum will be fixed in the next revision.

4. STATE OF P2.5, P2.6, AND P2.7 ON POWER-ON RESET CAN AFFECT OPERATION

Description:

The device does not fetch from internal flash memory if all three port pins (P2.5, P2.6, and P2.7) are held low during a power-on reset.

Work Around:

When internal code fetching is desired ($\overline{EA}$ = 1), ensure that at least one of the three pins (P2.5, P2.6, or P2.7) is not being held low during a power-on reset.

5. READ-MODIFY-WRITE INSTRUCTIONS INCORRECTLY ACTIVATE STRONG PULLUP

Description:

Any read-modify-write (RMW) instruction that has P0, P1, P2, or P3 as its destination (such as ANL P0, #data) can incorrectly activate the strong internal pullup for two clock cycles. This only occurs if a pin is at a logic 0 state and the result of the RMW instruction writes a logic 1 to the corresponding bit in the port latch, even if the bit was previously 1. If external logic connected to that pin is holding it at a logic 0, the strong internal driver can cause the pin to glitch momentarily to a logic 1. This behavior contradicts the data sheet that indicates that the strong internal pullup should only be activated when a 0-to-1 transition is required on a port pin. A complete list of RMW instructions is contained in the *Ultra-High-Speed Flash Microcontroller User's Guide*.

Work Around:

When using a port pin as an input, always make certain that any external device driving a logic 0 can sink sufficient current to keep the pin voltage below +0.8V (V_{IL}) during the temporary activation of the internal pullup (V_{OH2}).

6. STATE OF LOCK BITS CAN INTERFERE WITH BOOTSTRAP LOADER

Description:

Bootstrap loader mode does not operate correctly if any of the lock bits (LB1, LB2, LB3) are set.

Work Around:

If any of the lock bits had been set by a previous session, erase the part using the K command, exit and re-enter the bootstrap loader mode. The part then accepts bootstrap loader commands correctly.

7. TIMERS 1 AND 2 CLOCKED BY EXTERNAL SIGNAL PRODUCE INCORRECT BAUD RATE

Description:

When timer/counter 1 or 2 are configured as a counter that is clocked by an external signal (TMOD.6 = 1 and/or T2CON.1 = 1), the baud rate for the serial ports is incorrect.

Work Around:

None. Configure timer/counter 1 or 2 as a timer that is clocked by an internal signal (TMOD.6 = 0 and/or T2CON.1 = 0) in order to produce the correct serial port baud rate.

8. MOVX INSTRUCTIONS ALWAYS GENERATE PAGE MISS IN PAGE MODE 1

Description:

When the Page Mode 1 external memory bus structure has been selected, MOVX operations executed from internal flash memory, which access external MOVX memory, always generate a page miss memory cycle, regardless of the external MOVX address.

Work Around:

None

9. POWER-DOWN SLEW RATE REQUIREMENT IN CRYSTAL MULTIPLIER MODE

Description:

The microcontroller may not reset itself following a brownout ($0.4 < V_{CC} < V_{RST}$) if the crystal multiplier mode (CTM = 1) is enabled.

Work Around:

Performing a full power-down ($V_{CC} = 0$) will clear the condition. In default (1 clock per machine cycle) mode, this erratum does not occur and no work around is required.

If the crystal multipler, in either 2X or 4X mode, is used, the device must be placed into default sysclk/1 mode before Vcc drops below Vrst. This can be done by using the power-fail interrupt as follows:

1.) Enable the power-fail interrupt before the crystal multipler is engaged. Do this by setting the EPFI (WDCON.5) bit anytime before the CTM bit is set.

2.) The first instruction at 0033h (the start of the power-fail interrupt service routine) must be ORL PMR, #80h. This deactivates the crystal multiplier and returns the device to default sysclk/1 mode. A user-defined power-fail interrupt service routine, if present, can follow. If no user-defined power-fail interrupt service routine is specified, the next instruction should be an endless loop.

10. LOCK BIT SECURITY LEVELS 1, 2, AND 3 DO NOT FUNCTION PROPERLY

Description:

Security levels 1, 2, and 3 do not function properly and may not prevent access to internal flash memory if external program memory is used.

Work Around:

Use security level 4 if internal flash memory protection is required.