19-5920; Rev 5/12

DS1323
3.3V Flexible Nonvolatile Controller with Lithium Battery Monitor

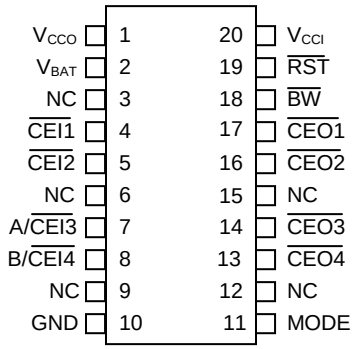
FEATURES

- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write-protects SRAM when V_{CC} is out of tolerance
- Automatically switches to battery backup when V_{CC} power failure occurs
- Flexible memory organization
  - Mode 0: 4 banks with 1 SRAM each
  - Mode 1: 2 banks with 2 SRAMs each
  - Mode 2: 1 bank with 4 SRAMs each
- Monitors voltage of a lithium cell and provides advanced warning of impending battery failure
- Signals low-battery condition on active low battery warning output signal
- Resets processor when power failure occurs and holds processor in reset during system power-up
- 10% power-fail detection
- Industrial temperature range of -40°C to +85°C

PIN DESCRIPTION

V_{CCI}	- +3.3V Power Supply Input
V_{CCO}	- SRAM Power Supply Output
V_{BAT}	- Backup Battery Input
A, B	- Address Inputs
$\overline{CEI1}$ - $\overline{CEI4}$	- Chip Enable Inputs
$\overline{CEO1}$ - $\overline{CEO4}$	- Chip Enable Outputs
$\overline{BW}$	- Battery Warning Output (Open Drain)
$\overline{RST}$	- Reset Output (Open Drain)
MODE	- Mode Input
GND	- Ground
NC	- No Connection

PIN ASSIGNMENT



DS1323E 20-Pin TSSOP
(173 mils)

DESCRIPTION

The DS1323 Flexible Nonvolatile Controller with Lithium Battery Monitor is a CMOS circuit that solves the application problem of converting CMOS SRAMs into nonvolatile memory. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, chip-enable outputs are inhibited to accomplish write protection and the battery is switched on to supply the SRAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. One DS1323 can support as many as four SRAMs arranged in any of three memory configurations.

In addition to battery-backup support, the DS1323 performs the important function of monitoring the remaining capacity of the lithium battery and providing a warning before the battery reaches end-of-life. Because the open-circuit voltage of a lithium backup battery remains relatively constant over the majority of its life, accurate battery monitoring requires loaded-battery voltage measurement. The DS1323 performs such measurement by periodically comparing the voltage of the battery as it supports an internal resistive load with a carefully selected reference voltage. If the battery voltage falls below the reference voltage under such conditions, the battery will soon reach end-of-life. As a result, the battery warning pin is activated to signal the need for battery replacement.

MEMORY BACKUP

The DS1323 performs all the circuit functions required to provide battery-backup for as many as four SRAMs. First, the device provides a switch to direct power from the battery or the system power supply (V_{CCI}). Whenever V_{CCI} is less than the V_{CCTP} trip point and V_{CCI} is less than the battery voltage V_{BAT}, the battery is switched on to provide backup power to the SRAM. This switch has voltage drop of less than 0.2 volts.

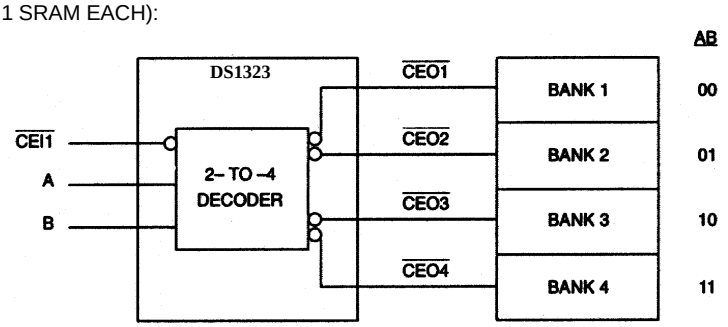
Second, the DS1323 handles power failure detection and SRAM write-protection. V_{CCI} is constantly monitored, and when the supply goes out of tolerance, a precision comparator detects power failure and inhibits the four chip enable outputs in order to write-protect the SRAMs. This is accomplished by holding $\overline{CEO1}$ through $\overline{CEO4}$ to within 0.2 volts of V_{CCO} when V_{CCI} is out of tolerance. If any $\overline{CEI}$ is active (low) at the time that power failure is detected, the corresponding $\overline{CEO}$ signal is kept low until the $\overline{CEI}$ signal is brought high again. Once the $\overline{CEI}$ signal is brought high, the $\overline{CEO}$ signal is taken high and held high until after V_{CCI} has returned to its nominal voltage level. If the $\overline{CEI}$ signal is not brought high by 1.5µs after power failure is detected, the corresponding $\overline{CEO}$ is forced high at that time. This specific scheme for delaying write protection for up to 1.5µs guarantees that any memory access in progress when power failure occurs will complete properly. Power failure detection occurs in the range of 2.8 to 3.0 volts.

MEMORY CONFIGURATIONS

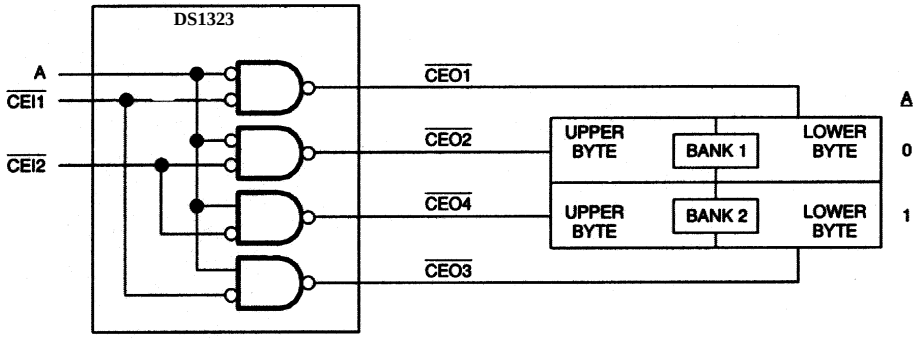
The DS1323 can be configured via the MODE pin for three different arrangements of the four attached SRAMs. The state of the MODE pin is latched at $V_{CCI} = V_{CCTP}$ on power-up. See Figure 1 for details.

MEMORY CONFIGURATIONS Figure 1

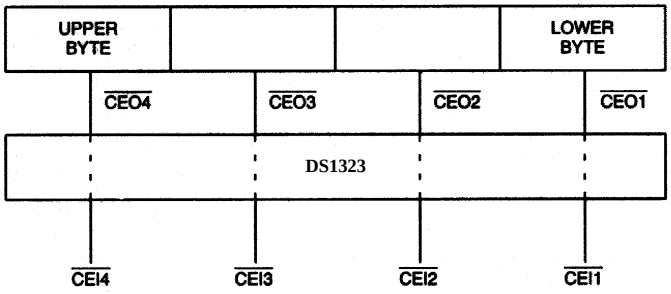
MODE = GND (4 BANKS WITH 1 SRAM EACH):



MODE = V_{CCO} (2 BANKS WITH 2 SRAM EACH):



MODE = Not Connected (1 BANK WITH 4 SRAMs):



BATTERY VOLTAGE MONITORING

The DS1323 automatically performs periodic battery voltage monitoring at a factory-programmed time interval of 24 hours. Such monitoring begins within t_{REC} after V_{CCI} rises above V_{CCTP} and is suspended when power failure occurs.

After each 24-hour period (t_{BTCN}) has elapsed, the DS1323 connects V_{BAT} to an internal 1MΩ test resistor (R_{INT}) for one second (t_{BTPW}). During this one second, if V_{BAT} falls below the factory-programmed battery voltage trip point (V_{BTP}), the battery warning output $\overline{BW}$ is asserted. While $\overline{BW}$ is active, battery testing will be performed with period t_{BTCW} to detect battery removal and replacement. Once asserted, $\overline{BW}$ remains active until the battery is physically removed and replaced by a fresh cell. The battery is still retested after each V_{CC} power-up, however, even if $\overline{BW}$ was active on power-down. If the battery is found to be higher than V_{BTP} during such testing, $\overline{BW}$ is deasserted and regular 24-hour testing resumes. $\overline{BW}$ has an open-drain output driver.

Battery replacement following $\overline{BW}$ activation is normally done with V_{CCI} nominal so that SRAM data is not lost. During battery replacement, the minimum time duration between old battery detachment and new battery attachment (t_{BDBA}) must be met or $\overline{BW}$ will not deactivate following attachment of the new battery. Should $\overline{BW}$ not deactivate for this reason, the new battery can be detached for t_{BDBA} and then re-attached to clear $\overline{BW}$.

NOTE: The DS1323 cannot constantly monitor an attached battery because such monitoring would drastically reduce the life of the battery. As a result, the DS1323 only tests the battery for one second out of every 24 hours and does not monitor the battery in any way between tests. If a good battery (one that has not been previously flagged with $\overline{BW}$) is removed between battery tests, the DS1323 may not immediately sense the removal and may not activate $\overline{BW}$ until the next scheduled battery test. If a battery is then reattached to the DS1323, the battery may not be tested until the next scheduled test.

NOTE: Battery monitoring is only a useful technique when testing can be done regularly over the entire life of a lithium battery. Because the DS1323 only performs battery monitoring when V_{CC} is nominal, systems which are powered down for excessively long periods can completely drain their lithium cells without receiving any advanced warning. To prevent such an occurrence, systems using the DS1323 battery monitoring feature should be powered up periodically (at least once every few months) in order to perform battery testing. Furthermore, anytime $\overline{BW}$ is activated on the first battery test after a power-up, data integrity should be checked via checksum or other technique.

POWER MONITORING

The DS1323 automatically detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CCI} falls below the trip point level in the range of 3.0 to 2.8 volts (10% tolerance) (V_{CCTP}), the V_{CCI} comparator activates the reset signal $\overline{RST}$.

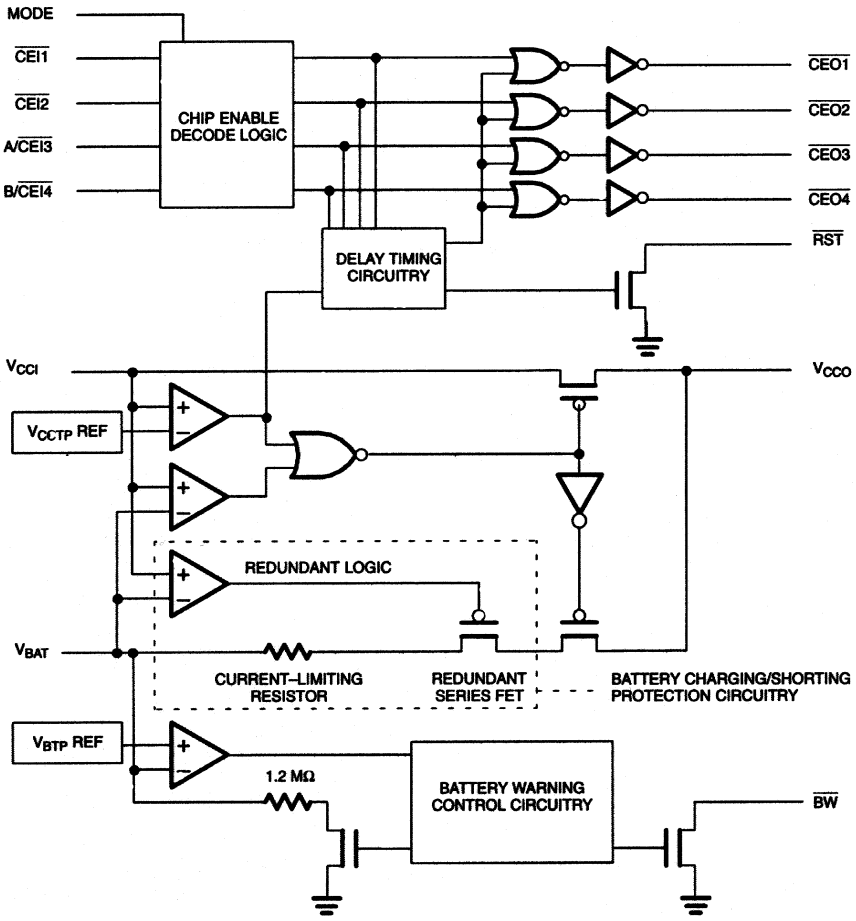
$\overline{RST}$ also serves as a power-on reset during power-up. After V_{CCI} exceeds V_{CCTP}, $\overline{RST}$ will be held active for 200ms nominal (t_{RPU}). This reset period is sufficiently long to prevent system operation during power-on transients and to allow t_{REC} to expire. $\overline{RST}$ has an open-drain output driver.

FRESHNESS SEAL MODE

When the battery is first attached to the DS1323 without V_{CC} power applied, the device does not immediately provide battery-backup power on V_{CCO}. Only after V_{CCI} exceeds V_{CCTP} will the DS1323 leave Freshness Seal Mode. This mode allows a battery to be attached during manufacturing but not used until

after the system has been activated for the first time. As a result, no battery energy is drained during storage and shipping.

FUNCTIONAL BLOCK DIAGRAM Figure 2



ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground..... -0.3V to +6.0V
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s)..... +300°C
Soldering Temperature (reflow) ..... +260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....73.8°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....20°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CCI}	3.0	3.3	3.6	V	2
Battery Supply Voltage	V_{BAT}	2.0		6.0	V	
Logic 1 Input	V_{IH}	2.0		V_{CCI}+0.3	V	3
Logic 0 Input	V_{IL}	-0.3		0.6	V	3

DC ELECTRICAL CHARACTERISTICS

($V_{CCI} \geq V_{CCTP}$, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC1}	TTL inputs		50	200	µA	4
Supply Current	I_{CC2}	CMOS inputs		30	100	µA	4, 5
RAM Supply Voltage	V_{CCO}		V_{CCI} -0.2			V	
RAM Supply Current	I_{CCO1}	$V_{CCO} \geq V_{CCI}$ - 0.2V			80	mA	
RAM Supply Current	I_{CCO2}	$V_{CCO} \geq V_{CCI}$ - 0.3V			140	mA	
V_{CC} Trip Point	V_{CCTP}		2.8	2.9	3.0	V	
V_{BAT} Trip Point	V_{BTP}		2.5	2.6	2.7	V	
Output Current	I_{OH}	2.2V	-1			mA	6, 7
Output Current	I_{OL}	0.4V			4	mA	6, 7
Input Leakage	I_{IL}		-1.0		+1.0	µA	
Output Leakage	I_{LO}		-1.0		+1.0	µA	
Battery Monitoring Test Load	R_{INT}		0.8	1.2	1.5	MΩ	

DC ELECTRICAL CHARACTERISTICS

($V_{CCI} < V_{BAT}$; $V_{CCI} < V_{CCTP}$, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Battery Current	I_{BAT}				100	nA	4
Battery Backup Current	I_{CCO3}	$V_{CCO} \geq V_{BAT}$ -0.2V			500	µA	
Supply Voltage	V_{CCO}		V_{BAT} -0.2			V	
$\overline{CEO}$ Output	V_{OHL}		V_{BAT} -0.2			V	8

CAPACITANCE

(T_A = +25°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance ($\overline{CEI}$, MODE)	C_{IN}			7	pF	
Output Capacitance ($\overline{CEO}$, $\overline{BW}$, $\overline{RST}$)	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

($V_{CCI} \geq V_{CCTP}$, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEI}$ to $\overline{CEO}$ Propagation Delay	t_{PD}		15	25	ns	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	9
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	10
V_{CC} Valid to $\overline{CEI}$ Inactive	t_{PU}			2	ms	
V_{CC} Valid to $\overline{RST}$ Inactive	t_{RPU}	150	200	350	ms	7
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	s	7

AC ELECTRICAL CHARACTERISTICS

($V_{CCI} < V_{CCTP}$, T_A = -40°C to +85°C.)

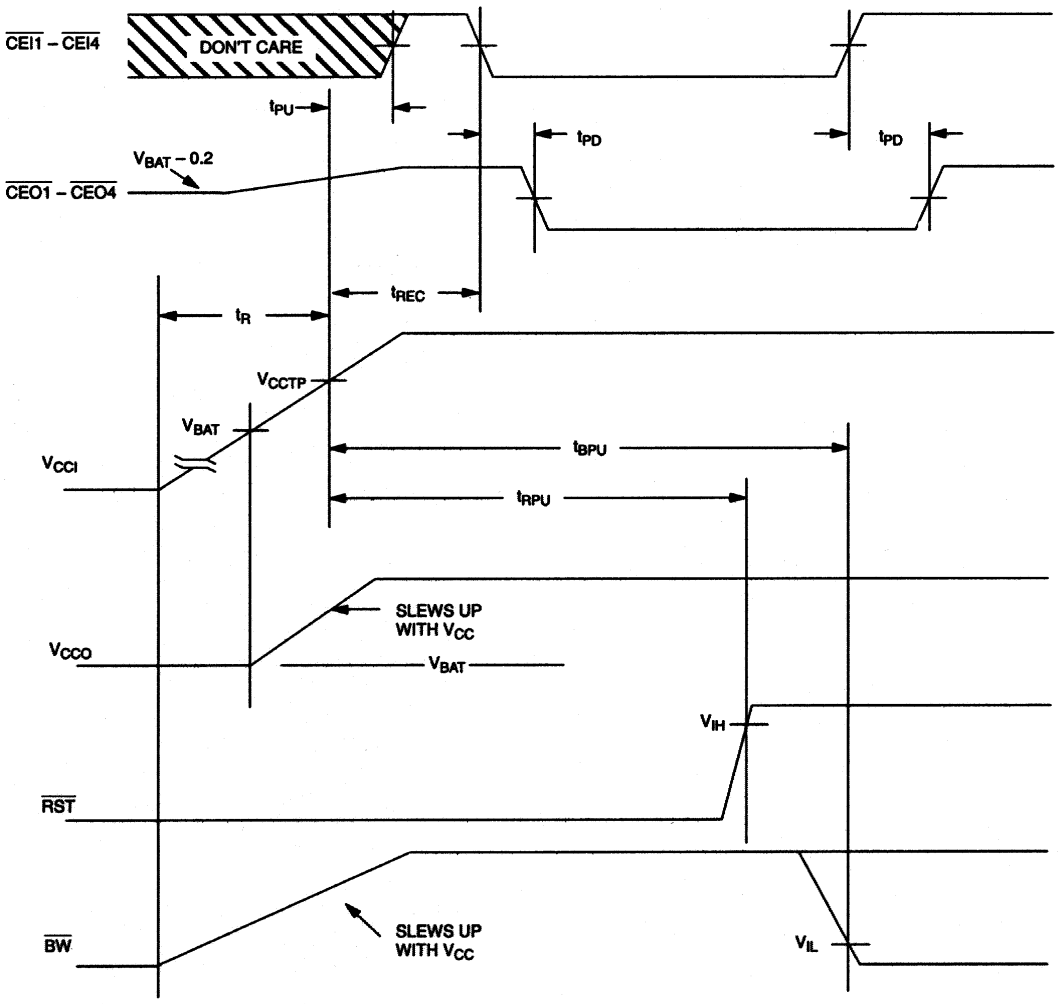
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Slew Rate	t_F	150			µs	
V_{CC} Fail Detect to $\overline{RST}$ Active	t_{RPD}			15	µs	7
V_{CC} Slew Rate	t_R	15			µs	

AC ELECTRICAL CHARACTERISTICS

($V_{CCI} \geq V_{CCTP}$, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Test to $\overline{BW}$ Active	t_{BW}			1	s	7
Battery Test Cycle-Normal	t_{BTCN}		24		hr	
Battery Test Cycle-Warning	t_{BTCW}		5		s	
Battery Test Pulse Width	t_{BTPW}			1	s	
Battery Detach to Battery Attach	t_{BDBA}	7			s	
Battery Attach to $\overline{BW}$ Inactive	t_{BABW}			1	s	7

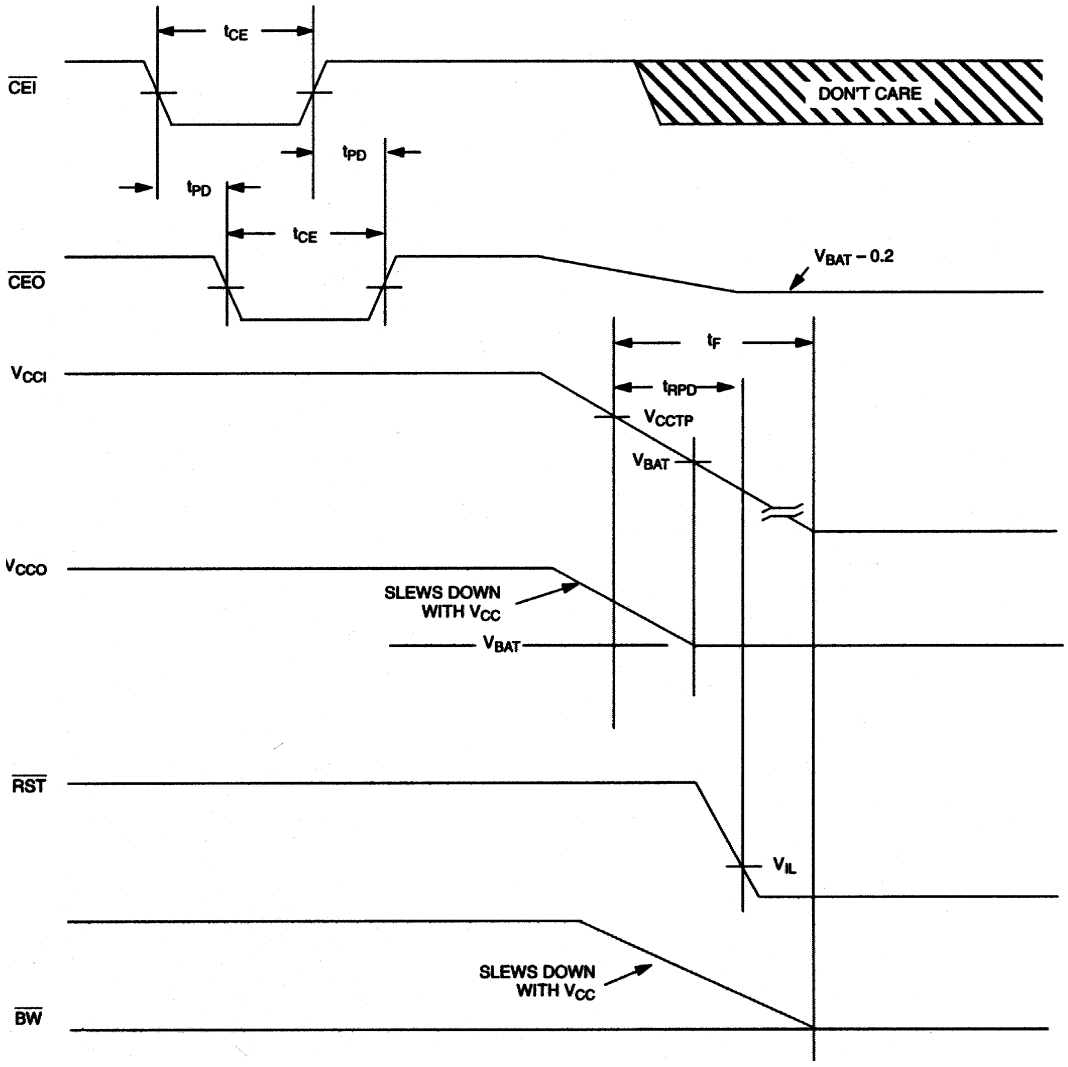
TIMING DIAGRAM: POWER-UP



NOTE:

If $V_{BAT} > V_{CCTP}$, V_{CCO} will begin to slew with V_{CCI} when $V_{CCI} = V_{CCTP}$.

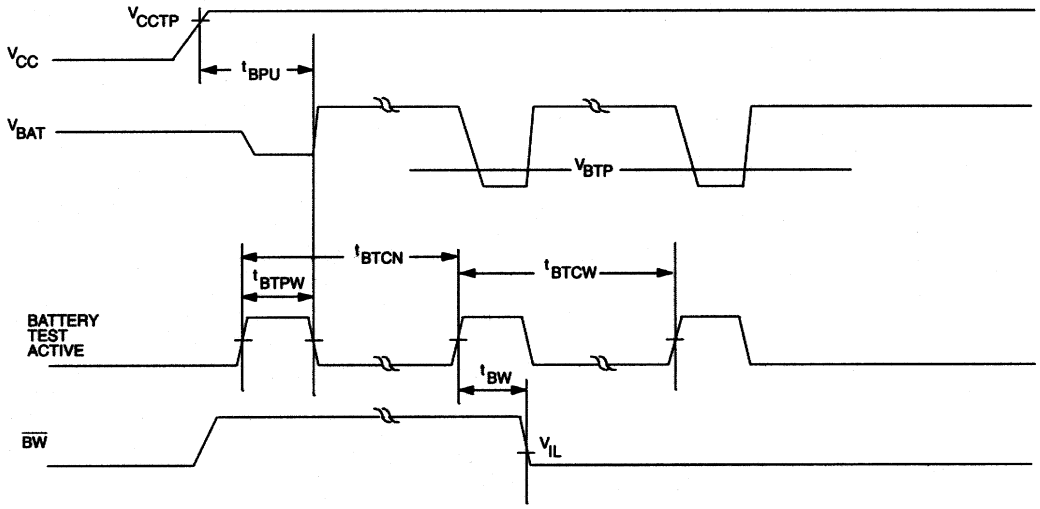
TIMING DIAGRAM: POWER-DOWN



NOTES:

If $V_{BAT} > V_{CCTP}$, V_{CCO} will slew down with V_{CCI} until $V_{CCI} = V_{CCTP}$.

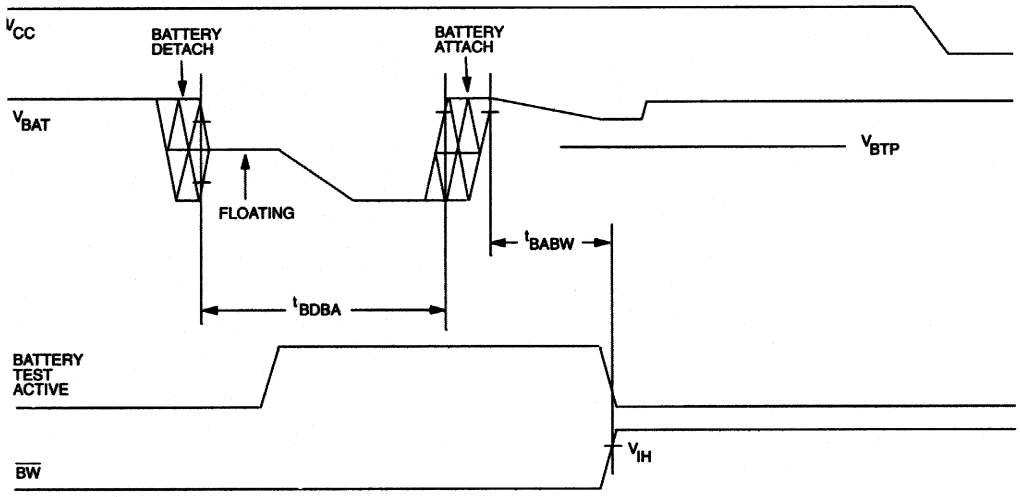
TIMING DIAGRAM: BATTERY WARNING DETECTION



NOTE:

t_{BW} is measured from the expiration of the internal timer to the activation of the battery warning output $\overline{BW}$.

TIMING DIAGRAM: BATTERY REPLACEMENT



NOTES:

2. All voltages referenced to ground.
3. In battery backup mode, inputs must never be below ground or above V_{CCO}.
4. Measured with outputs open.
5. All inputs within 0.3V of ground or V_{CCI}.
6. Measured with a load as shown in Figure 3.
7. $\overline{BW}$ and $\overline{RST}$ are open drain outputs and, as such, cannot source current. External pull-up resistors should be connected to these pins for proper operation. Both $\overline{BW}$ and $\overline{RST}$ can sink 10mA.
8. Chip Enable Outputs $\overline{CEO1}$ – $\overline{CEO4}$ can only sustain leakage current in the battery backup mode.
9. t_{CE} maximum must be met to ensure data integrity on power down.
10. $\overline{CEO1}$ through $\overline{CEO4}$ will be held high for a time equal to t_{REC} after V_{CCI} crosses V_{CCTP} on power-up.
11. The DS1323 is recognized by Underwriters Laboratories (UL) under file E99151.

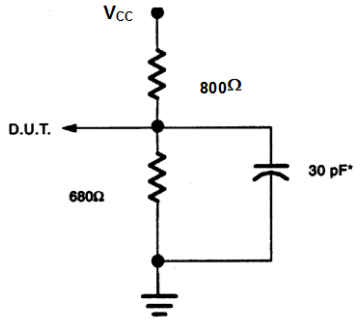
DC TEST CONDITIONS

Outputs Open
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: See below
Input Pulse Levels: 0 – 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

OUTPUT LOAD Figure 3

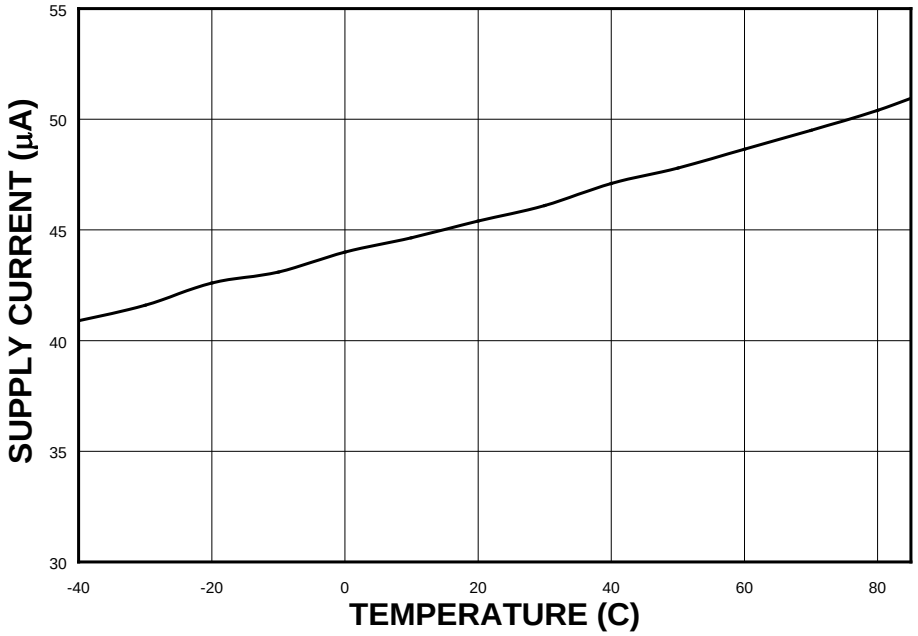


*INCLUDING SCOPE AND JIG CAPACITANCE

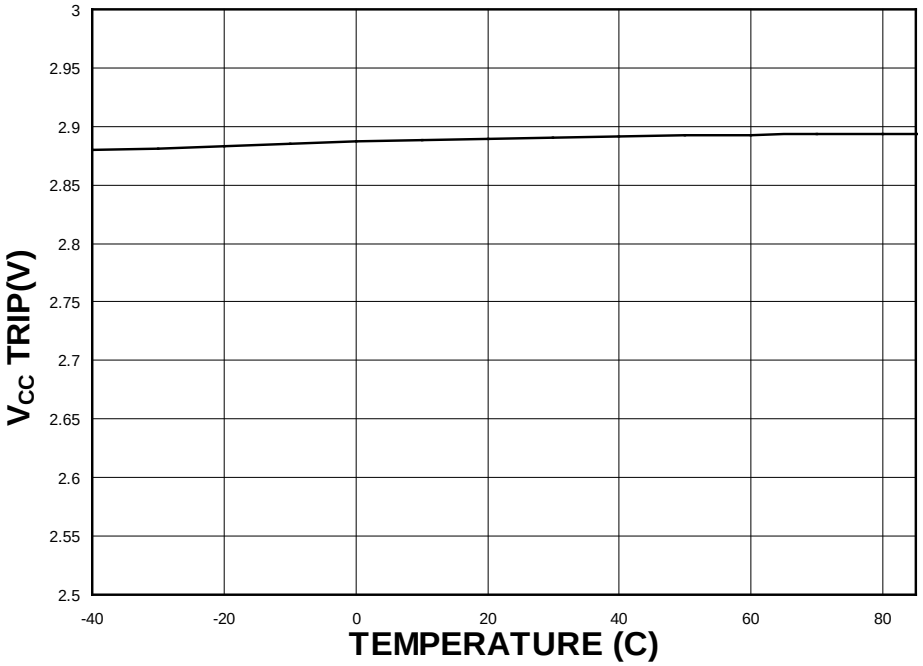
TYPICAL OPERATING CHARACTERISTICS

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified.)

SUPPLY CURRENT vs. TEMPERATURE



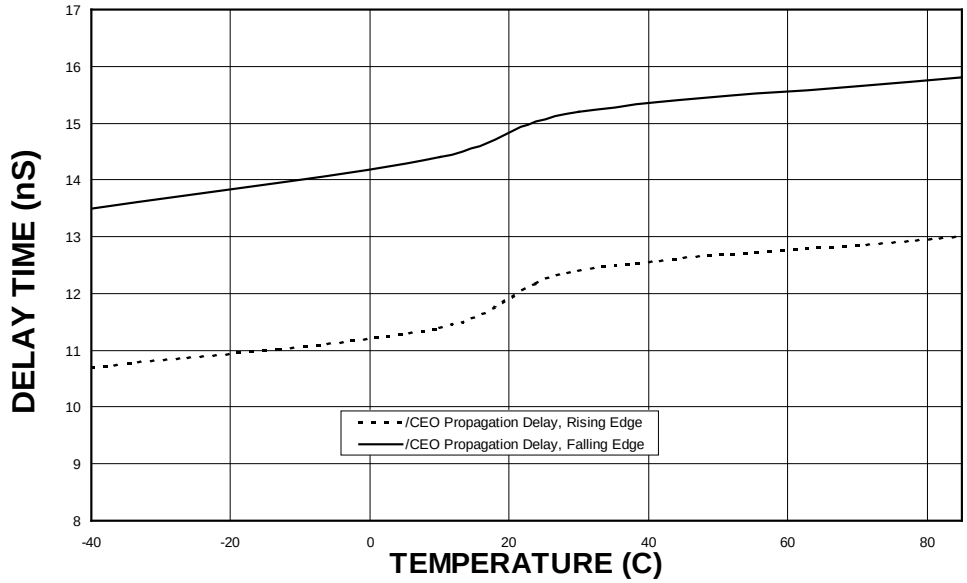
V_{CC} TRIP vs. TEMPERATURE



TYPICAL OPERATING CHARACTERISTICS (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified.)

/CE PROPAGATION DELAY vs. TEMPERATURE



ORDERING INFORMATION

PART	TEMP RANGE	OPERATING VOLTAGE (V)	PACKAGE TYPE
DS1323+	-40ºC to +85ºC	3.3	20 TSSOP
DS1323+T&R	-40ºC to +85ºC	3.3	20 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TSSOP	U20+1	**21-0066**	**90-0116**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
6/11	Deleted references to 16-pin DIP and 16-pin SO packages; updated the *Absolute Maximum Ratings* section; updated the *Recommended Operating Conditions*, *DC Electrical Characteristics*, *Capacitance*, *AC Electrical Characteristics* tables; updated *Notes*; updated the *Ordering Information* table; added the *Package Information* table	1, 3, 6, 7, 13
5/12	Corrected *Absolute Maximum Ratings* section for SA process; updated soldering information; added *Package Thermal Characteristics* section	6, 7, 11

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