DS3232M
ERRATA SHEET

Revision A1 Errata

The errata listed below describe situations where DS3232M revision A1 components perform differently than expected or differently than described in the data sheet. Maxim Integrated intends to correct these errata when the opportunity to redesign the product presents itself.

This errata sheet only applies to DS3232M revision A1 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively.

1) WRITING TO THE SRAM DATA SPACE CAN RESULT IN A 1Hz COUNTER CHAIN RESET, WHICH DELAYS THE SUBSEQUENT REAL-TIME DISPLAY BY A FRACTION OF 1 SECOND

Description:
When writing to the SRAM data space (14h–FFh), the 1Hz (1s) real-time clock counter chain can be reset, which delays the next increment of the clock registers.

Workaround:
Do not execute write cycles to SRAM memory locations if A2 = A1 = A0 = 0 (e.g., 18h, 20h, 28h, 30h, 38h, 40h, 48h, ..., F0h, or F8h).

19-6602; Rev 0; 4/13

maxim integrated™

DS3232M
REV A1 ERRATA

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/13	Initial release	—