DS4812
Low Voltage, High Slew Rate, Rail-To-Rail Dual Op-Amp

FEATURES

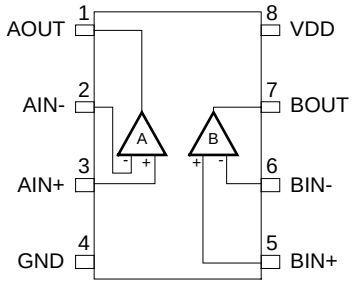
- High Slew Rate: 10V/µs
- High Gain Bandwidth: 6.5 MHz
- Supply Voltage Range 2.5 to 5.5V
- Rail-to-Rail Output Swing
- 1.75 mA Supply Current per Channel

ORDERING INFORMATION

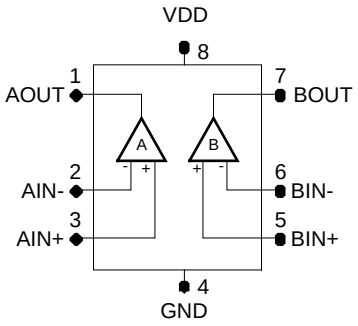
Part Number	Description
DS4812	8-pin DIP
DS4812S	8-pin SOIC
DS4812U	8-pin µ-SOP
DS4812X	8-bump CSP

For mechanical dimensions see web site.

PACKAGES/PINOUTS



300-mil DIP
150-mil SOIC
118-mil µ-SOP



8-bump CSP

DESCRIPTION

The DS4812 BiCMOS dual operational amplifier combines high slew rate and rail-to-rail output swing. The device provides 10V/µs of slew rate and 6.5 MHz of bandwidth while only consuming 1.5 mA of supply current per channel. Ideal low voltage BiFET substitute for low gain, high speed applications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} (see Note 1).....5.5V

Differential Input Voltage (see Note 2)....± V_{DD}

Input Voltage Range, V_I(see Note 1) .....-0.3V to V_{DD}

Input Current, I_{DD}.....± 4 mA

Output Current, I_O.....± 50 mA

Total current into V_{DD}.....± 50 mA

Total current out of GND.....± 50 mA

Duration of short-circuit current (See Note 3) unlimited

Operating Temperature .....0 ^oC to +70 ^oC

Storage Temperature.....-55 ^oC to +125 ^oC

Soldering Temperature.....See J-STD-020A Specification

NOTES:

1. Relative to GND.
2. Non-inverting input relative to inverting input. Excessive current flows when input is brought below GND - 0.3V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	2.5		5.5	V	1
Input Voltage Range	V_I	0		V_{DD} - 1.7	V	1
Common-Mode Input Voltage	V_{CM}	0		V_{DD} - 1.7	V	
Free-Air Operating Temperature	T_A	0		70	^oC	

NOTES:

1. Voltage referenced to GND.

ELECTRICAL CHARACTERISTICS

Conditions: (T_A: 0°C – 70°C. V_{DD} = 3.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Offset Voltage (V_{IC} = 0.5V, R_S = 50Ω, V_{OUT} = 1.5V)	V_{IO}		1	5	mV	
Temperature Coefficient of Input Offset Voltage (V_{IC} = 0.5V, R_S = 50Ω, V_{OUT} = 1.5V)	αV_{IO}		10		µV/°C	
Input Offset Current (V_{IC} = 0.5V, R_S = 50Ω, V_{OUT} = 1.5V)	I_{IO}		1	500	pA	
Input Bias Current (V_{IC} = 0.5V, R_S = 50Ω, V_{OUT} = 1.5V)	I_{IB}		2	500	pA	
Common-mode Input Voltage Range $\|V_{IO}\| \leq 10$mV	V_{ICR}	0		1.3	V	
High Level Output Voltage (I_{OH} = -0.5 mA)	V_{OH}	2.5	2.8		V	
Low Level Output Voltage (I_{OL} = 0.5 mA)	V_{OL}		0.15	0.5	V	
Large Signal Differential Voltage Amplification (V_{IC} = 0.5V, R_L = 10 kΩ, 1V ≤ V_O ≤ 2V)	A_{VD}	60	68		dB	
Common Mode Input Capacitance	$c_{i(c)}$		4		pF	
Common Mode Rejection Ratio (0V ≤ V_{IC} ≤ 1.0V, V_O = 1.5V)	CMRR	40	50		dB	
Supply Voltage Rejection Ratio (3V ≤ V_{DD} ≤ 5V, V_{IC} = V_{DD}/2 – 1V, no load)	k_{SVR}	70	80		dB	
Amplifier Supply Current (per channel) (V_O = 1.5V, no load)	I_{DD}		1.5	2.5	mA	
Slew Rate at Unity Gain (C_L = 50 pF)	SR	5	7.5		V/µs	
Unity Gain Bandwidth (C_L = 50 pF)	UGBW		5.0		MHz	
Phase Margin at Unity Gain (C_L = 50 pF)	ϕ_M		54		Degree	
Gain Margin (C_L = 50 pF)			6		dB	

ELECTRICAL CHARACTERISTICS cont.

Conditions: (T_A: 0°C – 70°C. V_{DD} = 5.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Offset Voltage (V_{IC} = 1.5V, R_S = 50Ω, V_{OUT} = 2.5V)	V_{IO}		1	5	mV	
Temperature Coefficient of Input Offset Voltage (V_{IC} = 1.5V, R_S = 50Ω, V_{OUT} = 2.5V)	αV_{IO}		10		µV/°C	
Input Offset Current (V_{IC} = 1.5V, R_S = 50Ω, V_{OUT} = 2.5V)	I_{IO}		1	500	pA	
Input Bias Current (V_{IC} = 1.5V, R_S = 50Ω, V_{OUT} = 2.5V)	I_{IB}		2	500	pA	
Common-mode Input Voltage Range $\|V_{IO}\| \leq 10$ mV	V_{ICR}	0		3.3	V	
High Level Output Voltage (I_{OH} = -1.0 mA)	V_{OH}	4.5	4.8		V	
Low Level Output Voltage (I_{OL} = 1.0 mA)	V_{OL}		0.15	0.5	V	
Large Signal Differential Voltage Amplification (V_{IC} = 1.5V, R_L = 10 kΩ, 1.5V ≤ V_O ≤ 3.5V)	A_{VD}	60	72		dB	
Common Mode Input Capacitance	$c_{i(c)}$		4		pF	
Common Mode Rejection Ratio (0V ≤ V_{IC} ≤ 2.7V, V_O = 2.5V)	CMRR	45	55		dB	
Supply Voltage Rejection Ratio (3V ≤ V_{DD} ≤ 5V, V_{IC} = V_{DD}/2 – 1V, no load)	k_{SVR}	70	80		dB	
Amplifier Supply Current (per channel) (V_O = 2.5V, no load)	I_{DD}		1.75	2.5	mA	
Slew Rate at Unity Gain (C_L = 50 pF)	SR	7	10		V/µs	
Unity Gain Bandwidth (C_L = 50 pF)	UGBW		6.5		MHz	
Phase Margin at Unity Gain (C_L = 50 pF)	ϕ_M		46		Degree	
Gain Margin (C_L = 50 pF)			4		dB	

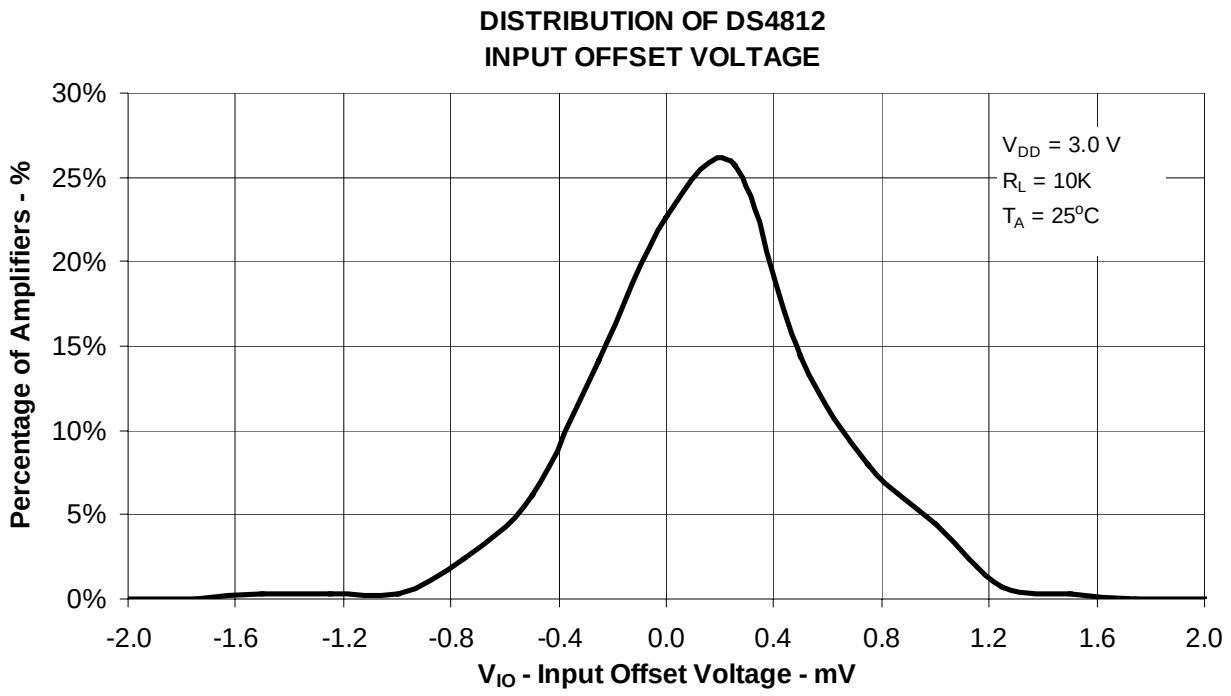


Figure 1.0

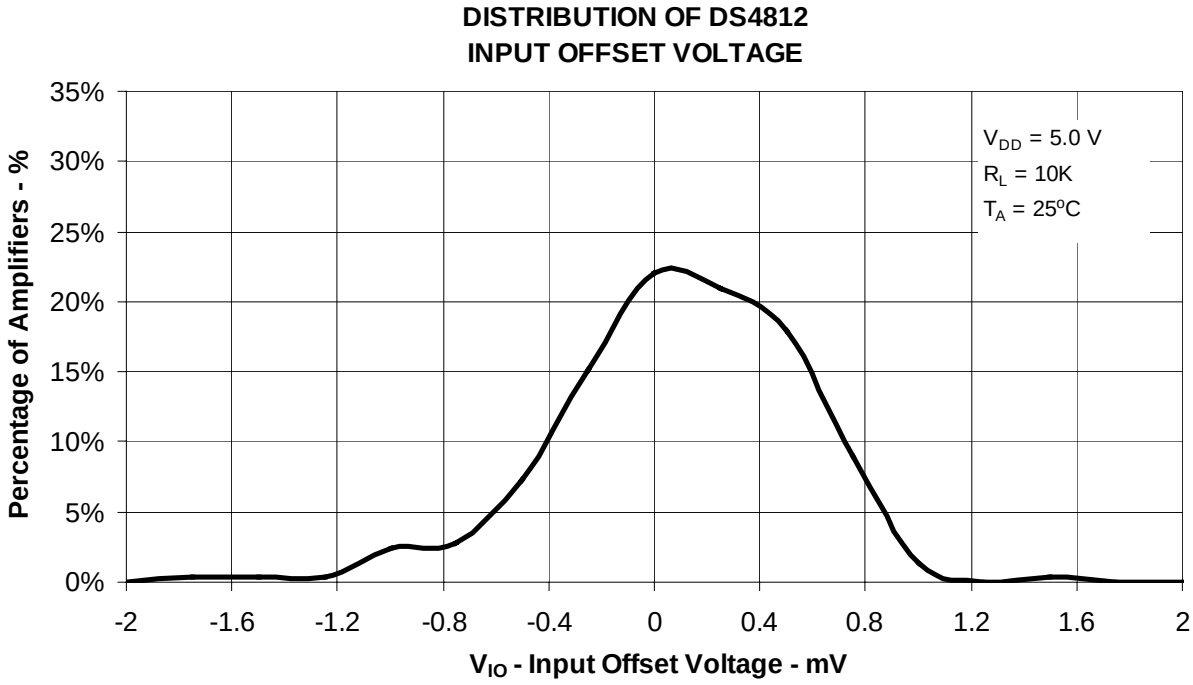


Figure 2.0

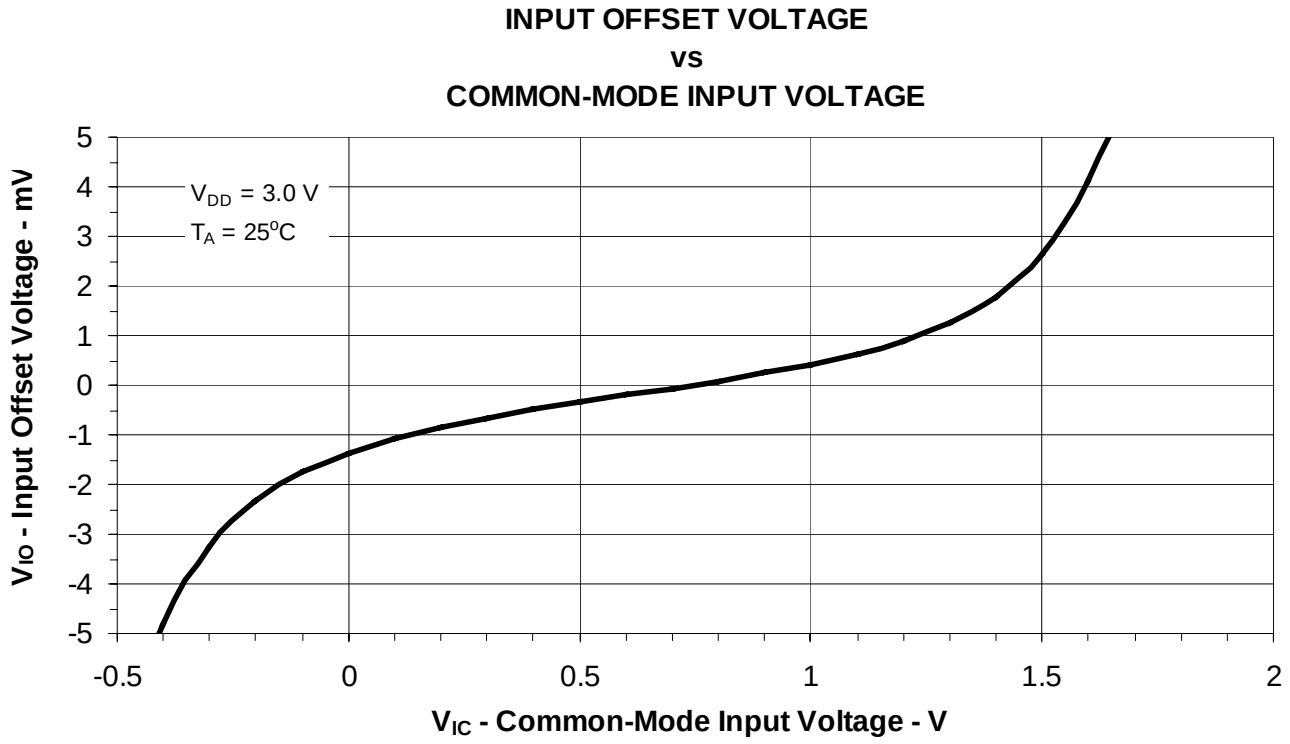


Figure 3.0

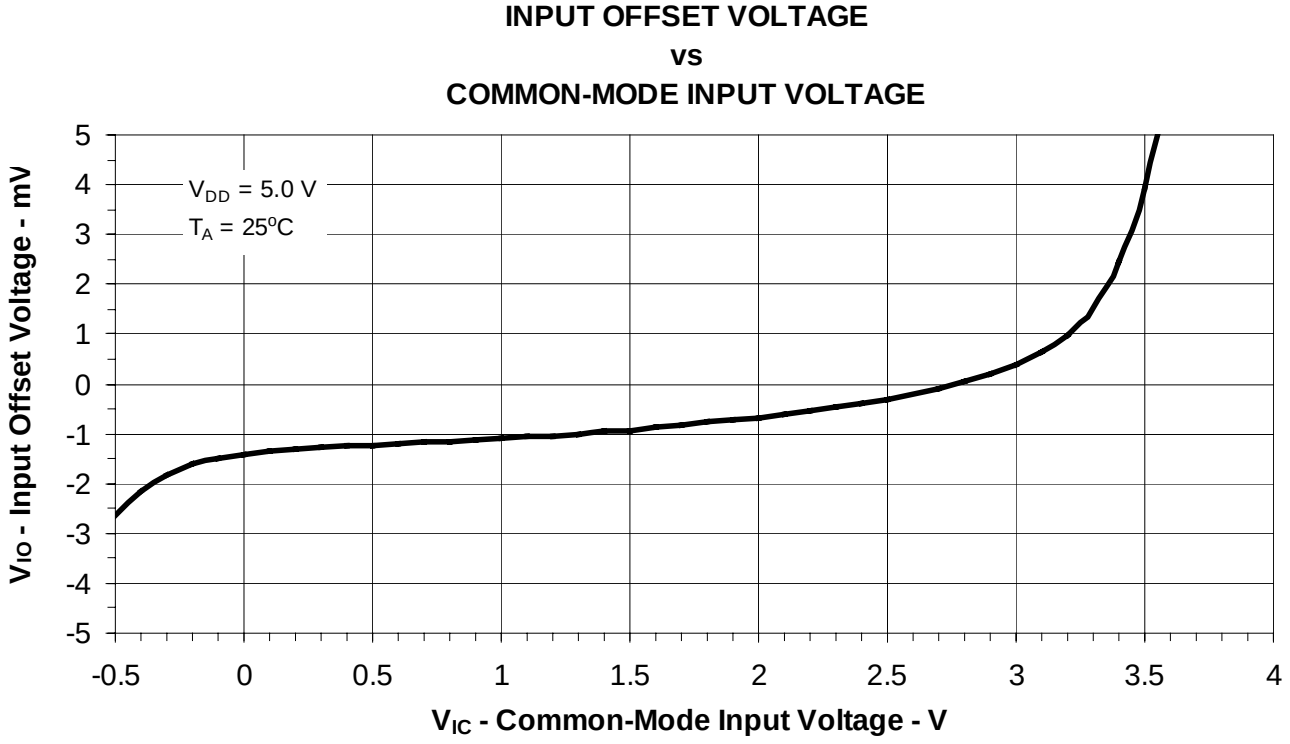


Figure 4.0

DISTRIBUTION OF DS4812
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

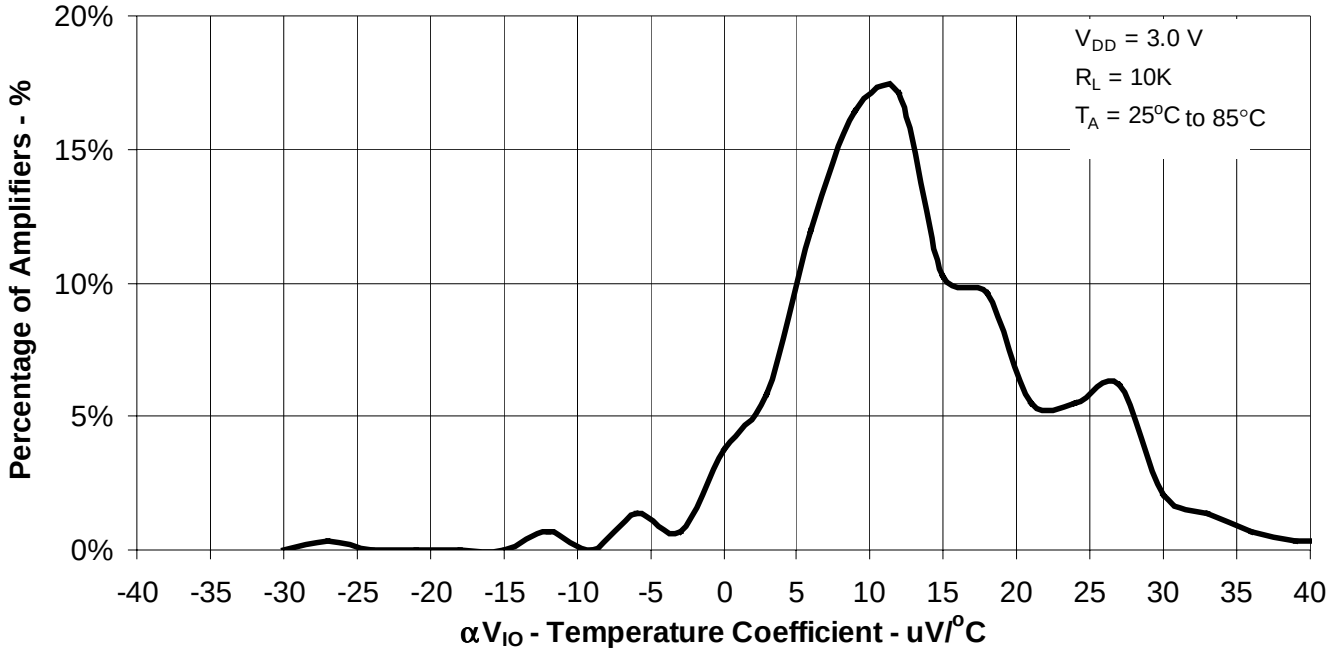
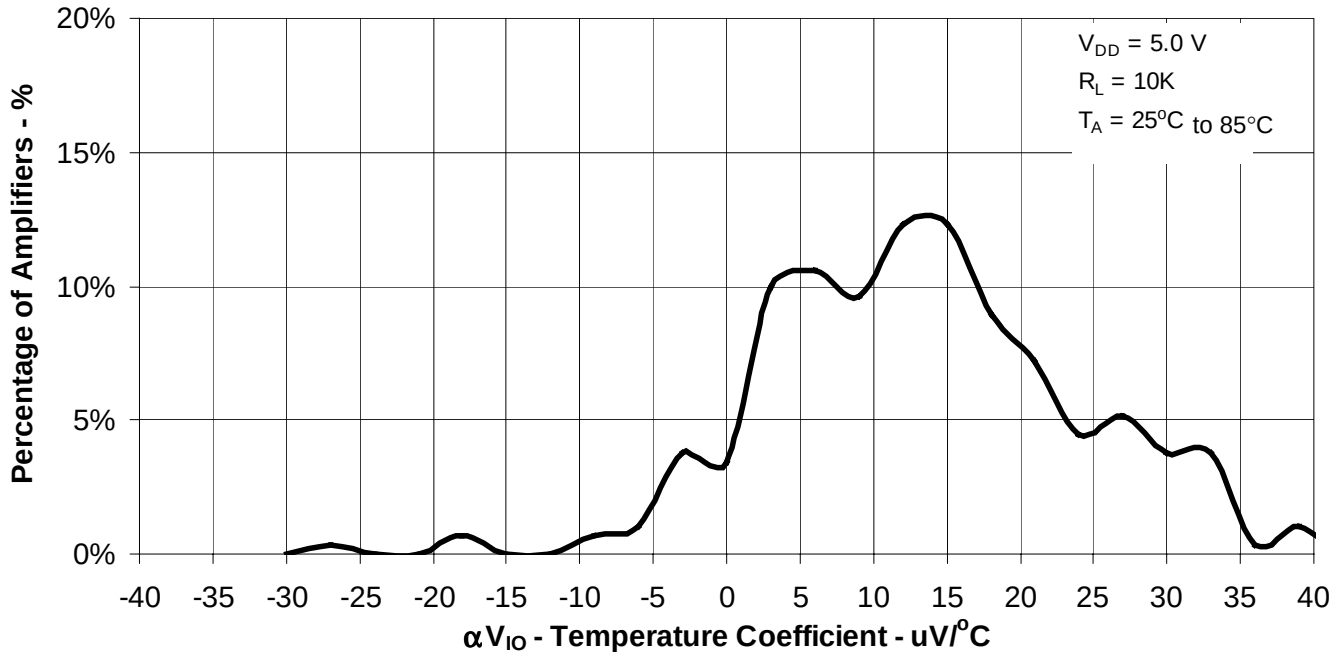


Figure 5.0

DISTRIBUTION OF DS4812
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT



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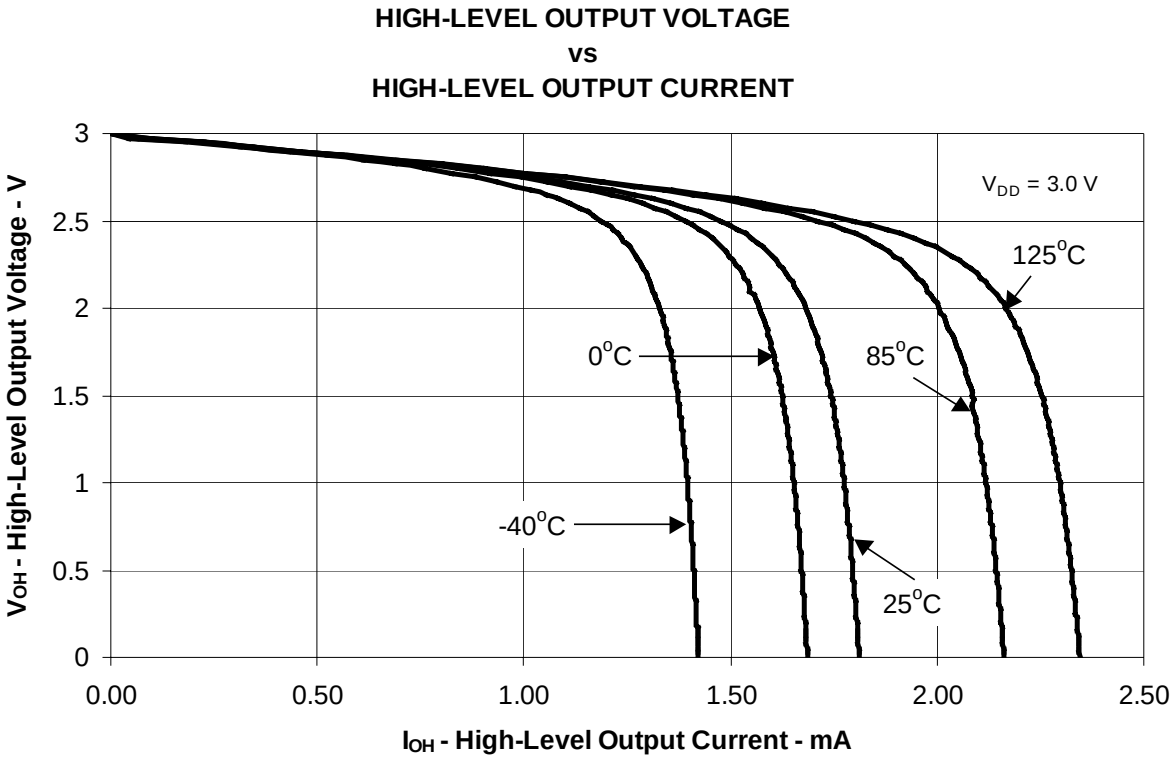


Figure 7.0

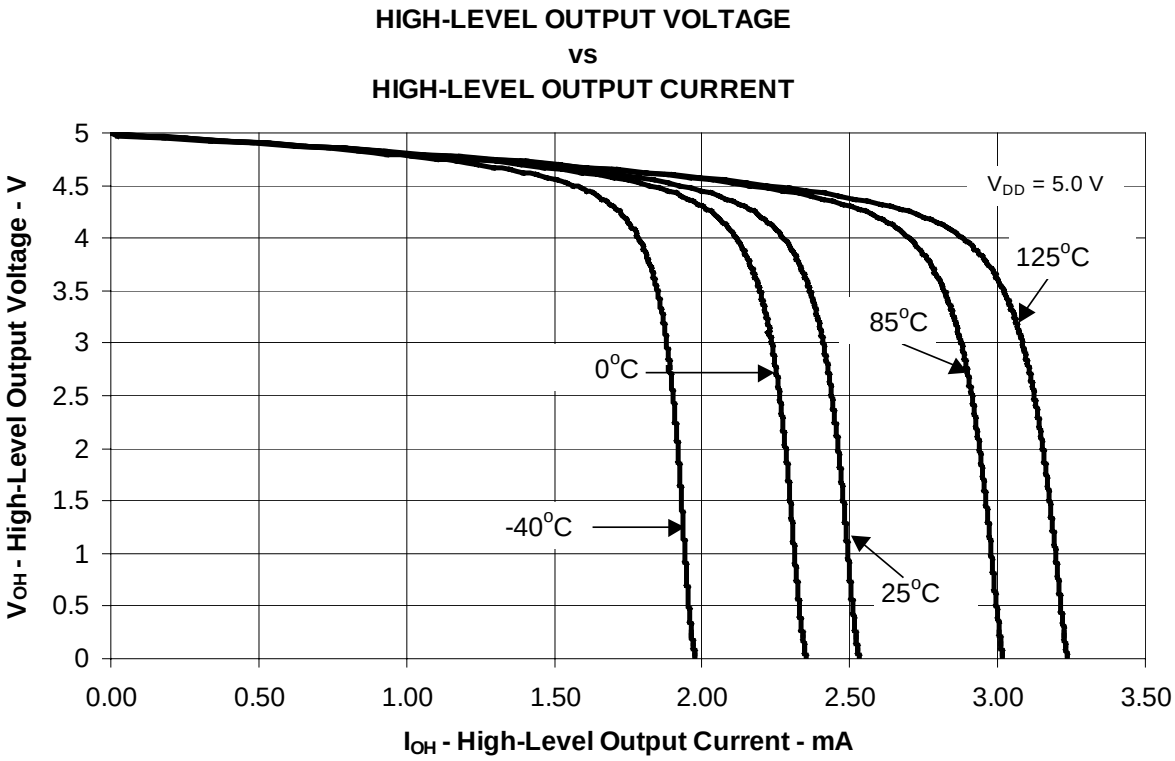


Figure 8.0

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

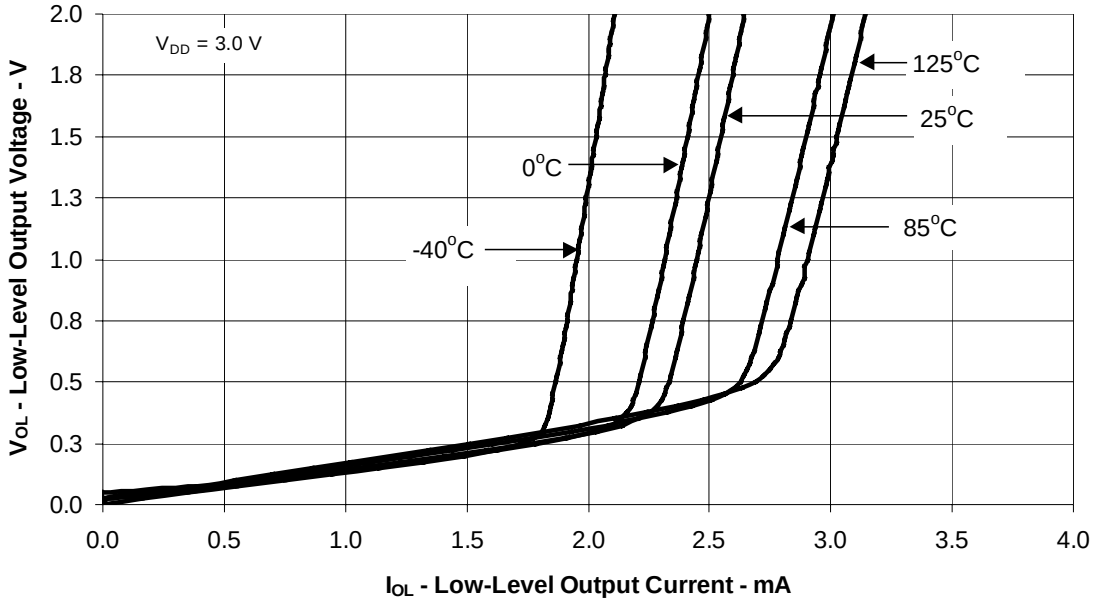


Figure 9.0

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

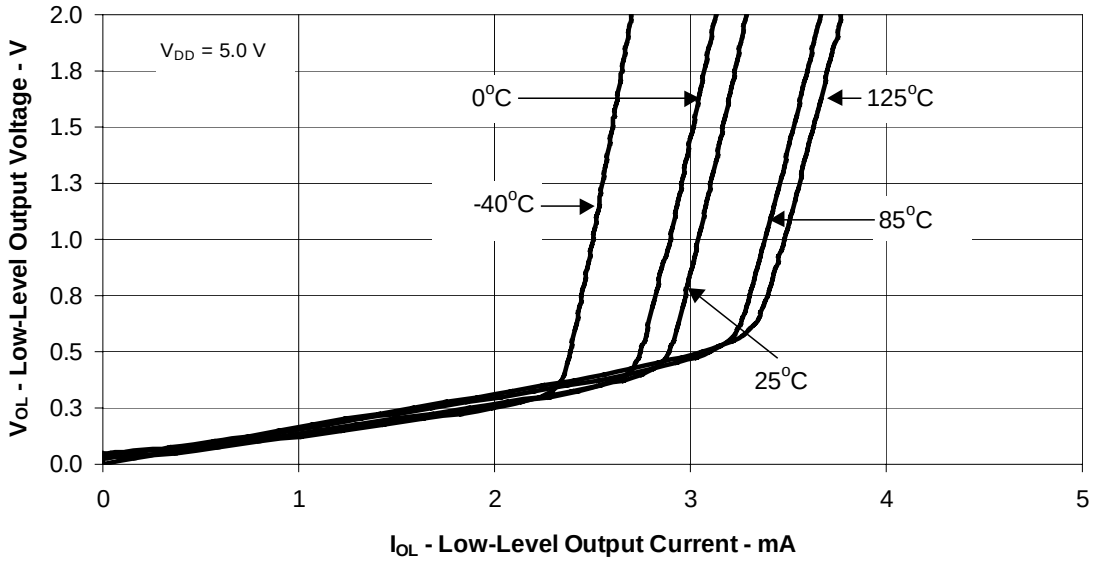


Figure 10.0

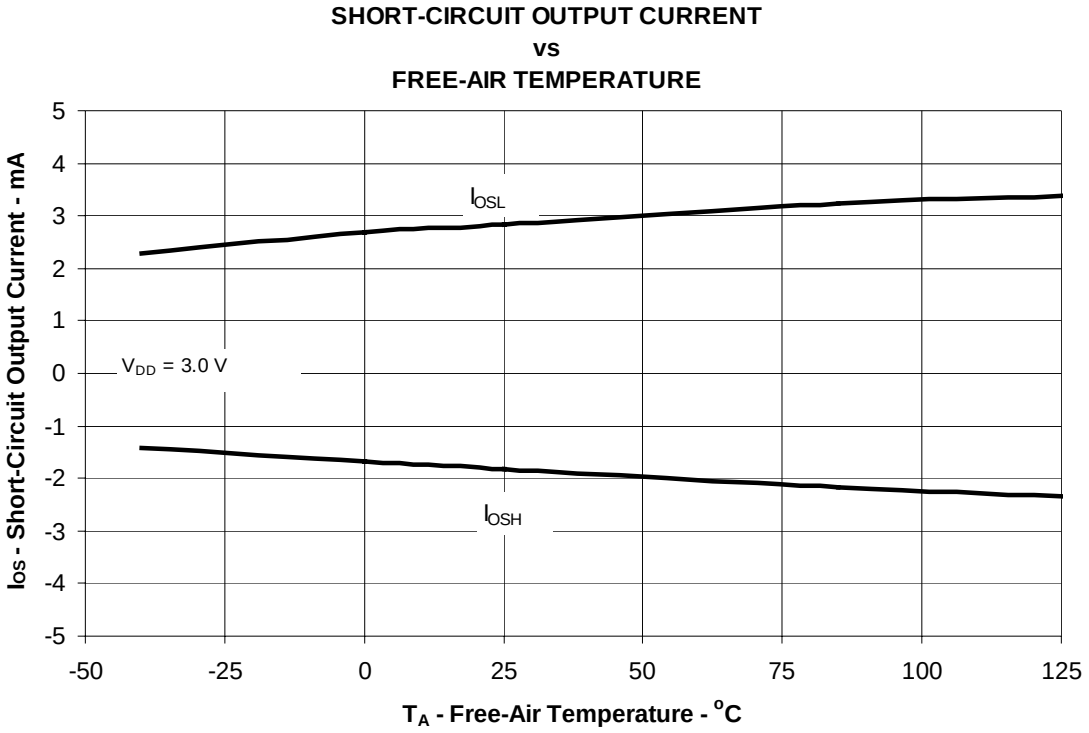


Figure 11.0

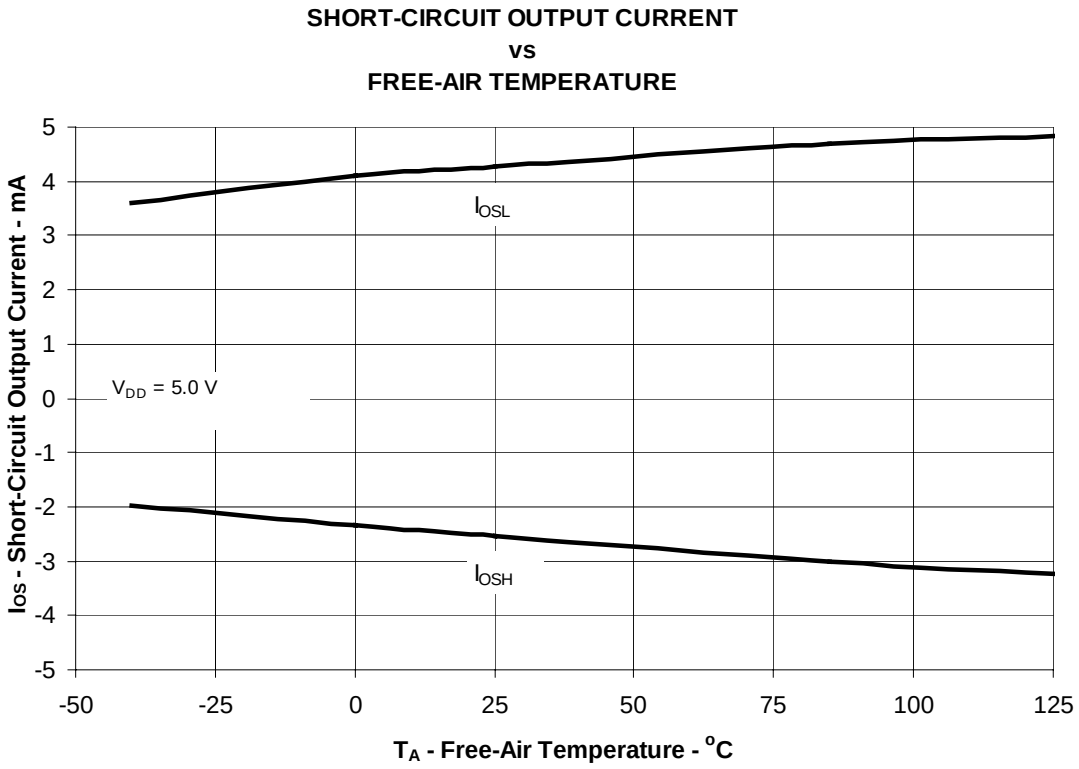


Figure 12.0

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

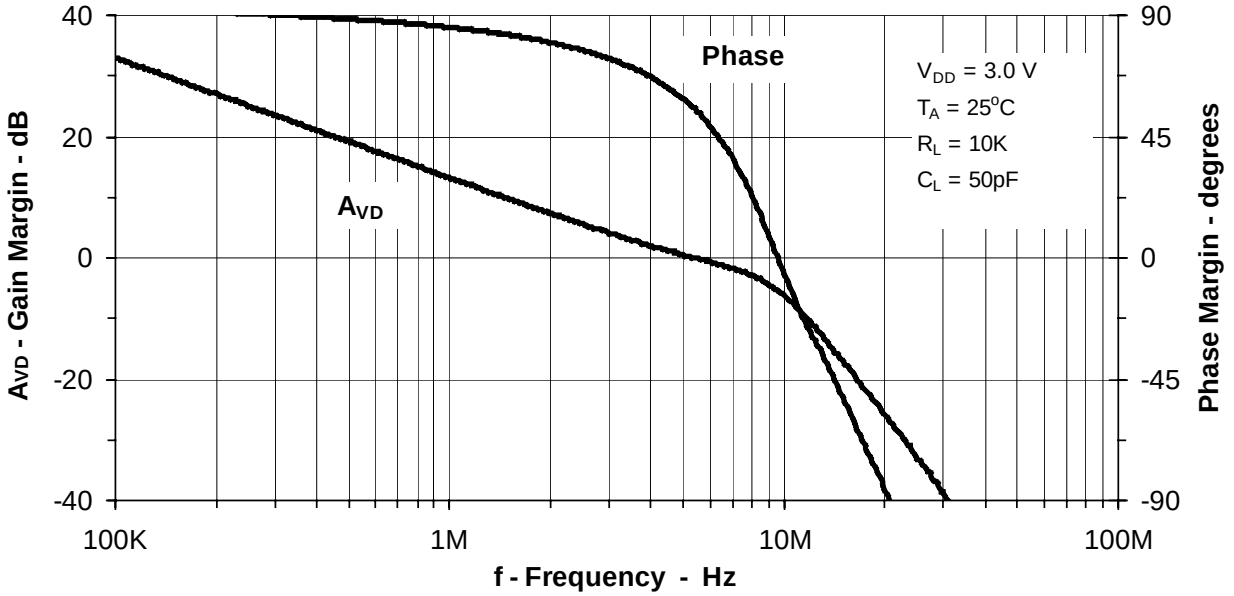


Figure 13.0

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

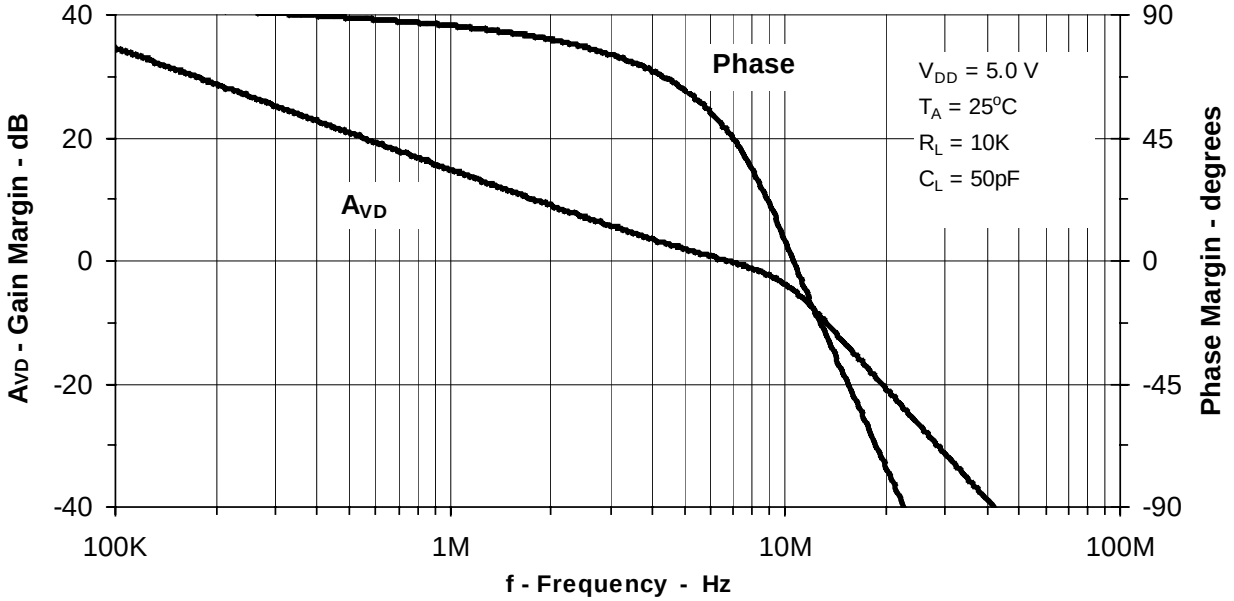


Figure 14.0

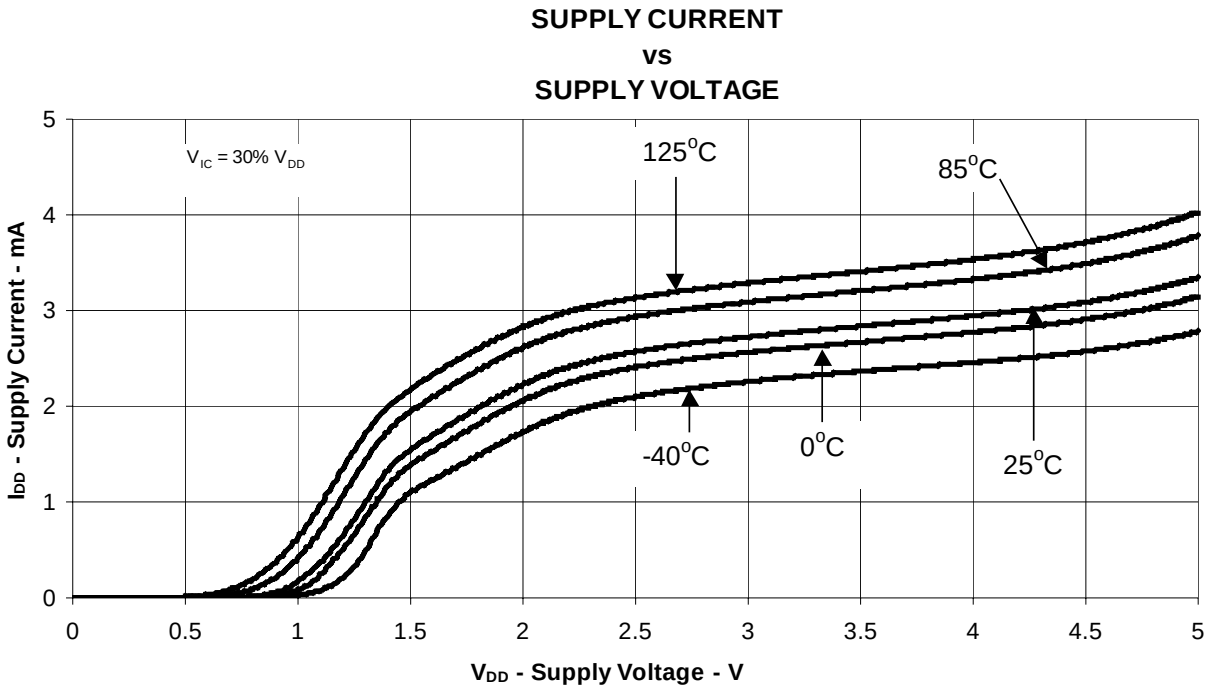
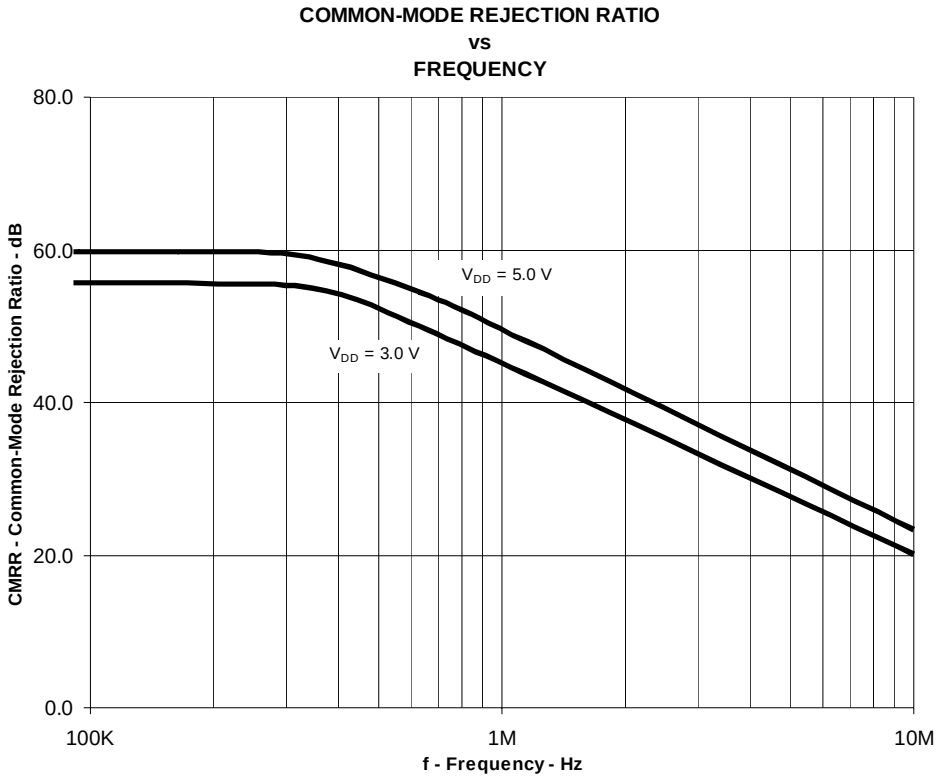


Figure 15.0



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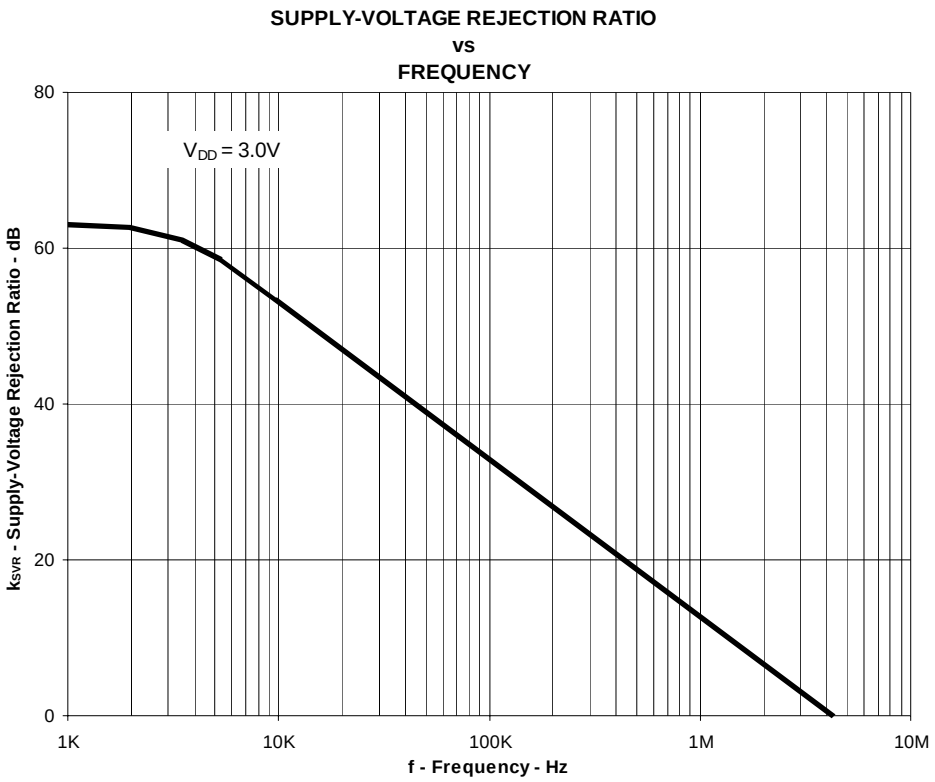


Figure 17.0

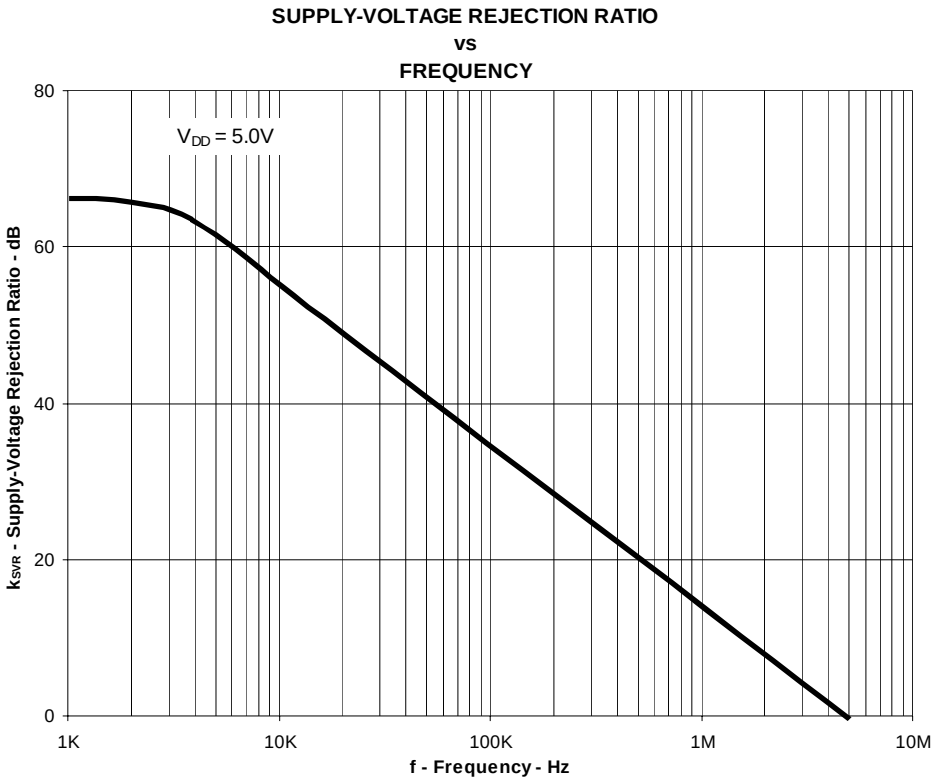


Figure 18.0

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

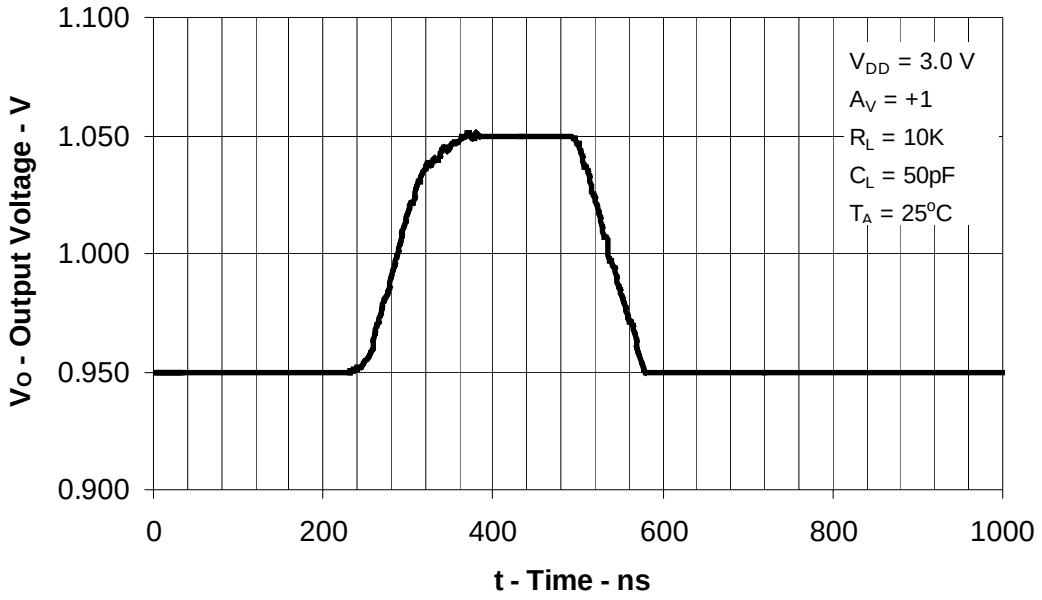


Figure 19.0

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

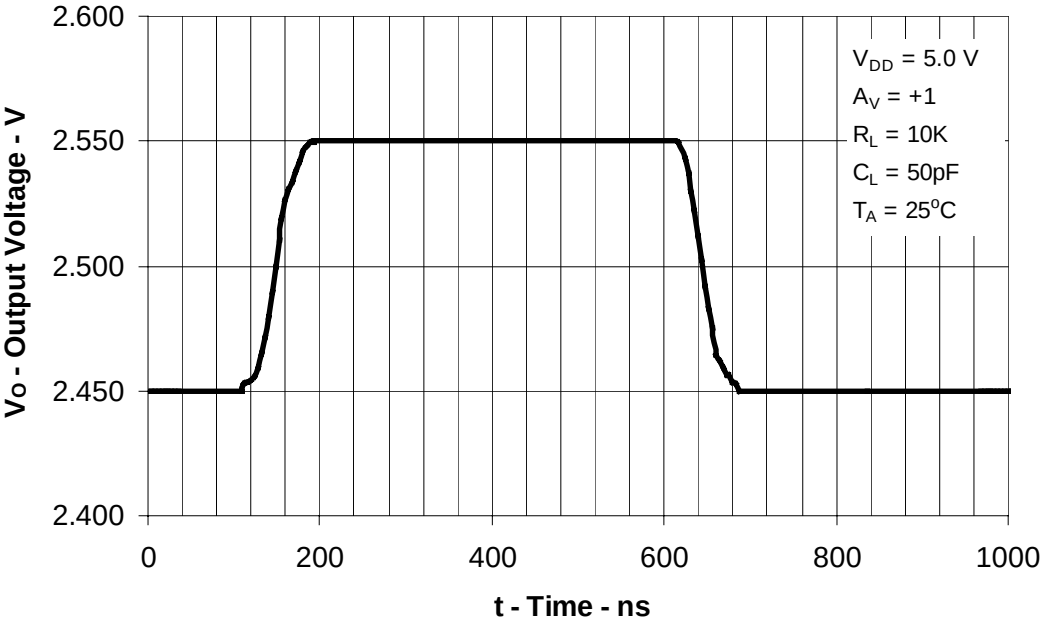


Figure 20.0

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

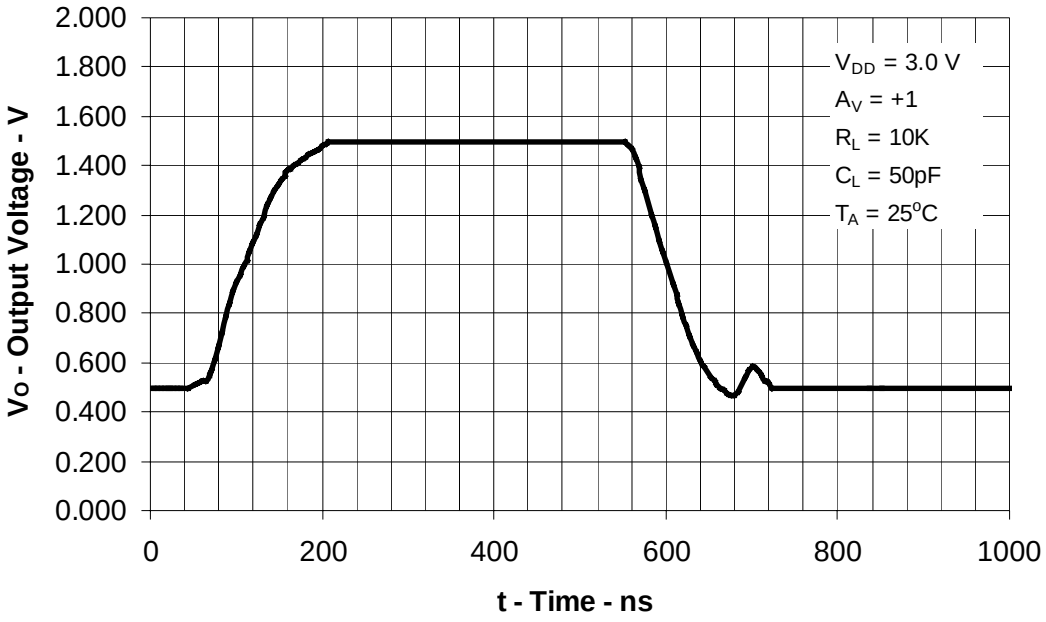


Figure 21.0

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

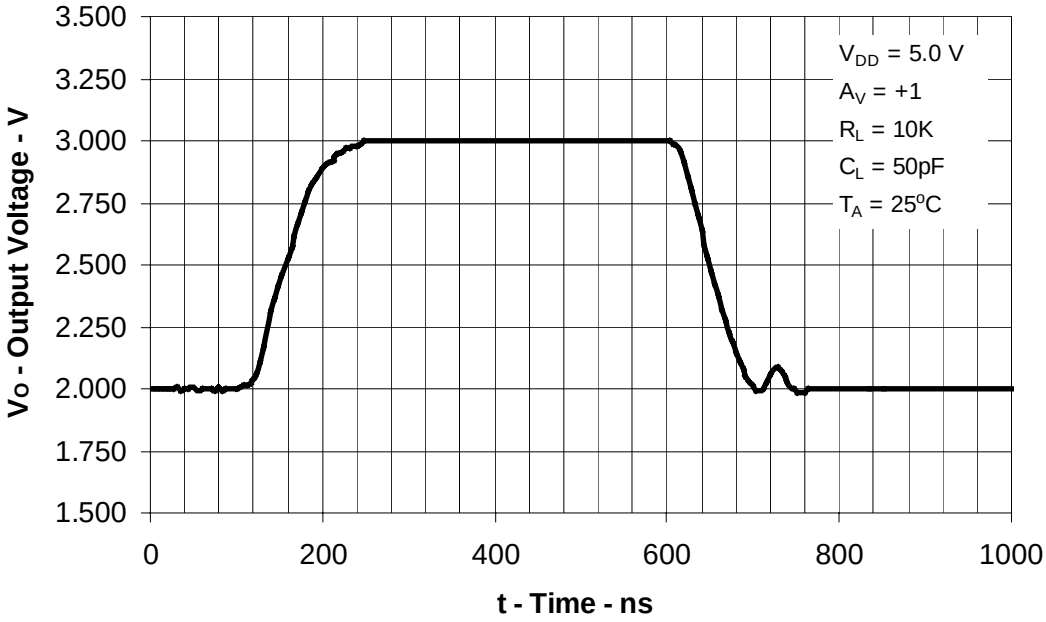


Figure 22.0

INVERTING SMALL-SIGNAL
PULSE RESPONSE

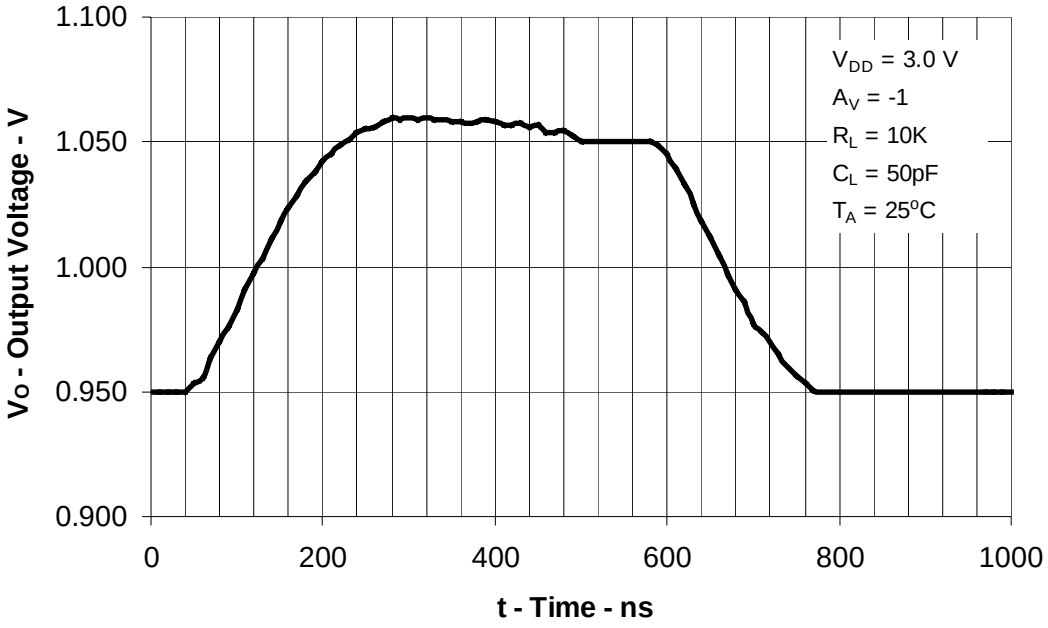


Figure 23.0

INVERTING SMALL-SIGNAL
PULSE RESPONSE

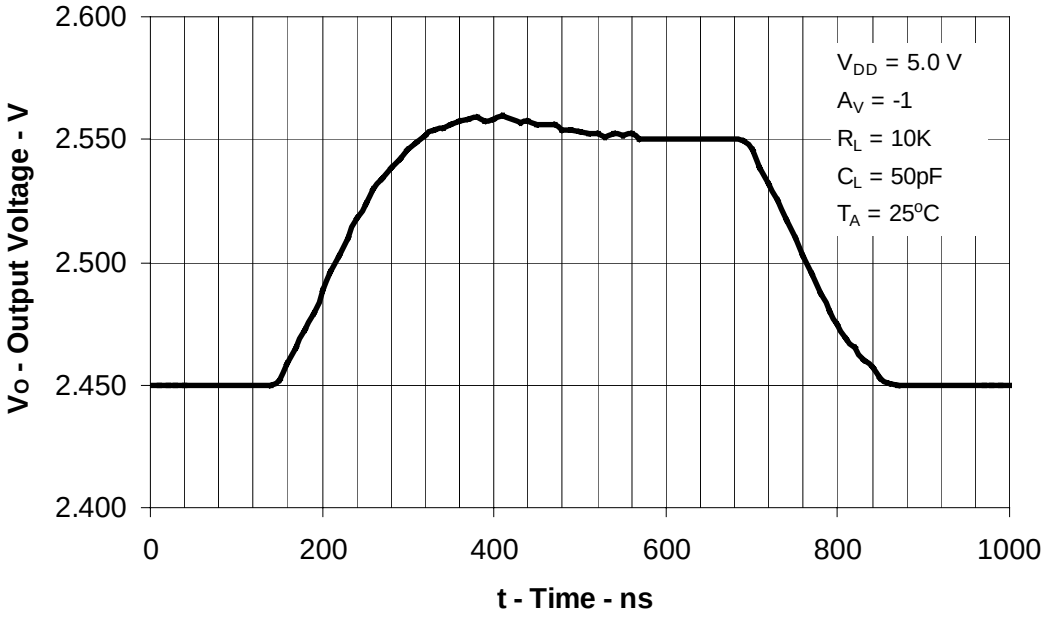


Figure 24.0

INVERTING LARGE-SIGNAL
PULSE RESPONSE

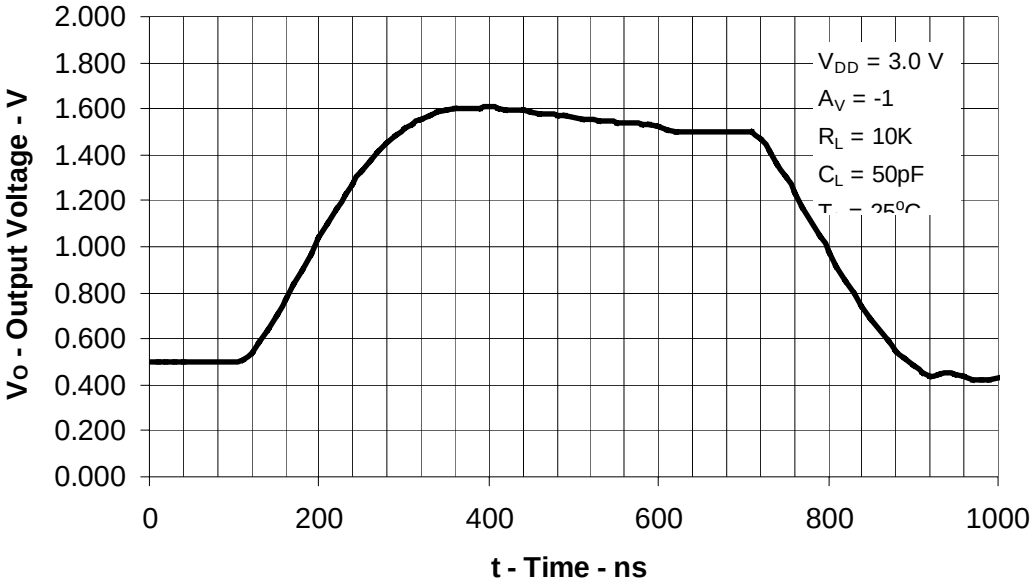
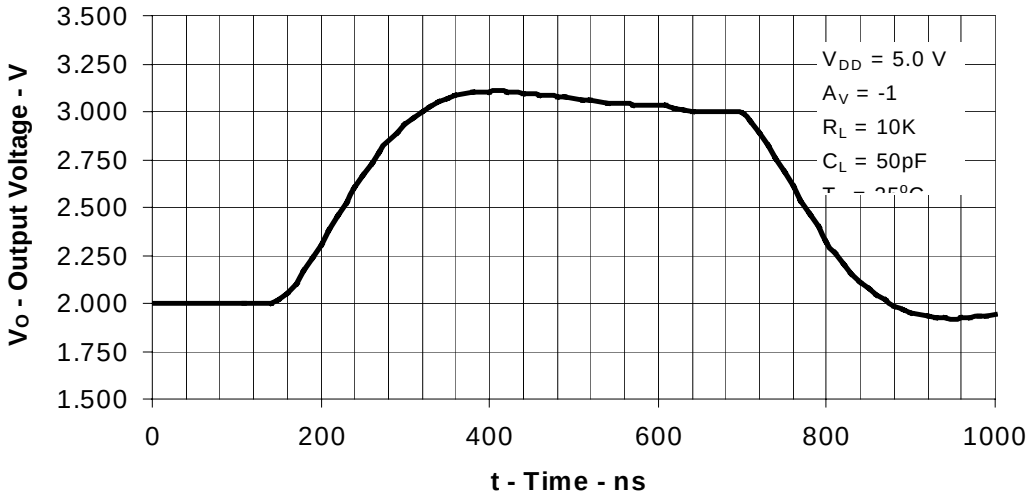


Figure 25.0

Figure 26.0

INVERTING LARGE-SIGNAL
PULSE RESPONSE



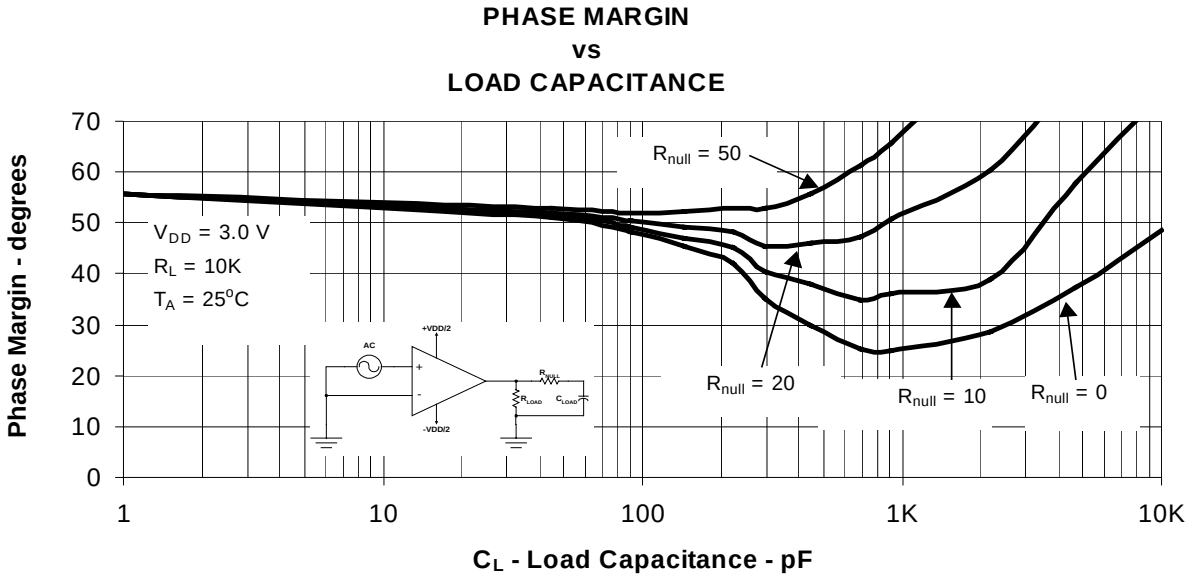


Figure 27.0

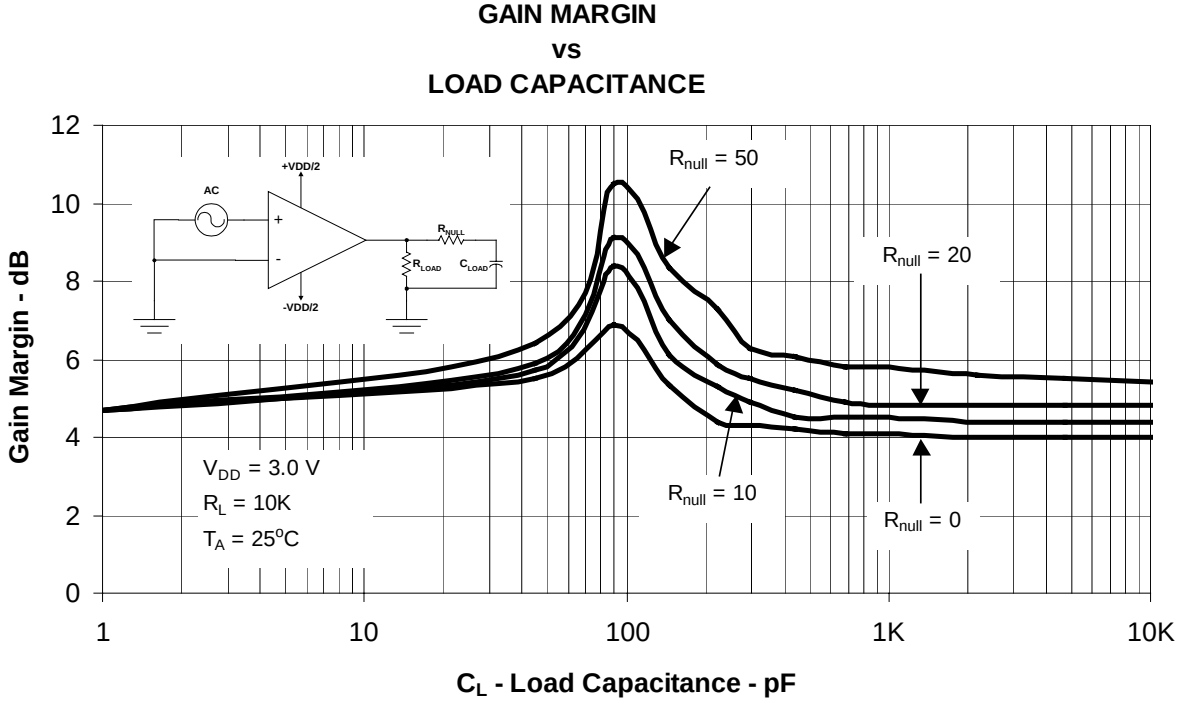


Figure 28.0

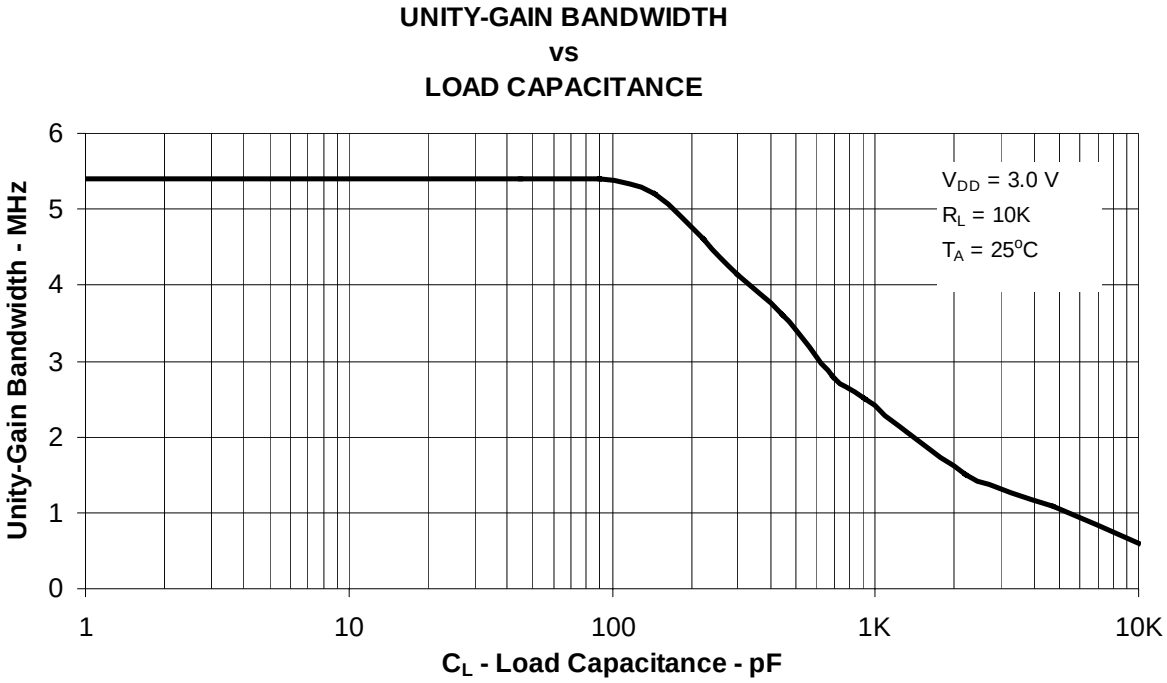

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE
Unity-Gain Bandwidth - MHz
6
5
4
3
2
1
0
1
10
100
1K
10K
C_L - Load Capacitance - pF
V_DD = 3.0 V
R_L = 10K
T_A = 25°C

Figure 29.0