19-0955; Rev 0; 8/07

MAX1215N Evaluation Kit

Evaluates: MAX1215N

General Description

The MAX1215N evaluation kit (EV kit) is a fully assembled and tested printed-circuit board (PCB) that contains all the components necessary to evaluate the performance of the MAX1215N analog-to-digital converter (ADC). The EV kit features a singled-ended-to-differential conversion circuit to drive the MAX1215N inputs. The digital outputs produced by the ADC can be captured with a user-provided high-speed logic analyzer or data-acquisition system. Additionally, the EV kit includes circuitry that generates a differential clock signal from a user-provided single-ended AC signal.

Features

- **Up to 250Msps Sampling Rate**
- **Low-Voltage and Low-Power Operation**
- **Fully Differential Signal Input Configuration**
- **On-Board Differential Output Drivers**
- **Fully Assembled and Tested**

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX1215NEVKIT#	0°C to +70°C*	68 QFN-EP**

#Denotes an RoHS-compliant EV kit.

**This limited temperature range applies to the EV kit PCB only. The MAX1215N IC temperature range is -40°C to +85°C.*

***EP = Exposed paddle.*

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C9, C13, C15, C16, C18, C19, C20, C35–C39, C49, C52	22	0.1µF ±10%, 10V X5R ceramic capacitors (0402) Murata GRM155R61A104K TDK C1005X5R1A104K
C10, C27, C28, C40	4	220µF ±20%, 6.3V tantalum capacitors (C case) AVX TPSC227M006R0250
C11, C30	2	22µF ±10%, 6.3V X5R ceramic capacitors (0805) TDK C2012X5R0J226K
C12	1	1pF ± 0.25pF, 50V C0G ceramic capacitor (0402) Murata GRM1555C1H1R0C TDK C1005C0G1H010C
C14, C33	2	2.2µF ±10%, 6.3V X5R ceramic capacitors (0603) Taiyo Yuden JMK107BJ225KA TDK C1608X5R0J225K
C21–C24	4	0.22µF ±10%, 6.3V X5R ceramic capacitors (0402) Taiyo Yuden JMK105BJ224KV TDK C1005X5R0J224K
C25, C26, C51, C53, C54, C55	6	0.1µF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H104K TDK C1608X7R1H104K
C29, C41	2	10µF ±20%, 6.3V X5R ceramic capacitors (0805) Murata GRM21BR60J106K TDK C2012X5R0J106M
C31, C43	0	Not installed, ceramic capacitors (0805)
C32, C42	2	1.0µF ±10%, 10V X5R ceramic capacitors (0603) Murata GRM188R61A105K TDK C1608X5R1A105K
C34, C44	0	Not installed, ceramic capacitors (0603)
C45–C48	0	Not installed, tantalum capacitors (C case)
C50, C56	2	0.01µF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H103K TDK C1608X7R1H103K
C58–C71	0	Not installed, ceramic capacitors (0402)
CLK, IN	2	SMA PCB vertical-mount connectors
J1	1	2 x 4-pin male header, 2.54mm
J2–J5	4	2 x 20-pin male headers, 2.54mm

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Component List (continued)

DESIGNATION	QTY	DESCRIPTION
JU1, JU2, JU3, JU5	4	3-pin headers
JU4	0	Not installed, 2-pin header
JU6	0	Not installed, 3-pin header
R1, R11, R13	0	Not installed, resistors (0603)
R2, R4–R7, R10, R12, R14, R15, R38, R39, R41, R43–R79	49	49.9Ω ±1% resistors (0402)
R3, R82	2	0Ω resistors (0603)
R8, R9	2	24.9Ω ± 0.1% resistors (0603) IRC PFC-W0603RLF-02-24R9-B
R16, R17	2	10Ω ±1% resistors (0603)
R18–R24, R28–R32, R34, R35	14	100Ω ±1% resistors (0603)
R25, R37	2	510Ω ±5% resistors (0603)
R26	1	10kΩ ±1% resistor (0603)
R27	1	5kΩ potentiometer, 19-turn, 3/8in Vishay T93YB-5K-10-D06 or Mouser 72-T93YB-5K
R33	1	3.16kΩ ±1% resistor (0603)
R36	1	1.82kΩ ±1% resistor (0603)
R40	1	100kΩ potentiometer, 12-turn, 1/4in Bourns 3266W-1-104 or Mouser 652-3266W-1-104
R42	1	13kΩ ±1% resistor (0603)
R80	0	Not installed, resistor—shorted by PC trace (0603)
R81	1	0Ω resistor (0402)
T1	1	1:1 800MHz RF transformer Mini-Circuits ADT1-1WT+
T2	1	1:1 250MHz RF transformer Coilcraft TTWB2010-1LB
TP1	1	Red test point
U1	1	MAX1215NEGK+D (68-pin QFN-EP, 10mm x 10mm)
U2	1	MAX9388EUP+ differential 4:1 multiplexer (20-pin TSSOP)
U3–U6	4	3.3V ECL quad differential receivers (20-pin SO) On Semiconductor MC100LVEL17DWG Digi-Key MC100LVEL17DWGOS-NG
Y1	0	Not installed, clock oscillator (9mm x 14mm)
—	5	Shunts
—	1	PCB: MAX1215N Evaluation Kit#

Component Suppliers

SUPPLIER	PHONE	WEBSITE
AVX Corp.	843-946-0238	www.avxcorp.com
IRC	361-992-7900	www.irctt.com
TDK Corp.	847-803-6100	www.component.tdk.com

Note: *Indicate that you are using the MAX1215N when contacting these component suppliers.*

Quick Start

Recommended Equipment

Before beginning, the following equipment is needed:

- DC power supplies:

Analog	(VCC)	1.8V, 1A
Digital	(OVCC)	1.8V, 200mA
Clock	(VCLK)	3.3V, 200mA
Buffers	(VPECL)	3.3V, 400mA

- One signal generator with low-phase noise and low jitter for clock input (e.g., HP/Agilent 8644B); bandpass filtering is strongly recommended (e.g., Allen Avionics, K&L Microwave)
- One signal generator for analog signal input (e.g., HP/Agilent 8644B); bandpass filtering is strongly recommended (e.g., Allen Avionics, K&L Microwave)
- Logic analyzer or data-acquisition system (e.g., HP/Agilent 16500C with high-speed state card HP/Agilent 16517A)
- Digital voltmeter

Procedure

The MAX1215N EV kit is a fully assembled and tested surface-mount board. Follow the steps below for board operation. **Caution: Do not turn on power supplies or enable signal generators until all connections are completed.**

1) Verify that shunts are installed in the following locations:

   JU1 (2-3) → U2 selects CLK

   JU2 (1-2) → divide-by-two disabled

   JU3 (2-3) → two's-complement output selected

   J1 (3-4) → internal reference enabled

   JU5 (2-3) → clock signal (CLK) duty cycle set to 50%

2) Connect the filtered clock signal generator to the SMA connector labeled CLK.

3) Connect the filtered analog input signal generator to the SMA connector labeled IN.

4) Connect the logic analyzer with a high-speed probe to either headers J2/J3 (LVDS-compatible signals) or J4/J5 (LVPECL-compatible signals). See Table 4 for header connections.

5) Connect a 1.8V, 1A power supply to VCC. Connect the ground terminal of this supply to GND closest to the VCC pad.

6) Connect a 1.8V, 200mA power supply to OVCC. Connect the ground terminal of this supply to GND closest to the OVCC pad.

7) Connect a 3.3V, 200mA power supply to VCLK. Connect the ground terminal of this supply to GND closest to the VCLK pad.

8) Connect a 3.3V, 400mA power supply to VPECL. Connect the ground terminal of this supply to GND closest to the VPECL pad.

9) Turn on all power supplies.

10) Enable the signal generators. Set the clock signal generator to output a 250MHz signal with an amplitude of $2.4V_{P-P}$. Set the analog input signal generator to output the desired frequency with an amplitude ≤ $2V_{P-P}$. For coherent sampling, the signal generators should be synchronized.

11) Enable the logic analyzer.

12) Capture data using the logic analyzer.

Detailed Description

The MAX1215N EV kit is a fully assembled and tested PCB that contains all the components necessary to evaluate the performance of the MAX1215N, 12-bit LVDS output ADC. The MAX1215N can be evaluated with a maximum clock frequency (f_{CLK}) of 250MHz.

The MAX1215N converter accepts differential inputs. Applications that only have a single-ended signal source available can use the on-board transformers (T1 and T2) to convert the singled-ended signal to a differential signal.

Differential receivers (U3–U6) buffer and convert the LVDS output signals of the MAX1215N to higher voltage LVPECL signals that can be captured by a wide variety of logic analyzers. The LVDS outputs are accessed at headers J2 and J3. The LVPECL outputs are accessed at headers J4 and J5.

The EV kit is designed as a four-layer PCB to optimize the PCB layout. Separate analog, digital, clock, and buffer power planes minimize noise coupling between analog and digital signals; 50Ω microstrip transmission lines are used for analog and clock inputs and 100Ω differential microstrip transmission lines are used for all digital LVDS outputs. All LVDS differential outputs are terminated with 100Ω termination resistors between true and complementary digital outputs. The trace lengths of the 100Ω differential LVDS lines are matched to within a few thousandths of an inch to minimize layout-dependent delays. All LVPECL differential outputs are Y- terminated with 49.9Ω resistors on each branch.

Power Supplies

The MAX1215N EV kit requires separate analog, digital output, clock, and buffer power supplies for best performance. Two 1.8V power supplies are used to power the analog and digital portions of the MAX1215N. The on-board clock circuitry is powered by a 3.3V power supply. A separate 3.3V power supply is used to power the output buffers (U3–U6) on the EV kit.

Clock

The MAX1215N requires a differential clock signal. However, only a single-ended clock signal source is required. The EV kit's on-board circuitry converts a singled-ended clock signal to the required differential signal. The frequency of the sinusoidal input clock signal determines the sampling frequency (f_{CLK}) of the ADC. A differential multiplexer (U2) processes the input signal to generate the required clock signal. The input signal should not exceed an amplitude of $2.6V_{P-P}$. The frequency of the clock signal should not exceed 250MHz.

The output clock duty cycle at U2 can be set to a fixed 50% duty cycle or can be adjusted whenever a single-ended signal is applied to the CLK SMA connector. Configure jumper JU5 to set the signal's duty cycle to 50% or to adjust the duty cycle with potentiometer R27. See Table 1 for configuring jumper JU5.

Table 1. Clock Duty Cycle (JU5)

SHUNT POSITION	U2 $\overline{D0}$ PIN	FUNCTION
1-2	Connected to potentiometer R27	Clock duty cycle is adjustable with R27
2-3*	Connected to VBB2	Clock duty cycle is set to 50%

**Default position.*

The MAX1215N EV kit also provides circuitry so the user can install a crystal oscillator (Y1, Valpey Fisher VF561E series recommended) to generate an on-board differential clock source. The differential line receiver and multiplexer IC (U2) can be configured to select between the SMA CLK signal and the crystal oscillator Y1 output signal by using jumper JU1. See Table 2 for configuring jumper JU1. **Note:** The crystal oscillator's duty cycle cannot be adjusted with jumper JU5.

Table 2. Selecting Clock Source (JU1)

SHUNT POSITION	U2 SEL0 PIN	CLOCK SOURCE SELECTION
1-2	Connected to VCLK	Selects crystal oscillator Y1
2-3*	Connected to GND	Selects SMA CLK input

**Default position.*

Clock Divider

The MAX1215N features an internal divide-by-two clock divider. Use jumper JU2 to enable/disable this feature. See Table 3 for shunt positions.

Table 3. Clock-Divider Shunt Settings (JU2)

SHUNT POSITION	MAX1215N CLKDIV PIN	DESCRIPTION
1-2*	Connected to VCC	Clock signal divided by 1
2-3	Connected to GND	Clock signal divided by 2

**Default position.*

Input Signal

The MAX1215N accepts differential analog input signals. However, the EV kit only requires a 50Ω terminated single-ended analog input signal with an amplitude of less than $2V_{P-P}$ provided by the user. The on-board transformers (T1 and T2) convert the single-ended analog input into a differential analog signal, which is applied to the ADC's differential input pins.

Optional Input Transformer

The MAX1215N EV kit uses two transformers to enhance the THD and the SFDR performance at high input frequencies (> 100MHz). These two transformers help reduce the increase of even-order harmonics at high frequencies. To use only one transformer, follow the directions below:

1) Remove transformer T1.

2) Install 0Ω resistors (0603) on R11 and R13.

Reference Voltage

There are two methods to set the full-scale range (FSR) of the MAX1215N. The MAX1215N EV kit can be configured to use the ADC's internal reference, or a stable, low-noise, external reference can be applied to the REFIO pad. Jumper J1 controls which reference source is used. See Table 4 for shunt settings.

Table 4. Reference Shunt Settings (J1)

SHUNT POSITION	DESCRIPTION
1-2	Internal reference disabled. Apply an external reference voltage to the REFIO pad
3-4*	Internal reference enabled
5-6	Increases FSR through potentiometer R40
7-8	Decreases FSR through potentiometer R40

**Default position.*

Output Signal

The MAX1215N features a single 12-bit, parallel, LVDS-compatible, digital output bus. The digital outputs also feature a clock bit (DCLKP/N) for data synchronization, and a data overrange bit (ORP/N). See Table 6 for header connections.

Output Format

The digital output coding can be chosen to be either in two's-complement or straight offset binary format by configuring jumper JU3. See Table 5 for shunt settings.

Table 5. Output-Format Shunt Settings (JU3)

SHUNT POSITION	MAX1215N $\overline{T}$/B PIN	DESCRIPTION
1-2	Connected to VCC	Digital output in straight offset binary
2-3*	Connected to GND	Digital output in two's complement

**Default position.*

Output Bit Locations

The digital outputs of the ADC are connected to two 40-pin headers (J2 and J3). PCB trace lengths are matched to minimize output skew and improve performance of the device. In addition, four differential receivers (U3–U6) buffer and level translate the ADC's digital outputs to LVPECL-compatible signals. The differential receivers increase the differential voltage swing and are able to drive large capacitive loads, which may be present at the logic analyzer connection. The outputs of the buffers are connected to two 40-pin headers (J4 and J5). See Table 6 for headers J4 and J5 bit locations.

Table 6. Output Bit Locations

BIT		UNBUFFERED (LVDS)	BUFFERED (LVPECL)	BIT		DESCRIPTION
D11	P	J2-10	J4-10	P	LD11	MSB
	N	J2-9	J4-9	N		
D10	P	J2-16	J4-16	P	LD10	Data bits
	N	J2-15	J4-15	N		
D9	P	J2-22	J4-22	P	LD9	
	N	J2-21	J4-21	N		
D8	P	J2-28	J4-28	P	LD8	
	N	J2-27	J4-27	N		
D7	P	J2-34	J4-34	P	LD7	
	N	J2-33	J4-33	N		
D6	P	J2-40	J4-40	P	LD6	
	N	J2-39	J4-39	N		
D5	P	J3-8	J5-8	P	LD5	
	N	J3-7	J5-7	N		
D4	P	J3-14	J5-14	P	LD4	
	N	J3-13	J5-13	N		
D3	P	J3-20	J5-20	P	LD3	
	N	J3-19	J5-19	N		
D2	P	J3-26	J5-26	P	LD2	
	N	J3-25	J5-25	N		
D1	P	J3-32	J5-32	P	LD1	
	N	J3-31	J5-31	N		
D0	P	J3-38	J5-38	P	LD0	LSB
	N	J3-37	J5-37	N		
OR	P	J2-4	J4-4	P	LOR	Overrange bit
	N	J2-3	J4-3	N		
DCLK	P	J3-2	J5-2	P	LDC0	Clock output signal
	N	J3-1	J5-1	N		

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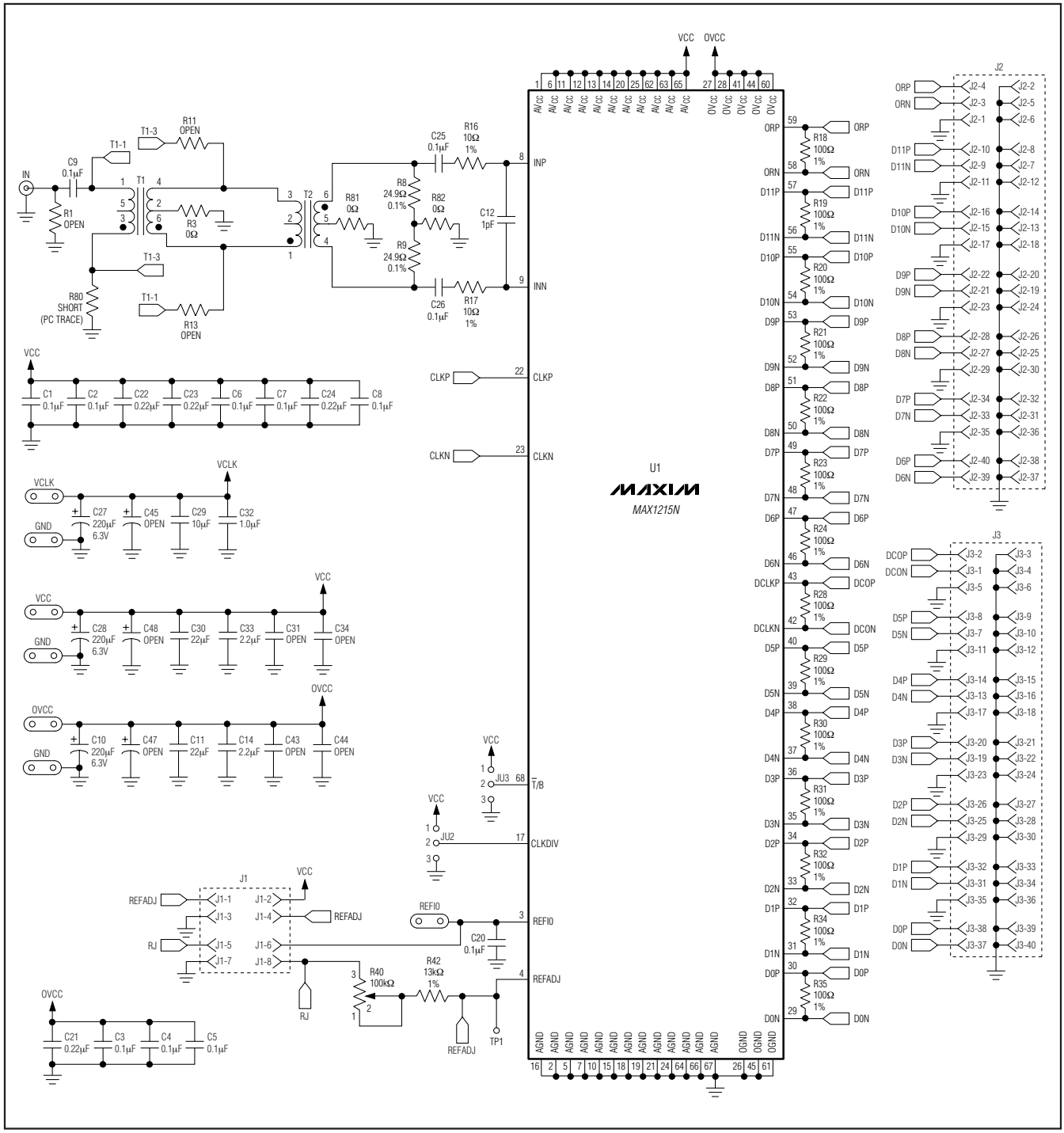

Figure 1a. MAX1215N EV Kit Schematic (Sheet 1 of 3)

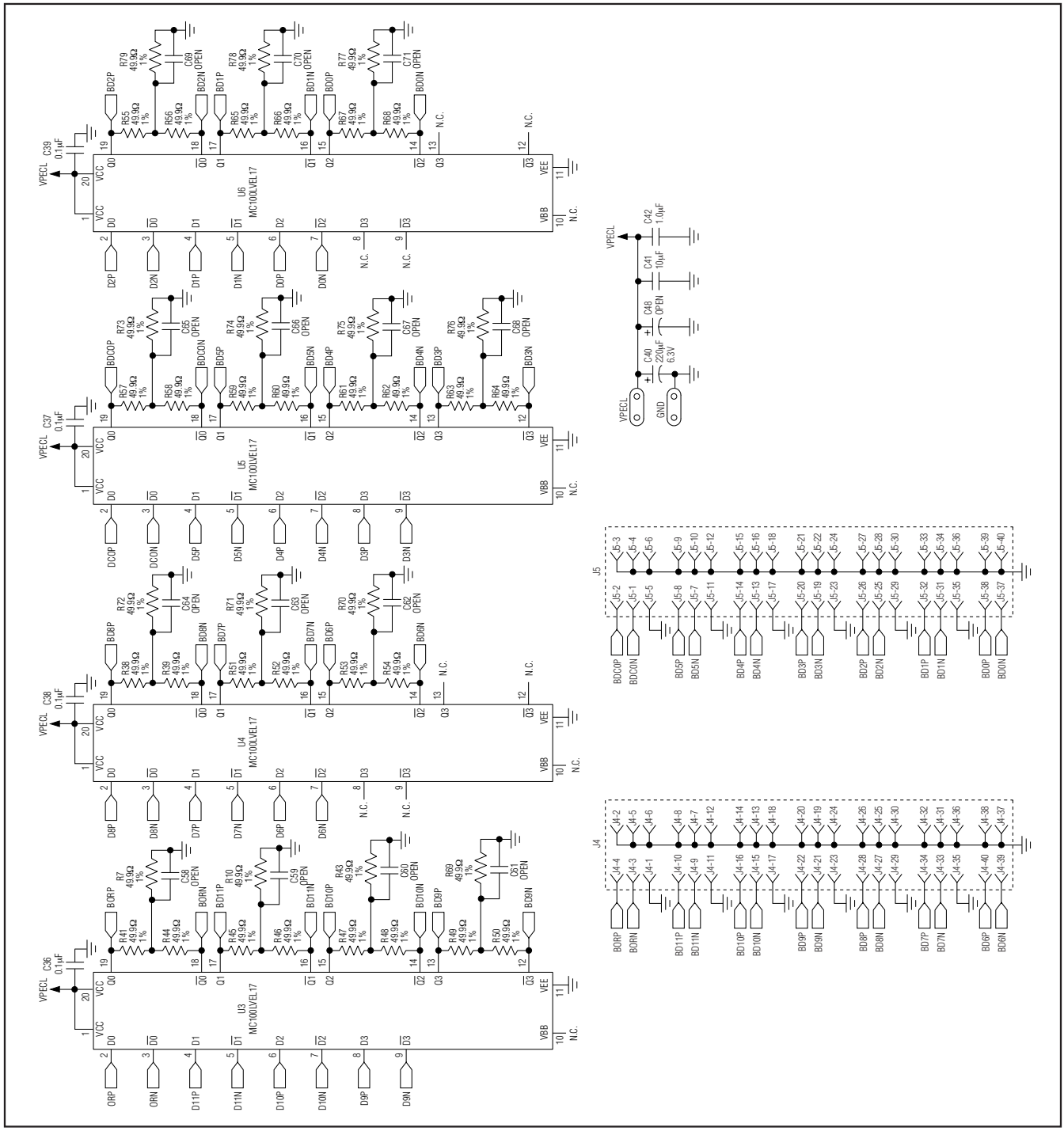

Figure 1b. MAX1215N EV Kit Schematic (Sheet 2 of 3)

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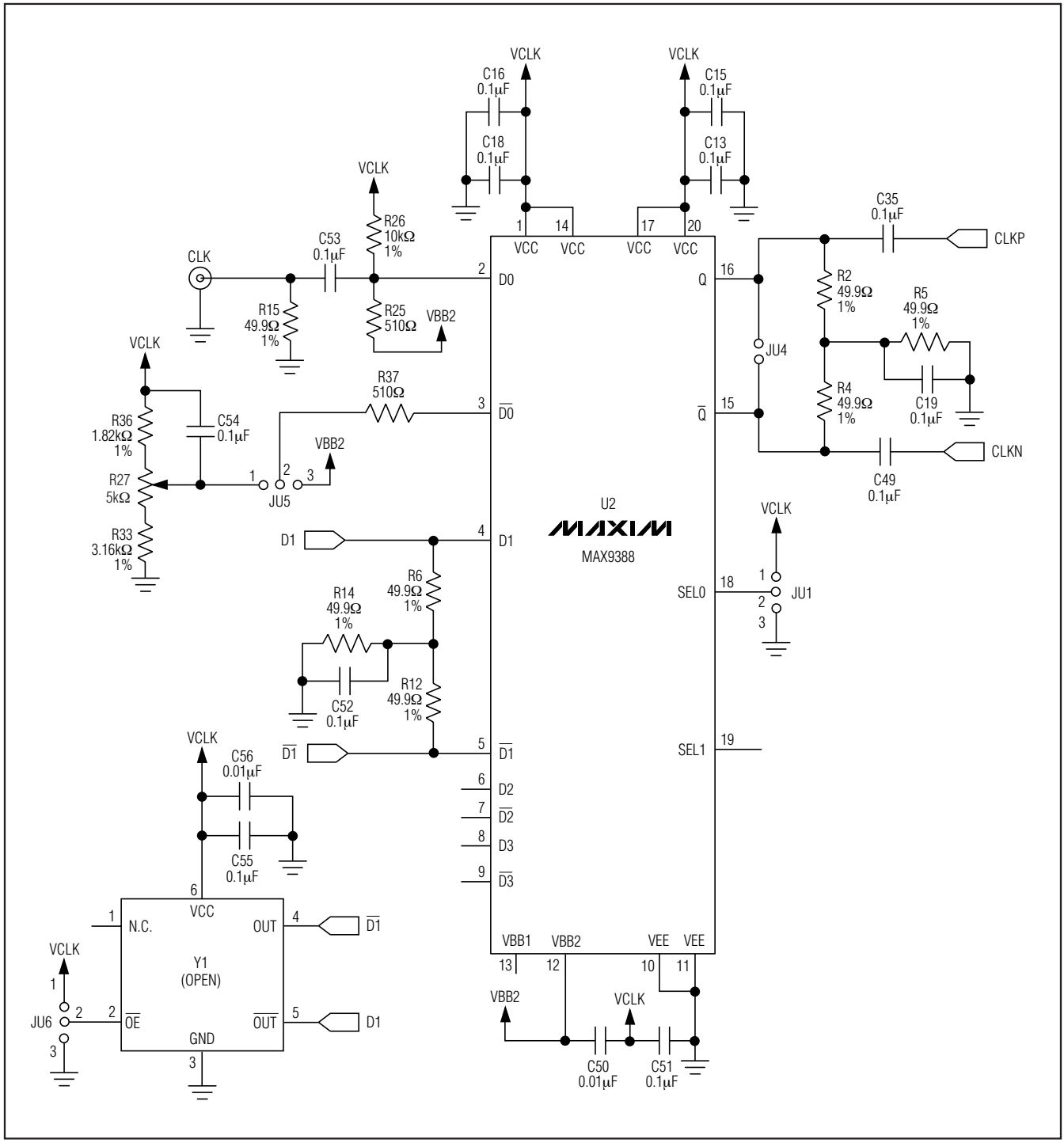

Figure 1c. MAX1215N EV Kit Schematic (Sheet 3 of 3)

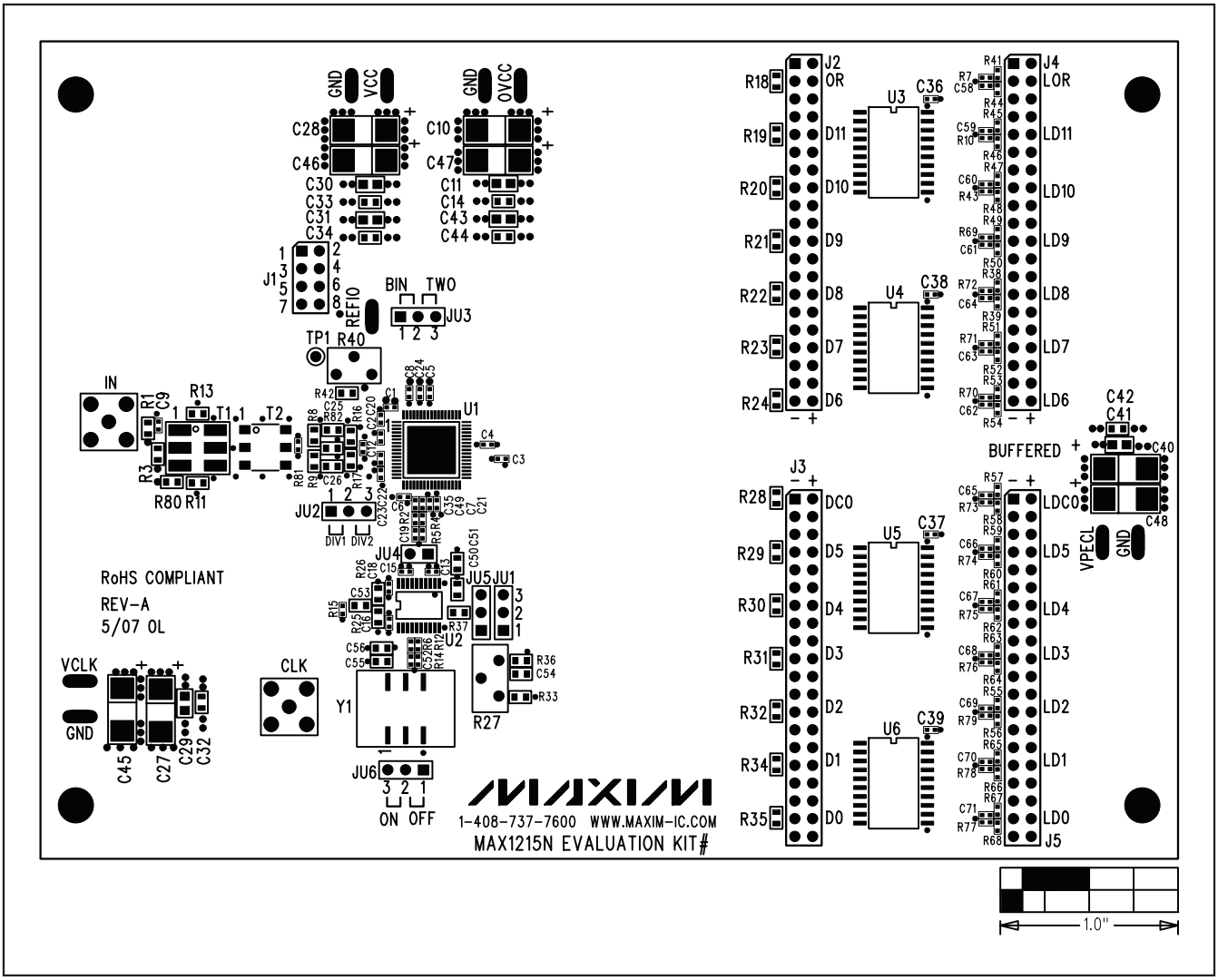

Figure 2. MAX1215N EV Kit Component Placement Guide—Component Side

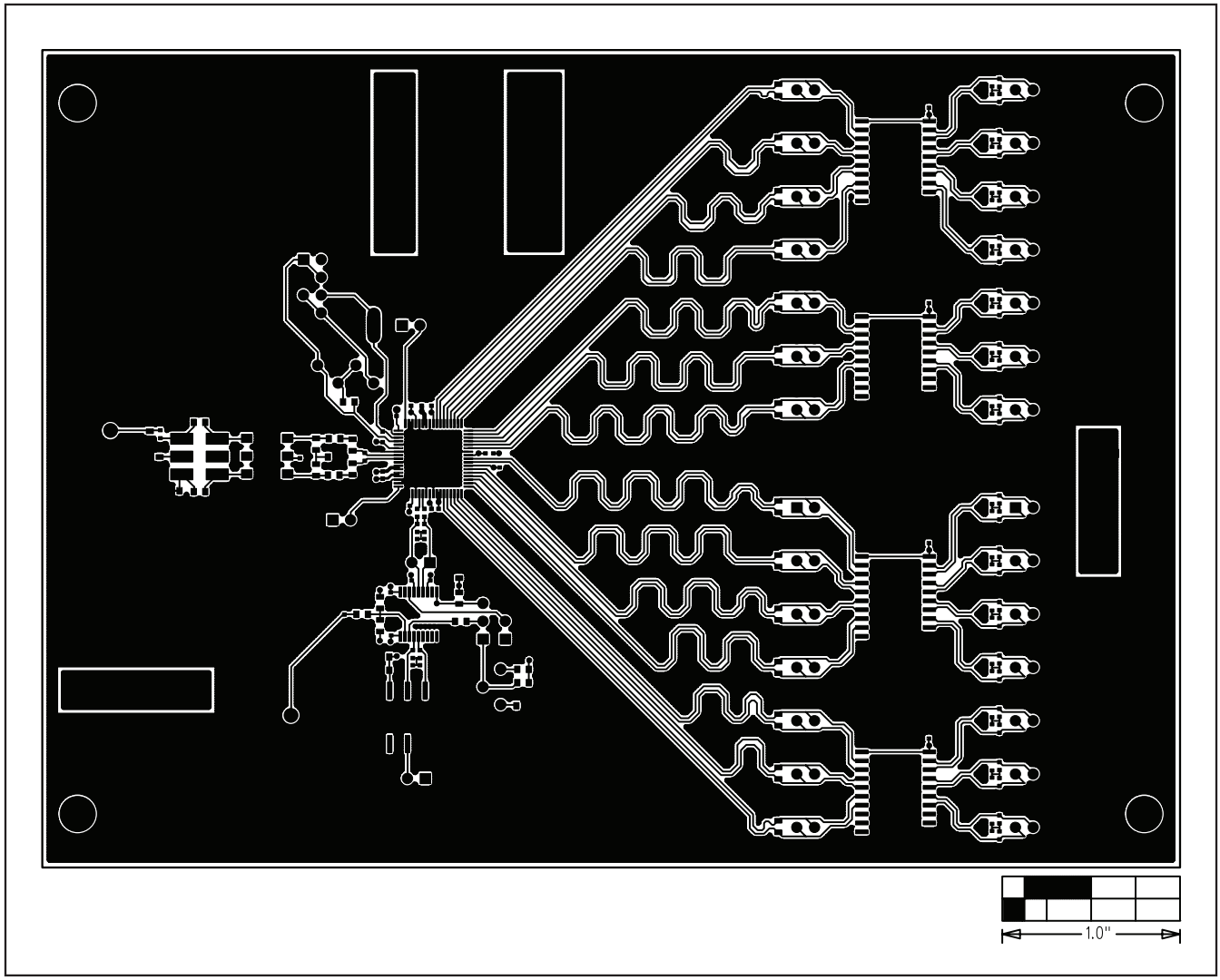

Figure 3. MAX1215N EV Kit PCB—Component Side

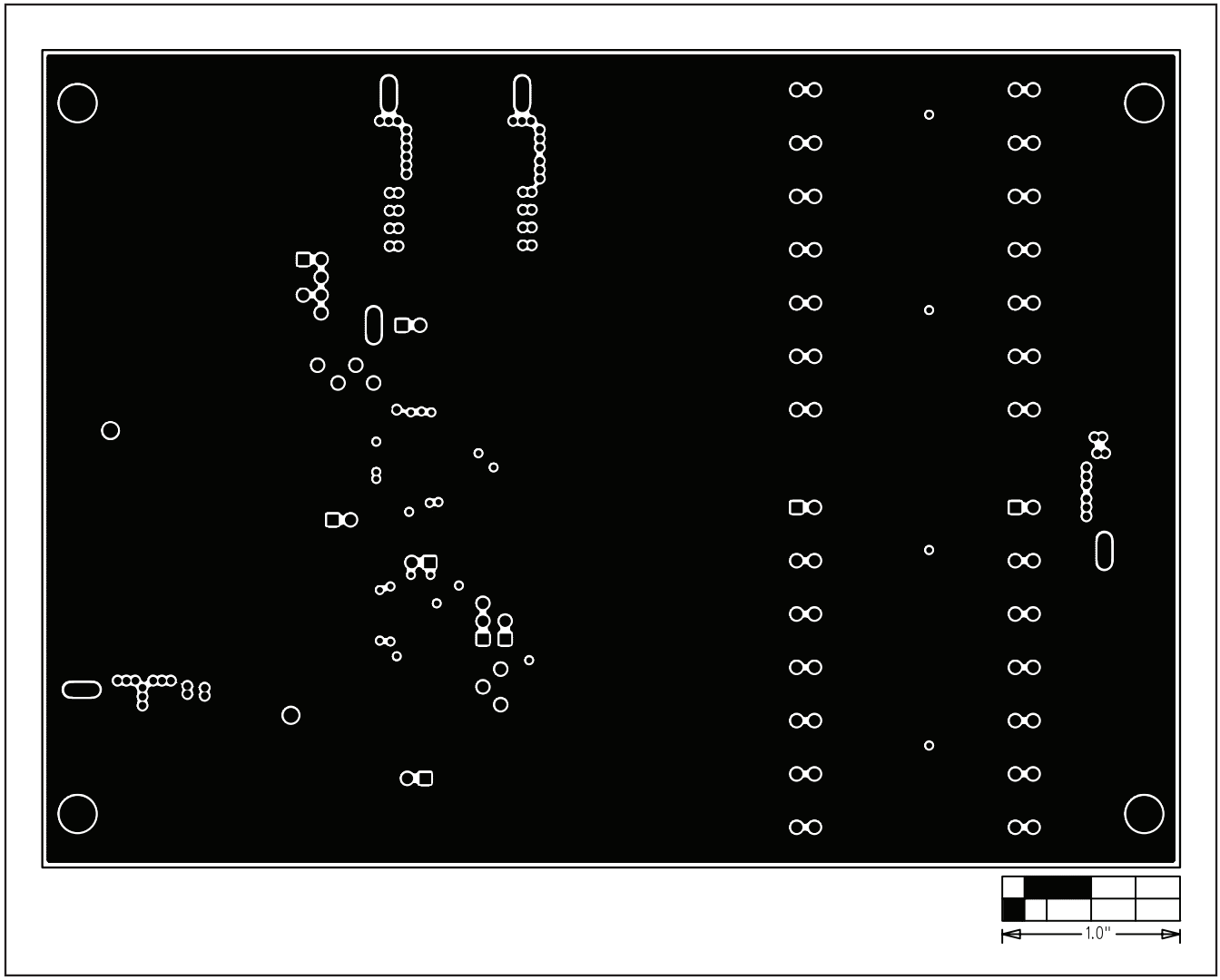

Figure 4. MAX1215N EV Kit PCB Layout—Ground Plane (Layer 2)

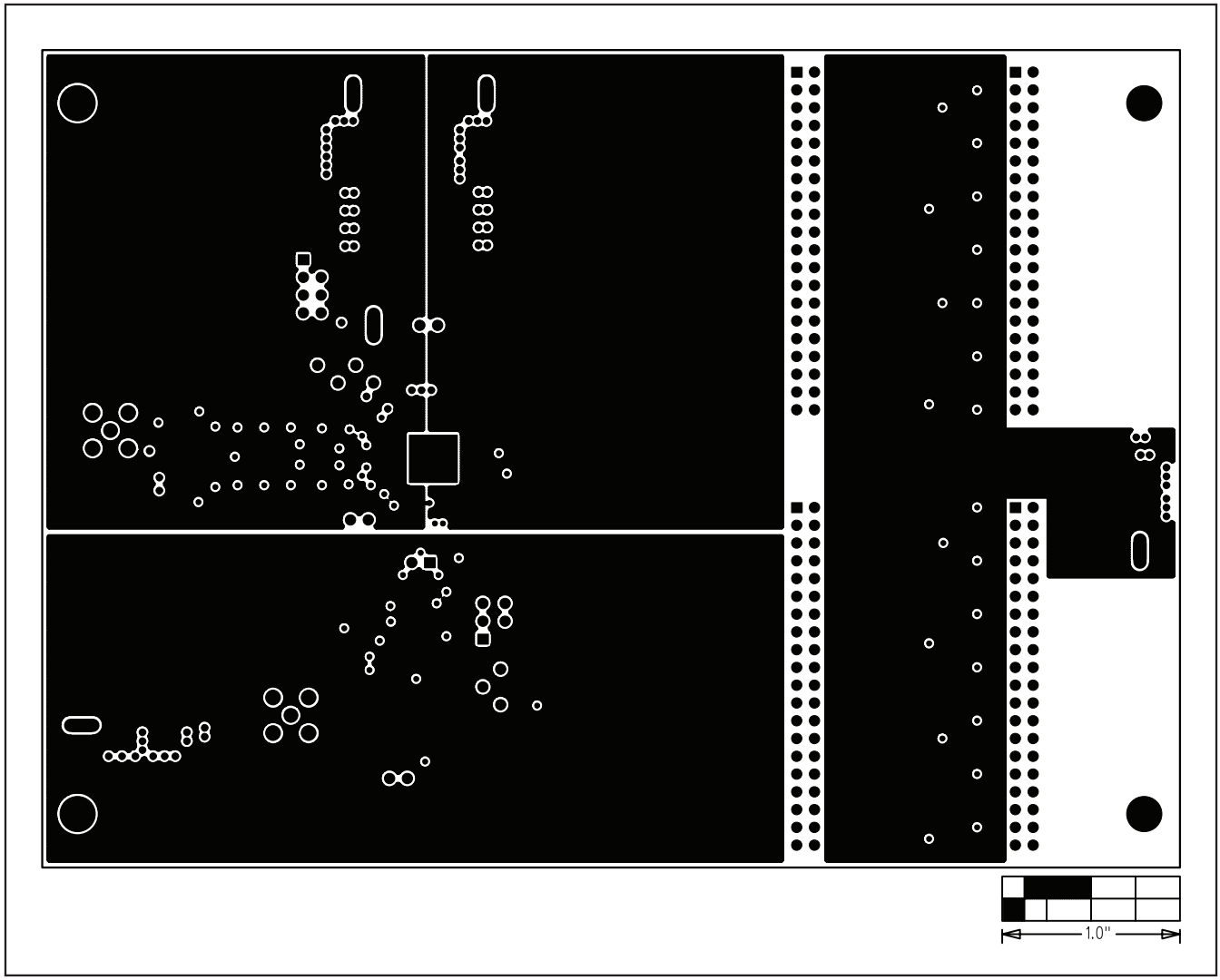

Figure 5. MAX1215N EV Kit PCB Layout—Power Plane (Layer 3)

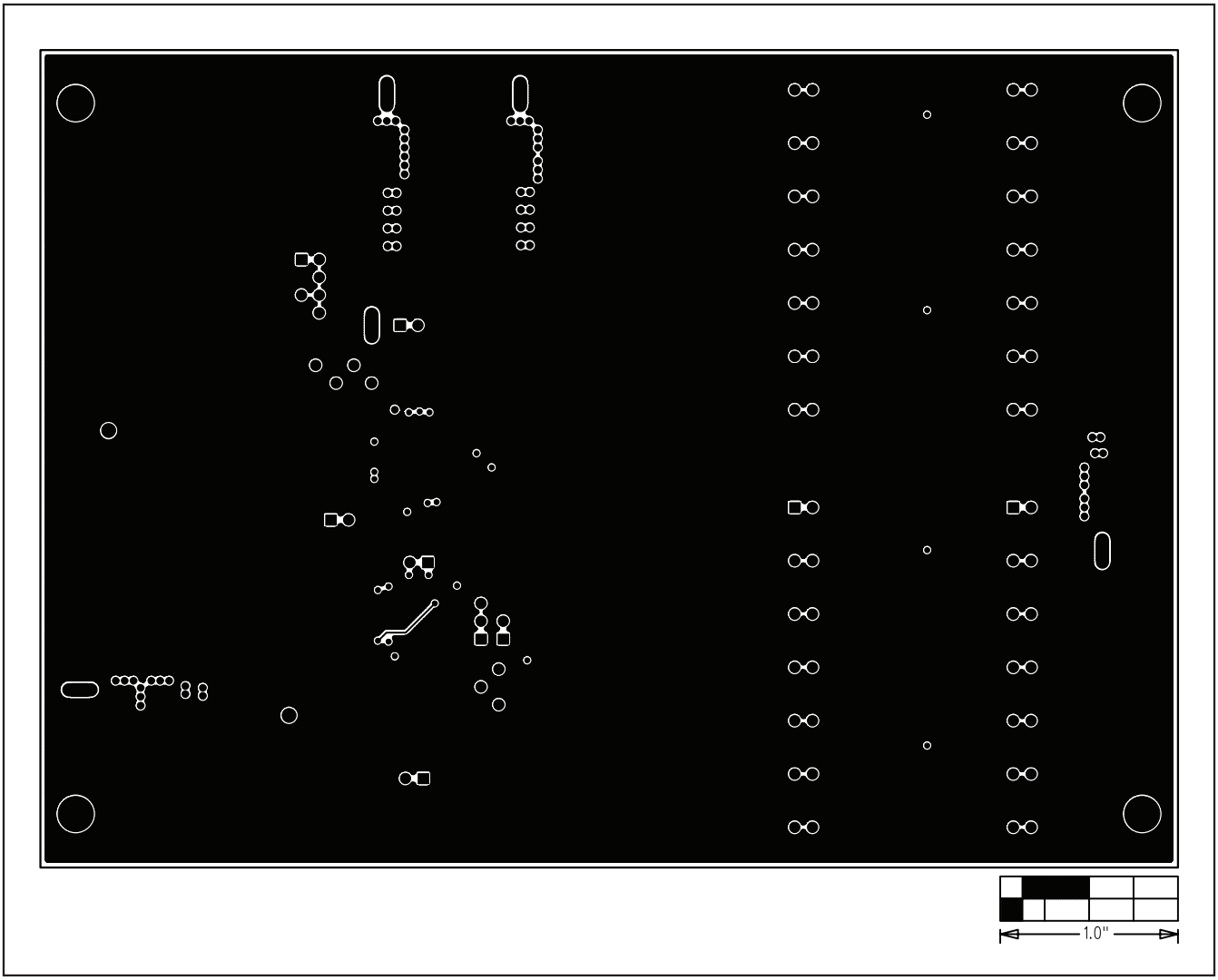

Figure 6. MAX1215N EV Kit PCB Layout—Solder Side