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Integrated Protection IC on 12V Bus with an Integrated MOSFET, Lossless Current Sensing, and PMBus Interface

MAX16545B/ MAX16545C

General Description

The MAX16545B/C is a circuit-breaker protection IC with an integrated low-resistance MOSFET and lossless current-sense circuitry featuring PMBus™/SMBus control and reporting. The IC is designed to provide the optimum solution for distribution, control, monitoring and protection of the system's 12V power supply. An internal LDO provides the bias supply voltage for the protection IC.

If no fault is detected, the MAX16545B/C initiates the startup. The device has been designed to provide controlled, monotonic startup. Programmable soft-start ramp and delay is implemented to limit the inrush current during startup. The MAX16545B is set for 16A Startup OCP, and the MAX16545C is set for 24A Startup OCP.

The IC monitors the current and the voltage of the 12V system power rail and provides multiple levels of protection with fast turn off if a fault is detected. Three methods of overcurrent protection are provided. Programmable moderate OCP level allows surge currents for a limited time. User-selectable severe OCP level provides a fast disconnect if a current exceeding the severe OCP threshold is detected. An additional fixed high shutdown OCP level provides instantaneous disconnect to further protect the device.

The lossless current sense provides high-accuracy current sensing over load and temperature, improving overall system energy efficiency, and reducing dissipation. A signal proportional to the load current is reported through an analog output and extensive reporting is provided through the SMBus/PMBus.

Output voltage is monitored at all times. If at any time the output voltage falls below the programmable output undervoltage lockout threshold, the PWRGD signal is asserted low. If at any time the input voltage falls below the programmable input undervoltage lockout threshold, the PWRGD signal is asserted low. The MAX16545B/C can be programmed through PMBus to provide input overvoltage protection. Input overvoltage protection is disabled by default. When enabled through PMBus, if the input voltage exceeds a programmable overvoltage threshold, the MOSFET is latched off and a fault is communicated.

The IC is used to distribute and control power to a system from the +12V power supply. See Basic Application Circuit.

Benefits and Features

- High Density (6.5mm x 4mm for 60A): Less than 25% of the Board Area of Conventional Solutions
  - Monolithic Integration of Power, Control, and Monitoring (Integrated Power MOSFET with 0.95mΩ Total Resistance in 12V Power Path (R_{DSON}), Including Package)
  - Integrated Lossless, Precise Current Sensing
  - Integrated LDO Provides V_{DD} Supply (1.8V Bias Supply)
- Enables Advanced System Power Management
  - PMBus/SMBus Telemetry with Extensive Status Monitoring and Reporting
  - Load Current Indicator (ILOAD) Pin Provides Analog Output Current Reporting with High Accuracy
  - Programmable Soft-Start for Inrush Current Limiting
  - Increases Power-Supply Reliability with IC Self-Protection Features
    - Very Fast Fault Detection and Isolation
    - V_{IN} to V_{OUT} Short Protection During Startup
    - Overtemperature Protection
  - Three Levels of Overcurrent Protection
    - Programmable Moderate OCP
    - Programmable Severe OCP Provides Isolation < 5µs.
    - Fail-Safe Safe OCP Provides Isolation < 250ns.

Applications

Servers, Networking, Storage, Communication Equipment and AC/DC Power Supplies

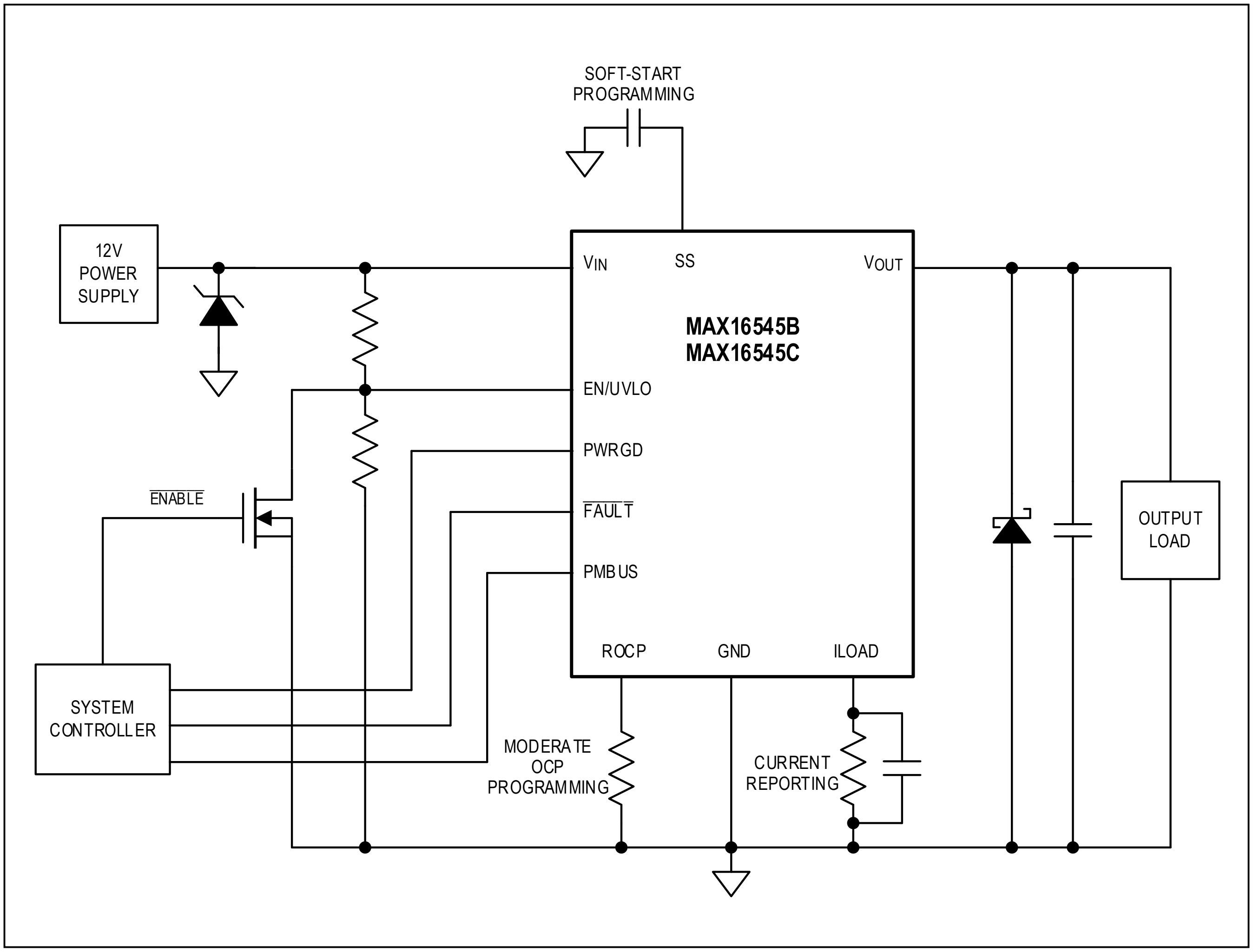
- Integrated Protection IC on 12V: Circuit Breaker, Hot Swap, Inrush Control

***Ordering Information* appears at end of data sheet.**

PMBus is a trademark of SMIF, Inc.

19-8779; Rev 6; 6/22

Basic Application Circuit



Absolute Maximum Ratings

Supply Voltage (V_{IN}) DC ....-0.3V to +16V
Supply Voltage (V_{IN}) 150µs ....+22V
Bias Supply Voltage (V_{DD})..................................-0.3V to +2.5V
PWRGD, $\overline{\text{FAULT}}$..-0.3V to +5.5V
EN/UVLO, ROCP ....-0.3V to +2.5V
SMBUS_CLK, SMBUS_DATA................................-0.3V to +6V
$\overline{\text{SMBUS\_ALERT}}$ ....-0.3V to +6V
SMBUS_ID ....-0.3V to +2.5V
ILOAD_IN, ILOAD ....-0.3V to +2.5V
Output Voltage (V_{OUT}) DC...................................-0.3V to +16V
V_{BST} (Relative to V_{OUT}) ....-0.3V to +2.5V
SS...-0.3V to +16V
Junction Temperature (T_J)...+150°C
Storage Temperature Range .... -65°C to +165°C
Peak Reflow Temperature ....+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ratings

Supply Voltage (V_{IN}) .... 10.8V to 13.2V
Bias Supply Voltage (V_{DD})................................. 1.76V to 1.94V
Junction Temperature (T_J)...................................0°C to +125°C

Package Information

PACKAGE TYPE: 22 FCQFN	
Package Code	P224A6F+1
Outline Number	21-1006
Land Pattern Number	90-0510
THERMAL RESISTANCE	
Junction to Case (θ_{JC}) (max)	0.31°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{IN} = 12V ±10%, T_A = T_J = 0°C to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = T_J = +32°C. Limits over operating temperature are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
12V SUPPLY (V_{IN})						
Supply Voltage Range	V_{IN}		10.8	12	13.2	V
Supply Current	I_{IN}	FET off	3.2		6.1	mA
		FET on: I_{OUT} = 0 (Note 1)	3.7		6.5	
		FET on: I_{OUT} = 60A (Note 1)			10	
INTEGRATED 1.8V LINEAR REGULATOR						
LDO Output Voltage Range	V_{DD}		1.76	1.85	1.94	V
V_{DD} UVLO, Falling			1.55	1.6	1.67	
V_{DD} UVLO, Rising			1.62	1.67	1.71	
V_{DD} UVLO Hysteresis		(Note 1)	30	60	80	mV
V_{DD} UVLO Speed		(Note 1)		2		µs
UNDERVOLTAGE LOCKOUT: 12V SUPPLY (V_{IN})						
$V_{IN_}$UVLO Rising Threshold	V_{IN_UVLO}	At EN/UVLO Pin	0.95	1	1.05	V
$V_{IN_}$UVLO Hysteresis				50		mV
Programmable 12V V_{IN} Undervoltage Threshold for Rising Input	V_{IN_UVLO}	Programmable through resistor-divider, measured at V_{IN} with 1% resistors on the divider.	8			V
Response Time	t_D	From EN/UVLO = 0V To FET Off (Note 1)		2		µs
EN/UVLO PIN INTERNAL PARAMETERS						
EN/UVLO Pin Leakage		EN/UVLO Pin = 1.8V	5	7.2	11	µA
EN/UVLO Internal-Pulldown Resistor			110	250	450	kΩ
BOOST VOLTAGE (V_{BST})						
V_{BST} Charging Time to 1.6V above V_{OUT}	t_{CHARGE}	C_{BST} = 100nF			275	µs
BST Voltage above V_{OUT}	V_{BST}			1.8		V
Rising UVLO Threshold above V_{OUT}	BOOST UVLO		0.8	1.2	1.6	V
Falling UVLO Threshold above V_{OUT}			0.7	1.1	1.5	
UVLO Hysteresis			60	130	400	mV
Falling-Lockout Response Time	t_D				2.3	µs
INTEGRATED MOSFET CHARACTERISTICS						
On-Resistance	$R_{DS(ON)}$	(Note 1)		0.95		mΩ

Electrical Characteristics (continued)

(V_{IN} = 12V ±10%, T_A = T_J = 0°C to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = T_J = +32°C. Limits over operating temperature are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVERCURRENT PROTECTION (OCP)						
Gain from ROCP Pin Current to I_{OUT}	G_{OCP}	(Note 1)		8		A/µA
Moderate OCP Voltage Threshold	V_{OCPM}	Referred to voltage over R_{OCP} (Note 1)		0.8		V
Moderate OCP Threshold Accuracy	V_{OCPM}	Referred to I_{OUT} using Equation 1 (Note 1)		±12		%
Moderate OCP Threshold Range	I_{OCP} (MODERATE)	(Note 1)	30		70	A
Allowable Range for No Fault Detection	R_{OCP}		26		380	kΩ
Moderate OCP Timeout	t_{OCPM}	I_{OUT} > Moderate OCP, I_{OUT} < Severe OCP PMBus Programmable, default 100µs (Note 1)		20		µs
				100		µs
				100		ms
				250		ms
Moderate OCP Fault Detect Delay Timeout Accuracy	t_{OCPM}	(Note 1)		±25		%
Severe OCP Threshold, % above Moderate OCP	$I_{OCP(SEVERE)}$	PMBus Programmable, default 130% (Note 1)		130		%
				150		%
Severe OCP Threshold Accuracy	$I_{OCP(SEVERE)}$	(Note 1)		±15		%
Severe OCP Delay	$t_{D(SEVERE)}$	From fault threshold exceeded to FET off		10		µs
Safe OCP Threshold	$I_{OCP(SAFE)}$			120		A
Safe OCP Threshold Accuracy	$I_{OCP(SAFE)}$			±20		%
Safe OCP Delay	$t_{D(SAFE)}$	From fault threshold exceeded to FET off			250	ns
Startup OCP Threshold	$I_{OCP(STARTUP)}$	PMBus programmable, MAX16545B default = 16A, MAX16545C default = 24A (Note 1)		16		A
				24		A
				8		A
Startup OCP Threshold Accuracy	$I_{OCP(STARTUP)}$	(Note 1)		±20		%
Startup OCP Delay	$t_{D(STARTUP)}$				10	µs
SOFT-START AND C_{OUT}						
Soft-Start Discharge Resistance	SS			1	2	kΩ
Soft-Start Charging Current	I_{SS}		24.8		38	µA
Soft-Start Time	t_{SS}	C_{SS} = 0nF, I_{OUT} = 0A			1.5	ms

Electrical Characteristics (continued)

(V_{IN} = 12V ±10%, T_A = T_J = 0°C to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = T_J = +32°C. Limits over operating temperature are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start Capacitor Discharge Threshold			0.10	0.21	0.29	V
C_{SS} Discharge Check Duration During Startup				2.2		s
FET V_{GS} UNDERVOLTAGE LOCKOUT						
V_{GS} Rising UVLO Threshold	V_{GS_UVLO}		0.87	1.3	1.61	V
V_{GS} Falling UVLO Threshold			0.74	1.17	1.47	V
V_{GS} UVLO Hysteresis			87	100	466	mV
V_{GS} UVLO Masking Time		V_{GS} UVLO masking time at startup	90	100	110	ms
PASS FET SHORT DETECTION DURING STARTUP						
Duration of V_{OUT} Discharge Check	$t_{DISCHARGE}$			2.2		s
Pulldown Resistance on V_{OUT} During Self-Check	$R_{DISCHARGE}$		400	455	560	Ω
Threshold for Self-Check Procedure	$V_{OUT\_SELFCHECK}$	PMBus Programmable, default 9V (Note 1)	5.8	6	6.2	V
			6.8	7	7.2	
			7.8	8	8.2	
			9.0	9.2	9.4	
Delay from Self-Check Pass to Start V_{OUT} Ramp	t_D	PMBus Programmable, default 0.02ms (Note 1)		0.02		ms
				10		
				20		
PWRGD PIN						
PWRGD Output-High Voltage	V_{OH}	External pullup leakage below 1µA			5.5	V
PWRGD Output-Low Voltage	V_{OL}	Sinking 4mA			0.4	V
Propagation Delay from V_{OUT_UVLO} Detect to $\overline{PWRGD}$ Pin Asserted Low	t_D				5	µs
Rising Threshold for PWRGD Asserted High	$V_{TH(PWRGD)}$	PMBus Programmable, default 11V (Note 1)		8		V
				9		
				10		
				11		
Accuracy			-5		+5	%
PWRGD Assertion Delay After V_{OUT} Settles		(Note 1)		5		ms
PWRGD Hysteresis		8V	0.36	0.41	0.46	V
PWRGD Hysteresis		9V	0.42	0.47	0.52	
PWRGD Hysteresis		10V	0.45	0.51	0.56	
PWRGD Hysteresis		11V	0.50	0.55	0.61	

Electrical Characteristics (continued)

(V_{IN} = 12V ±10%, T_A = T_J = 0°C to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = T_J = +32°C. Limits over operating temperature are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVERTEMPERATURE PROTECTION (OTP)						
Overtemperature Protection Threshold	T_{OTP}	PMBus programmable (Note 1)		135		°C
SMBus DATA (SMBUS_DATA) AND CLOCK (SMBUS_CLOCK) PINS						
Leakage Current		For pullup voltage = 5.5V		6.2	10	µA
Input-Low Voltage	V_{IL}				0.8	V
Input-High Voltage	V_{IH}		2.1			V
Output-Low Voltage	V_{OL}	SMBUS_DATA, sinking 4mA			0.4	V
External-Pullup Voltage	V_{OH} Max				5.5	V
$\overline{\text{SMBUS\_ALERT}}$ PIN						
Output-Low Voltage	V_{OL}	Sinking 4mA			0.4	V
Leakage Current		For pullup = 5.5V			1	µA
External-Pullup Voltage	V_{OH} Max				5.5	V
FAULT ISOLATION DELAY						
Fault-Detection Time	t_D	From fault detection to start of gate pulldown		60		ns
Pass FET Turn-Off Time	t_F	From start of gate pulldown to pass FET off		50		ns
$\overline{\text{FAULT}}$ PIN						
$\overline{\text{FAULT}}$ Input-High Voltage	V_{IH}		1			V
$\overline{\text{FAULT}}$ Input-Low Voltage	V_{IL}				0.66	V
$\overline{\text{FAULT}}$ Output-High Voltage	V_{OH}	External pullup, leakage below 1µA			5.5	V
$\overline{\text{FAULT}}$ Output-Low Voltage	V_{OL}	Sinking 4mA			0.4	V
Propagation Delay from Fault Detect to $\overline{\text{FAULT}}$ Asserted Low	t_d				140	ns
V_{IN} OVERVOLTAGE DETECTION						
Programmable Threshold for OV	V_{IN_OV}	PMBus programmable, default 16V (Note 1)		14		V
				16		
				17		
				18		
Deglitching Time	t_{FILTER_OV}			20		µs
Deglitching Time Accuracy				±5		%

Electrical Characteristics (continued)

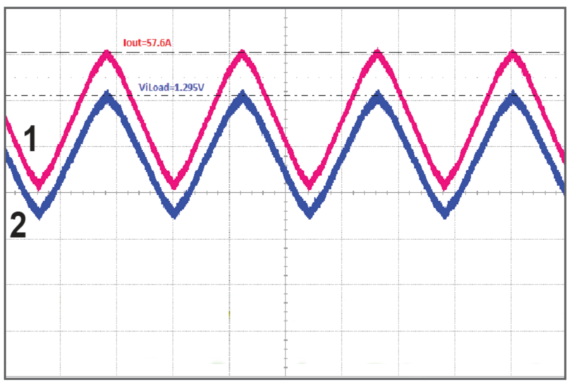
(V_{IN} = 12V ±10%, T_A = T_J = 0°C to +125°C, unless otherwise noted. Specifications are 100% production tested at T_A = T_J = +32°C. Limits over operating temperature are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT REPORTING (ILOAD) PIN						
Linear I_{OUT} Reporting Range		Current reporting range from single MAX16545B/C device.	0		70	A
Linear-Voltage Range			0		1.35	V
Offset Current		I_{OUT} = 0A		0.65		µA
Current-Reporting Gain	G_{ILOAD}	ILOAD current divided by I_{OUT} current (Note 1)		5		µA/A
Bandwidth		No capacitor in parallel with R_{LOAD} resistor.	100			kHz
CURRENT REPORTING (ILOAD_IN) PIN						
Linear Current Range. Gain from ILOAD_IN Pin to ILOAD Pin = 1	I_{LOAD_IN}	Only when used with VT503 (Note 2)	0		350	µA
ANALOG CURRENT REPORTING ACCURACY						
Analog Current-Reporting Accuracy	I_{OUT}	I_{OUT} = 60A (Note 2)	-1.3		+1.3	%
		I_{OUT} = 8A (Note 2)	-1.8		+1.8	
SMBus/PMBus TELEMETRY ACCURACY						
Digital Current-Reporting Accuracy	READ_IOUT (8Ch), READ_IIN (89h)	I_{OUT} = 60A (Note 2)	-1.6		+1.6	%
		I_{OUT} = 8A (Note 2)	-2.3		+2.3	
Digital Power-Reporting Accuracy	READ_PIN (97h)	I_{OUT} = 8A, V_{IN} = 12V, R_{LOAD} = 4.5kΩ (Note 2)	-3		+3	%
		I_{OUT} = 60A, V_{IN} = 12V, R_{LOAD} = 4.5kΩ (Note 2)	-2		+2	
Digital Input-Voltage Reporting Accuracy	READ_VIN (88h)		-1		+1	%
Digital Output-Voltage Reporting Accuracy	READ_VOUT (8Bh)	10.8V < V_{OUT} < 13.2V	-1		+1	%
		8V < V_{OUT} < 10.8V	-3		+3	
Digital-Temperature Reporting Accuracy	READ_ TEMPERATURE _1 (8Dh)	(Note 2)	-6		+6	°C
Digital-Energy Reporting Accuracy	READ_EIN (86h)	I_{OUT} = 60A	-2.5		+2.5	%
		I_{OUT} = 8A	-4.6		+4.6	

Note 1: Denotes specifications that apply for typical operating junction temperature (T_A = T_J = +32°C).
Note 2: Reporting accuracy presented includes 0.1% external resistor tolerance contribution.

Typical Operating Characteristics

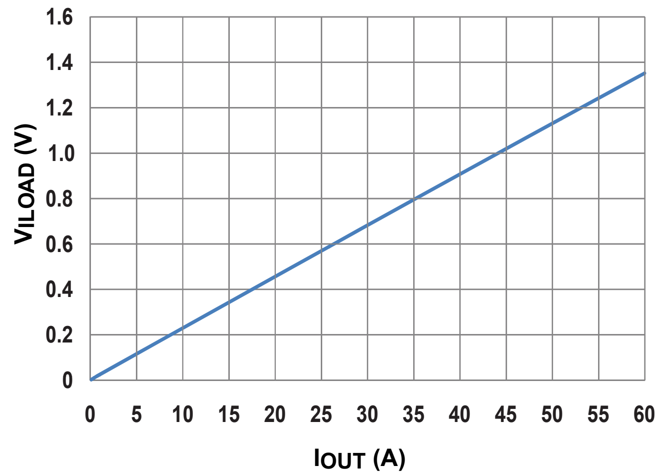
Output Current Monitoring and Reporting - Frequency Response



Time/div: 500µs

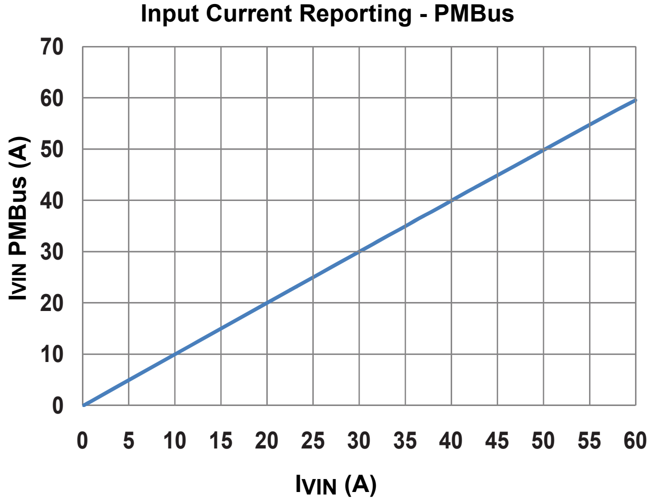
Conditions: I_{OUT} = 0A to 60A
1: I_{OUT} (20A/div)
2: V_{ILOAD} (500mV/div)

Output Current Monitoring and Reporting - Linearity



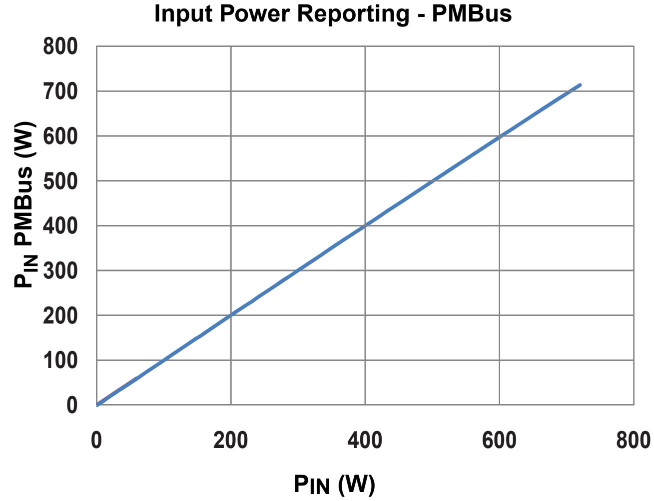
Conditions: R_{ILOAD} = 4.53kΩ (0.1%)
I_{OUT} = 0A to 60A

Input Current Reporting - PMBus



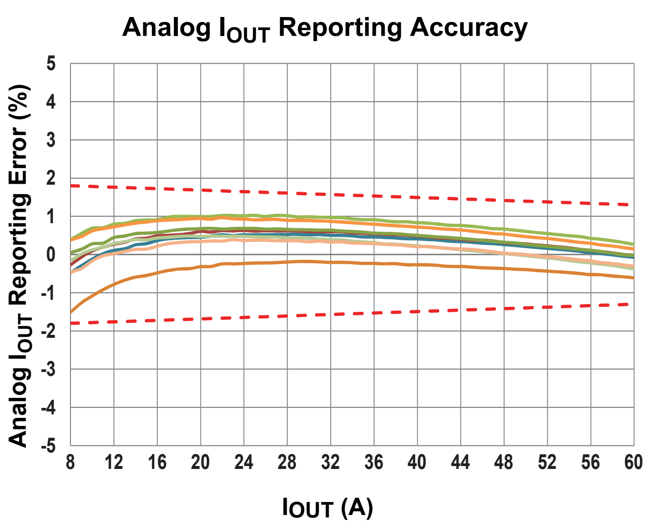
Conditions: I_{OUT} = 0A to 60A
V_{IN} = 12V
Reporting of PMBus Register 89h

Input Power Reporting - PMBus

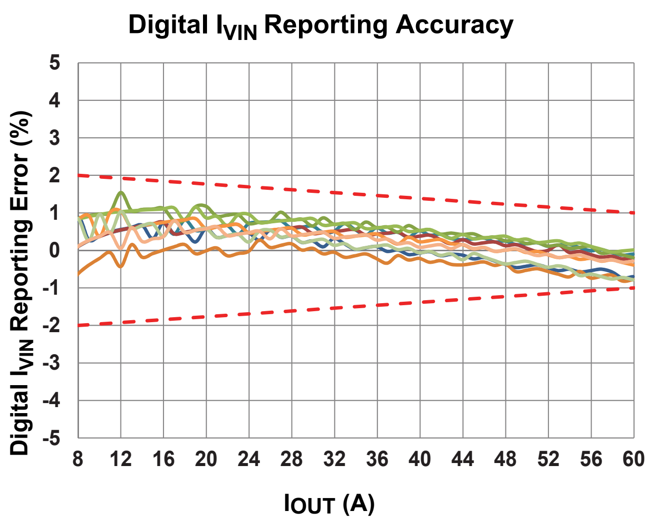


Conditions: I_{OUT} = 0A to 60A
V_{IN} = 12V
Reporting of PMBus Register 97h

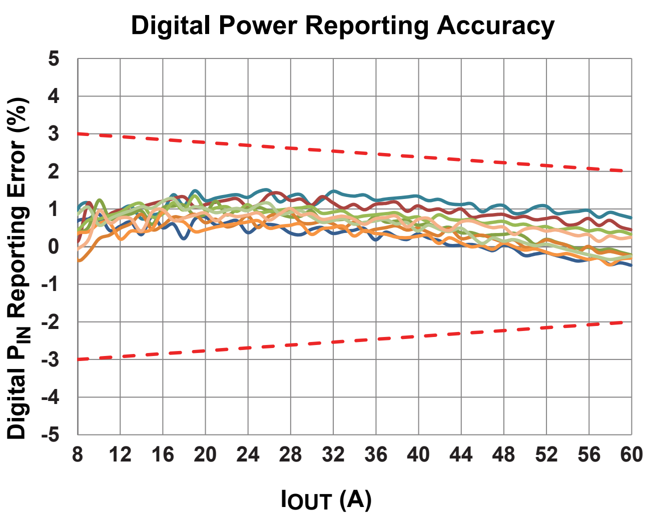
Typical Operating Characteristics (continued)



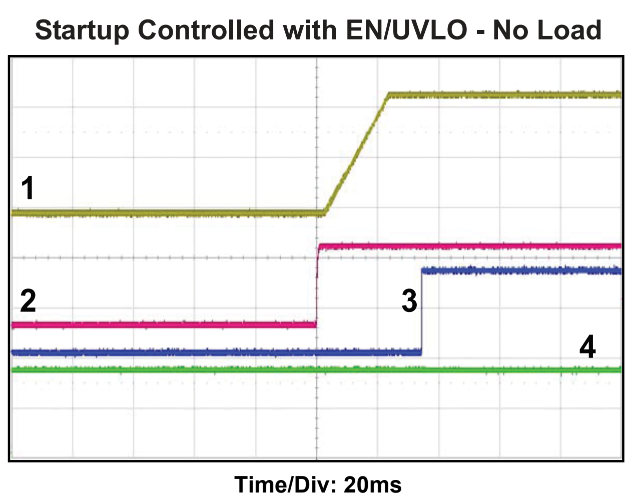
Conditions: I_{OUT} = 0-60A
V_{IN} = 12V
R_{ILOAD} = 4.53kΩ (0.1%)
Data on 8 Samples
Limits as defined in EC table



Conditions: I_{OUT} = 0A to 60A
V_{IN} = 12V
R_{ILOAD} = 4.53kΩ (0.1%)
Data on 8 Samples
Limits as defined in EC table



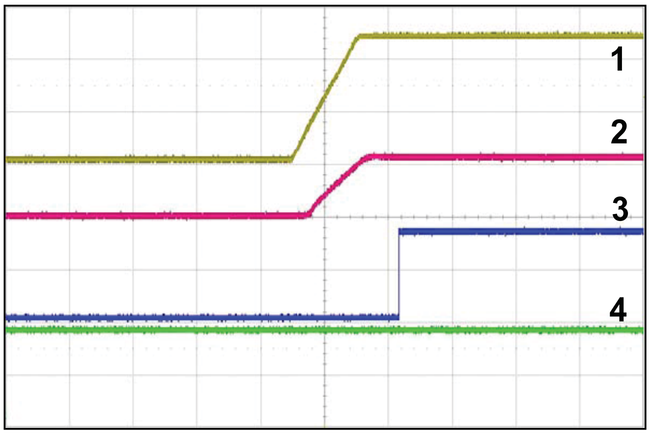
Conditions: I_{OUT} = 0-60A
V_{IN} = 12V
R_{ILOAD} = 4.53kΩ (0.1%)
Data on 8 Samples
Limits as defined in EC table



Conditions: C_{SS} = 47nF
C_{OUT} = 2 x 180µF + 6 x 10µF + 2 x 2.2µF
1. V_{OUT} (5V/div)
2. EN/UVLO (1V/div)
3. PWRGD (2V/div)
4. $\overline{FAULT}$ (2V/div)

Typical Operating Characteristics (continued)

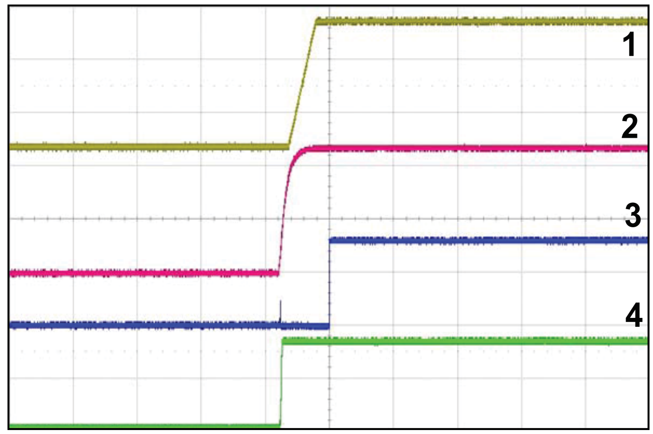
Startup Into Load, Controlled with EN/UVLO - 1Ω Resistive Load



Time/Div: 10ms

Conditions: R_{LOAD} = 1Ω, Present at Startup
C_{SS} = 22nF
C_{OUT} = 2 x 180µF + 6 x 10µF + 2 x 2.2µF
1. V_{OUT} (5V/div)
2. I_{OUT} (10A/div)
3. PWRGD (2V/div)
4. $\overline{FAULT}$ (2V/div)

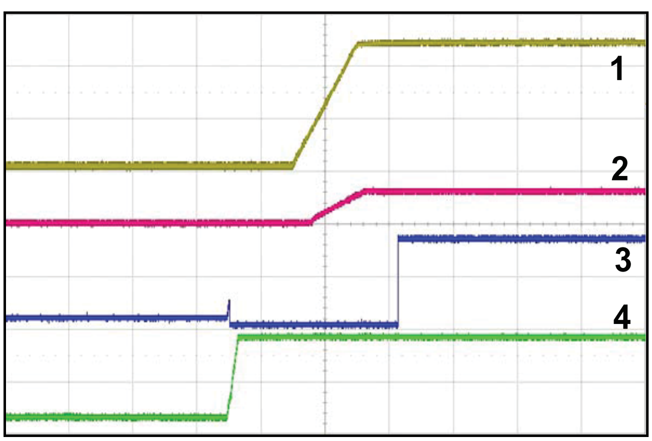
Startup Controlled with V_{IN} - No Load



Time/Div: 50ms

Conditions: C_{SS} = 47nF
C_{OUT} = 2 x 180µF + 6 x 10µF + 2 x 2.2µF
No Load at Startup
1. V_{OUT} (5V/div)
2. V_{IN} (5V/div)
3. PWRGD (2V/div)
4. $\overline{FAULT}$ (2V/div)

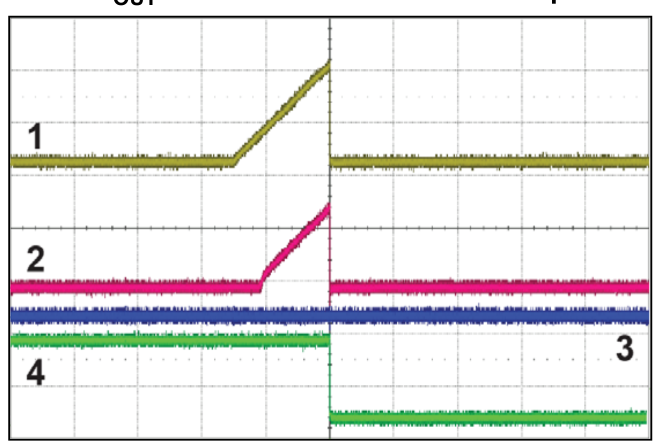
Startup Into Load, Controlled with V_{IN} - 1Ω Resistive Load



Time/Div: 10ms

Conditions: C_{SS} = 22nF
C_{OUT} = 4 x 330µF + 2 x 180µF + 1 x 10µF + 1 x 2.2µF
R_{LOAD} = 1Ω Present at Startup
1. V_{OUT} (5V/div)
2. I_{OUT} (20A/div)
3. PWRGD (2V/div)
4. $\overline{FAULT}$ (2V/div)

Start Into Short Condition - V_{OUT} to GND Short Present at Startup

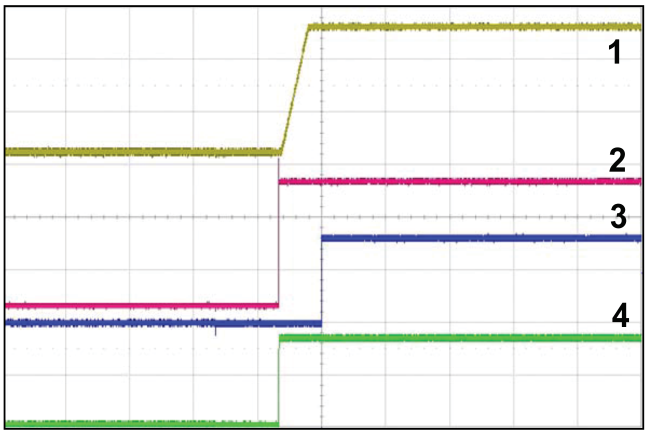


Time/Div: 500µs

Conditions: V_{OUT} Shorted to GND Prior to Startup
1. V_{OUT} (5V/div)
2. I_{VIN} (10A/div)
3. PWRGD (2V/div)
4. $\overline{FAULT}$ (2V/div)

Typical Operating Characteristics (continued)

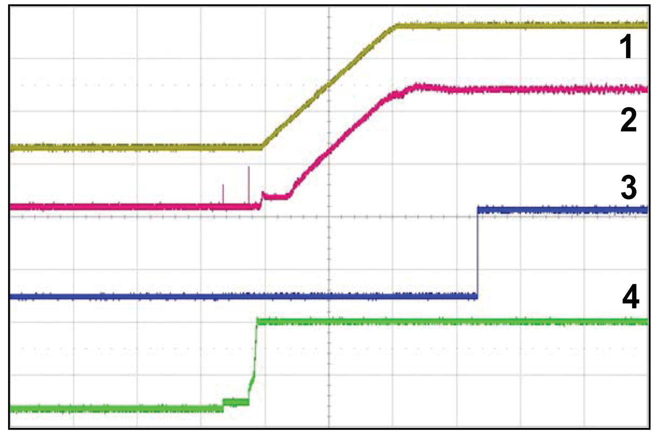
Hot Swap Startup - No Load



Time/Div: 50ms

Conditions: C_{SS} = 47nF
No Input Capacitors
C_{OUT} = 2 x 180µF + 6 x 10µF + 2 x 2.2µF
No Load Present at Startup
1. V_{OUT} (5V/div)
2. V_{IN} (5V/div)
3. PWRGD (2V/div)
4. $\overline{\text{FAULT}}$ (2V/div)

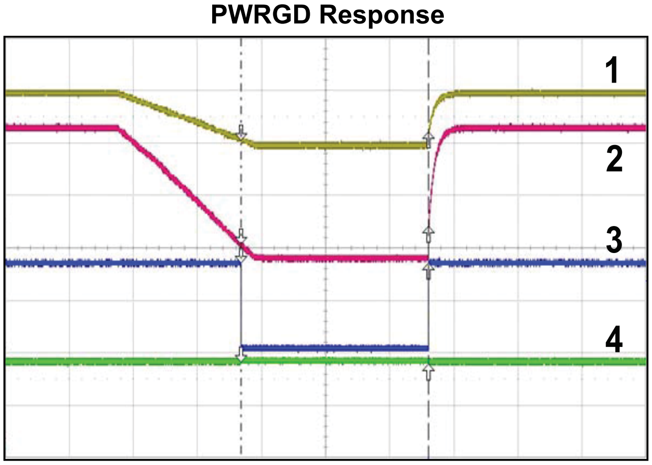
Hot Swap Startup Into Load - 1Ω Resistive Load



Time/Div: 5ms

Conditions: C_{SS} = 22nF
No Input Capacitors
C_{OUT} = 4 x 330µF + 2 x 180µF + 1 x 10µF + 1 x 2.2µF
R_{LOAD} = 1Ω Present at Startup
1. V_{OUT} (5V/div)
2. I_{OUT} (5A/div)
3. PWRGD (2V/div)
4. $\overline{\text{FAULT}}$ (2V/div)

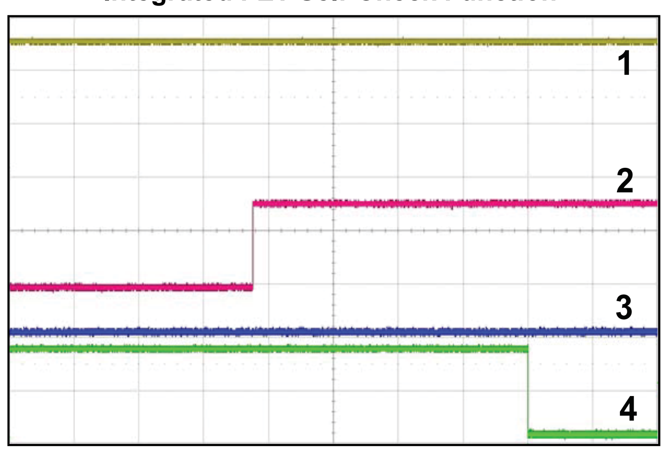
PWRGD Response



Time/Div: 50ms

Conditions: C_{SS} = 47nF
PWRGD Threshold = 8V
V_{IN_UVLO} Threshold = 6.2V
No Load
1. V_{OUT} (5V/div)
2. V_{IN} (2V/div)
3. PWRGD (2V/div)
4. $\overline{\text{FAULT}}$ (2V/div)

Integrated FET Self-Check Function

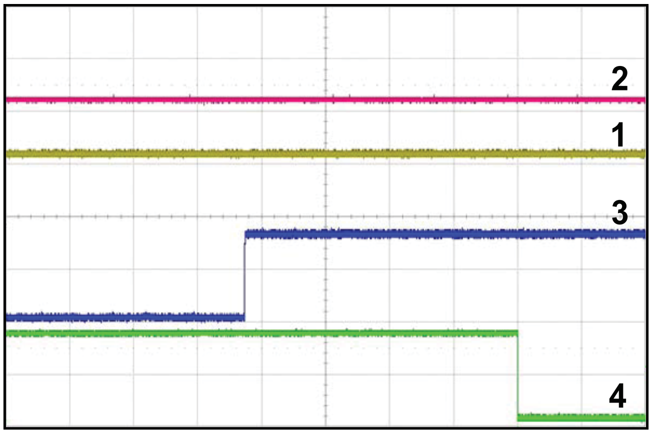


Time/Div: 500ms

Conditions: V_{OUT} Shorted to V_{IN} Prior to Startup
1. V_{OUT} (5V/div)
2. EN/UVLO (1V/div)
3. PWRGD (2V/div)
4. $\overline{\text{FAULT}}$ (2V/div)

Typical Operating Characteristics (continued)

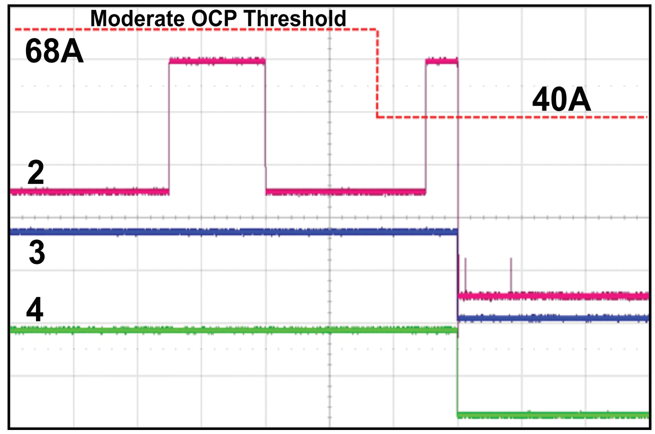
C_{SS} Discharge Fail Protection



Time/Div: 500ms

Conditions: C_{SS} = 47nF
SS Shorted to V_{IN} Prior to Startup
1. V_{OUT} (5V/div)
2. SS (5V/div)
3. EN/UVLO (1V/div)
4. $\overline{FAULT}$ (2V/div)

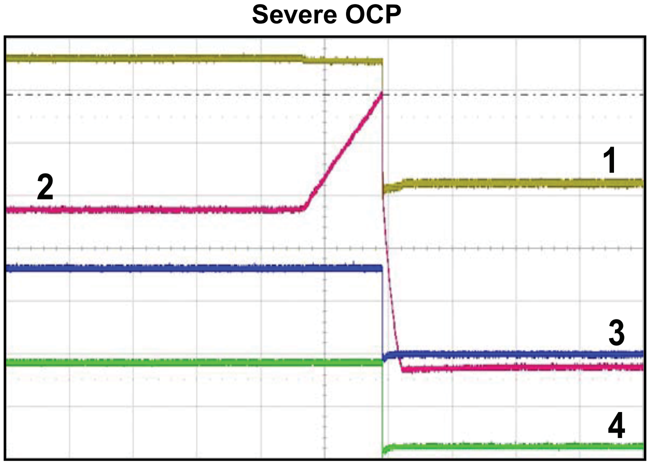
R_{OCP} Change During Operation



Time/Div: 200ms

Conditions: OCPM_High = 68A
OCPM_LOW = 40A
I_{OUT} = 20A to 45A
0.05A/µs
t = 600ms
Moderate OCP Timeout = 100ms
2. I_{OUT} (10A/div)
3. PWRGD (2V/div)
4. $\overline{FAULT}$ (2V/div)

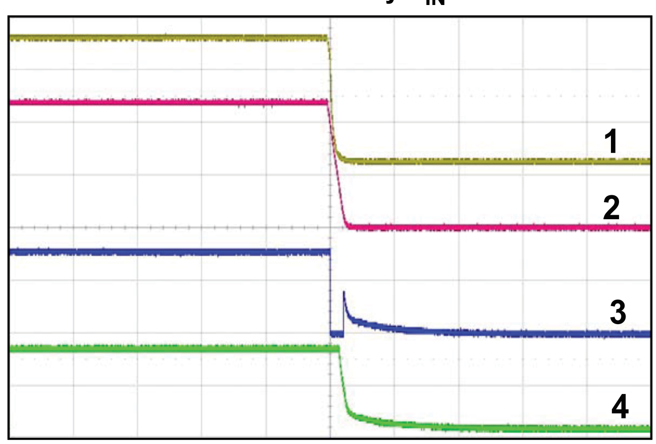
Severe OCP



Time/Div: 200µs

Conditions: I_{OUT} = 60A to 120A
OCPM = 68A
Moderate OCP Timeout = 250ms
Severe OCP Setting = 130%
1. V_{OUT} (5V/div)
2. I_{OUT} (20A/div)
3. PWRGD (2V/div)
4. $\overline{FAULT}$ (2V/div)

Shutdown Controlled by V_{IN} - No Load

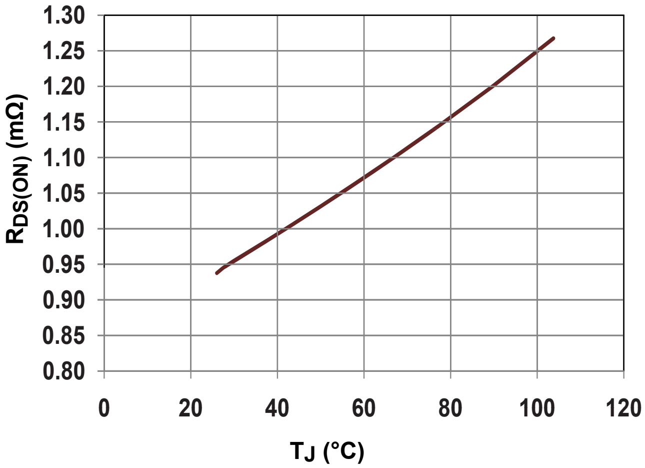


Time/Div: 1s

Conditions: I_{OUT} = 0A
$\overline{FAULT}$ and PWRGD Pullup Voltages Derived From 12V Supply
1. V_{OUT} (5V/div)
2. V_{IN} (5V/div)
3. PWRGD (2V/div)
4. $\overline{FAULT}$ (2V/div)

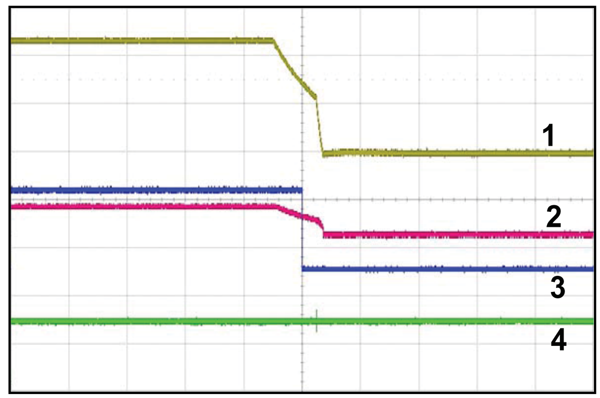
Typical Operating Characteristics (continued)

ON Resistance Including Package Resistance



Conditions: $R_{DS(ON)}$ vs. T_J measurements taken at T_A = 25°C,
No Airflow
No Heatsink

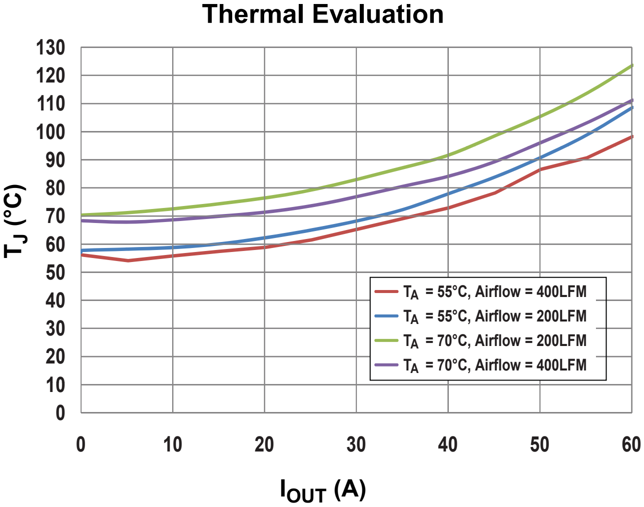
Shutdown Controlled by V_{IN}, 1Ω Resistive Load



Time/Div: 20ms

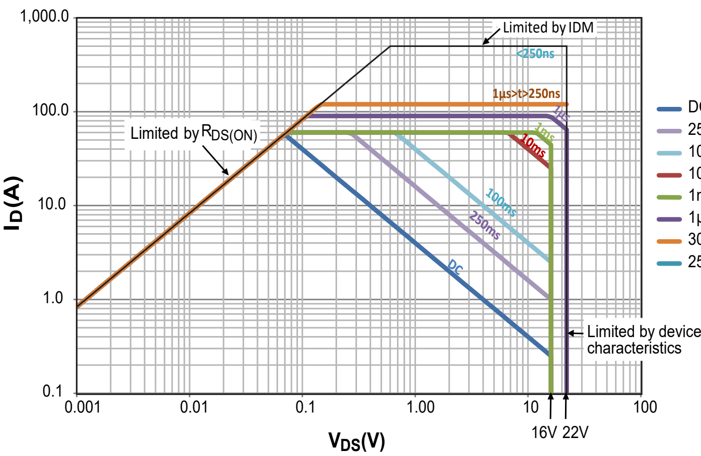
Conditions: R_{LOAD} = 1Ω
1. V_{OUT} (5V/div)
2. I_{OUT} (20A/div)
3. PWRGD (2V/div)
4. $\overline{FAULT}$ (2V/div)

Thermal Evaluation



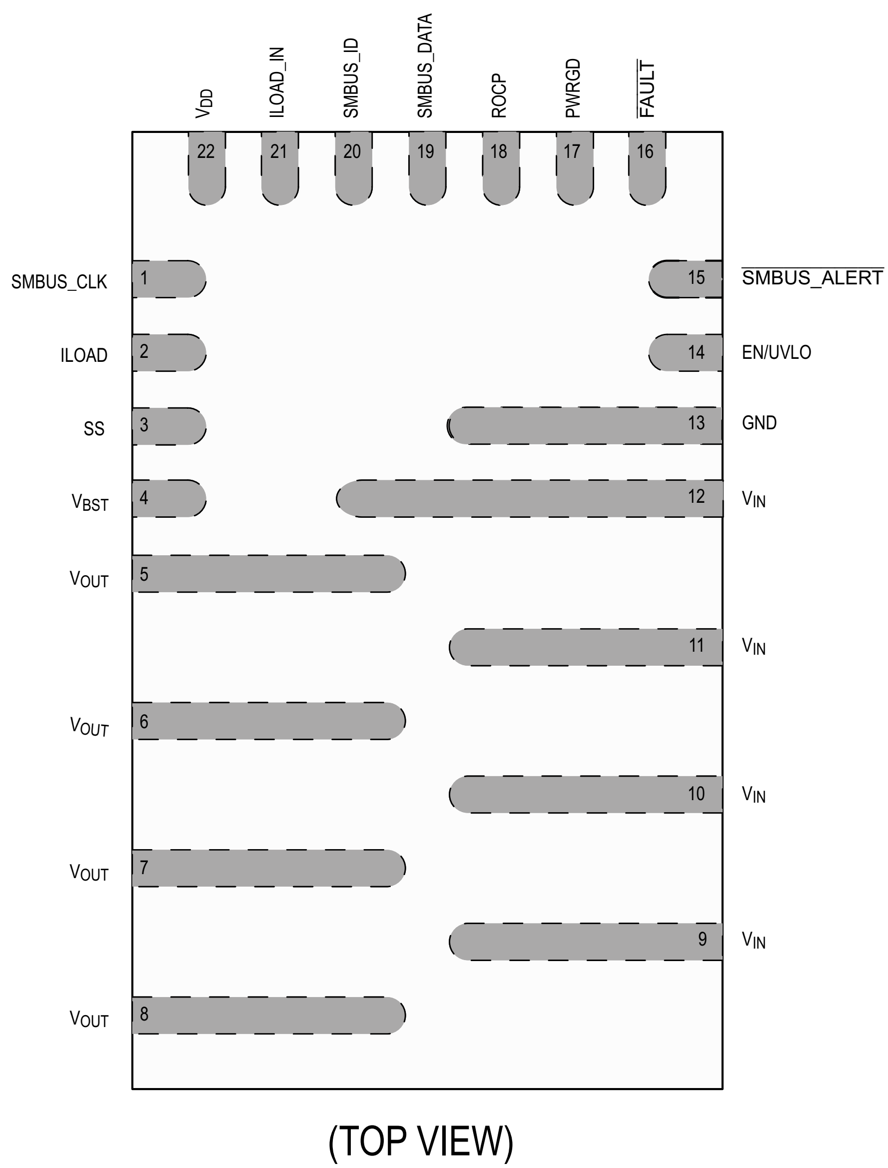
Conditions: I_{OUT} = 0A to 60A
Thermal Evaluation was performed on Maxim's evaluation board
No Heatsink

Single-Pulse Operating Area (SOA)



Conditions: T_J = 105°C

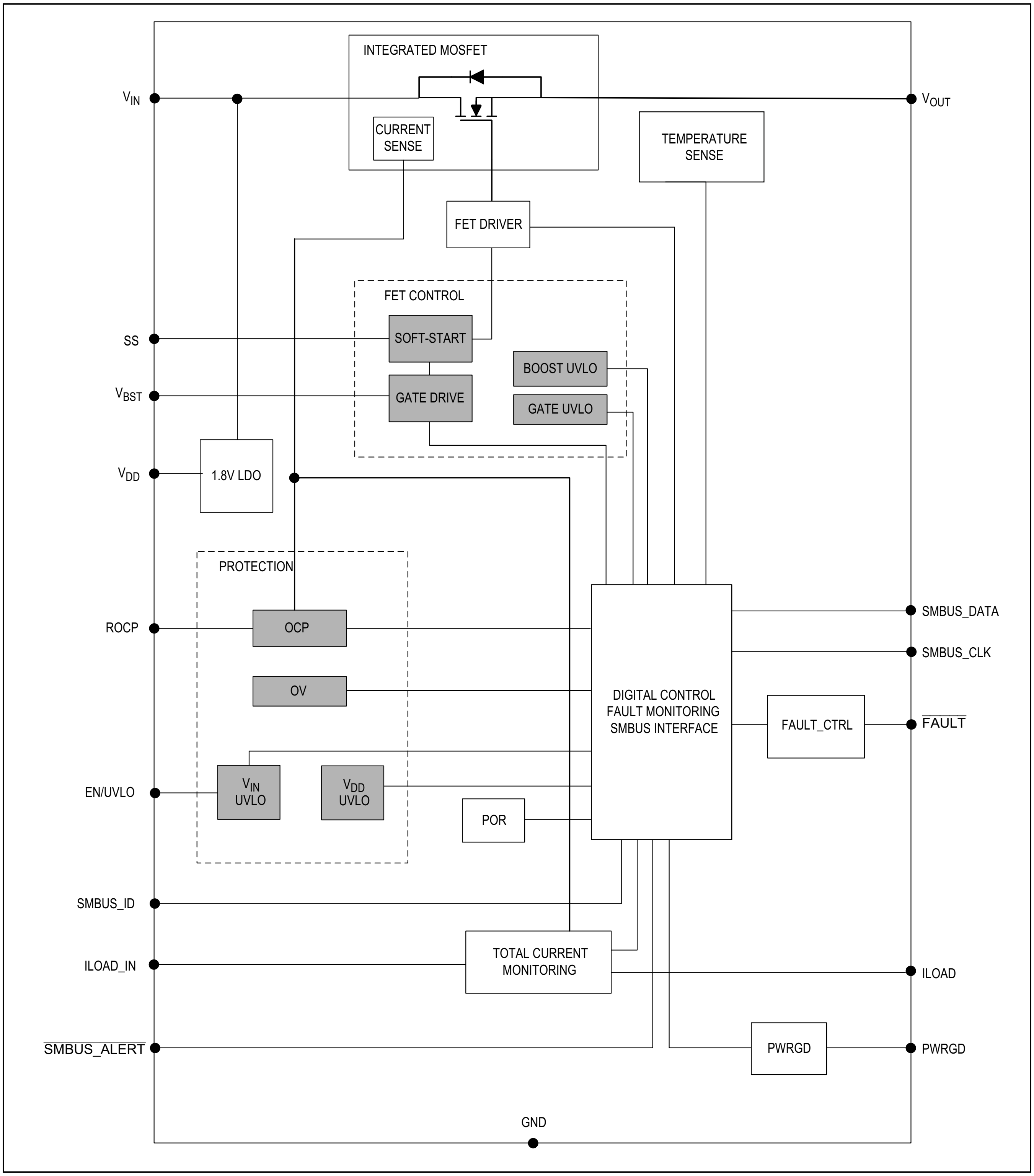
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	SMBUS_CLK	SMBus Clock Node.
2	ILOAD	Analog Current Representation of the Load Current. Connect this pin to ground through a properly sized resistor for proper voltage representation. Always keep this pin connected to ground through a resistor. A capacitor parallel to the R_{ILOAD} resistor is required (see Figure 6 for the recommended value).
3	SS	Soft-Start Node. A capacitor is connected from SS to GND to program soft-start. The soft-start program capacitor should not exceed 75nF. If a fast-load transient (di/dt > 2.5A/ms) resulting in fast and large transient output voltage deviation is possible in the application, an additional capacitor between SS and V_{OUT} is recommended to keep the pass FET V_{GS} above its UVLO threshold.
4	V_{BST}	Charge-Pump Supply for Pass FET Gate Drive. Connect this node to V_{OUT} through a 220nF bypass capacitor. This supply is designed to be used by the MAX16545B/C and the MAX16543 only. No additional load or external components other than a bypass capacitor are allowed on the BST pin.
5-8	V_{OUT}	12V Output Power—Load Side.
9-12	V_{IN}	12V Input Power—Power Supply Side.
13	GND	Ground. Connect this node to GND plane through vias for proper operation.
14	EN/UVLO	12V Input Voltage UVLO pin. Normally connected to the center node of a resistor-divider connected from V_{IN} to ground. A properly sized capacitor can be placed in parallel to the bottom resistor of the resistor-divider for additional filtering. In addition to 12V UVLO programming, this node can be used to enable/disable the MAX16545B/C.
15	$\overline{\text{SMBUS\_ALERT}}$	SMBus Alert. Open-drain, active-low pin.
16	$\overline{\text{FAULT}}$	Fault Communication (Bidirectional) Pin. This pin is used to indicate/receive detection of latching fault. See the *FAULT Reporting* section for more details. Connect this pin to the system bias supply rail through a 10kΩ resistor. 5V compliant, active-low pin.
17	PWRGD	Report V_{IN} and V_{OUT} status. See the *Power Good (PWRGD) Output* section for more details. Connect this pin to system bias supply rail through a 10kΩ resistor. 5V compliant.
18	ROCP	Moderate OCP Threshold Programming Input. Connect this pin to GND using an appropriate programming resistor. See the *Moderate OCP Threshold* section for additional details. No other components are allowed on this pin.
19	SMBUS_DATA	SMBus Data Node.
20	SMBUS_ID	SMBus Address Programming and Current Hysteresis Flag. Connect this pin to GND through a properly sized resistor to select desired address setting.
21	ILOAD_IN	System Current Reporting Input Pin. If current reporting from a single MAX16545B/C device is desired, connect this pin to GND through a 10kΩ resistor. Use this pin to sum currents from up to two MAX16543 devices if used in higher-current applications. In this case, the connection from the ILOAD pin of MAX16543 to ILOAD_IN of MAX16545B/C should be made through a 500Ω resistor. Refer to the *MAX16543 Follower Device* section for details.
22	V_{DD}	Internal 1.8V Linear Regulator (LDO) Output. Connect this pin to GND through a 1μF (or higher) capacitor. See Figure 6 for the correct value. No additional loads or components other than up to two MAX16543 devices and external properly sized capacitor are allowed on the V_{DD} pin.

Block Diagram



Theory of Operation

The MAX16545B/C integrated circuit-breaker IC is designed to provide a complete single-chip circuit-breaker protection solution for the 12V power bus, in applications where a power supply is either permanently connected (no removable assemblies), or is connected and disconnected at the input side only. It combines power monitoring and control functions with a low on-resistance pass FET device that acts as a disconnect switch to limit maximum power distributed to the load. The IC implements proprietary integrated lossless current sensing techniques to provide a highly accurate and compact circuit-breaker protection solution. The device integrates PMBus/SMBus interface for digital control and monitoring.

An integrated N-channel power MOSFET is driven by the FET control circuit that includes a boost circuit to provide a gate drive. An internal LDO provides V_{DD} bias supply, enabling effective use of the device in input hot-swap applications. See the *Block Diagram*.

Startup

The MAX16545B/C enables the integrated 1.8V V_{DD} LDO once the 12V supply voltage is high enough to guarantee LDO operation. Once V_{DD} is valid, the device reads the SMBus_ID programming resistor value to set the SMBus address, and initiates itself. During this period, the gate drive supply capacitor becomes fully charged. Once these two functions are complete, the device can be controlled through the enable input.

The enable input (EN/UVLO) has a precise threshold and provides a V_{IN_UVLO} function, where the enable voltage is derived from V_{IN} through a resistor-divider, with an optional control signal used in conjunction with the divider as shown in Figure 1 and Figure 5. The EN/UVLO pin must not be pulled high externally other than to pull the EN/UVLO pin high through a properly sized resistor-divider from the input supply. Though the enable signal can be pulled low to disable the part, this should only be allowed to occur when the input voltage supply is within operating range specified in *Electrical Characteristics* table.

Safe Operating Area (SOA)

During soft-start, it is important to keep the FET within its safe operating area. The peak current allowed during startup is shown in Figure 2. In case resistive short is possible in the application, it is required to use startup OCP feature to protect the device. The MAX16545B has a default startup OCP of 16A, and the MAX16545C has a default startup OCP of 24A. The startup OCP threshold must be programmed to a value lower than safe peak current. Figure 2 assumes pure capacitive or RC load on the output.

During normal operation, V_{GS_UVLO} ensures FET is operating in deep triode region while three levels of OCP limit the device operating current within safe boundaries. Refer to the SOA curves under *Typical Operating Characteristics* for more detail.

Self-Check

Once V_{BST_UVLO} has been cleared, the internal V_{DD_LDO} is fully enabled and the EN/UVLO pin is above the enable threshold, the MAX16545B/C initiates a timed output discharge as a self-check procedure. By default, the device initiates this procedure immediately after V_{BST_UVLO} has been cleared and the internal V_{DD_LDO} is fully enabled. If the output does not fall below the programmed self-check threshold after a fixed period, the pass FET could be potentially shorted and the IC asserts both $\overline{FAULT}$ and PWRGD pins low. The latched fault condition remains until restart (EN/UVLO, V_{IN} toggling or restarting through the OPERATION command). The threshold for the self-check procedure can be programmed to one of four different values through the SMBus. See the Config Register (D0h) for more details. If the output voltage is below the programmed self-check threshold, the self-check is considered passed and the device proceeds with startup.

Because the device actively discharges the output when disabled, it should not be used in applications where the output can remain powered through another path.

In addition a soft-start capacitor discharge procedure is performed during every restart. The MAX16545B/C utilizes an integrated resistive element, with resistance approximately 1kΩ, to discharge the C_{SS} capacitor. The device checks if the voltage across the C_{SS} capacitor is below the soft-start threshold shown in the *Electrical Characteristics* table after a fixed period of time. If the voltage across the C_{SS} capacitor is not below the soft-start threshold, the device latches the pass FET OFF and asserts the $\overline{FAULT}$ pin low.

The MAX16545B/C checks the R_{OCP} value at all times, including startup (after the bias supply is valid). This check ensures proper moderate OCP threshold selection. If the wrong R_{OCP} value is detected, the device reports the fault by asserting the $\overline{FAULT}$ signal low. Each latched fault condition is kept until restart (EN/UVLO, V_{IN} toggling or restarting through the OPERATION command).

Soft-Start

Once the self-check procedure is complete, the output voltage soft-start ramp is initiated. During startup, the C_{SS} capacitor is charged using a constant current source. Since the integrated FET is configured as a source follower, the output voltage is ramped monotonically at a rate determined by the external soft-start capacitor. The soft-start capacitor should not exceed 75nF.

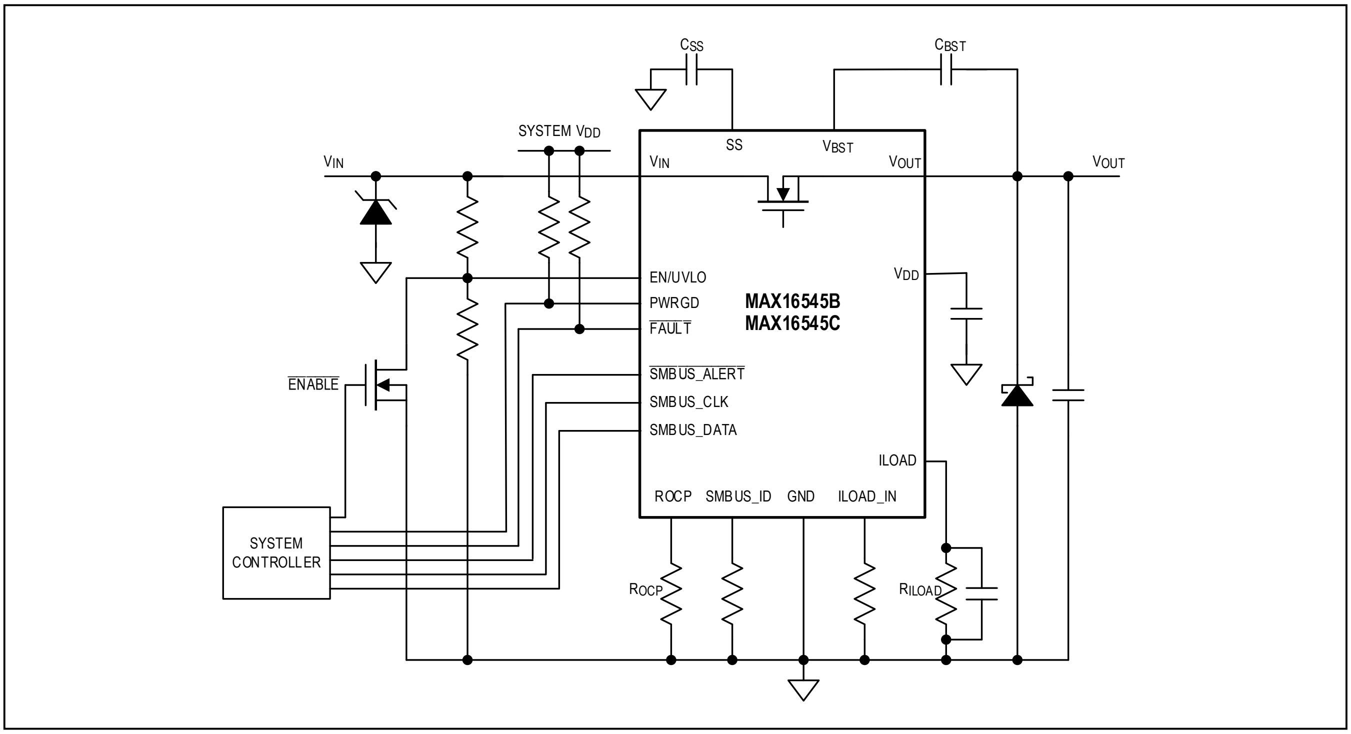


Figure 1. Configuration Example

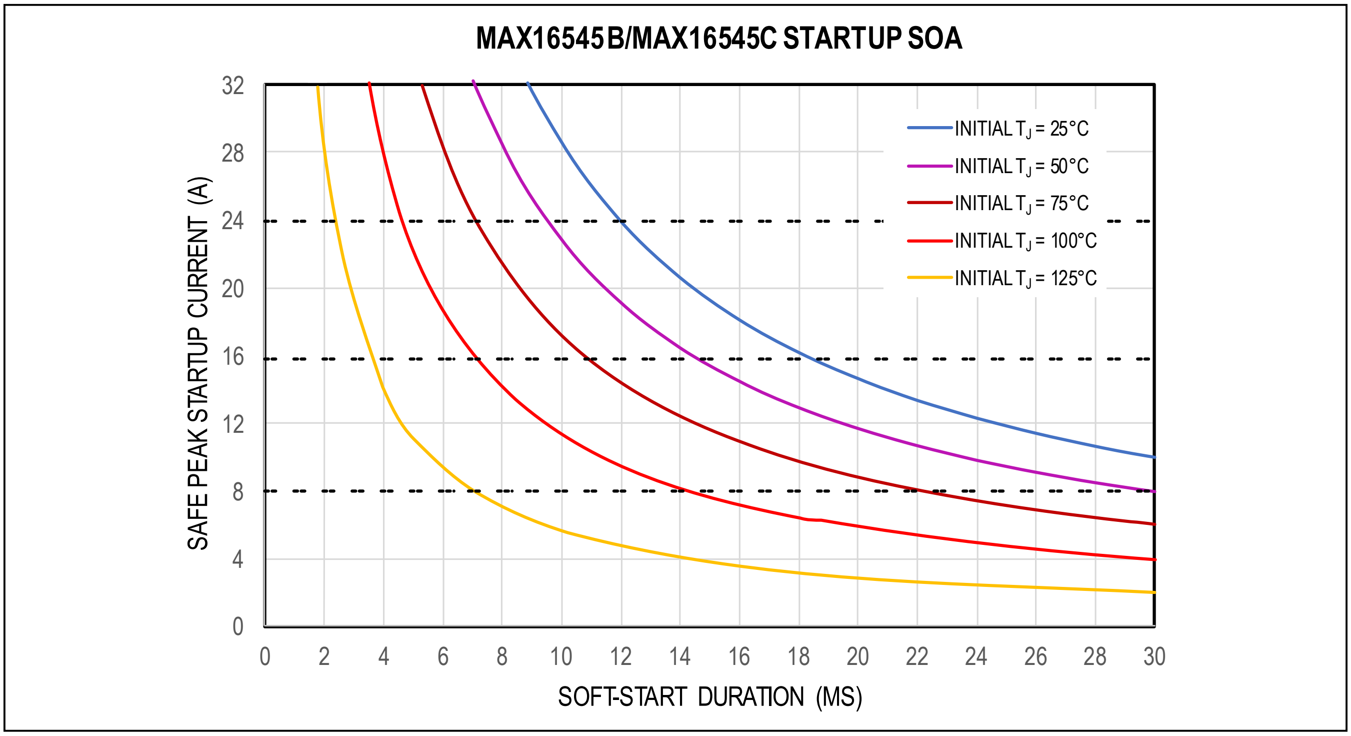


Figure 2. Startup SOA

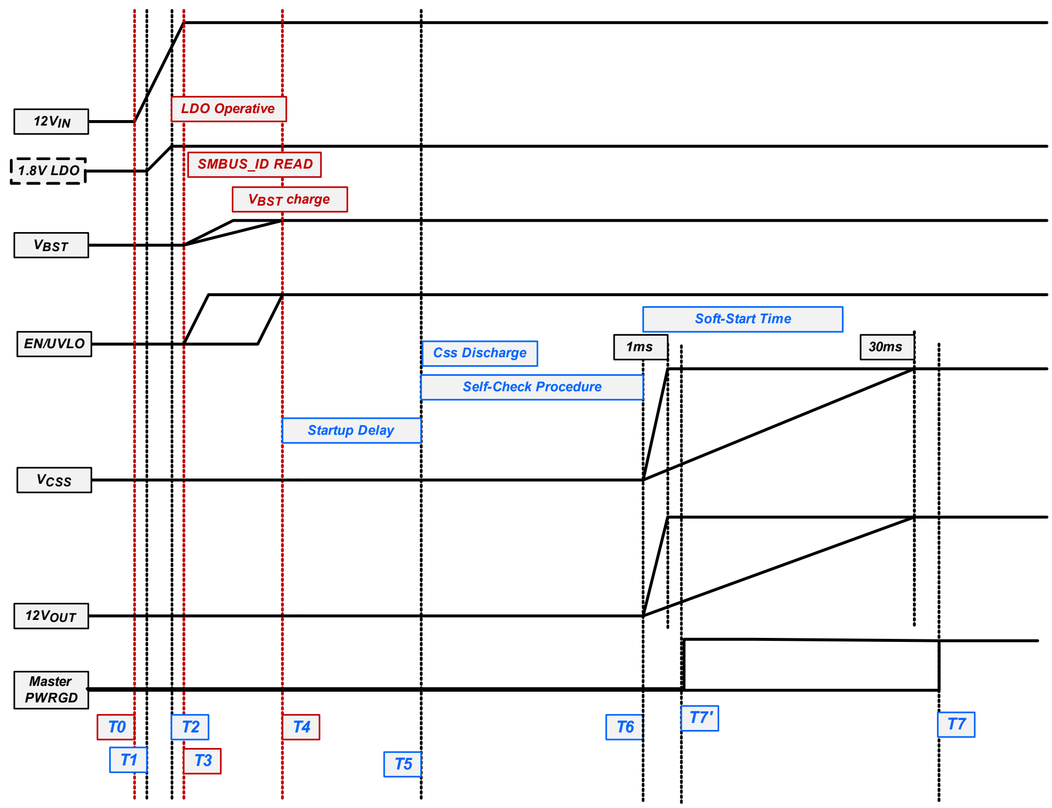


Figure 3. Startup Timing Diagram

V_{DD} Undervoltage Lockout

The MAX16545B/C implements V_{DD_UVLO} fault monitor and protection. V_{DD} is monitored at all times. Startup procedures are not initiated until V_{DD_UVLO} is cleared. If V_{DD} falls below V_{DD_UVLO} during normal operation, the part shuts down. Once V_{DD} returns to acceptable values, the part performs a turn-on procedure from soft-start delay phase.

Current Hysteresis

SMBUS_ID pin is used as current hysteresis flag after R_{SMBus_ID} decoding is done. If output current is greater than MFR_SPECIFIC_HYSTH level, the current hysteresis flag is set to high. If output current is less than MFR_SPECIFIC_HYSTL level, then the current hysteresis flag is set to low.

SMBus_ID Resistor Out of Range

After V_{DD_UVLO} is cleared, the SMBus_ID programming resistor is read. If it is out of range, a latching fault is tripped. This fault can be cleared by EN/UVLO, V_{IN} toggling, or restarting through the OPERATIONS command. The EN/UVLO toggling may mean pulling EN/UVLO above the threshold and then low after the fault is detected to reset the fault latch. The value is read again when EN/UVLO goes high for the second time.

V_{BST} and V_{GS} UVLO

V_{BST_UVLO} is checked when EN/UVLO is above the enable threshold and remains active while the device is enabled. The V_{BST_UVLO} can also be tripped before the FET is turned on, the latching fault can still be reset by EN/UVLO or V_{IN} toggling or restarting through the OPERATION command. The gate drive (V_{GS}) UVLO protection has 10μs internal deglitching filter to prevent false tripping due to output voltage overshoot if a large, fast-unloading transient is present. If additional filtering is desired, an external capacitor can be placed between V_{OUT} and V_{SS} pins. V_{BST} and V_{GS} UVLO are latching faults, which result in the pass FET being latched off and $\overline{FAULT}$ asserted low. V_{GS_UVLO} is masked for 100ms during startup to avoid tripping a latching fault.

V_{IN_UVLO}

The V_{IN} is sensed at the EN/UVLO pin through a resistor-divider that is used to program the desired V_{IN_UVLO} threshold. The V_{IN_UVLO} circuit has hysteresis, and if the EN/UVLO pin voltage falls below the programmed value during operation, the device turns the integrated FET off and PWRGD is deasserted. The integrated FET turns on again if the positive threshold is exceeded and performs self-test and soft-start. The MAX16545B/C supports V_{IN_UVLO} warning and fault reporting through PMBus.

Overvoltage Detection

The input voltage is constantly monitored, and if at any time it rises above PMBus programmed threshold, the Power-Good output is de-asserted.

Overcurrent Detection

The IC actively monitors load current on a 12V power bus at all times, including startup. Startup overcurrent proection (OCP) is active during startup. The startup OCP threshold can be changed to one of three programmable options using PMBus. Note that changing the startup OCP to a higher value can violate the startup SOA, in such cases, t_{SS} needs to be lowered to remain in SOA (Figure 2). If, at any time during startup, the load current exceeds the programmed startup OCP threshold, the integrated pass FET is turned off within 10µs and the $\overline{FAULT}$ pin is asserted low. This is a latching fault. The device provides three levels of overcurrent protection during normal operation (after the startup procedure is complete and the PWRGD flag is set high). The moderate OCP threshold is set using an external resistor and is therefore programmable over a wide continuous range. Moderate OCP threshold can be exceeded for a limited, programmable, timeout period without resulting in a fault condition. If the load current on the 12V power bus exceeds the moderate OCP threshold for the entire timeout period, but its magnitude is less than a programmable severe overcurrent threshold (Table 3), the integrated pass FET is latched off at the end of the timeout period and the $\overline{FAULT}$ pin will be asserted low to indicate a moderate OCP fault condition. Restarting the system requires EN/UVLO or V_{IN} toggling or restarting through the OPERATION command. Moderate OCP timeout is user programmable through PMBus with four different values.

Severe OCP is the second level of OCP. Severe OCP threshold is programmed relative to moderate OCP threshold. Fixed 10µs timeout is supported for the severe OCP. If at any time the load current exceeds the severe OCP threshold and the timeout is disabled, the device turns the integrated pass FET OFF and asserts the $\overline{FAULT}$ low. If timeout is enabled, the MAX16545B/C tolerates current exceeding the severe OCP threshold for the duration of the timeout. If the current is still higher than the severe OCP threshold by the end of the timeout, the device turns off and asserts $\overline{FAULT}$ low. Severe overcurrent protection is a latching fault.

The device features a third level of protection against severe overload faults, called safe OCP with internally-fixed threshold. If at any time the load current on a 12V power bus exceeds the safe OCP threshold, the device turns the pass FET OFF within 250ns and asserts the $\overline{FAULT}$ low. The severe OCP threshold should be set to a value less than the safe OCP threshold.

Table 1. Timing Diagram Example Shown in Figure 6

POINT/PERIOD	DESCRIPTION
t0	12V V_{IN} applied.
t1	The LDO has enough headroom to start up.
t2	The internal 1.8V LDO is ready and MAX16545B/C logic is fully operational. External bypass capacitors connected to the V_{DD} pin is fully charged.
t3-t14	SMBus ID resistor reading and V_{BST} charging. EN/UVLO signal status is ignored from T3 to T4.
t4	EN/UVLO is active. Startup check-up procedures can be started after the EN/UVLO is cleared.
t4-t5	User-programmable startup delay.
t5-t6	Self-test procedure. C_{SS} discharge.
t6-t7	V_{OUT} ramp
t7	Power good (PWRGD) output asserted.
t7+	PWRGD is high, normal operation starts.

The IC supports on-the-fly moderate OCP threshold changes. The concept is shown in Figure 4. If the resistance seen by the ROCP pin is changed during operation, the device adjusts the moderate OCP threshold matching the value selected by external resistive network.

Wrong R_{OCP} Protection

The MAX16545B/C is protected against out of range R_{OCP} values. Protection is enabled at any time, including startup. If the R_{OCP} resistor value is detected out of the permitted range, the device latches the integrated FET OFF, and it asserts the $\overline{\text{FAULT}}$ pin low. A EN/UVLO or V_{IN} toggling or a restart through the OPERATION command must be performed in order to clear the fault and restart the device. If R_{OCP} is changing during operation by the system (Figure 4), the design must be such that R_{OCP} is within range at all times.

Note: If the switch that changes OCP threshold is slower to transition, the effective resistance on the ROCP pin can cause severe OCP to trigger during on-the-fly transitions.

Overtemperature Protection (OTP)

The IC includes protection against overtemperature conditions (OTP). If the junction temperature exceeds the programmable fault threshold, the IC latches the integrated FET OFF and asserts the $\overline{\text{FAULT}}$ output low. To reenable the IC, the following options are available:

- Toggle EN/UVLO or V_{IN}
- Restart through the OPERATION command

Overtemperature fault and warning thresholds are user-programmable through the PMBus. Exceeding the overtemperature warning threshold does not latch the FET off.

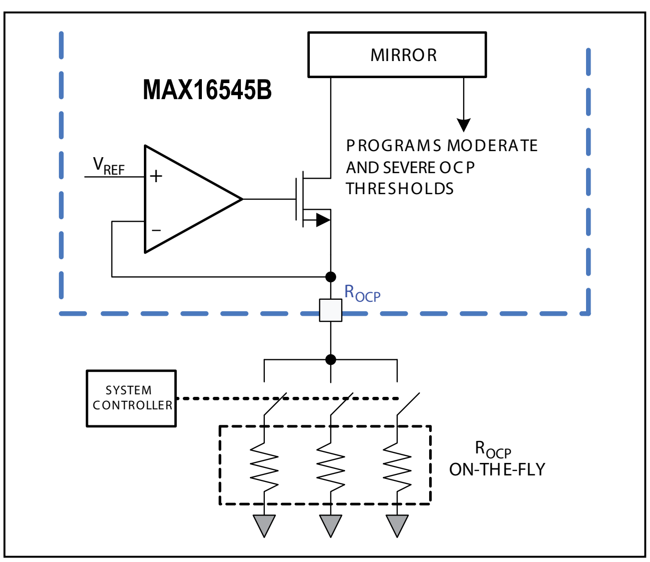


Figure 4. On-the-Fly Analog Programmable Moderate OCP Threshold

$\overline{\text{FAULT}}$ Reporting

The device provides a dedicated pin for fault reporting, $\overline{\text{FAULT}}$. If at any time a latching fault is detected, the $\overline{\text{FAULT}}$ pin is immediately latched low. EN/UVLO or V_{IN} toggling, or a restart through the OPERATION command is required to reset the device after latching fault detection.

Fault Input and $\overline{\text{FAULT}}$ Pullup

The $\overline{\text{FAULT}}$ pin is a bidirectional open-drain pin that can be used for fault communication, from an external circuitry to the MAX16545B/C. To communicate a fault to the device, the external circuitry must pull the $\overline{\text{FAULT}}$ pin low. If $\overline{\text{FAULT}}$ is externally pulled low, the device treats it as a latching fault. Therefore, the pullup voltage source must be considered to ensure the rail is operational and pulled high before the device startup cycle.

These are the options for the pullup rail:

- V_{DD}: 1.8V internal LDO rail. This rail is limited to 1.8V, thus the external system has to be compliant with it.
- System 3.3V or 5V rail. $\overline{\text{FAULT}}$ is 5V compliant, and therefore, an external higher voltage rail can be used for pullup. This rail has to be stable when the device is initiating its startup procedure. If it is not, a false fault communication can occur.

Power Good (PWRGD) Output

The MAX16545B/C provides a dedicated pin for power good reporting (PWRGD). PWRGD is asserted high after startup, when the output voltage exceeds the programmed PWRGD threshold and the FET is fully enhanced and operating in its resistive region. In all the other conditions, the PWRGD pin is deasserted low.

PWRGD is an open-drain pin, thus an external pull-up resistor connected to pullup supply rail is needed. Different options are available for the pullup rail:

- V_{DD}: 1.8V internal LDO rail. This rail is limited to 1.8V, thus the external system has to be compliant with it.
- System 3.3V or 5V rail. PWRGD is 5V compliant, and therefore an external higher voltage rail can be used for pullup.

Analog Load Current Signal Output

The IC includes an output pin, ILOAD to allow the user to monitor the load current device. The current sourced by the ILOAD pin is proportional to the current through the device with the ratio shown in the *Electrical Characteristics* table. A properly sized resistor between the ILOAD pin and GND should be added. A capacitor parallel to this resistor is required for proper operation. The MAX16545B/C reports zero current on the ILOAD pin

Table 2. Faults Detected and Actions

PARAMETER	DESCRIPTION	$\overline{FAULT}$ ASSERTED	LATCHING
V_{DD_UVLO}	Internal V_{DD} LDO UVLO	No	No
V_{BST_UVLO}	UVLO for V_{BST}	Yes (Note 1)	Yes
V_{GS_UVLO}	UVLO for V_{GS}	Yes	Yes
V_{IN_UVLO}	EN/UVLO pin below UVLO threshold	N/A (Note 2)	N/A (Note 2)
V_{IN_UV}	V_{IN} below PMBus programmed threshold	Yes	Yes
ROCP_FAULT	R_{OCP} detected out of valid range	Yes	Yes
R_SMBus_ID FAULT	SMBus_ID resistor detected out of range	Yes	Yes
CSS Discharge FAULT	Soft-start capacitor discharge failed	Yes	Yes
FET Short	Pass FET short detected during startup self-check	Yes	Yes
Startup OCP	Startup overcurrent fault detected	Yes	Yes
Moderate OCP	Moderate overcurrent fault detected	Yes	Yes
Severe OCP	Severe overcurrent fault detected	Yes	Yes
Safe OCP	Safe overcurrent fault detected	Yes	Yes
OTP	Overtemperature fault threshold exceeded	Yes	Yes
V_{IN_OV}	V_{IN} overvoltage detected	No	No

Note 1: If V_{BST_UVLO} fault occurs before startup, $\overline{FAULT}$ is not reported and status registers are not updated.
Note 2: V_{IN_UVLO} clears $\overline{FAULT}$ and the latching event.

during soft-start, it starts reporting load current 5ms after the pass FET V_{GS} is above its UVLO threshold.

If another device reports the current to the MAX16545B/C through the ILOAD_IN pin, the MAX16545B/C reports the total current on the ILOAD pin. When choosing a load resistor to provide a current reporting voltage, the total system current must be considered.

MAX16543 Follower Device

Up to two MAX16543 protection ICs can be used in parallel with the MAX16545B/C to increase total current capability. Specifically,

- MAX16545B/C + 1 × MAX16543, 90A current capability
- MAX16545B/C + 2 × MAX16543, 120A current capability

In these configurations, connect the ILOAD pins of MAX16543 to the ILOAD_IN pin of MAX16545B/C through 500Ω resistors for total current reporting. Refer to the MAX16543 datasheet for more details.

PMBus/SMBus Reporting and Warning

The MAX16545B/C provides PMBus-compliant digital telemetry through the SMBus as shown in Table 4. The IC supports input power and input energy reporting. For average values the sample size is programmable. Peak values for input/output voltage, output current, input power and temperature are stored in dedicated manufacturer-specific registers. The device also provides warning functions based on programmable warning thresholds, as per the PMBus specification. The sample size for warning flags is also programmable.

The device supports fault and status reporting except for V_{BST_UVLO} fault at startup. If the V_{BST_UVLO} occurs at startup the device latches off, $\overline{FAULT}$ is not reported, and status registers are not updated.

Table 3. Requirements for PWRGD Assertion

PARAMETER	CONDITION
V_{OUT}	V_{OUT} > PWRGD threshold
V_{IN}	$V_{IN} > V_{IN\_UVLO}$
Self-Check	MOSFET (V_{IN} to V_{OUT}) short not detected during startup
V_{GS}	FET is on and in triode region. There's a minimum delay of 5ms before PWRGD assertion after this condition is met.

Configuration

The MAX16545B/C is configured using both analog programming resistors and PMBus. See Table 5 and Table 6 for programmable parameters.

Moderate OCP Threshold

The moderate overcurrent protection (OCP) threshold is externally programmable through a resistor connected to the ROCP pin. The moderate OCP threshold is programmed as shown in Equation 1 and Equation 2. See the *Electrical Characteristics* table for V_{OCPM} and GOCP.

Equation 1:

$$I_{OCP} = \frac{V_{OCPM}}{R_{OCP}} \times GOCP$$

where:

I_{OCP} = moderate overcurrent protection threshold (A)

V_{OCPM} = overcurrent protection reference voltage shown in *Electrical Characteristics* table (V)

GOCP = overcurrent protection gain shown in *Electrical Characteristics* table (A/A)

R_{OCP} = Value of overcurrent protection programming resistor (Ω)

Equation 2:

$$R_{OCP} = \frac{V_{OCPM}}{I_{OCP}} \times GOCP$$

where:

I_{OCP} = moderate overcurrent protection threshold (A)

V_{OCPM} = overcurrent protection reference voltage shown in *Electrical Characteristics* table (V)

GOCP = overcurrent protection gain shown in *Electrical Characteristics* table (A/A)

R_{OCP} = Value of overcurrent protection programming resistor (Ω)

Design Example

To set moderate OCP to 68.7A nominal, using Equation 2:

Equation 3:

$$R_{OCP} = \frac{0.8V}{68.7A} \times \left(8 \times 10^{6}\right)$$
$$= 93.1k\Omega$$

Table 4. PMBus/SMBus Reporting

PARAMETER	DESCRIPTION
V_{IN}	Input voltage (PMBus compliant)
V_{OUT}	Output voltage (PMBus compliant)
I_{OUT}	Output current (PMBus compliant)
P_{IN}	Input power (PMBus compliant)
E_{IN}	Input energy (PMBus compliant)
Temperature	MAX16545B/C chip temperature (PMBus compliant)
Peak V_{IN}	Peak value of input voltage (direct reading)
Peak V_{OUT}	Peak value of output voltage (direct reading)
Peak I_{OUT}	Peak value of output current (direct reading)
Peak P_{IN}	Peak value of input power (direct reading)
Peak Temperature	Peak value of IC temperature (direct reading)

Soft-Start Capacitor C_{SS}

During startup, the pass FET device is operated as a source follower. The soft-start capacitor, C_{SS} is connected between the MOSFET's gate and ground and is charged from a fixed current source. The external C_{SS} capacitor therefore charges linearly and this produces a linear monotonic ramp for V_{OUT}. The ramp rate is programmable by selecting the appropriate value for C_{SS}.

The ramp rate for the voltage across C_{SS} and, hence, V_{OUT} is given by Equation 4.

Equation 4:

$$\frac{dV}{dt} = \frac{I_{SS}}{C_{SS}}$$

where:

dV/dt = voltage ramp rate of V_{OUT} (V/µs)

I_{SS} = MAX16545B/C soft-start current source (mA)

C_{SS} = external C_{SS} capacitor value (nF)

Assuming V_{IN} = 12V, Equation 4 can be used to derive the soft-start time (Equation 5).

Equation 5:

$$t_{SS} = \frac{12V \times C_{SS}}{I_{SS}}$$

where:

t_{SS} = ramp duration (µs)

I_{SS} = MAX16545B/C soft-start current (mA)

C_{SS} = external soft-start capacitor value (nF)

Table 5. MAX16545B/C Programmability

PARAMETER	PROGRAMMABILITY TYPE	COMPONENT	I/O
Moderate OCP Threshold	Analog	ROCP	ROCP
Softstart Ramp Rate	Analog	CSS	SS
Input UVLO Threshold	Analog	Divider	EN/UVLO
SMBus Address	Programming Resistor	RSMBus_ID	SMBus_ID
Moderate OCP Timeout	Digital	SMBus	SMB_DATA
Startup OCP Threshold	Digital	SMBus	SMB_DATA
Severe OCP Threshold	Digital	SMBus	SMB_DATA
Startup Delay	Digital	SMBus	SMB_DATA
Input OV Threshold	Digital	SMBus	SMB_DATA
Output PWRGD Threshold (Sets V_{OUT_UVLO} and Self-Test Thresholds)	Digital	SMBus	SMB_DATA
Self-Check Threshold	Digital	SMBus	SMB_DATA
Overtemperature Warning and Fault Thresholds	Digital	SMBus	SMB_DATA
Input Overpower Warning Threshold	Digital	SMBus	SMB_DATA
Reporting and Warning Averaging Sample Size	Digital	SMBus	SMB_DATA
V_{IN} Undervoltage Warning	Digital	SMBus	SMB_DATA
V_{OUT} Undervoltage Warning	Digital	SMBus	SMB_DATA
V_{IN} Undervoltage Fault	Digital	SMBus	SMB_DATA
Overcurrent Warning	Digital	SMBus	SMB_DATA
Overcurrent Hysteresis	Digital	SMBus	SMB_DATA

Table 6. MAX16545B/C Reporting External Components

PARAMETER	PROGRAMMABILITY TYPE	COMPONENT	I/O
ILOAD Voltage Gain	Analog	R_{ILOAD}	ILOAD

Assuming the load inrush current is due to the output capacitance only, the load current is given by Equation 6 and Equation 7.

Equation 6:

$$I_{VIN} = I_{OUT} = C_{OUT} \times \frac{dV}{dt}$$

where:

I_{OUT} = load inrush current(A)

C_{OUT} = load capacitance (μF)

Equation 7:

$$I_{VIN} = I_{OUT} = \frac{C_{OUT} \times I_{SS}}{C_{SS}}$$

where:

I_{OUT} = load inrush current(A)

C_{OUT} = load capacitance (μF)

C_{SS} = external soft-start capacitor value (nF)

I_{SS} = MAX16545B/C soft-start current (mA)

Therefore, the soft-start capacitor can be selected based on the design value of inrush current using Equation 8.

Equation 8:

$$C_{SS} = \frac{C_{OUT} \times I_{SS}}{I_{INRUSH}}$$

where:

I_{INRUSH} = desired maximum inrush current due to C_{LOAD} (A)

C_{OUT} = load capacitance (mF)

C_{SS} = external soft-start capacitor value (nF)

I_{SS} = MAX16545B/C soft-start current (μA)

The max value of t_{SS} is 30ms to guarantee linear startup as specified in the *Electrical Characteristics* table, select C_{SS} to meet this requirement.

Note that unloading transients with di/dt > 2.5A/ms can be large enough to cause output voltage transients > ~100mV. Under these conditions, an additional capacitor between SS and V_{OUT} is recommended to ensure the pass FET V_{GS} remains above its UVLO threshold. This capacitor has no noticeable effect on soft-start ramp time as the differential voltage from V_{OUT} to SS remains approximately constant during soft-start.

Design Example

Assume a maximum design value for inrush current of 10A, and a load capacitance of 2mF.

$$C_{SS} = \frac{2mF \times 30\mu A}{10A}$$

$$= 6nF \text{ minimum (to meet inrush maximum)}$$

Use Equation 5 to show that corresponding t_{SS} in this example is 2.4ms.

Input UVLO

The input UVLO is set using a resistor-divider, as shown in Figure 5. The enable threshold, V_{IN_UVLO} is given in the *Electrical Characteristics* table. The corresponding value for the V_{IN} rail is given by Equation 9.

Equation 9:

$$V_{IN} = \frac{V_{IN\_UVLO}}{K}$$

or

Equation 10:

$$K = \frac{V_{IN\_UVLO}}{V_{IN}}$$

where:

V_{IN} = 12V rail input voltage to enable device (V)

V_{IN_UVLO} = EN/UVLO threshold (V)

K = resistor-divider ratio, R2/(R1 + R2)

Design Example

To set input UVLO to 10.8V. Using Equation 10.

Equation 11:

$$K = \frac{1.0V}{10.8V}$$

$$= 0.0926$$

where:

R2 is set to 2.26kΩ

R1 = 20kΩ to guarantee startup at min supply voltage

SMBus Address Programming

The SMBus address is programmed to one of sixteen values using the external resistor as shown in Table 7.

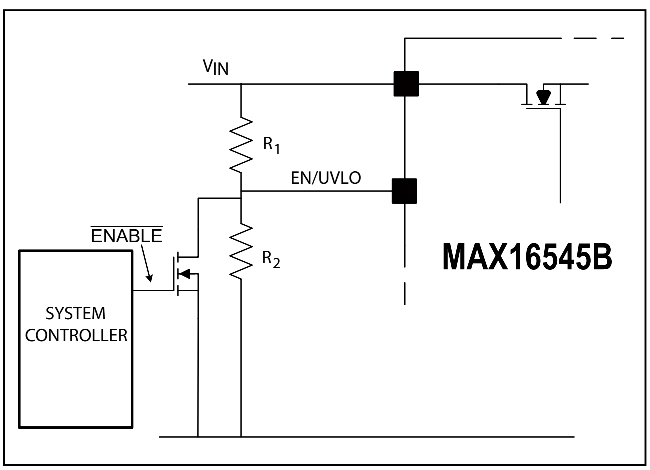


Figure 5. Programming Resistors for Input UVLO

ILOAD Reporting

The current reporting voltage is set using an external resistor connected from ILOAD to ground. The maximum voltage is shown in the *Electrical Characteristics* table. The reporting voltage gain is given by Equation 12. Assuming a maximum signal voltage of 1.35V, Equation 13 can be used to select a value for R_{ILOAD} based on a desired full-scale current.

Equation 12:

$$V_{ILOAD} = R_{ILOAD} \times I_{LOAD} \times G_{ILOAD}$$

Equation 13:

$$R_{ILOAD} = \frac{1.35V}{I_{LOAD\_FSD} \times G_{ILOAD}}$$

where:

V_{ILOAD} = current reporting voltage (V)

R_{ILOAD} = external current reporting resistor (Ω)

I_{LOAD} = load current I_{OUT} = I_{VIN} (A)

I_{LOAD_FSD} = desired full scale of current reporting (A)

G_{ILOAD} = current reporting gain from the *Electrical Characteristics* table

Table 7. SMBus Address Programming Resistor Values

	R_{SMBus_ID} (kΩ)	SMBus Address
0	1.78	40h
1	2.37	41h
2	3.16	42h
3	4.22	43h
4	5.62	44h
5	7.5	45h
6	9.76	46h
7	13	47h
8	17.4	10h
9	23.2	11h
10	30.9	12h
11	41.2	13h
12	54.9	50h
13	73.2	51h
14	97.6	52h
15	127	53h

***Note:** R_{SMBus_ID} resistor tolerance should be 1% or better.*

For example, to set the full-scale current reported to 67.5A.

$$R_{ILOAD} = \frac{1.35V}{67.5A \times (5 \times 10^{-6})}$$

$$= 4K\Omega$$

Note: R_{ILOAD} tolerance should be 0.1% or better.

PMBus Reporting and Warning Settings

The MAX16545B/C provides single sample, averaged and peak values for voltage, current and power reporting, and single reading or averaged readings for warnings. The limits for these parameters and warnings should be set through PMBus prior to operation if a value other than the default is required.

Averaging for voltage, power, and current uses an accumulate and dump technique, whereas temperature uses a shifting window/rolling average. Power is calculated for every voltage and current sample (as opposed to using averaged voltage and current), and the result is accumulated in a dedicated register for averaging.

Two independently programmable averaging sample sizes are used for reporting and warning/status register use for voltage, current, and power.

- Reporting: 2^N samples, with N = 0 to 16 (1 sample to 32K samples)
  Sample size is set using Reg_DDh (CONFIG_2, manufacturer-specific register)
- Warning: 2^M samples, with M = 0 to 3 (1 sample to 8 samples)
  Sample size is set using Reg D0h (CONFIG, manufacturer-specific register)

Setting SMBus Programmable Parameters

See Table 8 for parameters that are programmed through the SMBus. If a setting other than the default shown below is required, it must be programmed through SMBus. Note that some parameters have an enable bit as well as value bits.

Table 8. Parameters Programmed Through SMBus and Default Values

PARAMETER	DEFAULT VALUE
Overtemperature Protection Threshold	135°C
V_{OUT} PWRGD/Self Check Thresholds	11V/9V
Moderate OCP Timeout	100µs
Startup Delay	0µs
Severe OCP Threshold	130%
Input OV Threshold	16V
Overtemperature Warning Threshold	220°C (disabled by default)
Input Power Warning Threshold	(Disabled by default)
Overcurrent Warning	(Disabled by default)
V_{IN} Undervoltage Warning	(Disabled by default)
V_{OUT} Undervoltage Warning	(Disabled by default)
Current Hysteresis	(Disabled by default)
Startup OCP	MAX16545B = 16A MAX16545C = 24A

Table 9. PMBus/SMBus Registers (Note 1)

ADDRESS (HEX)	NAME	TYPE	BYTES	DEFAULT (HEX)
1	**OPERATION**	RW	1	80
3	**CLEAR_FAULTS**	WO	0	0
19	**CAPABILITY**	RO	1	B0
1B	**SMBALERT_MASK**	(Note 2)	2	0000
43	**VOUT_UV_WARN_LIMIT**	RW	2	0000
4A	**IOUT_OC_WARN_LIMIT**	RW	2	03FF
4F	**OT_FAULT_LIMIT**	RW	2	0358
51	**OT_WARN_LIMIT**	RW	2	03FF
58	**VIN_UV_WARN_LIMIT**	RW	2	0000
59	**VIN_UV_FAULT_LIMIT**	RW	2	0000
6B	**PIN_OP_WARN_LIMIT**	RW	2	7FFF
78	**STATUS_BYTE**	RO	1	0
79	**STATUS_WORD**	RO	2	0
7A	**STATUS_VOUT**	RO	1	0
7B	**STATUS_IOUT**	RO	1	0
7C	**STATUS_INPUT**	RO	1	0
7D	**STATUS_TEMPERATURE**	RO	1	0
7E	**STATUS_CML**	RO	1	0
80	**STATUS_MFR_SPECIFIC**	RO	1	0

ADDRESS (HEX)	NAME	TYPE	BYTES	DEFAULT (HEX)
86	**READ_EIN**	RO	2	0
88	**READ_VIN**	RO	2	0
89	**READ_IIN**	RO	2	0
8B	**READ_VOUT**	RO	2	0
8C	**READ_IOUT**	RO	2	0
8D	**READ_TEMPERATURE**	RO	2	0
97	**READ_PIN**	RO	2	0
98	**PMBUS_REVISION**	RO	1	22
99	**MFR_ID**	BLK	5	VLTR
9A	**MFR_MODEL**	BLK	6	VT505
9B	**MFR_REVISION**	BLK	2	3
D0	CONFIG	RW	2	0
D1	PEAK_VIN	RO	2	0
D2	PEAK_IOUT	RO	2	0
D3	PEAK_PIN	RO	2	0
D4	PEAK_TEMP	RO	2	0
D5	CLEAR_PEAKS	WO	0	0
DD	CONFIG2	RW	1	0
F2	MFR_SPEC_HYSTL	RW	2	03FF
F3	MFR_SPEC_HYSTH	RW	2	03FF
F4	MFR_SPEC_HYST_STAT	RO	1	0

Note 1: Registers shown in bold (1h–9Dh) comply with PMBus Power Management Management Protocol Specifications. Refer to the PMBus specification and Table 15 for more details.

Note 2: SMBALERT_MASK is written to a write_word command and read with a read from a write_block_read_process_call with a num_bytes field of 1.

SMBUS_ALERT Behavior

Any of the STATUS bits (with some exception) asserts the alert line (SMBUS_ALERT) low.

Exceptions are:
- Bit off of STATUS_BYTE/STATUS_WORD
- Bit POWERGOOD# of STATUS_WORD

Alert line can be configured to mask any of the STATUS bits using the SMBALERT_MASK register.

The only ways to release the alert line are:
- CLEAR_FAULTS command
- ARA (see SMBUS spec v2.0)

Table 10. Register 80h (STATUS_MFR_SPECIFIC) Interpretation

BIT #	BIT NAME	DESCRIPTION	READING	INDICATION
[7]	SELFCHECK_FAULT	Pass FET and soft-start self-check	0	Pass
			1	Fail
[6]	ROCP_FAULT	R_{OCP} check	0	Pass
			1	Fail
[5]	R_SMBUSID_FAULT	SMBus_ID programming resistor check	0	Pass
			1	Fail
[4]	FOLLOWER_FAULT	Fault input	0	No Fault Input
			1	Fault Input
[3]	GATE_UVLO_FAULT	V_{GS_UVLO} fault	0	No Fault
			1	Fault
[2]	BST_UVLO_FAULT	V_{BST_UVLO} fault	0	No Fault
			1	Fault
[1]	—	Not used	0	—
			1	—
[0]	—	Always read as 0	0	—

Table 11. MAX16545B/C PMBus Register Map

ADDRESS	DEC	NAME	TYPE	WIDTH	DEFAULT	LOW BYTE								HIGH BYTE							
						b7	b6	b5	b4	b3	b2	b1	b0	b15	b14	b13	b12	b11	b10	b9	b8
01	1	OPERATION	RW	1	80	enable	0	0	0	0	0	0	0								
03	3	CLEAR_ FAULTS	WO	0	0																
19	25	CAPABILITY	CN	1	B0	1	0	1	1	0	0	0	0								
1B	27	SMBALERT_ MASK	**	2	0000																
43	67	VOUT_UV_ WARN_LIMIT	RW	2	0	vout_uv_w arn_th[7]	vout_uv_w arn_th[6]	vout_uv_w arn_th[5]	vout_uv_w arn_th[4]	vout_uv_w arn_th[3]	vout_uv_w arn_th[2]	vout_uv_w arn_th[1]	vout_uv_w arn_th[0]	0	0	0	0	0	0	vout_uv_w arn_th[9]	vout_uv_w arn_th[8]
4A	74	IOUT_OC_ WARN_LIMIT	RW	2	03FF	ocp_warn_ th[7]	ocp_warn_ th[6]	ocp_warn_ th[5]	ocp_warn_ th[4]	ocp_warn_ th[3]	ocp_warn_ th[2]	ocp_warn_ th[1]	ocp_warn_ th[0]	0	0	0	0	0	0	ocp_warn_ th[9]	ocp_warn_ th[8]
4F	79	OT_FAULT_ LIMIT	RW	2	0358	ovt_fault_t h[7]	ovt_fault_t h[6]	ovt_fault_t h[5]	ovt_fault_t h[4]	ovt_fault_t h[3]	ovt_fault_t h[2]	ovt_fault_t h[1]	ovt_fault_t h[0]	0	0	0	0	0	0	ovt_fault_t h[9]	ovt_fault_t h[8]
51	81	OT_WARN_ LIMIT	RW	2	03FF	ovt_warn_t h[7]	ovt_warn_t h[6]	ovt_warn_t h[5]	ovt_warn_t h[4]	ovt_warn_t h[3]	ovt_warn_t h[2]	ovt_warn_t h[1]	ovt_warn_t h[0]	0	0	0	0	0	0	ovt_warn_t h[9]	ovt_warn_t h[8]
47	87	VIN_OV_WARN_ LIMIT	RW	2	03FF	ov_warn_t h[7]	ov_warn_t h[6]	ov_warn_t h[5]	ov_warn_t h[4]	ov_warn_t h[3]	ov_warn_t h[2]	ov_warn_t h[1]	ov_warn_t h[0]	0	0	0	0	0	0	ov_warn_t h[9]	ov_warn_t h[8]
58	88	VIN_UV_WARN_ LIMIT	RW	2	0	uv_warn_t h[7]	uv_warn_t h[6]	uv_warn_t h[5]	uv_warn_t h[4]	uv_warn_t h[3]	uv_warn_t h[2]	uv_warn_t h[1]	uv_warn_t h[0]	0	0	0	0	0	0	uv_warn_t h[9]	uv_warn_t h[8]
59	89	VIN_UV_FAULT_ LIMIT	RW	2	0	vin_uv_ fault_th[7]	vin_uv_ fault_th[6]	vin_uv_ fault_th[5]	vin_uv_ fault_th[4]	vin_uv_ fault_th[3]	vin_uv_ fault_th[2]	vin_uv_ fault_th[1]	vin_uv_ fault_th[0]	0	0	0	0	0	0	vin_uv_ fault_th[9]	vin_uv_ fault_th[8]
6B	107	PIN_OP_WARN_ LIMIT	RW	2	FFFF	op_warn_t h[7]	op_warn_t h[6]	op_warn_t h[5]	op_warn_t h[4]	op_warn_t h[3]	op_warn_t h[2]	op_warn_t h[1]	op_warn_t h[0]	op_warn_t h[15]	op_warn_t h[14]	op_warn_t h[13]	op_warn_t h[12]	op_warn_t h[11]	op_warn_t h[10]	op_warn_t h[9]	op_warn_t h[8]
78	120	STATUS_BYTE	RO	1	0	0	OFF	0	IOUT_OC_ FAULT	VIN_UV_ FAULT	TEMPER- ATURE	CML	NOA								
79	121	STATUS_ WORD	RO	2	0	0	OFF	0	IOUT_OC_ FAULT	VIN_UV_ FAULT	TEMPER- ATURE	CML	NOA	VOUT	IOUT/ POUT	INPUT	MFR_ SPE CIFIC	POWER- GOOD#	0	0	BAD_ FET_ HEALTH
7A	122	STATUS_VOUT	RO	1	26	0	0	VOUT_ UV_ WARNING	0	0	0	0	0								
7B	123	STATUS_IOUT	RO	1	0	IOUT_OC_ FAULT	0	IOUT_OC_ WARNING	0	0	0	0	0								
7C	124	STATUS_INPUT	RO	1	0	VIN_OV_ FAULT	0	VIN_UV_ WARNING	VIN_UV_F AULT	Unit off for low in V	IIN_OC_FA ULT	IIN_OC_W ARNING	PIN_OP_ WARNING								
7D	125	STATUS_ TEMPERATURE	RO	1	0	OT_FAULT	OT_ WARNING	0	0	0	0	0	0								
7E	126	STATUS_CML	RO	1	0	invalid/ unsup- ported cmd	invalid/ unsup- ported data	PEC Failed	0	0	0	Other com- munication fault	0								
80	128	STATUS_MFR_ SPECIFIC	RO	1	0	SELFCHE CK_FAULT	ROCP_ FA ULT	R_SMBUS _ID_FAULT	FOLLOWE R_FAULT	GATE_ UVL_ FAULT	BST_UVL O_FAULT	0	0								
86	134	READ_EIN	BLK	7	0	8'h06	enrgy_ cnt[7:0]	enrgy_ cnt[15:8]	roll_ cnt[7:0]	samp_ cnt[7:0]	samp_ cnt[15:8]	samp_ cnt[23:16]									
88	136	READ_VIN	RO	2	0	vadc_ ave[7]	vadc_ ave[6]	vadc_ ave[5]	vadc_ ave[4]	vadc_ ave[3]	vadc_ ave[2]	vadc_ ave[1]	vadc_ ave[0]	0	0	0	0	0	0	vadc_ ave[9]	vadc_ ave[8]
89	137	READ_IIN	RO	2	0	iadc_ ave[7]	iadc_ ave[6]	iadc_ ave[5]	iadc_ ave[4]	iadc_ ave[3]	iadc_ ave[2]	iadc_ ave[1]	iadc_ ave[0]	0	0	0	0	0	0	iadc_ ave[9]	iadc_ ave[8]

Table 11: MAX16545B/C PMBus Register Map (continued)

ADDRESS	DEC	NAME	TYPE	WIDTH	DEFAULT	LOW BYTE								HIGH BYTE							
						b7	b6	b5	b4	b3	b2	b1	b0	b15	b14	b13	b12	b11	b10	b9	b8
8B	139	READ_VOUT	RO	2	0	vadc_ ave[7]	vadc_ ave[6]	vadc_ ave[5]	vadc_ ave[4]	vadc_ ave[3]	vadc_ ave[2]	vadc_ ave[1]	vadc_ ave[0]	0	0	0	0	0	0	vadc_ ave[9]	vadc_ ave[8]
8C	140	READ_IOUT	RO	2	0	iadc_ ave[7]	iadc_ ave[6]	iadc_ ave[5]	iadc_ ave[4]	iadc_ ave[3]	iadc_ ave[2]	iadc_ ave[1]	iadc_ ave[0]	0	0	0	0	0	0	iadc_ ave[9]	iadc_ ave[8]
8D	141	READ_ TEMPERATURE_1	RO	2	0	tadc_ ave[7]	tadc_ ave[6]	tadc_ ave[5]	tadc_ ave[4]	tadc_ ave[3]	tadc_ ave[2]	tadc_ ave[1]	tadc_ ave[0]	0	0	0	0	0	0	tadc_ ave[9]	tadc_ ave[8]
97	151	READ_PIN	RO	2	0	pwr_ calc[7]	pwr_ calc[6]	pwr_ calc[5]	pwr_ calc[4]	pwr_ calc[3]	pwr_ calc[2]	pwr_ calc[1]	pwr_ calc[0]	0	pwr_ calc[14]	pwr_ calc[13]	pwr_ calc[12]	pwr_ calc[11]	pwr_ calc[10]	pwr_ calc[9]	pwr_ calc[8]
98	152	PMBUS_ REVISION	RO	1	03	0	0	1	0	0	0	1	0								
99	153	MFR_ID	BLK	5	"VLTR"	8'h04	"V"	"L"	"T"	"R"											
9A	154	MFR_MODEL	BLK	6	"VT505"	8'h05	"V"	"T"	"5"	"0"	"5"										
9B	155	MFR_REVISION	BLK	2	"1"	8'h01	"1"														
D0	208	CONFIG	RW	2	0	ocp_cfg	mocp_ cfg[1]	mocp_ cfg[0]		ov_th[1]	ov_th[0]	num_aves_ alert[1]	num_aves_ alert[0]			disable_ iadc	ss_cfg[1]	ss_cfg[0]	otp_cfg	pwrgd_ cfg[1]	pwrgd_ cfg[0]
D1	209	PEAK_VIN	RO	2	0	vadc_ peak[7]	vadc_ peak[6]	vadc_ peak[5]	vadc_ peak[4]	vadc_ peak[3]	vadc_ peak[2]	vadc_ peak[1]	vadc_ peak[0]	0	0	0	0	0	0	vadc_ peak[9]	vadc_ peak[8]
D2	210	PEAK_IOUT	RO	2	0	iadc_ peak[7]	iadc_ peak[6]	iadc_ peak[5]	iadc_ peak[4]	iadc_ peak[3]	iadc_ peak[2]	iadc_ peak[1]	iadc_ peak[0]	0	0	0	0	0	0	iadc_ peak[9]	iadc_ peak[8]
D3	211	PEAK_PIN	RO	2	0	pwr_ peak[7]	pwr_ peak[6]	pwr_ peak[5]	pwr_ peak[4]	pwr_ peak[3]	pwr_ peak[2]	pwr_ peak[1]	pwr_ peak[0]	pwr_ peak[15]	pwr_ peak[14]	pwr_ peak[13]	pwr_ peak[12]	pwr_ peak[11]	pwr_ peak[10]	pwr_ peak[9]	pwr_ peak[8]
D4	212	PEAK_TEMP	RO	2	0	tadc_ peak[7]	tadc_ peak[6]	tadc_ peak[5]	tadc_ peak[4]	tadc_ peak[3]	tadc_ peak[2]	tadc_ peak[1]	tadc_ peak[0]	0	0	0	0	0	0	tadc_ peak[9]	tadc_ peak[8]
D5	213	CLEAR_PEAKS	WO	0	0																
DD	221	CONFIG_2	RW	2	0	0	0	ocp_su_cfg [1]	ocp_su_ cfg [0]	num_aves_ reporting[3]	num_aves_ reporting[2]	num_aves_ reporting[1]	num_aves_ reporting[0]								
F2	242	MFR_SPECIFIC_ HYST L	RW	2	03FF	hystl[7]	hystl[6]	hystl[5]	hystl[4]	hystl[3]	hystl[2]	hystl[1]	hystl[0]							hystl[9]	hystl[8]
F3	243	MFR_SPECIFIC_ HYST H	RW	2	03FF	hysth[7]	hysth[6]	hysth[5]	hysth[4]	hysth[3]	hysth[2]	hysth[1]	hysth[0]							hysth[9]	hysth[8]
F4	244	MFR_SPECIFIC_ HYST _STATUS	RO	1	0	0	0	0	0	Iout > oc_warn_ limit	HYST pin status	HYST > reg_F3	HYST < reg_F2								
FD	253	PEAK_VOUT	RO	2	0	vout_ peak[7]	vout_ peak[6]	vout_ peak[5]	vout_ peak[4]	vout_ peak[3]	vout_ peak[2]	vout_ peak[1]	vout_ peak[0]	0	0	0	0	0	0	vout_ peak[9]	vout_ peak[8]

CONFIG Register (D0h)

This is a 2-byte register used to configure the MAX16545B/C. The default value is 0000h. The meaning of the bits of this register is shown in Table 12.

CONFIG_2 Register (DDh)

This single-byte register allows the selection of the number of samples to average for voltage, current and power reporting. It also sets the threshold for startup OCP. Only bits 5:0 are used; bits 7:6 have no effect and should be left as 00b. The meaning of the bits of this register is shown in Table 13.

Table 12. Register D0h

BIT #	BIT NAME	SETTINGS (BINARY)	DESCRIPTION
[13]	I-ADC disable	0	I-ADC enabled (default value)
		1	I-ADC dsabled
[12:11]	ss_cfg[1:0]	00	Soft-start delay = 0ms (default value)
		01	Soft-start delay = 10ms
		10	Soft-start delay = 20ms
		11	Not used
[10]	Not Used		
[9:8]	pwrgd_th[1:0]	00	Power good threshold = 11V, self-check threshold = 9V
		01	Power good threshold = 10V, self-check threshold = 8V
		10	Power good threshold = 9V, self-check threshold = 7V
		11	Power good threshold = 8V, self-check threshold = 6V
[7]	ocp_cfg	0	Severe OCP = 130% of Moderate OCP (default value)
		1	Severe OCP = 150% of moderate OCP
[6:5]	mocp_cfg[1:0]	00	Moderate OCP timeout = 100µs (default value)
		01	Moderate OCP timeout = 250ms
		10	Moderate OCP timeout = 100ms
		11	Moderate OCP timeout = 10µs
[3:2]	ov_th[1:0]	00	Set V_{IN_OV} threshold = 16V (default value)
		01	Set V_{IN_OV} threshold = 14V
		10	Set V_{IN_OV} threshold = 17V
		11	Set V_{IN_OV} threshold = 18V
[1:0]	num_aves_alert[1:0]	00	Sets averaging for PMBus warning levels to one sample (default value)
		01	Sets averaging for PMBus warning levels to two samples
		10	Sets averaging for PMBus warning levels to four samples
		11	Sets averaging for PMBus warning levels to eight samples

Peak Voltage, Current, Power, and Temperature Reporting

The two-byte registers shown in Table 14 provide readings of the peak values for input/output voltage, output current, input power and temperature in 10 bits direct format.

These registers can be reset with the CLEAR_PEAKS command (send byte D5h) or power cycling the part.

Table 13. Register DDh

BITS #	BIT NAME	SETTING (BINARY)	STARTUP OCP SETTING/AVERAGING SAMPLE SIZE
[5:4]	su_ocp_cfg	00 01 10 11	16A 24A 8A Not Used
[3:0]	num_aves_reporting	0	1 sample
		1	2 samples
		10	4 samples
		11	8 samples
		100	16 samples
		101	32 samples
		110	64 samples
		111	128 samples
		1000	256 samples
		1001	512 samples
		1010	1024 samples
		1011	2048 samples
		1100	4096 samples
		1101	8192 samples
		1110	16384 samples
		1111	32768 samples

Note: *One sample for voltage/power/energy reporting is 2ms and 1ms for current reporting.*

Table 14. Manufacturer-Specific Direct Reporting Registers

REGISTER ADDRESS	REGISTER NAME	PARAMETER
D1h	PEAK_VIN	Peak Input Voltage
D2h	PEAK_IOUT	Peak Output Current
D3h	PEAK_PIN	Peak Input Power
D4h	PEAK_TEMP	Peak Temperature
FDh	PEAK_VOUT	Peak Output Voltage

PMBus Reporting Format

The MAX16545B/C uses the PMBus DIRECT number format; the actual readings in their respective units correlate with the numerical values read from registers, as shown in Equation 14.

- Current/Voltage/Temperature: 10-bit resolution
- Power: 16-bit two's complement representation

Equation 14:

$$X = \frac{1}{m}\left(Y \times 10^{-R} - b\right)$$

where:

X = the calculated, real-world value in the appropriate units (A, V, °C, etc.);

m = the slope coefficient, is a two byte, two's complement integer;

Y = is a two byte two's complement integer received from the PMBus device;

b = the offset is a two byte, two's complement integer

R = the exponent is a one byte, two's complement integer.

The values used in the MAX16545B/C for the parameters above are shown in Table 15. Note that current and power readings depend on the value of R_{LOAD}, the external current reporting resistor connected between ILOAD and GND.

Table 15. PMBus Equation Parameters

PMBUS REGISTER	FORMAT	DATA BYTES	m	b	R	UNITS
READ_IOUT (8Ch)*, READ_IIN (89h)*	Direct	2	3.824 x R_{LOAD}	-4300	-3	A
READ_VOUT (8Bh), READ_VIN (88h)	Direct	2	7578	0	-2	V
READ_TEMPERATURE_1 (8Dh)	Direct	2	205	6545	-2	°C
READ_PIN (97h)	Direct	2	0.895 x R_{LOAD}	-9100	-2	W
READ_EIN (86h)**	Direct	2	3.505 x R_{LOAD}	0	-5	**

**Digital current reporting is available even if the FET is OFF.*

***Refer to the PMBus specifications for more details on definition and calculation.*

Input Capacitance (C_{IN}) Selection

Use of input capacitors is highly recommended to guarantee the input voltage is stable and noise free. For applications requiring no input capacitors before the MAX16545B/C, the input-voltage ripple should be less than 300mV peak-to-peak.

Output Capacitance (C_{OUT}) Selection

The maximum output capacitance can be calculated as shown in Equation 15.

Equation 15:

$$C_{OUT} = \frac{(I_{INRUSH} \times C_{SS})}{I_{SS}}$$

where:

C_{SS} = Soft-start programming capacitance.

I_{SS} = Soft-start current, 30µA (typ).

C_{OUT} = Maximum load capacitance that can be used at soft-start with a purely capacitive load.

I_{INRUSH} = Desired maximum inrush current during startup. Select I_{INRUSH} lower than startup OCP ($I_{OCP(STARTUP)}$) and within startup SOA, refer to Figure 2.

Design Example

Assume a design value for maximum inrush current of 10A, and a soft-start capacitance of 25nF.

Assume 12V application and 30µA (typ) soft-start current; soft-start time in this case is 0.01ms. The maximum safe operating output current is 22A at 0.01ms (refer to the Startup SOA in Figure 2) and the default Startup OCP level is 16A (refer to Table 8).

The designed maximum inrush current of 10A is lower than 16A startup OCP and within startup SOA. The designed value is valid. Hence, the maximum load capacitance is calculated as shown in Equation 16.

Equation 16:

$$C_{OUT} = \frac{(10A \times 25nF)}{30\mu A} = 8.33mF$$

Additionally, the recommended output capacitance should be less than 10mF to prevent false triggering of self-check during startup into precharged output.

Input TVS Diode Selection

The use of a transient voltage suppression (TVS) diode at input is necessary to clamp input-voltage transient within rating of V_{IN} pin of MAX16545B/C (see the *Absolute Maximum Ratings* section).

A general guide to select the proper TVS diode is listed below:

- Choose TVS diode reverse-standoff voltage (V_{RWM}) ≥ operating voltage of MAX16545B/C, 12V (typ).
- Choose TVS diode peak-pulse current (I_{PPM}) ≥ maximum transient peak-pulse current of the MAX16545B/C, 60A (typ).
- Choose TVS clamping voltage (V_C) ≤ maximum voltage handling capability of the MAX16545B/C, 22V (typ) for 150µs.

Recommend SMCJ13A based on selection criteria above.

Output Schottky diode selection

The use of a Schottky diode at output is necessary to clamp the negative output-voltage spike within the rating of V_{OUT} pin of the MAX16545B/C (see the *Absolute Maximum Ratings* section). Select the proper Schottky diode with low forward-voltage drop (V_F) and peak forward-surge current (I_{FSM}) higher than the expected inductive current.

Reverse Current is Not Allowed During Output “Hot-Plug”

The MAX16545B/C devices must not be used in applications where a removable load assembly can be connected while there is stored energy on the input of the removable load. This is because stored energy in a load device can force current backwards through the pass-FET body diode, and the MAX16545B/C was not designed for this condition.

However, output load cards and devices (such as disk drives) may be removed and replaced while the system is powered, provided that the system design guarantees that the load device cannot be reconnected while there is still electrical charge on the input capacitance of the load device.

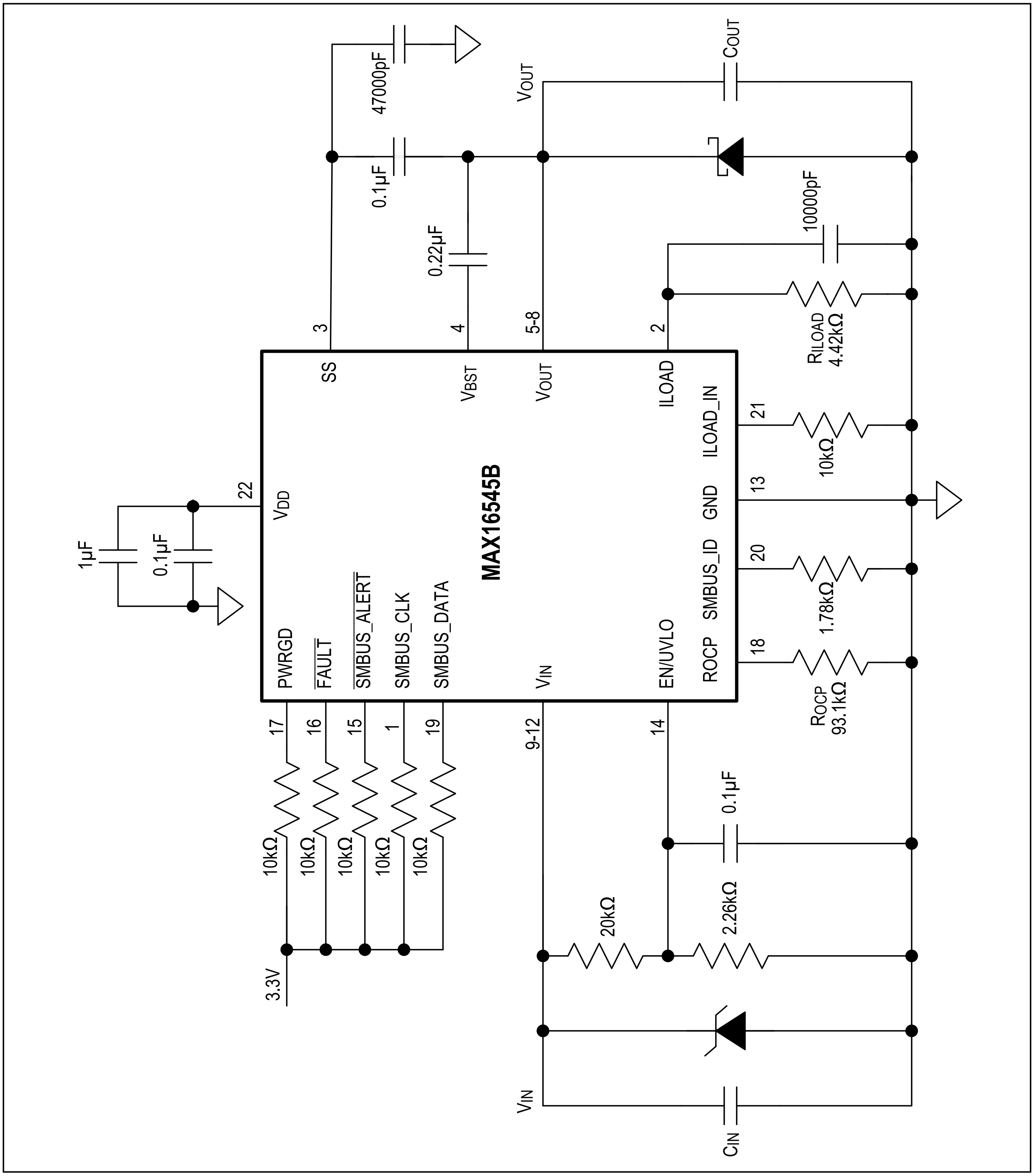


Figure 6. Reference Schematic

MAX16545B Layout Recommendations

Please request Application Note 6848, Optimal Application Circuit and Layout Guidelines for the MAX16545 and MAX16543, for detailed information on circuit board layout. Important layout details are summarized here.

V_{IN} and V_{OUT}

- Minimize input and output trace inductance by using wide and multiple V_{IN} and V_{OUT} planes for optimal thermal performance.
- Use multiple vias to connect interlaying power planes.
- Place input capacitors (where applicable) as close to the IC as possible.
- Place output capacitors as close to the IC as possible.

Example

The EV kit layout in Figure 7 shows use of large, wide power planes for V_{IN} and V_{OUT} on the top layer. C_{IN} and C_{OUT} are close to the IC. The other V_{IN} and V_{OUT} power layers are connected with multiple vias between the pins.

Ground

- Use a trace approximately 0.1mm wide by 0.7mm long from the ground pin (pin 13) on the top layer to the second-layer AGND island.

V_{BST} and SS

Place the V_{BST} and SS capacitors on the top layer as close to the pins as possible.

V_{DD}

Add a V_{DD} plane on the top layer to decouple the V_{DD} caps close to the IC to form a tighter loop to ground.

ROCP and ILOAD

The ROCP and ILOAD resistors should be placed as close to the IC as possible.

ILOAD_IN

Connect a 10kΩ resistor to ground.

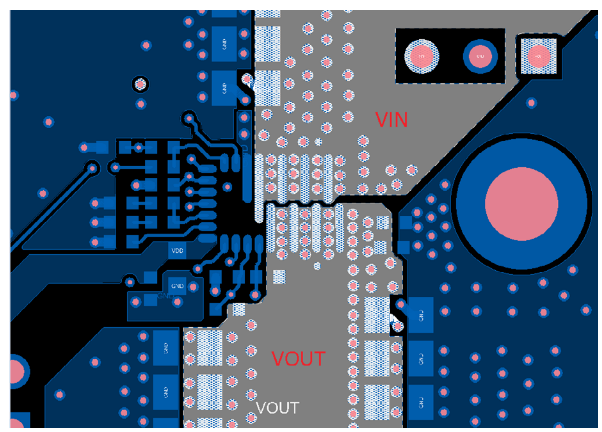


Figure 7. Top Layer (Power)

Ordering Information

PART NUMBER	DESCRIPTION	PACKAGE	DRAWING NUMBER	SHIPPING METHOD	PACKAGE MARKING
MAX16545BGPF+	Startup OCP = 16A	22 FCQFN	ES AP-3236	2.5kµ Tape & Reel	MAX16545B
MAX16545BGPF+T					
MAX16545CGPF+	Startup OCP = 24A				MAX16545C
MAX16545CGPF+T					

+Denotes a lead(Pb)-free/RoHS-compliant part.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	12/18	Add new MAX16545C version, Improved Figure 2, Startup SOA	1, 5, 18, 19, 21, 28, 34, 35, 38
2	2/19	Revised application use-case and circuit layout guidelines. Clarified TOC titles and descriptions.	1, 9, 12-14, 18, 35, 37
3	4/19	Revised title of “Output Hot-Plug” warning in the *Detailed Description* section	35
4	6/19	Added “future product” note to the *Ordering Information* table.	38
5	10/19	Removed “future product” note from MAX16545C and corrected overvoltage protection to detection only	7, 17, 21, 23, 25, 28, 32, 33, 38
6	6/22	Updated Soft-Start Charging Current (min) in the *Electrical Characteristics* table	5