19-4756; Rev 1; 4/10

EVALUATION KIT AVAILABLE

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

MAX17115

General Description

The MAX17115 includes a high-performance step-up regulator, a high-accuracy, high-voltage, low-dropout linear regulator (LDO), a high-performance buffer amplifier, and a logic-controlled high-voltage switch block.

The DC-DC converter is a high-frequency (1.2MHz/640kHz) current-mode step-up regulator with a built-in power MOSFET. It provides fast-transient response to pulsed loads while producing efficiencies over 88%. The built-in power MOSFET allows output voltages as high as 18V from inputs from 2.5V to 5.5V. A programmable soft-start function controls startup inrush currents.

The operational amplifier, typically used to drive the LCD backplane (VCOM), features high-output short-circuit current (200mA), fast slew rate (45V/µs), and wide bandwidth (20MHz). Its rail-to-rail input and output maximize application flexibility. The high-voltage LDO is adjustable and has a high accuracy of ±0.5%. It is typically used to drive a gamma reference divider string. The high-voltage switch control block modulates the shape of the gate-on supply and provides an adjustable delay for power-up sequencing.

The high-voltage stress (HVS) function is used to temporarily increase the source-driver supply voltage of the LCD panel for aging tests. The HVS digital input controls an open-drain internal switch, which is typically used to change the feedback divider of the step-up regulator.

The MAX17115 is available in a lead-free, 32-pin, thin QFN package. The package is a 5mm x 5mm square with a maximum thickness of 0.8mm for thin LCD panel design.

Applications

LCD Monitors

LCD TVs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17115ETJ+	-40°C to +85°C	32 TQFN

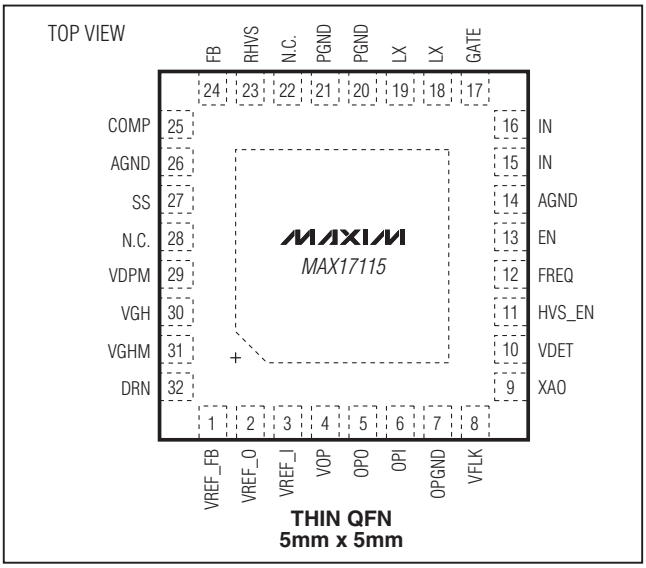
+Denotes a lead(Pb)-free/RoHS-compliant package.

Features

- **2.5V to 5.5V Input Supply Range**
- **Pin-Programmable 640kHz/1.2MHz Switching Frequency**
- **Current-Mode Step-Up Converter**
  Fast-Transient Response to Pulsed Load
  High-Accuracy Output Voltage (0.8%)
  Built-In 20V, 4.6A, 0.1Ω n-Channel Power MOSFET
  Cycle-by-Cycle Current Limit
  High Efficiency (88%)
- **Programmable Soft-Start**
- **High-Performance Operational Amplifier**
  200mA Output Short-Circuit Current
  45V/µs Slew Rate
  20MHz -3dB Bandwidth
  Rail-to-Rail Input and Output
- **High-Voltage LDO**
  High ±0.5% Accuracy
  40mA Guaranteed Output Current
- **Logic-Controlled High-Voltage Switch with Adjustable Delay**
- **High-Voltage Stress Mode**
- **Built-In Sequencing**
- **Thermal-Overload Protection**
- **Gate Driver for Input-Side True Shutdown™ Switch**
- **Logic-Level Shutdown Input**
- **Timer-Delayed Fault Shutdown for Boost-Regulator Output**

True Shutdown is a trademark of Maxim Integrated Products, Inc.

Pin Configuration



Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

ABSOLUTE MAXIMUM RATINGS

IN, VFLK, EN to AGND ..... -0.3V to +7.5V
VDET, XAO, HVS_EN, RHVS, VREF_FB, FREQ to AGND ..... -0.3V to +7.5V
VDPM, FB, COMP, GATE, SS to AGND ..... -0.3V to (V_{IN} + 0.3V)
PGND, OPGND to AGND ..... -0.3V to +0.3V
VREF_O to AGND ..... -0.3V to (V_{VREF_I} + 0.3V)
LX to PGND ..... -0.3V to +22V
VOP, VREF_I to AGND ..... -0.3V to +22V
VGH to AGND ..... -0.3V to +40V
VGHM, DRN to AGND ..... -0.3V to (V_{VGH} + 0.3V)
VGHM to DRN ..... -0.3V to +40V
OPI, OPO to OPGND ..... -0.3V to (V_{VOP} + 0.3V)
OPO Maximum Continuous Output Current ..... ±75mA
LX, PGND RMS Current Rating (per pin) 1.6A
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C) 2758mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{EN} = +5V, Circuit of Figure 1, V_{VOP} = +16V, V_{VGH} = 30V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
IN Input-Supply Range	(Note 1)	2.5		6.0	V
IN Undervoltage Lockout	V_{IN} rising, hysteresis = 200mV	2.0	2.25	2.49	V
IN Quiescent Current	V_{FB} = 1.3V, LX not switching		0.5	1	mA
	V_{FB} = 1.2V, switching		2.5	5	
Thermal Shutdown	Temperature rising		+160		°C
	Hysteresis		15		
HIGH-VOLTAGE LDO					
VREF_I Input Voltage Range		10		18	V
VREF_I Undervoltage Lockout	V_{VREF_I} rising		5.4	5.8	V
VREF_I Input-Bias Current	No load		100	250	µA
VREF_O Dropout Voltage	VREF_I - VREF_O; I_{VREF_O} = 30mA		0.25	0.5	V
VREF_FB Regulation Voltage	1mA ≤ I_{VREF_O} ≤ 30mA	1.234	1.240	1.246	V
	10V < V_{VREF_I} < 18V, I_{VREF_O} = 20mA, V_{VREF_O} = 9V	-0.9		+0.9	mV/V
VREF_O Maximum Output Current		40			mA
STEP-UP REGULATOR					
Output-Voltage Range		V_{IN}		18	V
FB Regulation Voltage	No load	1.228	1.24	1.252	V
FB Fault Trip Level	Falling edge		1.00		V
FB Fault Delay	V_{FB} = 0.95V		55		ms
FB Load Regulation	1mA < I_{LOAD} < 0.5A		-0.1		%
FB Line Regulation	V_{IN} = 2.5V to 6V		0.05	0.15	%/V
FB Input-Bias Current	V_{FB} = 1.24V; T_A = +25°C		120	250	nA
FB Transconductance	I_{COMP} = +2.5µA	100	250	500	µS
LX Current Limit	V_{FB} = 1.2V, duty cycle = 75%	3.9	4.6	5.4	A

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = +5V, Circuit of Figure 1, V_{VOP} = +16V, V_{VGH} = 30V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LX On-Resistance	V_{IN} = 5V		0.10	0.2	Ω
	V_{IN} = 3V		0.13	0.26	
LX Bias Current	V_{LX} = 20V, T_A = +25°C		10	25	µA
Current-Sense Transresistance	V_{IN} = 5V	0.08	0.15	0.25	V/A
OSCILLATOR					
Frequency	V_{FREQ} = 0V	500	640	780	kHz
	V_{FREQ} = 5V	1000	1200	1400	
FREQ Pulldown Current	V_{FREQ} = 5V	3	6	9	µA
Maximum Duty Cycle	V_{FREQ} = 0V or 5V	89	93	96	%
Minimum On-Time			100		ns
SOFT-START					
SS Reset Resistance	V_{EN} = 0V, I_{SS} = 10mA		10	20	Ω
SS Charge Current	V_{SS} = 1.2V	2	4	6	µA
SS Done Threshold	SS voltage rising		1.4		V
SS Time	33nF on SS pin		6.6		ms
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
VDPM Capacitor Charge Current	MLG startup, V_{VDPM} = 0V	4	5	6	µA
VDPM Turn-On Threshold	VDPM rising	1.21	1.24	1.27	V
VDPM Pulldown Resistance	I_{VDPM} = 10mA		10	20	Ω
VFLK Input Low Voltage	V_{IN} = 2.5V to 6V			0.7	V
VFLK Input High Voltage	2.5V < V_{IN} < 4.5V	1.9			V
	4.5V < V_{IN} < 6V	2.3			
VFLK Input Leakage Current	V_{VFLK} = 0V or 5V, T_A = +25°C	-1		+1	µA
VFLK-to-VGH Propagation Delay	VFLK rising and falling		200		ns
VGH Input-Voltage Range				35	V
VGH Input Current	V_{VDPM} = 1.5V, V_{VFLK} = 5V		300	450	µA
	V_{VDPM} = 1.5V, V_{VFLK} = 0V		200	350	µA
VGH-to-VGHM Resistance	V_{VDPM} = 1.5V, V_{VFLK} = 5V, I = 10mA		8	15	Ω
VGHM-to-DRN Resistance	V_{VDPM} = 1.5V, V_{VFLK} = 0V, I = 10mA		30	60	Ω
INPUT SERIES SWITCH GATE DRIVER					
GATE Output Sink Current	V_{GATE} = 5V	8	10	12	µA
	V_{GATE} = 0.2V	10	20		mA
GATE Done Voltage Threshold	GATE falling		0.3	0.5	V
GATE Output Voltage Low	I_{GATE} = 1mA		0.01	0.05	V
GATE Output Voltage High	I_{GATE} = -1mA, V_{EN} = 0V	V_{IN} - 0.05	V_{IN} - 0.02		V
OPERATIONAL AMPLIFIER					
VOP Supply Range		6		18	V
VOP Overvoltage Threshold	VOP rising	19	20	21	V
VOP Supply Current	No load		3	5	mA

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = +5V, Circuit of Figure 1, V_{VOP} = +16V, V_{VGH} = 30V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VOP Input Offset Voltage	V_{OPI} = V_{VOP}/2	-14		+14	mV
OPI Input-Bias Current	V_{OPO}, V_{OPI} = V_{VOP} /2, T_A = +25°C	-50		+50	nA
Input Common-Mode Voltage Range		0		V_{VOP}	V
OPO Output Voltage High	I_{OPO} = +5mA, V_{OPI} = V_{VOP}	V_{VOP} - 100	V_{VOP} - 40		mV
OPO Output Voltage Low	I_{OPO} = -5mA, V_{OPI} = 0V		40	100	mV
Slew Rate	20% to 80% of V_{VOP}, C_{LOAD} = 10pF, R_{LOAD} = 10kΩ		45		V/µs
-3dB Bandwidth	C_{LOAD} = 10pF, R_{LOAD} = 10kΩ		20		MHz
Short-Circuit Current	Sourcing, V_{OPI} = V_{VOP} - 3V, V_{OPO} = V_{VOP} - 4V	100	200		mA
	Sinking, V_{OPI} = 3V, V_{OPO} = 4V	100	200		
Power-Supply Rejection Ratio	DC,10V ≤ V_{VOP} ≤ 18V	60			dB
XAO FUNCTION					
VDET Threshold	VDET falling, V_{IN} = 5V	1.22	1.24	1.26	V
VDET Hysteresis			50		mV
VDET Input-Bias Current	V_{VDET} = 0V or 5V, T_A = +25°C	-1		+1	µA
XAO Output Voltage	V_{VDET} = 0V, I_{XAO} = 10mA		0.1	0.4	V
HIGH-VOLTAGE STRESS MODE					
HVS_EN Input Low Voltage				0.8	V
HVS_EN Input High Voltage		2.1			V
HVS_EN Pulldown Resistance			300		kΩ
RHVS Output Voltage	(Note 1)			6	V
RHVS Leakage Current	V_{RHVS} = 6V, V_{HVS_EN} = 0V, T_A = +25°C				µA
RHVS On-Resistance	V_{HVS_EN} = 5V, I_{RHVS} = 10mA		6	20	Ω
CONTROL INPUTS					
Input Low Voltage [EN, FREQ]	V_{IN} = 2.5V to 6V			0.6	V
Input High Voltage [EN, FREQ]	V_{IN} = 4.5V to 6V		2.4		V
	V_{IN} = 2.5V to 4.5V	1.9			
Hysteresis [EN, FREQ]			0.15		V
Input-Bias Current [EN]	T_A = +25°C	-1		+1	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{EN} = +5V, Circuit of Figure 1, V_{VOP} = +16V, V_{VGH} = 30V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
IN Input Supply Range	(Note 1)	2.5		6.0	V
IN Undervoltage Lockout	V_{IN} rising, hysteresis = 200mV	2.0		2.5	V
IN Quiescent Current	V_{FB} = 1.3V, LX not switching			1	mA
	V_{FB} = 1.2V, switching			5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = +5V, Circuit of Figure 1, V_{VOP} = +16V, V_{VGH} = 30V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-VOLTAGE LDO					
VREF_I Input-Voltage Range		10		18	V
VREF_I Undervoltage Lockout	VREF_I rising			5.8	V
VREF_I Input-Bias Current	No load			250	µA
VREF_O Dropout Voltage	I_{VREF_O} = 30mA, VREFI - VREFO			0.5	V
VREF_FB Regulation Voltage	1mA ≤ I_{VREF_O} ≤ 30mA	1.23		1.25	V
	10V < V_{VREF_I} < 18V, I_{VREF_O} = 20mA, V_{VREF_O} = 9V	-0.9		+0.9	mV/V
VREF_O Maximum Output Current		40			mA
STEP-UP REGULATOR					
Output-Voltage Range		V_{IN}		18	V
FB Regulation Voltage	No load	1.228		1.252	V
FB Line Regulation	V_{IN} = 2.5V to 6V			0.15	%/V
FB Transconductance	I_{COMP} = ±2.5µA	80		550	µS
LX SWITCH					
LX Current Limit	V_{FB} = 1.2V, duty cycle = 75%	3.9		5.4	A
LX On-Resistance	V_{IN} = 5V			0.2	Ω
	V_{IN} = 3V			0.26	
Current-Sense Transresistance		0.08		0.25	V/A
OSCILLATOR					
Frequency	V_{FREQ} = 0V	500		780	kHz
	V_{FREQ} = 5V	1000		1400	
FREQ Pulldown Current	V_{FREQ} = 5V	3		9	µA
Maximum Duty Cycle	V_{FREQ} = 0V or 5V	89		96	%
SOFT-START					
SS Reset Resistance	V_{EN} = 0V, I_{SS} = 10mA			20	Ω
SS Charge Current	V_{SS} = 1.2V	2		6	µA
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
VDPM Capacitor Charge Current	MLG startup, V_{VDPM} = 0V	4		6	µA
VDPM Turn-On Threshold	VDPM rising	1.21		1.27	V
VDPM Pulldown Resistance	I_{VDPM} = 10mA			20	Ω
VFLK Input Low Voltage	V_{IN} = 2.5V to 6V			0.7	V
VFLK Input High Voltage	2.5V < V_{IN} < 4.5V	1.9			V
	4.5V < V_{IN} < 6V	2.3			
VGH Input-Voltage Range				35	V
VGH Input Current	V_{VDPM} = 1.5V, VFLK = IN			450	µA
	V_{VDPM} = 1.5V, VFLK = AGND			350	
VGH-to-VGHM Resistance	V_{VDPM} = 1.5V, V_{VFLK} = 5V, I = 10mA			15	Ω
VGHM-to-DRN Resistance	V_{VDPM} = 1.5V, V_{VFLK} = 0V, I = 10mA			60	Ω

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = +5V, Circuit of Figure 1, V_{VOP} = +16V, V_{VGH} = 30V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SERIES SWITCH GATE DRIVER					
GATE Output Sink Current	V_{GATE} = 5V	8		12	µA
	V_{GATE} = 0V	10			mA
GATE Done Voltage Threshold	GATE falling			0.5	V
GATE Output Voltage Low	I_{GATE} = 1mA			0.05	V
GATE Output Voltage High	I_{GATE} = -1mA, V_{EN} = 0V	V_{IN} - 0.05			V
OPERATIONAL AMPLIFIER					
VOP Supply Range		6		18	V
VOP Overvoltage Threshold	VOP rising	19		21	V
VOP Supply Current	No load			5	mA
VOP Input Offset Voltage	V_{OPI} = V_{VOP}/2	-14		+14	mV
Input Common-Mode Voltage Range		0		V_{VOP}	V
OPO Output Voltage High	I_{OPO} = +5mA, V_{OPI} = V_{VOP}	V_{VOP} - 100			mV
OPO Output Voltage Low	I_{OPO} = -5mA, V_{OPI} = 0V			100	mV
Short-Circuit Current	Sourcing, V_{OPI} = V_{VOP} - 3V, V_{OPO} = V_{VOP} - 4V	100			mA
	Sinking, V_{OPI} = 3V, V_{OPO} = 4V	100			
Power-Supply Rejection Ratio	DC, 10V ≤ V_{VOP} ≤ 18V	60			dB
XAO FUNCTION					
VDET Threshold	VDET falling, V_{IN} = 5V	1.22		1.26	V
XAO Output Voltage	V_{VDET} = 0V, I_{XAO} = 10mA			0.4	V
HIGH-VOLTAGE STRESS MODE					
HVS_EN Input Low Voltage				0.8	V
HVS_EN Input High Voltage		2.1			V
HVS_EN Pulldown Resistance			300		kΩ
RHVS Output Voltage	(Note 1)			6	V
RHVS On-Resistance	V_{HVS_EN} = 5V, I_{RHVS} = 10mA			20	Ω
CONTROL INPUTS					
Input Low Voltage [EN, FREQ]	V_{IN} = 2.5V to 6V			0.6	V
Input High Voltage [EN, FREQ]	V_{IN} = 4.5V to 6V	2.4			V
	V_{IN} = 2.5V to 4.5V	1.9			

Note 1: For 5.5V < V_{IN} < 6.0V, use IC for no longer than 1% of IC lifetime. For continuous operation, input voltage should not exceed 5.5V.

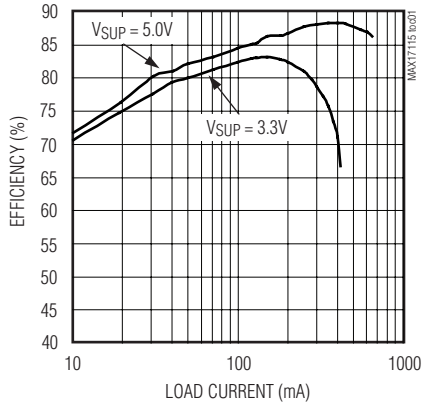
Note 2: Specifications to T_A = -40°C are guaranteed by design, not production tested.

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

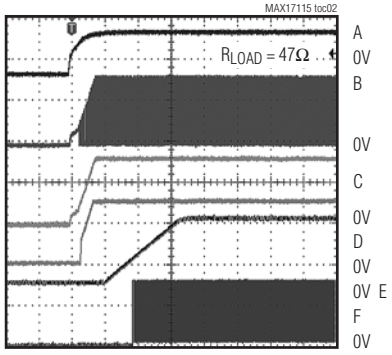
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 5V, V_{MAIN} = 16V, T_A = +25°C, unless otherwise noted.)

STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT

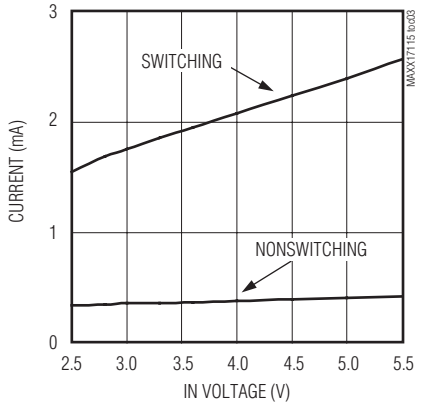


POWER-UP SEQUENCE

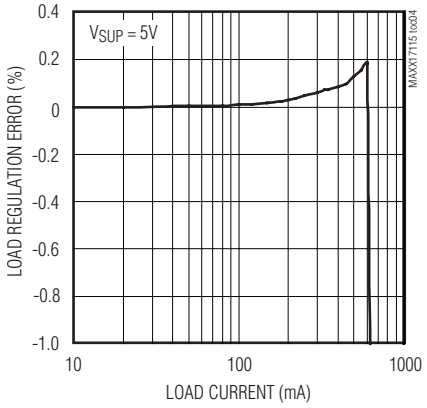


A: V_{SUP}, 5V/div
B: V_{LX}, 10V/div
C: V_{MAIN}, 10V/div
D: V_{VREF_O}, 10V/div
E: V_{VDPM}, 2V/div
F: V_{VGHM}, 20V/div

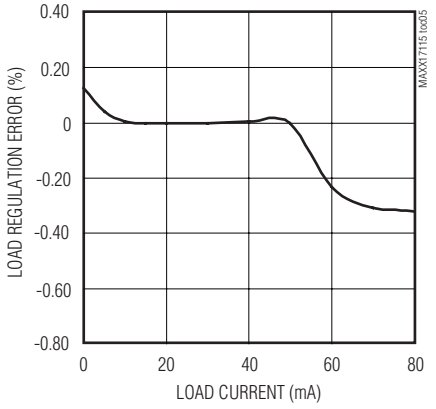
IN SUPPLY QUIESCENT CURRENT vs. IN VOLTAGE



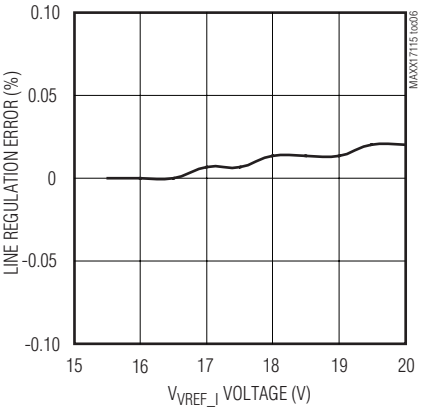
STEP-UP REGULATOR OUTPUT LOAD REGULATION vs. LOAD CURRENT



REFERENCE VOLTAGE OUTPUT LOAD REGULATION vs. LOAD CURRENT



REFERENCE VOLTAGE OUTPUT LINE REGULATION (%)

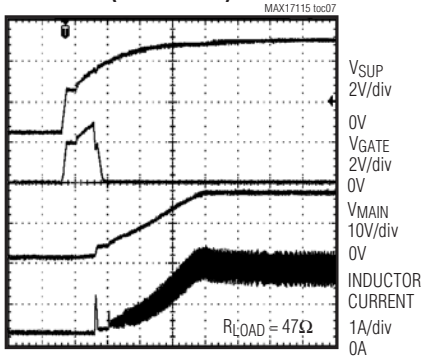


Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

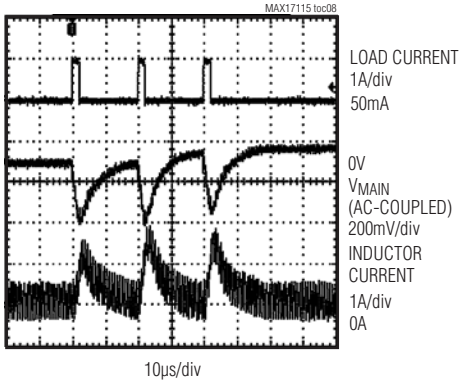
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 5V, V_{MAIN} = 16V, T_A = +25°C, unless otherwise noted.)

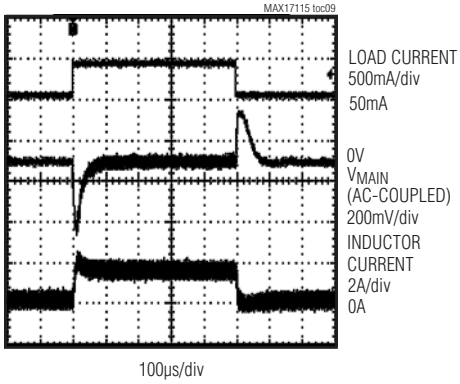
STEP-UP REGULATOR SOFT-START (HEAVY LOAD)



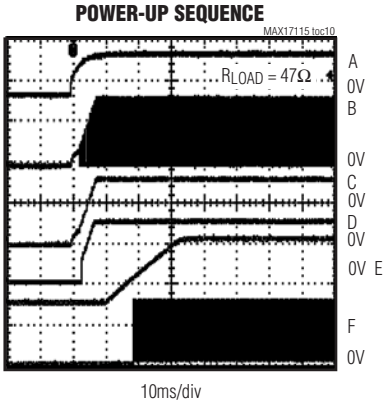
STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE



STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE

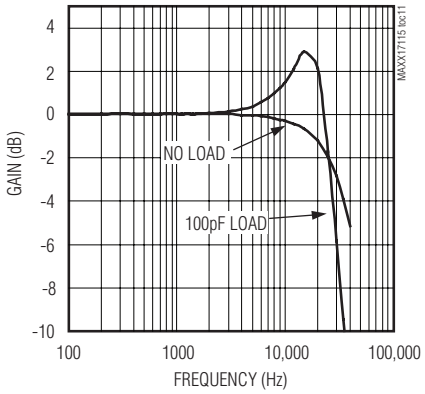


POWER-UP SEQUENCE

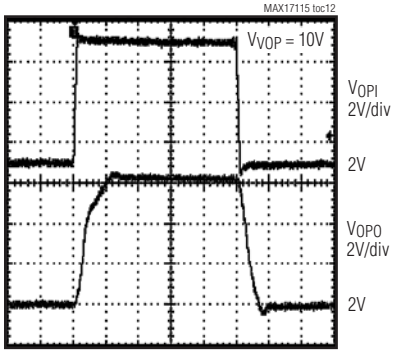


A: V_{SUP}, 5V/div
B: V_{LX}, 10V/div
C: V_{MAIN}, 10V/div
D: V_{VREF_O}, 10V/div
E: V_{VDPM}, 2V/div
F: V_{VGHM}, 20V/div

OPERATIONAL AMPLIFIER FREQUENCY RESPONSE



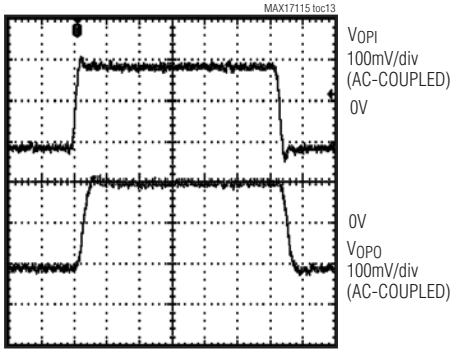
OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



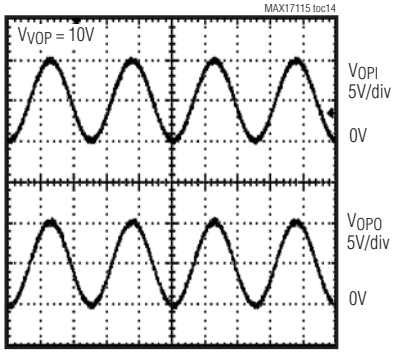
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 5V, V_{MAIN} = 16V, T_A = +25°C, unless otherwise noted.)

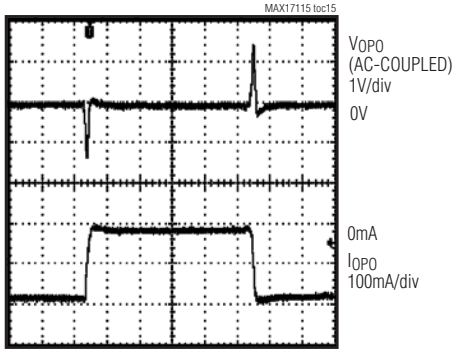
OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE



OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT



OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE



Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

Pin Description

PIN	NAME	FUNCTION
1	VREF_FB	High-Voltage LDO Regulator Feedback Input. Connect VREF_FB to the center of a resistive voltage-divider between VREF_O and AGND to set the LDO output voltage. Place the resistive voltage-divider within 5mm of VREF_FB.
2	VREF_O	High-Voltage LDO Regulator Output. Bypass VREF_O to AGND with a minimum 2.2µF capacitor within 5mm of the pin.
3	VREF_I	High-Voltage LDO Regulator Supply Input. Bypass VREF_I to AGND with a minimum 1µF capacitor within 5mm of the pin.
4	VOP	Operational Amplifier Supply Input. Typically connected to the output of the step-up regulator. Bypass VOP to OPGND with a minimum 1µF capacitor within 5mm of the pin.
5	OPO	Operational Amplifier Output. OPO is high impedance in shutdown.
6	OPI	Operational Amplifier Noninverting Input
7	OPGND	Operational Amplifier Ground
8	VFLK	High-Voltage Switch Control Input. When VFLK is high, the high-voltage switch between VGH and VGHM is on and the high-voltage switch between VGHM and DRN is off. When VFLK is low, the switch between VGH and VGHM is off and the switch between VGHM and DRN is on. VFLK is inhibited by the IN UVLO and when the voltage on VDPM is less than 1.24V.
9	XAO	Reset and XAO Function Output
10	VDET	Voltage-Detection Input. Connect VDET to the center of a resistive voltage-divider between IN and AGND to set the threshold voltage for the XAO function.
11	HVS_EN	High-Voltage Stress Control Input. When HVS_EN is high, the internal switch between RHVS and AGND is on. When HVS_EN is low, RHVS is high impedance.
12	FREQ	Frequency-Select Input. Connect FREQ to AGND to select the step-up regulator's 640kHz operating frequency. Connect FREQ to IN to select the step-up regulator's 1.2MHz operating frequency. This input has 6µA pulldown current.
13	EN	Shutdown Control Input. Connect EN to AGND to disable the boost operation. Connect EN to IN to enable the boost operation.
14, 26	AGND	Analog Ground
15, 16	IN	Power-Supply Input. IN supplies the internal reference and other internal circuitry. Connect IN to the input supply voltage and bypass IN to AGND with a minimum 1µF ceramic capacitor. (Pin 15 supplies current to internal analog circuits. Using an RC filter on pin 15 improves noise performance of the IC. Minimum resistor should be used on pin 16 due to high current through pin 16.)
17	GATE	External p-Channel MOSFET Gate-Drive Output. If used, connect GATE to the gate of an external p-channel MOSFET between the input supply and the step-up converter's inductor (see Figure 1). If not used, leave GATE unconnected.
18, 19	LX	Step-Up Regulator Switching Node. Drain of the internal n-channel MOSFET between LX and PGND. Connect the inductor and catch diode here and minimize trace area for lowest EMI.
20, 21	PGND	Power Ground. Source of the internal n-channel MOSFET between LX and PGND.
22, 28	N.C.	No Connection. Not internally connected.
23	RHVS	Open-Drain Output of the Internal n-Channel MOSFET to AGND. Connect RHVS to FB through a resistor to adjust the step-up converter's output to a higher voltage. If unused, leave RHVS unconnected. When HVS_EN is low, RHVS is high impedance. When HVS_EN is logic-high, RHVS connects to AGND.
24	FB	Step-Up Regulator Feedback Input. Connect FB to the center of a resistive voltage-divider between the step-up regulator output and AGND to set the regulator's output voltage. Place the resistive voltage-divider within 5mm of FB.

Pin Description (continued)

PIN	NAME	FUNCTION
25	COMP	Compensation Pin for Error Amplifier. Connect a series RC from COMP to AGND. Typical values are 47.5kΩ and 560pF.
27	SS	Soft-Start Control Pin. Connect a capacitor (C_{SS}) to this pin. Leave SS unconnected if a slow soft-start is not desired. The soft-start capacitor is charged by a 4µA current source. The full current limit is reached after around t = C_{SS} x 200µs/nF. The soft-start capacitor is discharged to AGND when EN is low. On EN's rise, the soft-start capacitor is quickly charged to 0.4V, after which, soft-start begins.
29	VDPM	High-Voltage Switch Delay Input. Connect a capacitor from VDPM to AGND to set the high-voltage switch startup delay.
30	VGH	High-Voltage Switch Supply Input. Source of the internal high-voltage p-channel MOSFET between VGH and VGHM. Bypass VGH to PGND with a minimum of 0.1µF capacitor within 5mm of VGH.
31	VGHM	High-Voltage Switch Output. VGHM is the common junction of the internal high-voltage MOSFETs. VGHM is typically used to power the gate-driver IC's positive supply input.
32	DRN	High-Voltage Switch Input. Drain of the internal high-voltage MOSFET switch between DRN and VGHM.
—	EP	Exposed Pad. Connect EP to AGND.

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

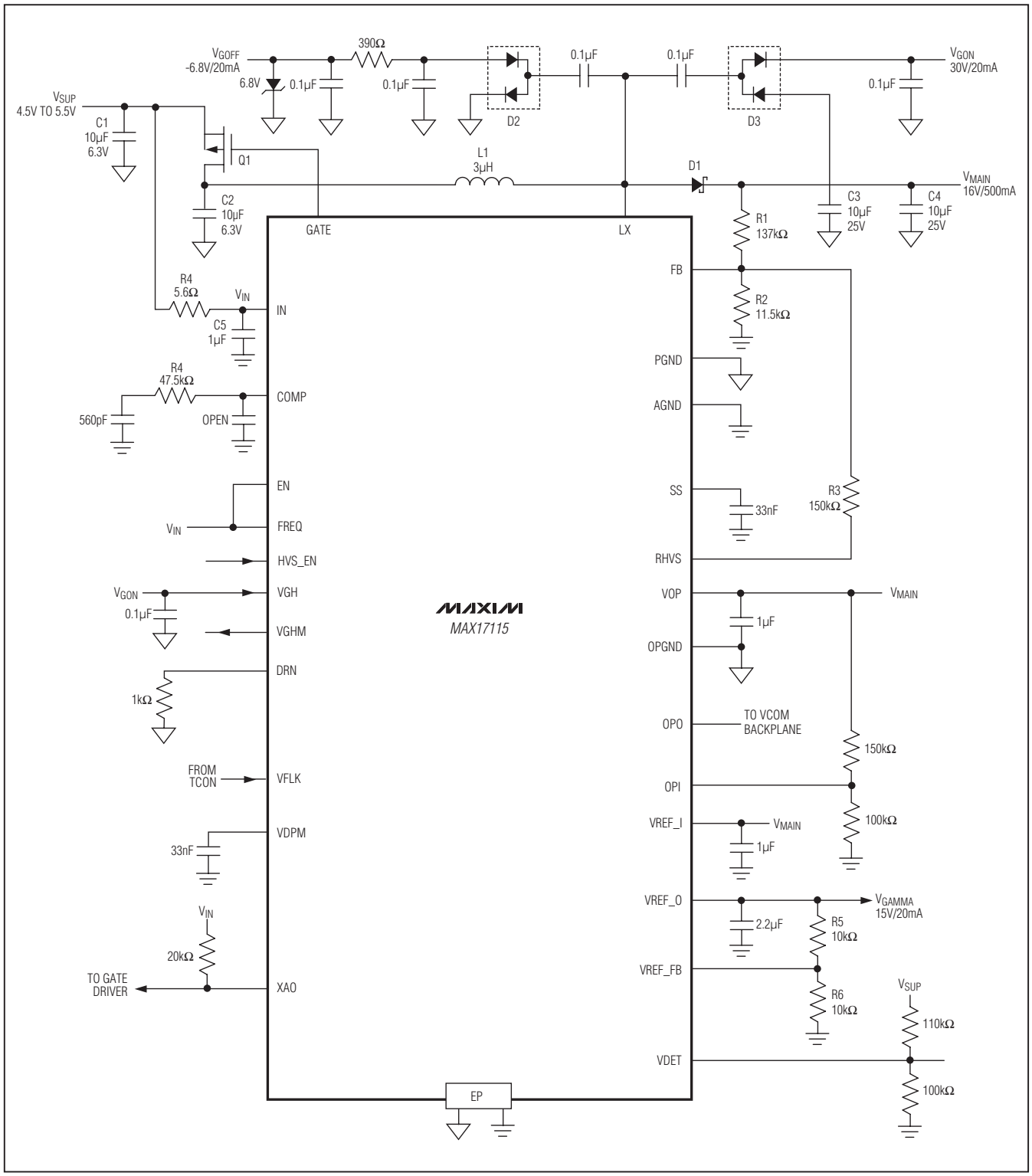


Figure 1. Typical Operating Circuit

Table 1. Component List

REFERENCE DESIGNATION	DESCRIPTION
C1, C2	10µF, 6.3V X5R ceramic capacitors (0805) TDK C2012X5R0J106K
C3, C4	10µF, 25V X5R ceramic capacitors (1206) TDK C3216X5R1E106M
D1	3A, 30V Schottky diode (M-flat) Toshiba CMS02
D2, D3	200mA, 100V dual diodes (SOT23) Fairchild MMBD4148SE
L1	3.0µH, 3A inductor Sumida CDRH6D28-3R0
Q1	SC-70 SiA443DJ, p-channel MOSFET, -20V/63mΩ Vishay PowerPak

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild Semiconductor	847-803-6100	847-390-4405	www.fairchildsemi.com
Sumida Corp.	408-822-2000	408-822-2102	www.sumida.com
TDK Corp.	847-545-6700	847-545-6720	www.component.tdk.com
Toshiba America Electronic Components, Inc.	949-455-2000	949-859-3963	www.toshiba.com/taec
Vishay	402-563-6866	402-563-6296	www.vishay.com

Typical Operating Circuit

The MAX17115 typical operating circuit (Figure 1) is a complete power-supply system for TFT LCD displays. The circuit generates a +16V/500mA source-driver supply and +30V/20mA and -6.8V/20mA gate-driver supplies. The input-voltage range for the IC is from +2.5V to +6.0V. The listed load currents in Figure 1 are available from a +4.5V to +5.5V supply. Table 1 lists some recommended components, and Table 2 lists the contact information of component suppliers.

Detailed Description

The MAX17115 contains a high-voltage step-up regulator, a high-accuracy linear regulator, a high-performance amplifier, a high-voltage switch control block for gate-driver supply modulation, and a logic-controlled open-drain MOSFET switch to AGND for high-voltage stress aging tests. Figure 2 shows the MAX17115 functional diagram.

Step-Up Regulator

The main step-up regulator employs a current-mode, fixed-frequency (1.2MHz/640kHz-selectable) PWM architecture to maximize loop bandwidth and provides fast-transient response to pulsed loads typical of TFT-LCD panel source drivers. High switching frequency operation allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. A current-control external capacitor-controlled programmable soft-start minimizes inrush currents. The output voltage can be set from V_{IN} to 18V with an external resistive voltage-divider.

The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN}-V_{IN}}{V_{MAIN}}$$

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

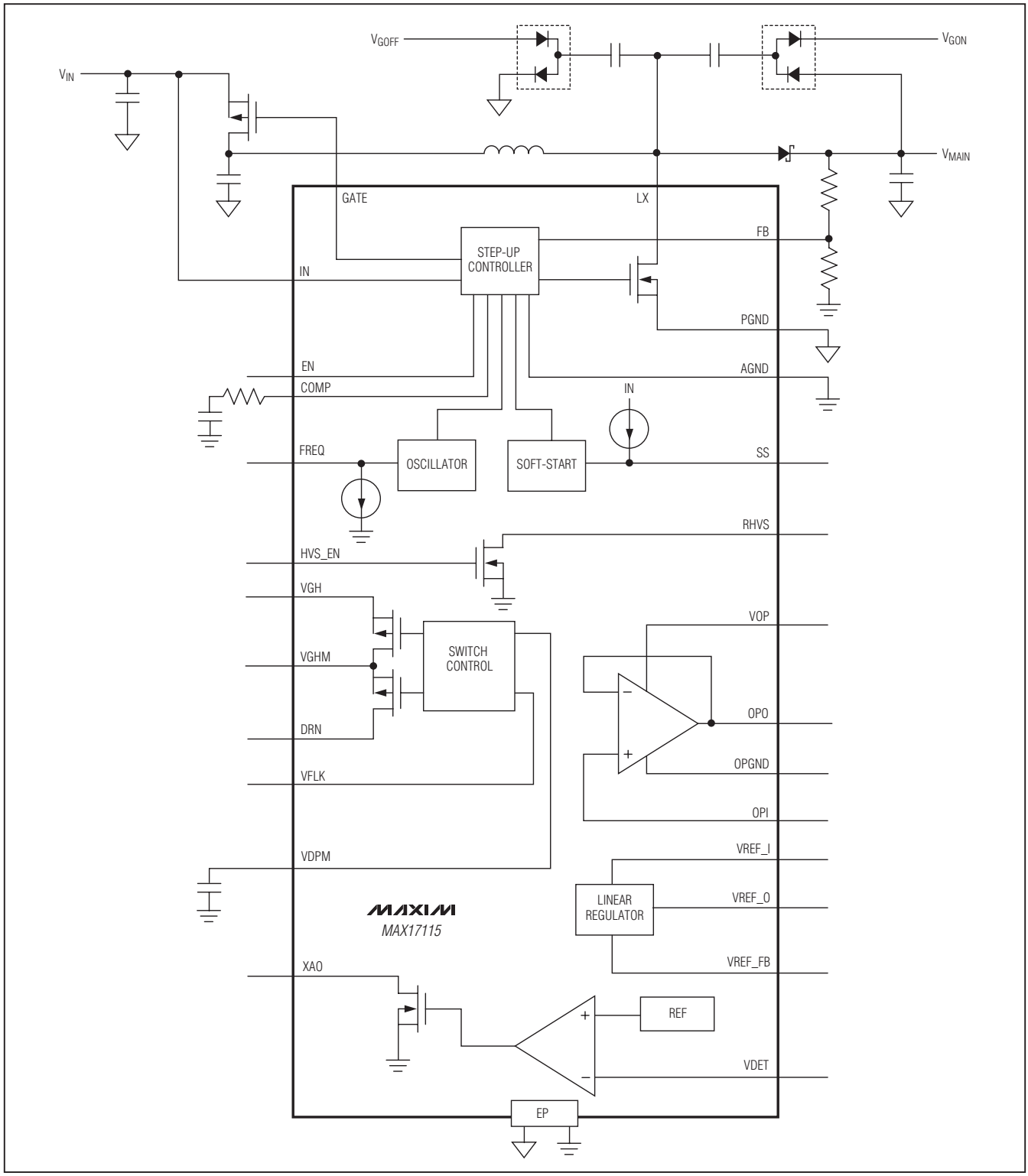


Figure 2. MAX17115 Functional Diagram

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

Figure 3 shows the functional diagram of the step-up regulator. An error amplifier compares the signal at FB to 1.24V and changes the COMP output. The voltage at COMP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceeds the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the boost diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Operational Amplifier

The MAX17115 has one operational amplifier. The buffer amplifier is typically used to drive the LCD backplane voltage (VCOM) in TFT LCDs. It features high output current, 45V/µs slew rate, and 20MHz/3dB bandwidth. The rail-to-rail input and output capability maximizes system flexibility.

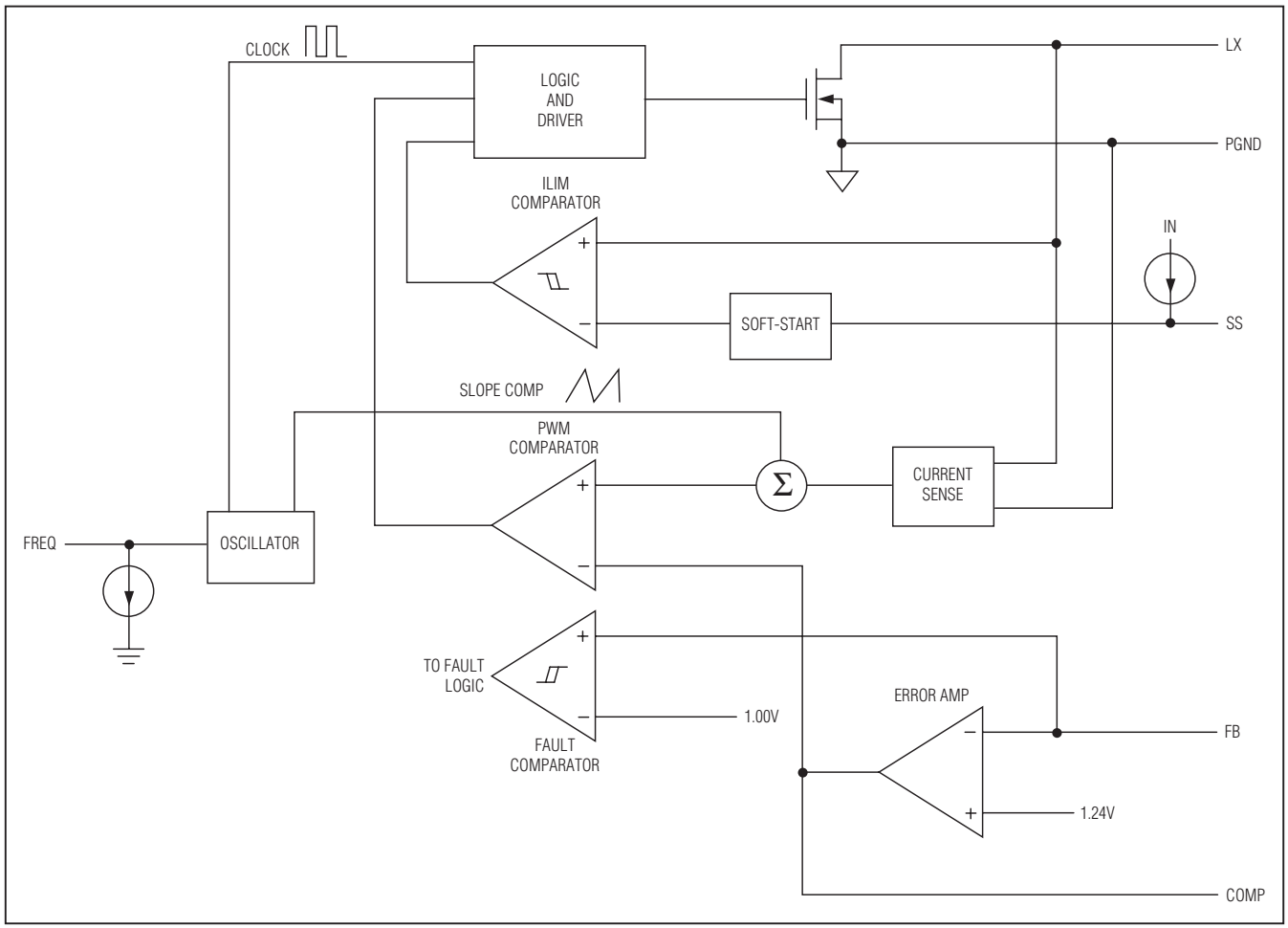


Figure 3. Step-Up Regulator Functional Diagram

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

Short-Circuit Current Limit

The operational amplifier limits short-circuit current to approximately ±200mA if the output is directly shorted to VOP or to OPGND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ) and activates the thermal-fault protection, shutting off all the IC's outputs. The IC restarts automatically when the device cools down by approximately 15°C.

Driving a Pure Capacitive Load

In general, the LCD backplane (VCOM) consists of a distributed series capacitance and resistance, a load that can be easily driven by the buffer. However, if the buffer is used in an application with a pure capacitive load, steps must be taken to ensure stable operation.

As the buffer amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between OPO and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω, and the typical value of the capacitor is 10nF.

Undervoltage Lockout (UVLO)

The UVLO circuit compares the input voltage at IN with the UVLO threshold (2.25V typ) to ensure the input voltage is high enough for reliable operation. The wide 200mV (typ) hysteresis prevents supply transients from causing a restart. The startup procedure begins when the input voltage exceeds the UVLO rising threshold and EN goes above threshold. During normal operation, if the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator, turns off the linear regulator, pulls GATE high to turn off the external p-channel MOSFET, disables the buffer, placing its output into a high-impedance state, and disables the switch control block, placing VGHM into a high-impedance state.

High-Accuracy High-Voltage LDO Regulator

The LDO features high output accuracy (±0.5%) and low-dropout (LDO) voltage (0.25V typ) and can supply at least 40mA. The LDO is typically used to drive a gamma buffer reference resistor string and its output voltage is adjustable through a resistor-divider.

Power-Up Sequence and Soft-Start

Once IN exceeds its UVLO (2.25V typ) and EN is above its logic-high threshold, the startup procedure begins. GATE is initially high and pulled low to turn on the external p-channel MOSFET if no output fault is detected. After GATE reaches its GATE-done threshold, the main step-up regulator's soft-start begins. With the main step-up regulator's soft-start, the voltage on VOP and VREF_I rises. Once VOP or VREF_I exceeds the UVLO, the relative buffer amplifier and LDO are enabled. Figure 4 shows the power-up sequence.

The IC employs a current-based, external-capacitor adjustable soft-start for the step-up regulator to control inrush current and voltage overshoot and to ensure a well-defined startup behavior. The voltage level on the SS pin directly controls an internal current limit. The current limit reaches its full current limit at approximately:

$$t = C_{SS} \times 200\mu s/nF$$

The step-up regulator output voltage usually reaches regulation before C_{SS} reaches its fully charged state.

A capacitor (C_{VDPM}) from VDPM to AGND determines the switch-control-block startup delay. After the soft-start routine is complete, a 5µA current source starts charging C_{VDPM}. Once the capacitor voltage exceeds 1.24V (typ), the switch-control block is enabled as shown in Figure 4. After the switch-control block is enabled, VGHM can be connected to VGH or DRN through the internal high-voltage p-channel switches, depending upon the state of VFLK. Before startup (EN is low) or when IN is less than its UVLO, both VGHM switches are turned off and VDPM is internally connected to AGND to discharge C_{VDPM}. Select C_{VDPM} to set the delay time using the following equation:

$$C_{VDPM} = DELAY\_TIME \times \frac{5\mu A}{1.24V}$$

Switch-Control Block

The switch-control block is not activated until all four of the following conditions are satisfied:

- The input voltage exceeds its UVLO.
- The soft-start routine of the boost regulator is complete.
- No fault condition is detected.
- V_{VDPM} exceeds its turn-on threshold. VDPM begins charging when SS reaches the internal threshold. Once activated, if VFLK is high, the 5Ω (typ) internal p-channel switch between VGH and VGHM turns on and the 30Ω (typ) p-channel switch between VGHM

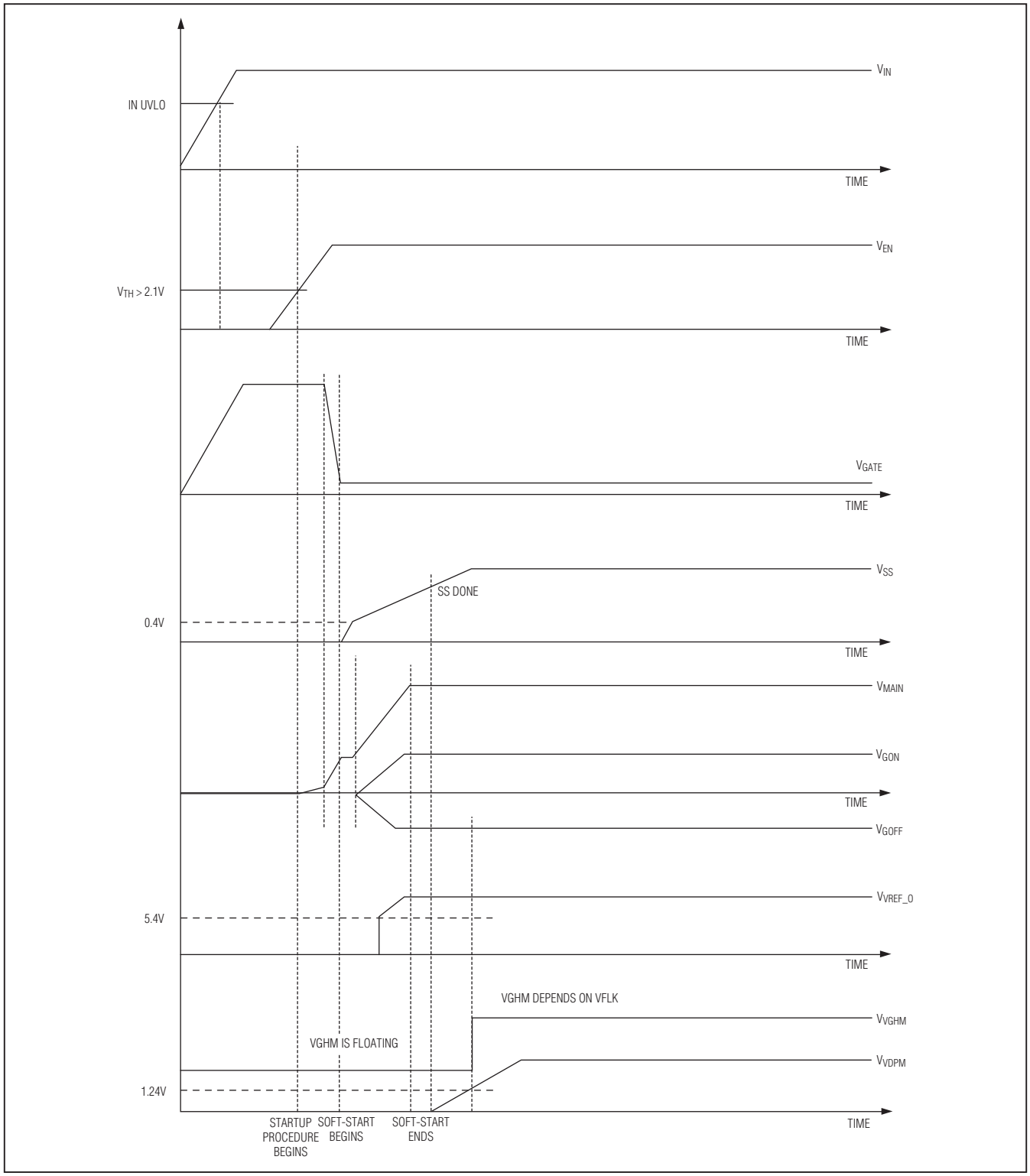


Figure 4. Power-Up Sequence

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

and DRN turns off. If VFLK is low, the 5Ω (typ) internal p-channel switch between VGH and VGHM turns off and the 30Ω (typ) p-channel switch between VGHM and DRN turns on. Before activation, neither switch is turned on and VGHM is in a high-impedance state.

Fault Protection

During steady-state operation, if the output of the main regulator does not exceed its respective fault-detection threshold, the MAX17115 activates an internal fault timer. If the continuous fault exceeds the fault-timer duration (55ms typ), the MAX17115 sets the fault latch to shut down all the outputs and turn off the external p-channel MOSFET (GATE is pulled high). Once the fault condition is removed, cycle the input voltage to clear the fault latch and reactivate the device.

The MAX17115 also provides OVP for the output of the step-up regulator by monitoring the voltage on the VOP pin. During normal operation, if VOP is higher than the VOP overvoltage threshold (20V typ), the step-up converter stops switching to prevent excessive voltage from damaging the MAX17115. Once VOP drops below the threshold voltage, the step-up regulator resumes switching and regulates the needed output voltage.

Thermal-Overload Protection

Thermal-overload protection prevents excessive power dissipation from overheating the MAX17115. When the junction temperature exceeds T_J = +160°C (typ), a thermal sensor immediately activates the fault protection to shut down all outputs and turns off the external p-channel MOSFET (GATE is pulled high), allowing the device to cool down. Once the device cools down by approximately 15°C, the MAX17115 starts up automatically. The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

High-Voltage Stress (HVS) Mode

The HVS mode is used to increase the supply voltage of TFT LCD for aging tests. The MAX17115 provides an internal open-drain switch to AGND that is typically used to change the feedback divider impedance of the step-up regulator (FB). Connect an appropriate resistor from RHVS to FB to implement this feature.

A control input (HVS_EN) determines when the switch is turned on. When HVS_EN is high, the internal switch is turned on and the output voltage is adjusted according to the resistor connected to the feedback input. Conversely, when HVS_EN is low, the switch is turned off and the output remains in its original voltage setting.

XAO Function

XAO is an open-drain output that connects to AGND whenever V_{IN} is below its UVLO threshold (2.25V typ) or V_{VDET} is below its detection threshold (1.24V typ). In the meantime, VGHM is tied to VGH. XAO is guaranteed to remain low until V_{IN} falls below the XAO UVLO level (1.7V max).

Design Procedure

Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient-response time, and output-voltage ripple. Size and cost are also important factors to consider.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and conduction losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase size and can increase conduction losses in the inductor. Low-inductance values decrease the size, but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant, LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full-load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.6. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

In Figure 1, the LCD's gate-on and gate-off supply voltages are generated from two unregulated charge pumps driven by the step-up regulator's LX node. The additional load on LX must therefore be considered in the inductance and current calculations. The effective maximum output current, $I_{MAIN(EFF)}$ becomes the sum of the maximum load current of the step-up regulator's output plus the contributions from the positive and negative charge pumps:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + \eta_{NEG} \times I_{NEG} + (\eta_{POS} + 1) \times I_{POS}$$

where $I_{MAIN(MAX)}$ is the maximum step-up output current, η_{NEG} is the number of negative charge-pump stages, η_{POS} is the number of positive charge-pump stages, I_{NEG} is the negative charge-pump output current, and I_{POS} is the positive charge-pump output current, assuming the initial pump source for I_{POS} is V_{MAIN}.

Using the typical operating circuit of Figure 1, calculate the approximate inductor value using the typical input voltage (V_{SUP}), the maximum output current ($I_{MAIN(EFF)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics* section, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{SUP}}{V_{MAIN}}\right)\left(\frac{V_{MAIN} - V_{SUP}}{I_{MAIN(EFF)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage ($V_{SUP(MIN)}$) using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from the appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(EFF)} \times V_{MAIN}}{V_{SUP(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{SUP(MIN)} \times (V_{MAIN} - V_{IN(MIN)})}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17115's LX current limit (I_{LIM}) should exceed I_{PEAK}, and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering Figure 1, the maximum load current ($I_{MAIN(MAX)}$) is 500mA, with a 16V output and a typical input voltage of 5V. The effective full-load step-up current is:

$$I_{MAIN(EFF)} = 500mA + 1x\ 20mA + (1+1) \times 20mA = 560mA$$

Considering the typical operating circuit, the switching frequency is set to 1.2MHz, the maximum load current ($I_{MAIN(MAX)}$) is 500mA with a 16V output and a typical input voltage of 5V. Choosing an LIR of 0.5 and estimating efficiency 88% at this operating point:

$$L = \left(\frac{5V}{16V}\right)^2\left(\frac{16V - 5V}{0.56A \times 1.2MHz}\right)\left(\frac{0.88}{0.5}\right) \approx 3.0\mu H$$

Using the circuit's minimum input voltage (4.5V) and estimating efficiency of 83% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.56A \times 16V}{4.5V \times 0.83} = 2.40A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{4.5V \times (16V - 4.5V)}{3.0\mu H \times 16V \times 1.2MHz} \approx 0.90A$$

$$I_{PEAK} = 2.40A + \frac{0.90A}{2} = 2.85A$$

Output-Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's ESR:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} \times f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} \times R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors,

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

the output-voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input-Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. Two 10µF ceramic capacitors are used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in the typical operating circuit. Ensure a low-noise supply at IN by using adequate C_{IN}. Alternatively, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC lowpass filter (see R4 and C5 in Figure 1).

Rectifier Diode

The MAX17115's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 3A Schottky diode complements the internal MOSFET well.

Step-Up Regulator Output-Voltage Selection

The output voltage of the main step-up regulator is set by connecting a resistive voltage-divider from the output (V_{MAIN}) to AGND with the center tap connected to FB (see Figure 1). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{V_{FB}} - 1\right)$$

where V_{FB}, the step-up regulator's feedback set point, is 1.24V. Place R1 and R2 close to the IC.

High-Voltage Stress (HVS) Mode Output-Voltage Setting

See Figure 1 for the typical operating circuit. R3 is connected to FB to change the output voltage whenever HVS_EN is high. The required value for R3 can be calculated with the following equation:

$$R3 = \frac{R1}{\frac{V_{MAIN\_HVS}}{V_{FB}} - \left(1 + \frac{R1}{R2}\right)}$$

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability. For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{253 \times V_{SUP} \times V_{OUT} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{V_{OUT} \times C_{OUT}}{10 \times I_{MAIN(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient-response waveforms.

High-Voltage LDO Linear Regulator

Output-Voltage Selection

The output voltage of the high-accuracy LDO is set by connecting a resistive voltage-divider from the output (VREF_O) to AGND with the center tap connected to VREF_FB (see Figure 1). Select R6 in the 10kΩ to 50kΩ range. Calculate R5 with the following equation:

$$R5 = R6 \times \left(\frac{V_{VREF\_O}}{V_{VREF\_FB}} - 1\right)$$

where V_{VREF_FB}, the LDO's feedback set point, is 1.24V. Place R5 and R6 close to the IC.

Input and Output Capacitor Selection

To ensure stability of the LDO, use a minimum of 1µF on the regulator's input (VREF_I) and a minimum of 2.2µF on the regulator's output (VREF_O). Place the capacitors near the pins and connect their ground connections directly together.

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation include the power dissipated in the step-up regulator and the power dissipated by the buffer amplifier and high-voltage LDO.

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

Step-Up Regulator

The largest portions of power dissipation in the step-up regulator are the internal MOSFET, the inductor, and the output diode. If the step-up regulator has 90% efficiency, approximately 3% to 5% of the power is lost in the internal MOSFET, approximately 3% to 4% in the inductor, and approximately 1% in the output diode. The remaining 1% to 3% is distributed among the input and output capacitors and the PCB traces. If the input power is approximately 5W, the power loss in the internal MOSFET is approximately 150mW to 250mW. The following formula can be used to estimate the power loss in the internal power MOSFET (excluding switching losses):

$$P_{LX\_ON} = I^2_{IN(DC,MAX)} \times R_{DSON} \times D$$

where RDSON is the on-resistance for the internal power MOSFET.

Operational Amplifiers

The power dissipated in the buffer amplifier depends on the output current, the output voltage, and the supply voltage:

$$PD_{SOURCE} = I_{OPO\_SOURCE} \times (V_{VOP} - V_{OPO})$$

$$PD_{SINK} = I_{OPO\_SINK} \times V_{OPO}$$

where I_{OPO_SOURCE} is the output current sourced by the amplifier, and I_{OPO_SINK} is the output current that the amplifier sinks.

High-Voltage LDO Regulator

The power dissipation of the high-voltage LDO depends on load current and the voltage drop between VREF_I and VREF_O. It can be estimated by the following formula:

$$P_{LR} = I_{LOAD} \times V_{DROP}$$

where I_{LOAD} is the output current from the LDO and V_{DROP} is the voltage drop between VREF_I and VREF_O.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of high-current loops by placing the inductor, the output diode, and the output capacitors near the input capacitors and near the LX and PGND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), and to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance. Create a power-ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the operational amplifier divider ground connection, the COMP, VDPM and SS capacitor ground connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.
- Place all feedback voltage-divider resistors within 5mm of their respective feedback pins. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Take care to avoid running any feedback trace near LX or the switching nodes in the charge pumps, or provide a ground shield.
- Place the IN pin bypass capacitors as close as possible to the device. The ground connection of the IN bypass capacitor should be connected directly to the AGND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient response.
- Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from feedback nodes (FB) and analog ground. Use DC traces to shield necessary.

Refer to the MAX17115 evaluation kit for an example of proper PCB layout.

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 TQFN	T-3255+4	21-0140

Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	0
1	4/10	Added reflow temperature and removed a line in the fault-protection description	2, 4, 6, 18, 22