Click here to ask an associate for production status of specific part numbers.

4V to 60V, 50mA, Ultra-Small, High Efficiency, Synchronous Step-Down DC-DC Converter

MAX17553

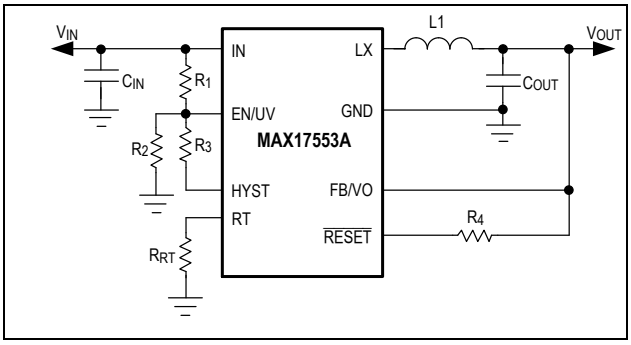
Product Highlights

- Reduces External Components and Total Cost
  - No Schottky–Synchronous Operation
  - Internal Control Loop Compensation
  - Internal Fixed Soft-Start
  - All-Ceramic Capacitors, Ultra-Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4V to 60V Input Voltage Range
  - Adjustable Output Range from 0.8V up to 90% of V_{IN} (MAX17553C)
  - Delivers Up to 50mA Load Current
  - 150kHz to 1.5MHz Adjustable Switching Frequency
- Reduces Power Dissipation
  - 91.5% Full Load Efficiency (V_{IN} = 24V, V_{OUT} = 5V)
  - Higher Light-Load Efficiency with Discontinuous-Conduction Mode (DCM) Operation
  - Power Loss Reduction with External Boot-Strap Input (FB/VO) for Internal Circuitry (MAX17553A and MAX17553B only)
  - 3.8µA Shutdown Current
- Flexible Design
  - Programmable EN/UV and HYST Threshold
  - Open-Drain Output ($\overline{RESET}$) for Output Status Monitoring
- Robust Operation
  - Built-in Hiccup Mode Overload Protection
  - Overtemperature Protection
  - CISPR32 Class B Compliant
  - Wide -40°C to +125°C Ambient Operating Temperature, -40°C to +150°C Junction Temperature

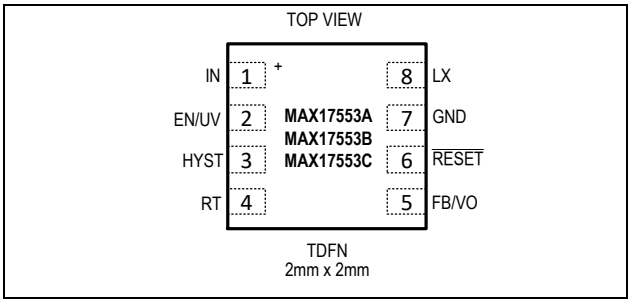
Key Applications

- Factory Automation
  Within the many different applications in the Factory Automation space, one key need is the ability to generate less heat. Heat within the system needs to be managed to prevent overheating and shutdown. The MAX17553 generates less heat as it is a fully synchronous integrated FETs DC-DC converter with high efficiency.
- Aftermarket Market Automotive
  An example of within the aftermarket automotive space where the MAX17553 would provide a benefit is the asset tracking application. Asset tracking has increased in popularity as the ability to wireless connect to these monitors has become easier. Typically, these units are designed to be as small as possible. The MAX17553 has integrated FETs, integrated compensation, delivering a small solution size. Small size and fewer components help drive overall design costs down for the system.
- General Point of Load
  General point of load is a generic term that applies to a switching regulator that serves many applications and design environments. The robustness of the power conversion is critical to any environment. With an operating range of -40ºC to +125ºC, current limit protection, overtemperature protection, and the ability to adhere to the CISPR32 class B emission standards, the MAX17553 delivers highly efficient power conversion in the most adverse environments and provides the designer the peace of mind that it is robust and reliable.

Simplified Application Diagram



Pin Description



***Ordering Information* appears at end of data sheet.**

19-101434; Rev 1; 4/22

 © 2022 Analog Devices, Inc. All rights reserved.

Absolute Maximum Ratings

IN to GND ..... -0.3V to +70V

LX to GND ..... -0.3V to V_{IN} + 0.3V

EN/UV to GND ..... -0.3V to V_{IN} + 0.3V

RT to GND ..... -0.3V to +6V

HYST, $\overline{RESET}$ to GND ..... -0.3V to +6V

FB/VO to GND (MAX17553A, MAX17553B) ..... -5.5V to +6V

FB/VO to GND (MAX17553C) ..... -0.3V to +6V

Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (T_A = +70°C, 8-Pin TDFN, derate 6.2mW/°C above +70°C) 496mW

Operating Temperature Range (Note 1) ..... -40°C to +125°C

Junction Temperature ..... -40°C to +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... +300°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 TDFN	
Package Code	T822CN+1
Outline Number	21-0487
Land Pattern Number	90-0349
Thermal Resistance, Four Layer Board	
Junction-to-Ambient (θ_{JA})	162 °C/W
Junction-to-Case Thermal Resistance (θ_{JC})	20 °C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages.* Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial.*

Electrical Characteristics

(V_{IN} = $V_{EN/UV}$ = 24V, V_{GND} = 0V, C_{IN} = 1µF, $V_{FB/VO}$ = 1.05 × V_{FB-REG}, LX = RT = HYST = $\overline{RESET}$ = Unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted. (Note 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)							
Input Voltage Range	V_{IN}			4		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UV}$ = 0V			3.8		µA
Input Supply Current	I_{IN-NL}	No Load (Note 3)	MAX17553A		166		µA
			MAX17553B		275		
			MAX17553C		388		
ENABLE/UNDERVOLTAGE (EN/UV)							
EN/UV Threshold	V_{ENR}	$V_{EN/UV}$ rising		1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UV}$ falling		1.068	1.09	1.112	
	$V_{EN-TRUESD}$	$V_{EN/UV}$ falling, true shutdown			0.75		
EN/UV Input Leakage Current	$I_{EN/UV}$	$V_{EN/UV}$ = 1.3V, T_A = +25°C		-100		+100	nA
HIGH-SIDE AND LOW-SIDE MOSFETS							
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.05A (Sourcing)			5.4	10	Ω
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.05A (Sinking)			1.5	3	Ω
LX Leakage Current	I_{LX_LKG}	T_A = +25°C, V_{LX} = (V_{GND} + 1V) to (V_{IN} - 1V)		-1.5		1	µA
SOFT-START (SS)							
Soft-Start Time	t_{SS}			2.88	3.2	3.52	ms
SS Delay		V_{EN} > V_{ENR}			170	275	µs
FEEDBACK/VOUTPUT (FB/VO)							
FB Regulation Voltage	V_{FB-REG}	MAX17553A		3.25	3.3	3.35	V
		MAX17553B		4.93	5	5.07	
		MAX17553C		0.79	0.8	0.81	
FB Input Bias Current	I_{FB}	MAX17553A/MAX17553B			360		µA
		MAX17553C, T_A = T_J = 25˚C		-100		+100	nA
CURRENT LIMIT							
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$			155	180	205	mA
Valley Current-Limit Threshold	$I_{VALLEY-LIMIT}$	up to 2×t_{SS}		85	110	125	mA
		after 2×t_{SS}		0	22	32	
Zero-Cross Threshold	I_{ZX}			-6	2	10	mA
OSCILLATOR (RT)							
Switching Frequency Accuracy				-10		+10	%
Switching Frequency	f_{SW}	R_{RT} = Unconnected		275	310	345	kHz

(V_{IN} = $V_{EN/UV}$ = 24V, V_{GND} = 0V, C_{IN} = 1µF, $V_{FB/VO}$ = 1.05 × V_{FB-REG}, LX = RT = HYST = $\overline{RESET}$ = Unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted. (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency Adjustable Range		See the Switching Frequency (RT) section for more details	150		1500	kHz
TIMING						
Minimum On-Time	t_{ON_MIN}			80	105	ns
Minimum Off-Time	t_{OFF_MIN}			75	95	ns
Hiccup Timeout				64		ms
OUTPUT VOLTAGE STATUS ($\overline{RESET}$)						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 10mA			400	mV
$\overline{RESET}$ Output Leakage Current		T_A = +25°C, $V_{\overline{RESET}}$ = 5.5V	-100		+100	nA
FB/VO Thresholds for $\overline{RESET}$ Rising	V_{OKR}		93	95	97	%
FB/VO Thresholds for $\overline{RESET}$ Falling	V_{OKF}		90	92	94	%
$\overline{RESET}$ Delay After FB/VO Reach 95% Regulation	t_D			30		µs
HYST						
HYST Output Level Low		V_{IN} = 2V, $V_{EN/UV}$ < V_{ENF}, I_{HYST} = 100µA,			0.4	V
HYST Hi-Z Output Leakage Current		T_A = T_J = +25°C, V_{HYST} = 1.2V, $V_{EN/UV}$ > V_{ENR}	-100		+100	nA
HYST Sink Capability					100	µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		160		°C
Thermal Shutdown Hysteresis				20		°C

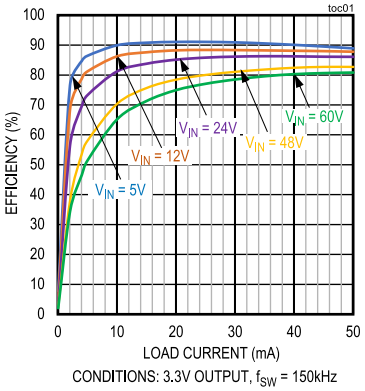
Note 2: All the Electrical Specifications are 100% production tested at T_A = +25°C. Specifications over the operating temperature range are guaranteed by design and characterization.

Note 3: No load current is measured in the application circuits. For MAX17553C, the output voltage is programmed to 3.3V.

Typical Operating Characteristics

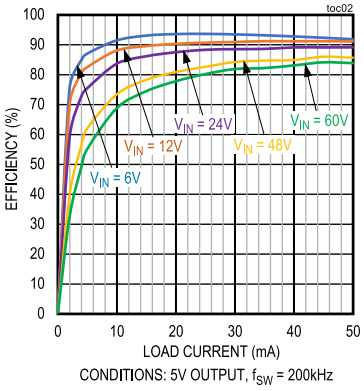
(V_{IN} = $V_{EN/UV}$ = 24V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted. All voltages are referenced to GND, unless otherwise noted.)

MAX17553A, EFFICIENCY vs. LOAD CURRENT
FIGURE 3 CIRCUIT



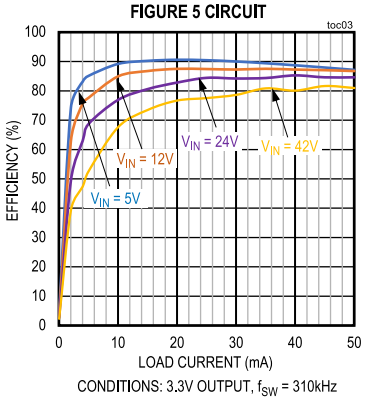
CONDITIONS: 3.3V OUTPUT, f_{SW} = 150kHz

MAX17553B, EFFICIENCY vs. LOAD CURRENT
FIGURE 4 CIRCUIT



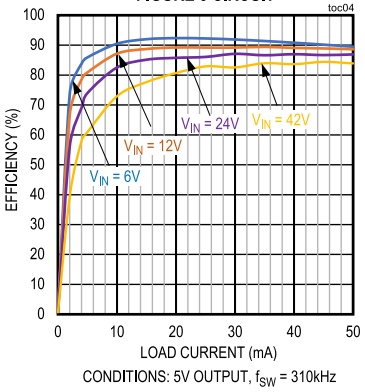
CONDITIONS: 5V OUTPUT, f_{SW} = 200kHz

MAX17553A, EFFICIENCY vs. LOAD CURRENT
FIGURE 5 CIRCUIT



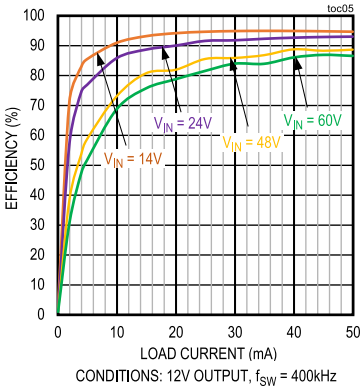
CONDITIONS: 3.3V OUTPUT, f_{SW} = 310kHz

MAX17553B, EFFICIENCY vs. LOAD CURRENT
FIGURE 6 CIRCUIT



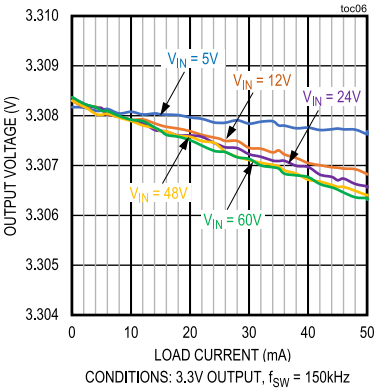
CONDITIONS: 5V OUTPUT, f_{SW} = 310kHz

MAX17553C, EFFICIENCY vs. LOAD CURRENT
FIGURE 7 CIRCUIT



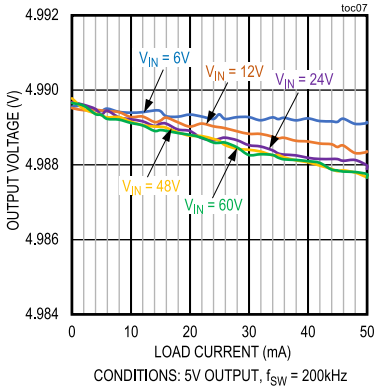
CONDITIONS: 12V OUTPUT, f_{SW} = 400kHz

MAX17553A, OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 3 CIRCUIT



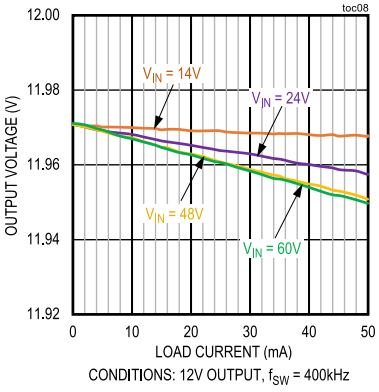
CONDITIONS: 3.3V OUTPUT, f_{SW} = 150kHz

MAX17553B, OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 4 CIRCUIT



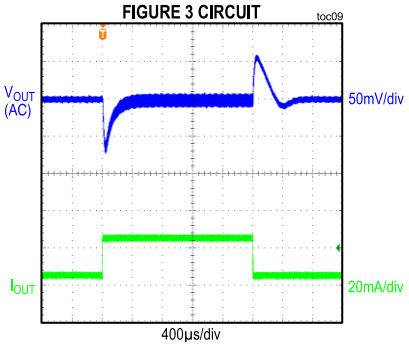
CONDITIONS: 5V OUTPUT, f_{SW} = 200kHz

MAX17553C, OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 7 CIRCUIT



CONDITIONS: 12V OUTPUT, f_{SW} = 400kHz

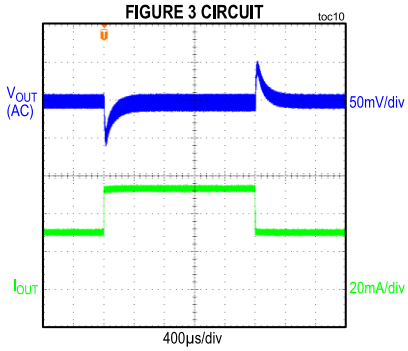
MAX17553A
LOAD TRANSIENT BETWEEN 5mA AND 25mA
FIGURE 3 CIRCUIT



CONDITIONS: 3.3V OUTPUT, f_{SW} = 150kHz

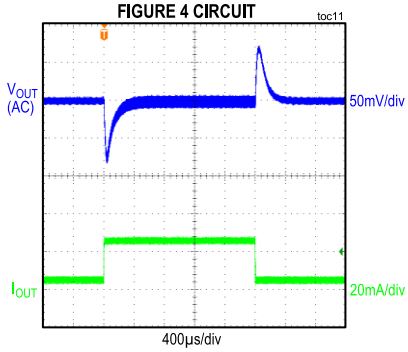
(V_{IN} = $V_{EN/UV}$ = 24V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted. All voltages are referenced to GND, unless otherwise noted.)

MAX17553A
LOAD TRANSIENT BETWEEN 25mA AND 50mA
FIGURE 3 CIRCUIT



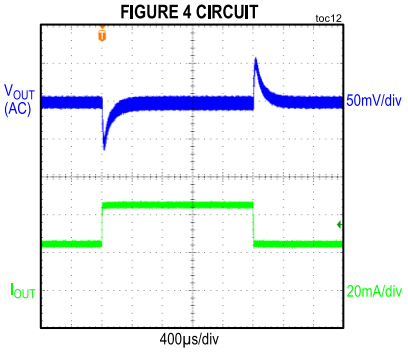
CONDITIONS: 3.3V OUTPUT, f_{SW} = 150kHz

MAX17553B
LOAD TRANSIENT BETWEEN 5mA AND 25mA
FIGURE 4 CIRCUIT



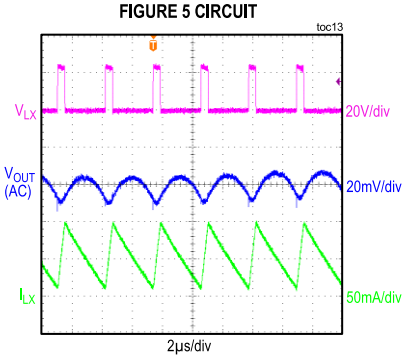
CONDITIONS: 5V OUTPUT, f_{SW} = 200kHz

MAX17553B
LOAD TRANSIENT BETWEEN 25mA AND 50mA
FIGURE 4 CIRCUIT



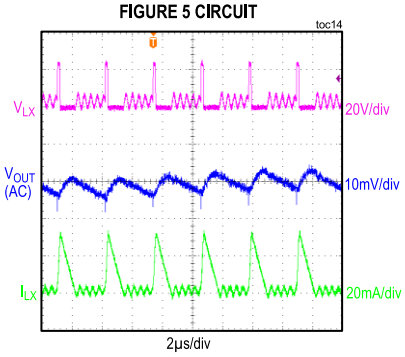
CONDITIONS: 5V OUTPUT, f_{SW} = 200kHz

MAX17553A, STEADY STATE PERFORMANCE
FIGURE 5 CIRCUIT



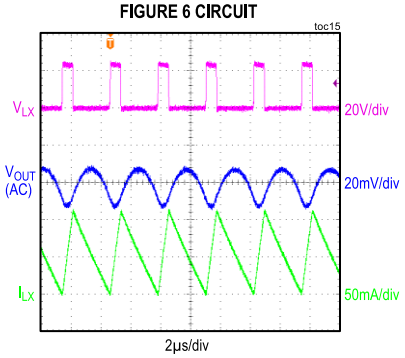
CONDITIONS: 3.3V OUTPUT, 50mA LOAD, f_{SW} = 310kHz

MAX17553A, STEADY STATE PERFORMANCE
FIGURE 5 CIRCUIT



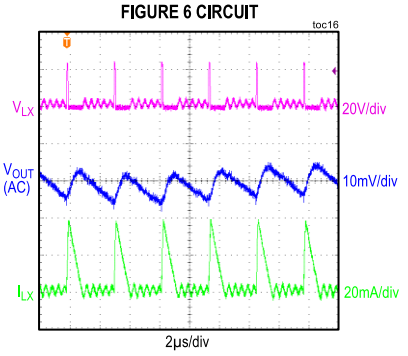
CONDITIONS: 3.3V OUTPUT, 5mA LOAD, f_{SW} = 310kHz

MAX17553B, STEADY STATE PERFORMANCE
FIGURE 6 CIRCUIT



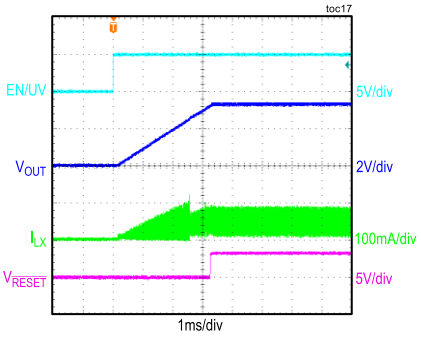
CONDITIONS: 5V OUTPUT, 50mA LOAD, f_{SW} = 310kHz

MAX17553B, STEADY STATE PERFORMANCE
FIGURE 6 CIRCUIT



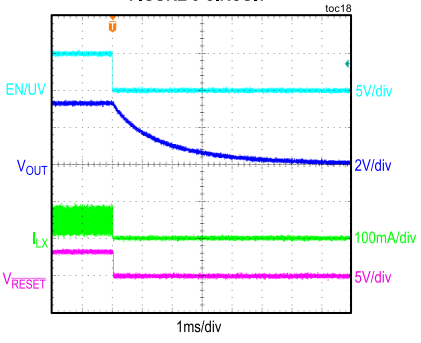
CONDITIONS: 5V OUTPUT, 5mA LOAD, f_{SW} = 310kHz

MAX17553A, SOFT-START THROUGH EN/UV
FIGURE 5 CIRCUIT



CONDITIONS: 3.3V OUTPUT, 66Ω LOAD, f_{SW} = 310kHz

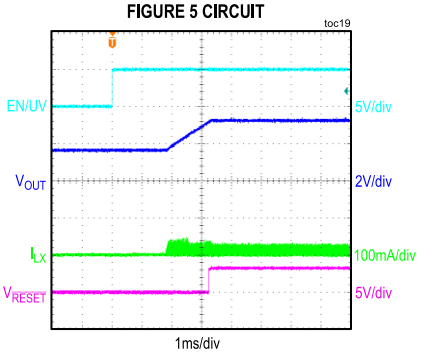
MAX17553A, SHUT DOWN THROUGH EN/UV
FIGURE 5 CIRCUIT



CONDITIONS: 3.3V OUTPUT, 66Ω LOAD, f_{SW} = 310kHz

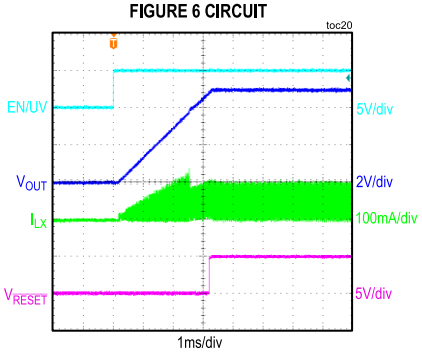
(V_{IN} = $V_{EN/UV}$ = 24V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted. All voltages are referenced to GND, unless otherwise noted.)

MAX17553A
SOFT-START WITH PREBIAS VOLTAGE OF 1.65V
FIGURE 5 CIRCUIT



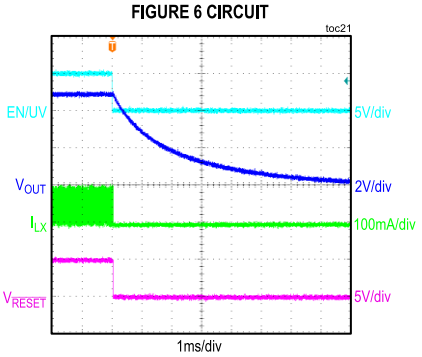
CONDITIONS: 3.3V OUTPUT, 660Ω LOAD, f_{SW} = 310kHz

MAX17553B, SOFT-START THROUGH EN/UV
FIGURE 6 CIRCUIT



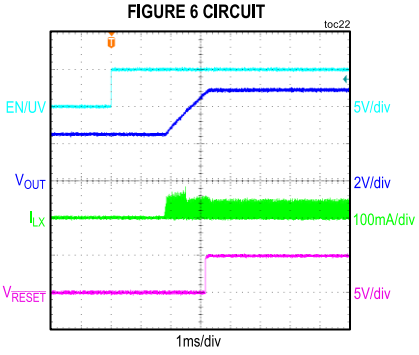
CONDITIONS: 5V OUTPUT, 100Ω LOAD, f_{SW} = 310kHz

MAX17553B, SHUT DOWN THROUGH EN/UV
FIGURE 6 CIRCUIT



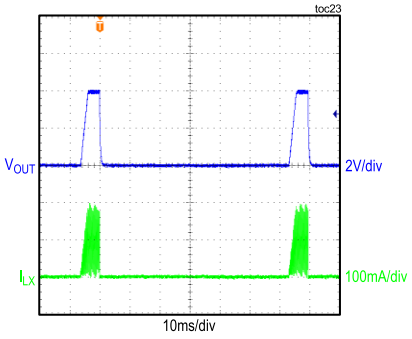
CONDITIONS: 5V OUTPUT, 100Ω LOAD, f_{SW} = 310kHz

MAX17553B
SOFT-START WITH PREBIAS VOLTAGE OF 2.5V
FIGURE 6 CIRCUIT



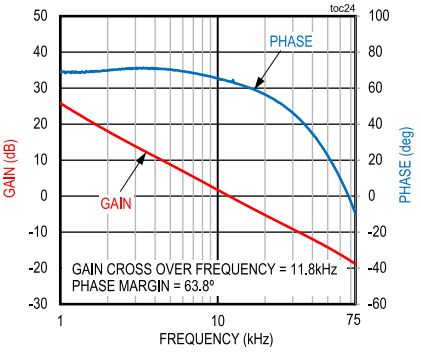
CONDITIONS: 5V OUTPUT, 1kΩ LOAD, f_{SW} = 310kHz

MAX17553B, OVERLOAD PROTECTION
FIGURE 6 CIRCUIT



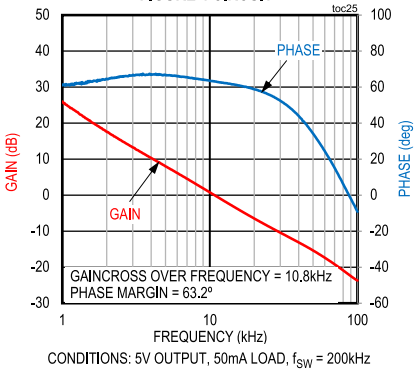
CONDITIONS: 5V OUTPUT, 38Ω LOAD, f_{SW} = 310kHz

MAX17553A, BODE PLOT
FIGURE 3 CIRCUIT



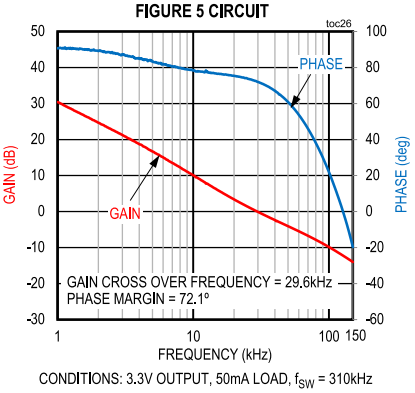
CONDITIONS: 3.3V OUTPUT, 50mA LOAD, f_{SW} = 150kHz

MAX17553B, BODE PLOT
FIGURE 4 CIRCUIT



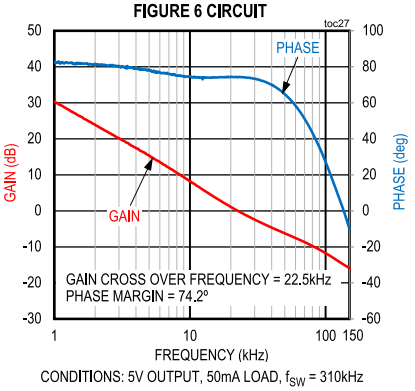
CONDITIONS: 5V OUTPUT, 50mA LOAD, f_{SW} = 200kHz

MAX17553A, BODE PLOT
FIGURE 5 CIRCUIT



CONDITIONS: 3.3V OUTPUT, 50mA LOAD, f_{SW} = 310kHz

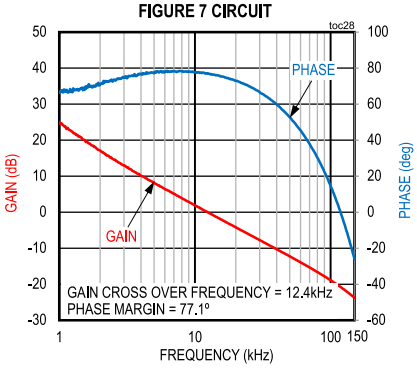
MAX17553B, BODE PLOT
FIGURE 6 CIRCUIT



CONDITIONS: 5V OUTPUT, 50mA LOAD, f_{SW} = 310kHz

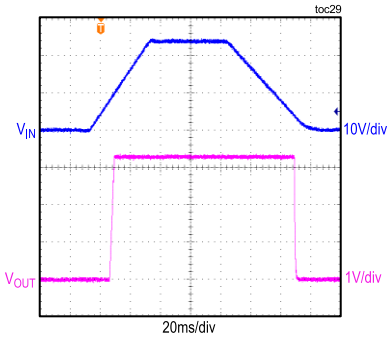
(V_{IN} = $V_{EN/UV}$ = 24V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted. All voltages are referenced to GND, unless otherwise noted.)

MAX17553C, BODE PLOT
FIGURE 7 CIRCUIT



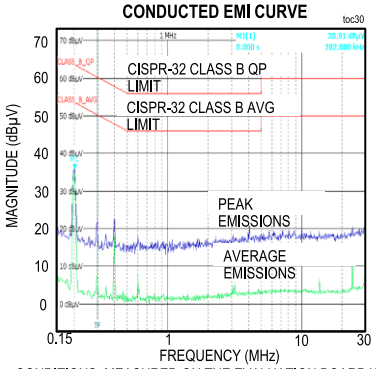
CONDITIONS: 12V OUTPUT, 50mA LOAD, f_{SW} = 400kHz

MAX17553A
TURN-ON/TURN-OFF WITH EN/UV AND HYST



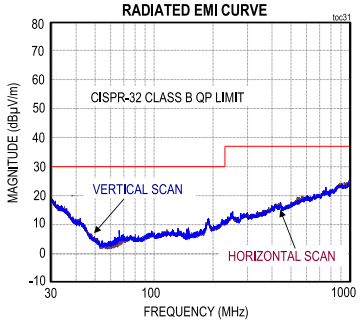
CONDITIONS: 3.3V OUTPUT, 66Ω LOAD, f_{SW} = 310kHz
TURN-ON VOLTAGE = 8V, TURN-OFF VOLTAGE = 4V

MAX17553B, 5V OUTPUT, 50mA LOAD CURRENT
CONDUCTED EMI CURVE



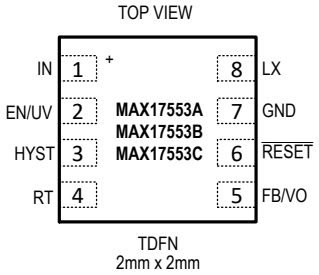
CONDITIONS: MEASURED ON THE EVALUATION BOARD WITH
L2 = 15µH, C2 = 4.7µF/100V/X7R/1206

MAX17553B, 5V OUTPUT, 50mA LOAD CURRENT
RADIATED EMI CURVE



CONDITIONS: MEASURED ON THE EVALUATION BOARD

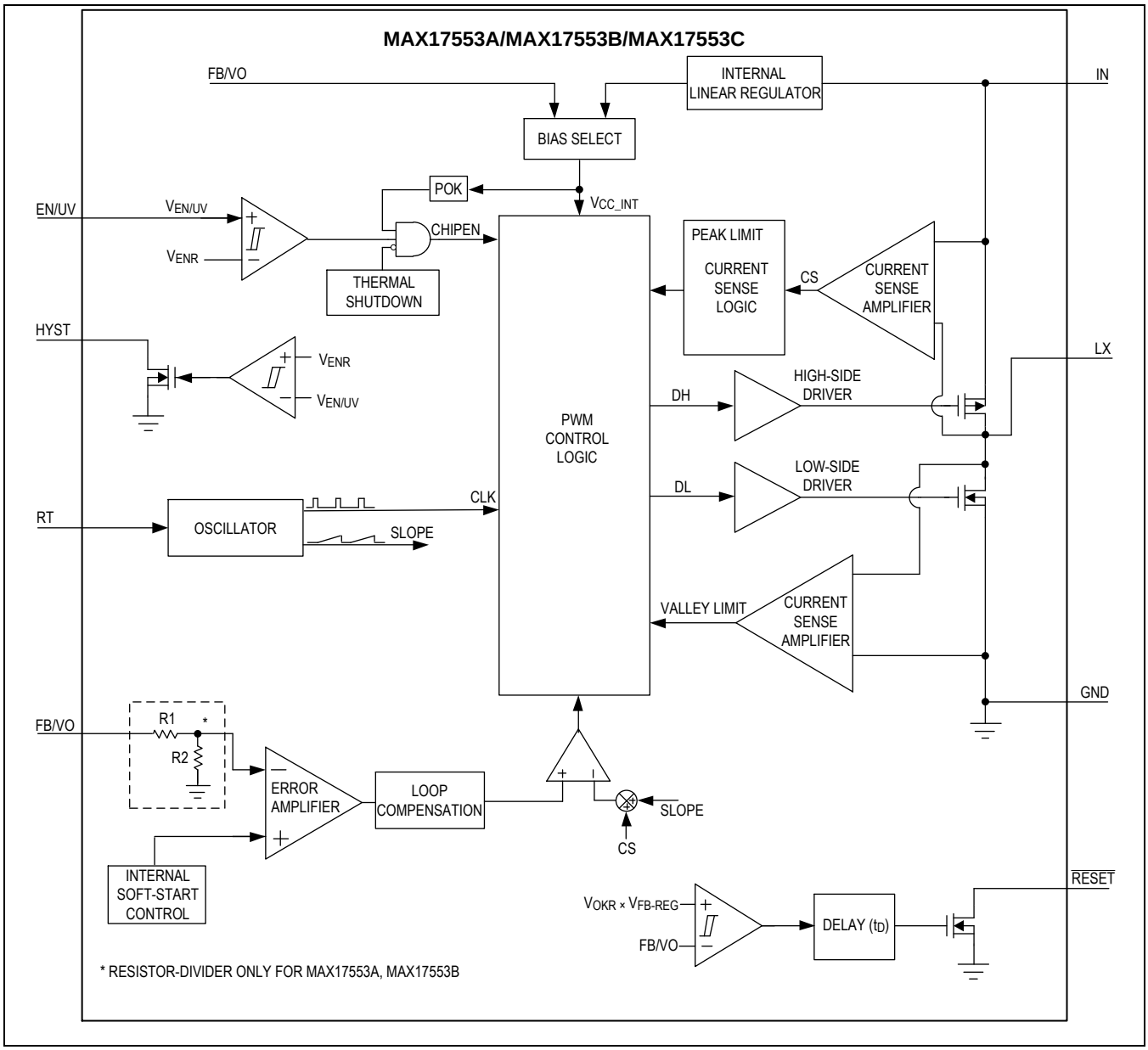
Pin Configuration



Pin Descriptions

PIN	NAME	FUNCTION
1	IN	Power Supply Input Pin. Decouple to GND with a 1µF capacitor. Place the capacitor close to IN and GND pins.
2	EN/UV	Enable/Undervoltage Lockout Pin. Drive EN/UV high to enable the output voltage. Connect to the midpoint of a resistor divider from IN to GND to set the input voltage at which the device turns ON. The allowed minimum turn off input voltage is 3.85V. Pull low to GND to disable the device.
3	HYST	Converter Turn ON/OFF Hysteresis Programming Pin. Connect HYST to EN/UV with an external resistor to set the required hysteresis. HYST goes high impedance when EN/UV > 1.215V (typ) and pulls low when EN/UV < 1.09V (typ).
4	RT	Programmable Switching Frequency Input. Connect a resistor from RT to GND to program oscillator frequency between 150kHz and 1.5MHz. Leave the RT pin unconnected for a default 310kHz switching frequency. See the *Switching Frequency* section for more details.
5	FB/VO	Feedback Input. For fixed output voltage parts (MAX17553A and MAX17553B), connect the output voltage node (V_{OUT}) to FB/VO pin for both feedback and boot-strap function. Connect FB/VO to the center node of an external resistor-divider from the output to GND to set the output voltage for MAX17553C. See the *Adjusting the Output Voltage* section for more details.
6	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB/VO drops below 92% (typ) of its set value. $\overline{\text{RESET}}$ goes high impedance 30µs after FB/VO rises above 95% (typ) of its set value. See *Electrical Characteristics* section for more details.
7	GND	Ground. Connect GND to the power ground plane. Connect all the circuit ground connections together at a single point. See the *PCB Layout Guidelines* section.
8	LX	Switching Node Pin. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown mode.

Functional Block Diagram



Detailed Description

The MAX17553 is an ultra-small, high-efficiency, high voltage, synchronous step-down DC-DC converter with integrated MOSFETs that operates over a wide input voltage range from 4V to 60V and delivers up to 50mA of load current. The MAX17553 is available in three variants: MAX17553A, MAX17553B, and MAX17553C. MAX17553A and MAX17553B are fixed 3.3V and 5V output voltage devices, respectively. MAX17553C is an adjustable output (0.8V to 0.9 x V_{IN}) device. The feedback-voltage regulation accuracy of the converters over the -40°C to +125°C temperature range is ±1.5% for MAX17553A and MAX17553B, and ±1.25% for MAX17553C.

The device features a peak-current-mode control architecture. During normal operation, at each rising edge of the clock, the high-side p-MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side p-MOSFET on-time, the inductor current ramps up. During the rest of the switching cycle or until the inductor current reaches zero, the high-side p-MOSFET remains off and the low-side n-MOSFET remains on, and the inductor current ramps down. The device features the Discontinuous Conduction Mode (DCM), in which the negative inductor current is inhibited to enable higher light load efficiency. In DCM, the device operates at a fixed switching frequency until the minimum on-time is reached. If the load demand is less than the energy corresponding to the minimum on-time pulse, the converter skips pulses to maintain output voltage regulation.

A fixed soft-start time of 3.2ms (typ) allows users to reduce input inrush current. An open-drain $\overline{\text{RESET}}$ feature provides a power-good signal to the system upon achieving successful regulation of the output voltage.

Enable/Undervoltage Input with HYST

The device features an enable/undervoltage lockout (EN/UV) and a hysteresis (HYST) pin that allows the user to turn the device on or off at the desired input-voltage level. EN/UV can also be used to enable/disable the converter. Driving EN/UV low (below V_{ENF}) disables both power MOSFETs (as well as other internal circuitry) and reduces IN quiescent current to below 3.8µA (typ). Driving EN/UV high (above V_{ENR}) enables the converter. An external voltage-divider between IN and EN/UV to GND and an external resistor from HYST to EN/UV adjusts the input voltage at which the device turns on or turns off. See the *Setting the Input Undervoltage Level with Hysteresis* section for more details.

When EN/UV voltage is above 1.215V (typ), the device's internal error-amplifier reference voltage starts to ramp up after an internal delay of 170µs (typ). The duration of the soft-start ramp is 3.2ms (typ), allowing for a smooth increase of the output voltage.

The device supports prebiased startup. When the device starts into a prebiased output, both the high-side and the low-side MOSFETs are turned off so that the converter does not sink current from the output. High-side and low-side MOSFETs do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Reset Output

The device includes an open-drain $\overline{\text{RESET}}$ output to monitor the output voltage. $\overline{\text{RESET}}$ goes to high impedance 30µs (typ) after the regulator output voltage increase above 95% (typ) of the nominal set voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops below 92% (typ) of the nominal set voltage. $\overline{\text{RESET}}$ also goes low when EN/UV is pulled low, and during hiccup time out period.

Switching Frequency

The switching frequency (RT) of the device can be programmed from 150kHz to 1.5MHz by using a resistor connected from RT to GND. The switching frequency (f_{SW}) is related to the resistor (R_{RT}) connected at the RT pin by the following equation:

$$R_{RT} = \frac{500}{\left(\frac{11.6}{t_{SW} - 0.045}\right) - 0.5}$$

$$t_{SW} = \frac{1}{f_{SW}}$$

Where R_{RT} is in kΩ and t_{SW} is in µs. Leave the RT pin unconnected for the default 310kHz (typ) switching frequency. The value of R_{RT} in the range of 165kΩ (308kHz) and 248kΩ (215kHz) is not allowed for user programming to ensure proper configuration of the internal adaptive-loop compensation scheme.

Operating Input Voltage Range

The minimum operating input voltage is determined by the minimum off-time and circuit voltage drops. The minimum operating input voltage for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS\text{-}ONL(MAX)}\right)}{1 - f_{SW(MAX)} \times t_{OFF\_MIN(MAX)}} + I_{OUT(MAX)} \times \left(R_{DS\text{-}ONH(MAX)} - R_{DS\text{-}ONL(MAX)}\right)$$

where

V_{OUT} = Steady-state output voltage in V

$I_{OUT(MAX)}$ = Maximum load current in A

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor in Ω

$f_{SW(MAX)}$ = Maximum switching frequency in Hz

$t_{OFF\_MIN(MAX)}$ = Worst case minimum switch off-time (95ns)

$R_{DS\text{-}ONL(MAX)}$ and $R_{DS\text{-}ONH(MAX)}$ = Worst-case on-state resistances of low-side and high-side MOSFETs respectively in Ω

Overcurrent Protection

The device implements a hysteretic peak current limit protection scheme to protect the internal MOSFETs and inductor under output short circuit conditions. When the inductor peak current exceeds $I_{PEAK\text{-}LIMIT}$ (0.18A typ), the high-side MOSFET is turned off and the low-side MOSFET is turned on to reduce the inductor current. After the current is reduced to $I_{VALLEY\text{-}LIMIT}$ (0.11A typ during startup and 0.022A typ during steady state), the high-side MOSFET is turned on at the rising edge of the next clock pulse. Since the inductor current is bounded between the two values, the inductor current runaway doesn't happen in this scheme. The device enters hiccup mode if the inductor current hits $I_{PEAK\text{-}LIMIT}$ for 16 consecutive times. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 64ms (typ). Once the hiccup timeout period expires, soft-start is attempted again. Hiccup mode of operation ensures low power dissipation under output short-circuit condition.

Thermal-Shutdown Protection

Thermal shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds +160°C (typ), a thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C (typ). Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown protection in normal operation.

Applications Information

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The required minimum inductance for a given application can be determined from the following equation:

$$L \geq \frac{6.8 \times V_{OUT}}{f_{SW}}$$

where L is inductance in H, V_{OUT} is output voltage and f_{SW} is the switching frequency in Hz. Select a low-loss inductor closest to the calculated value with acceptable dimensions. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit, $I_{PEAK-LIMIT}$ (180mA typ).

Since the MAX17553 operates in DCM, the device switches at a fixed frequency until the minimum on-time (t_{ON_MIN}) is reached. If the load demand is less than the energy corresponding to the minimum on-time pulse, the converter skips switching pulses to maintain the output voltage regulation. For the selected inductor (L_{SEL}), use the following formula to calculate the minimum load current required to operate at a fixed switching frequency:

$$I_{OUT\_MIN} = \frac{0.5 \times (V_{IN} - V_{OUT}) \times V_{IN} \times t^2_{ON\_MIN} \times f_{SW}}{V_{OUT} \times L_{SEL}}$$

where:

V_{IN} = Operating input voltage in V

t_{ON_MIN} = Minimum on-time in s

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces switching noise and voltage ripple on the input. Use low-ESR ceramic capacitors with high ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Decouple IN to GND with a minimum of 1µF/1206 package or equivalent capacitor. Calculate the input capacitance using the following equation based on the input ripple requirement:

$$C_{IN} = \frac{I_{OUT(MAX)} \times \left(\frac{V_{OUT}}{V_{IN}}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

V_{IN} = Input voltage in V

V_{OUT} = Steady-state output voltage in V

$I_{OUT(MAX)}$ = Maximum load current in A

f_{SW} = Switching frequency in Hz

ΔV_{IN} = Allowable input voltage ripple in V

η = Efficiency

In applications where the source is far from the device input, an appropriate electrolytic capacitor should be added to provide necessary damping for potential oscillations caused by the inductance of the input power path and input ceramic capacitor.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. It should be noted that dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels and should be appropriately derated to ensure the required output capacitance is obtained in the application. The output capacitor has two functions. It stores sufficient energy to support the output voltage under load transient conditions and stabilizes the device's internal control loop. The minimum required output capacitance is as follows:

FREQUENCY RANGE (KHZ)	MINIMUM OUTPUT CAPACITANCE (µF)
150 to 215	$25/V_{OUT}$
308 to 1500	$12/V_{OUT}$

Setting the Input Undervoltage Level with Hysteresis

The device offers an adjustable input undervoltage and adjustable hysteresis levels. Set the voltage at which the device turns on/off with a resistive voltage-divider connected from IN to GND and a resistor from HYST to EN/UV (see *Figure 1*). Connect the center node of the resistive voltage-divider to EN/ UV pin. Choose R1 to be 3.32MΩ (max) and then calculate R2 and R3 as follows:

$$R2=\frac{V_{ENF}\times R1}{(V_{IN(OFF)}-V_{ENF})}$$

$$R3=\frac{V_{ENR}\times R1\times R2}{\left(V_{IN(ON)}\times R2-V_{ENR}\times (R1+R2)\right)}$$

where $V_{IN(ON)}$ and $V_{IN(OFF)}$ are the voltages at which the device is required to turn on and turn off respectively. While selecting the above resistors, the HYST pin sink current capability given in *Electrical Characteristics* should be considered.

When the HYST function is not used, connect the HYST pin to GND (see *Figure 1*) and calculate R2 as follows:

$$R2=\frac{V_{ENR}\times R1}{(V_{IN(ON)}-V_{ENR})}$$

If the EN/UV pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the signal source output and the EN/UV pin to reduce voltage ringing on the line.

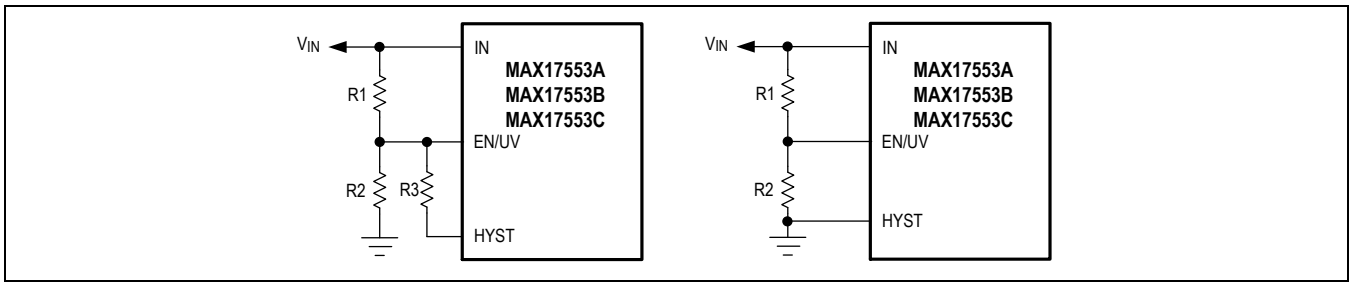


Figure 1. Setting the Input Undervoltage Level With and Without Hysteresis

Adjusting the Output Voltage

For MAX17553A and MAX17553B, connect FB/VO directly to the output node of the step-down converter. The output voltage of MAX17553C can be programmed from 0.8V to 0.9 x V_{IN}. Set the output voltage by using a resistive feedback divider from output to GND (see *Figure 2*). Connect the center node of the divider to the FB pin. Choose R_B less than or equal to 100kΩ and calculate R_U with the following equation:

$$R_U=R_B\times\left[\frac{V_{OUT}}{0.8}-1\right]$$

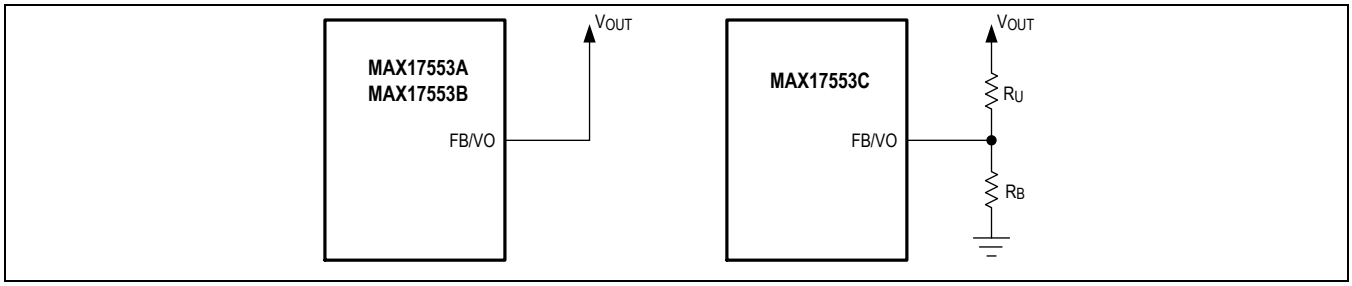


Figure 2. Setting the Output Voltage

Power Dissipation

At any particular operating condition, the power loss that contributes to temperature rise of the device is estimated as follows:

$$P_{LOSS} = P_{OUT} \times \left(\frac{1}{\eta} - 1\right) - \left(I_{OUT}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where:

P_{OUT} = Output power,

η = Efficiency of the converter,

R_{DCR} = DC resistance of the inductor.

See *Typical Operating Characteristics* for more information on efficiency at typical operating conditions. The Theta-JA (θ_{JA}) of the package is given as follows:

$$\theta_{JA} = 162°C/W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + \left(\theta_{JA} \times P_{LOSS}\right)$$

Junction Temperature greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current-carrying loop is proportional to the area enclosed by the loop, inductance is reduced if the loop area is very small. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the IN pins of the IC. This eliminates as many trace inductance effects as possible and gives the IC a cleaner voltage supply.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity. PCB layout also affects the thermal performance of the design. For a sample layout that ensures first pass success, refer to the MAX17553 evaluation kit layout available at *www.maximintegrated.com*.

Typical Application Circuits

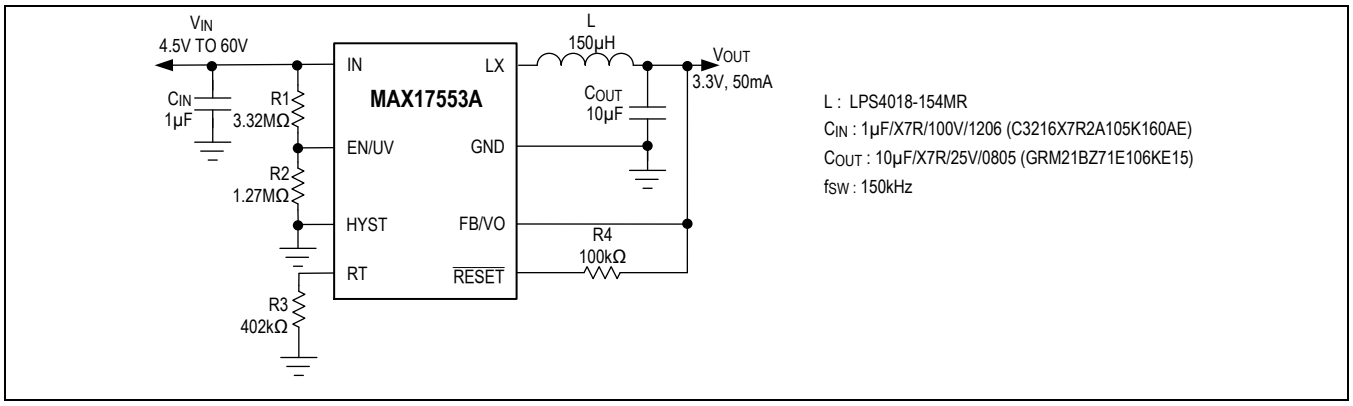


Figure 3. High-Efficiency 3.3V, 50mA Regulator

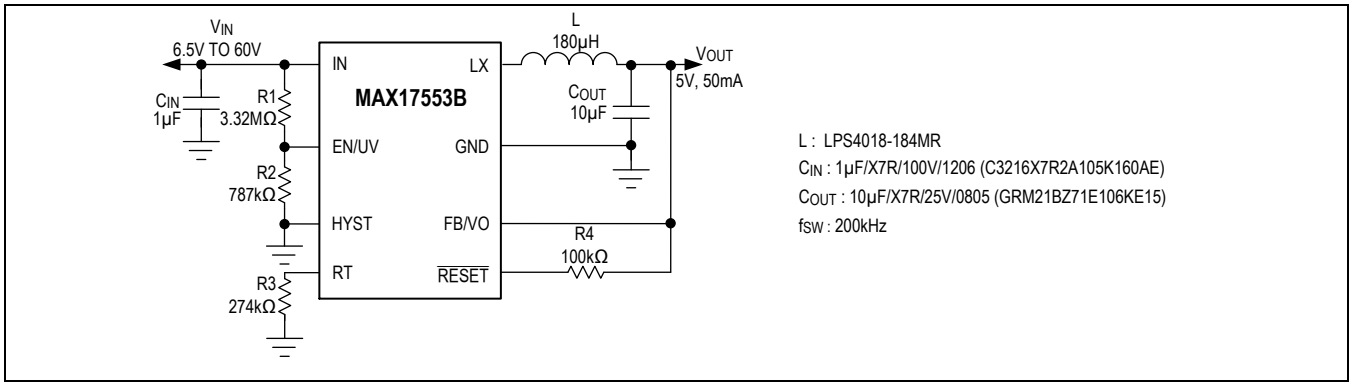


Figure 4. High-Efficiency 5V, 50mA Regulator

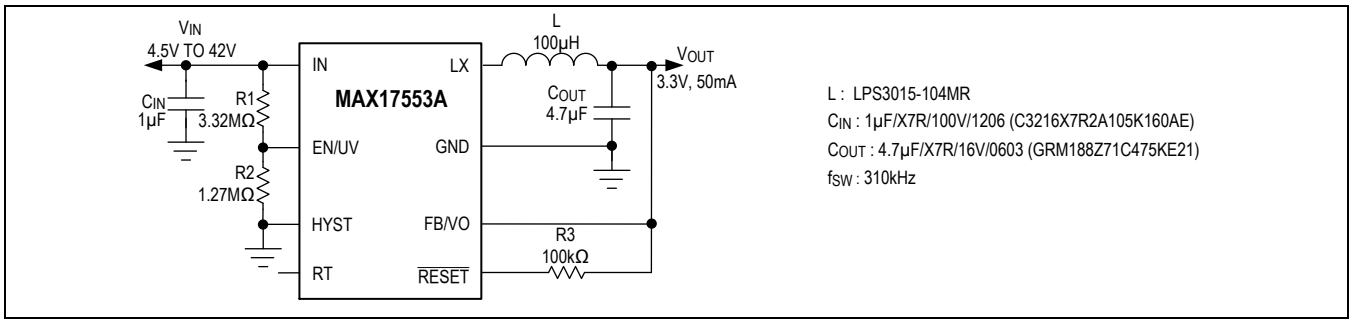


Figure 5. Small-Footprint 3.3V, 50mA Regulator

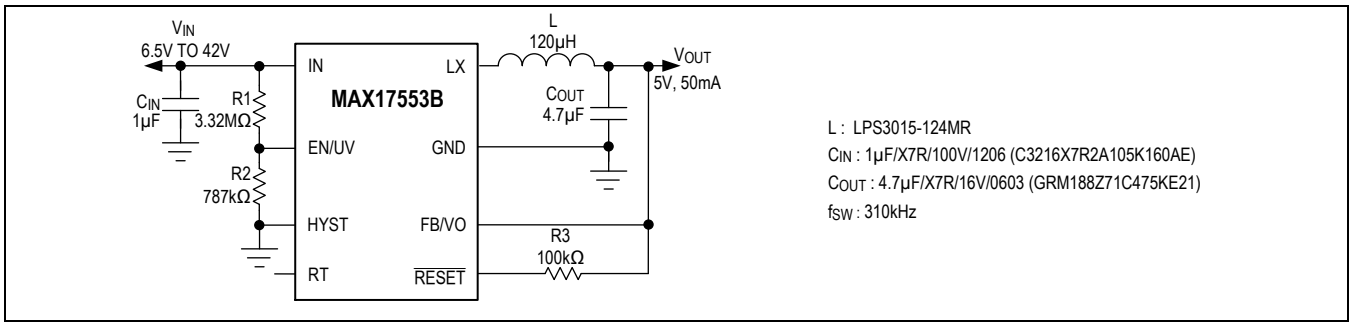


Figure 6. Small-Footprint 5V, 50mA Regulator

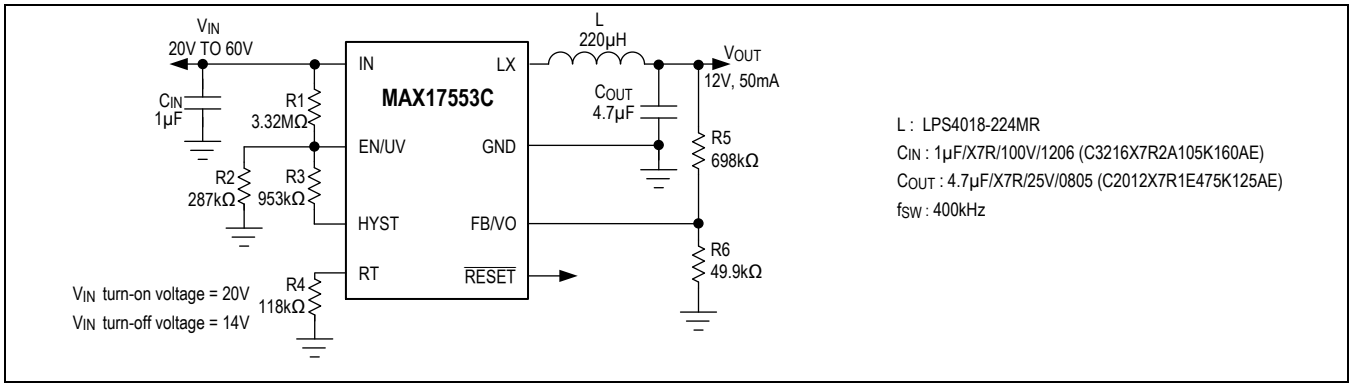


Figure 7. 12V, 50mA Regulator

Ordering Information

PART NUMBER	OUTPUT VOLTAGE	PIN-PACKAGE
MAX17553AATA+	3.3	8-TDFN
MAX17553AATA+T	3.3	8-TDFN
MAX17553BATA+	5	8-TDFN
MAX17553BATA+T	5	8-TDFN
MAX17553CATA+	Adjustable	8-TDFN
MAX17553CATA+T	Adjustable	8-TDFN

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/22	Release for Market Intro	—
1	4/22	Updated Electrical Characteristics table	3, 4

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.