19-5942; Rev 0; 7/11

MAX19192 Evaluation Kit

Evaluates: MAX19192

General Description

The MAX19192 evaluation kit (EV kit) is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX19192 dual, 8-bit analog-to-digital converter (ADC). The ADC accepts AC- or DC-coupled, differential, or single-ended analog inputs. The digital output produced by the ADC can be easily captured with a user-supplied high-speed logic analyzer. The EV kit operates from a 3.3V to 6V supply and utilizes four LDO regulators to power the analog and digital power rails. The EV kit includes circuitry that generates a clock signal from an AC sine-wave signal provided by the user.

Features

- **Up to 10Msps Sampling Rate**
- **Dual-Channel ADC**
- **Ultra-Low-Power Operation**
- **Single 3.3V to 6V Power-Supply Operation**
- **Single-Ended or Fully Differential Input-Signal Configuration**
- **AC- or DC-Coupled Input-Signal Configuration**
- **Configurable Reference Voltage**
- **On-Board Clock-Shaping Circuit**
- **Proven PCB Layout**
- **Fully Assembled and Tested**

Ordering Information

PART	TYPE
MAX19192EVKIT#	EV Kit

#Denotes RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C6, C9, C19, C21–C26, C35, C37, C39, C41, C48	19	0.1µF ±10%, 16V X7R ceramic capacitors (0603) TDK C1608X7R1C104K
C7, C12, C14, C20	4	1000pF ±10%, 50V X7R ceramic capacitors (0603) TDK C1608X7R1H102K
C8, C13, C15	3	0.33µF ±10%, 6.3V X5R ceramic capacitors (0603) TDK C1608X5R0J334K
C10, C11, C16, C17	4	22pF ±5%, 50V C0G ceramic capacitors (0603) TDK C1608C0G1H220J
C18, C28, C30, C32, C34, C36, C38, C40, C42	9	2.2µF ±10%, 10V tantalum capacitors (A case) AVX TAJA225K010R
C27, C29, C31, C33, C43–C46	8	1µF ±10%, 50V X7R ceramic capacitors (0603) TDK C1608X7R1C105K
C47	1	10µF ±10%, 10V tantalum capacitor (A case) AVX TAJB106M010R
C49, C50	2	0.01µF ±10%, 16V X5R ceramic capacitors (0402) TDK C1005X5R1A103K
CLKIN, D/E_INA, D/E_INB, S/E_INA+, S/E_INA-, S/E_INB+, S/E_INB-	7	SMA PC-mount connectors
J1	1	20-pin (2 x 10) header
J2	1	128-pin high-speed connector Samtec QSH-060-01-L-DA
JU1–JU4, JU7, JU8, JU11	7	3-pin headers
JU5, JU6, JU9, JU10, JU12–JU15	8	2-pin headers
L1–L4	4	600Ω, 350mA ferrite beads Fair-Rite 2512066017Y0
R1–R4, R18	5	49.9Ω ±1% resistors (0603)
R5, R6, R31–R40, R41–R44	0	Not installed, resistors (0603) R5, R6, R41–R44 are open; R31–R40 are short (PC trace)

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Component List (continued)

DESIGNATION	QTY	DESCRIPTION
R7–R10, R17	5	2kΩ ±1% resistors (0603)
R11, R12, R13, R14	4	24.9Ω ±1% resistors (0603)
R15, R20	2	4.02kΩ ±1% resistors (0603)
R16	1	5kΩ, 12-turn potentiometer Murata PV37Y502C31A00
R19	1	6.04kΩ ±1% resistor (0603)
R21–R30	10	100Ω ±1% resistors (0603)
R45, R46	0	Not installed, resistors—short (PC trace) (0402)
T1, T2	2	RF transformers Mini-Circuits TT1-6-KK81
U1	1	Dual 10Msps 8-Bit ADC (28 QFN-EP) Maxim MAX9192ETI+

DESIGNATION	QTY	DESCRIPTION
U2	1	Dual CMOS differential line receiver (8 SO) Maxim MAX9113ESA+
U3	1	Buffer/driver, three-state output (48 TSSOP) Texas Instruments SN74ALVCH16244DGG
U4, U5	2	3V LDO regulators (5 SC70) Maxim MAX8510EXK30+ (Top Mark: AAS)
U6, U7	2	1.8V LDO regulators (5 SC70) Maxim MAX8891EXK18+ (Top Mark: ATJ)
—	15	Shunts (JU1–JU15)
—	1	PCB: MAX19192 EVALUATION KIT

Component Suppliers

SUPPLIER	PHONE	WEBSITE
AVX Corporation	843-946-0238	www.avx.com
Fair-Rite Products Corp.	845-895-2055	www.fair-rite.com
Mini-Circuits	718-934-4500	www.minicircuits.com
Murata Electronics North America Inc.	847-803-6100	www.murata-northamerica.com
TDK Corp.	847-803-6100	www.component.tdk.com
Texas Instruments Inc.	972-644-5580	www.ti.com

Note: *Indicate that you are using the MAX19192 when contacting these component suppliers.*

Quick Start

Required Equipment

- MAX19192 EV kit
- 3.3V to 6V, 300mA DC power supplies
- Function generator with low-phase noise and low jitter for clock input (e.g., HP 8644B)
- Two function generators for analog signal inputs (e.g., HP 8644B)
- Logic analyzer (e.g., HP 16500C)
- Analog anti-aliasing filters
- Digital voltmeter

Procedure

The EV kit is a fully assembled and tested surface-mount board. Follow the steps below for board operation. **Caution: Do not turn on the power supply or enable function generators until all connections are completed.**

1) Verify that shunts are installed on pins 2-3 on jumpers JU7 and JU8 (fully operational, outputs enabled).
2) Verify that no shunts are installed on jumpers JU9 and JU10.
3) Verify that a shunt is installed on pins 1-2 on jumper JU11 (internal reference mode).

4) Connect the logic analyzer to header J1. Both channel A and channel B data signals are multiplexed on header J1. Control signal A/$\overline{B}$ on pin J1-11 indicates whether data is from channel A (high) or from channel B (low).
5) Verify that shunts are installed on jumpers JU12–JU15 (on-board LDOs enabled).
6) Connect the 3.3V power supply to the VIN pad. Connect the ground terminal of this supply to the OGND PCB pad.
7) Enable the power supply.
8) With a voltmeter, verify that 1.24V is measured across test point TP1 and GND. If the voltage is not 1.24V, adjust potentiometer R16 until 1.24V is obtained.
9) Connect the clock function generator to the CLKIN SMA connector.
10) Connect the output of the analog signal function generator to the input of the suggested anti-aliasing filters.
    a) To evaluate **differential AC-coupled** analog signals, verify that shunts are installed on pins 2-3 on jumpers JU1–JU4. Connect the output of the analog anti-aliasing filter to the D/E_INA and D/E_INB SMA connectors.
    b) To evaluate **single-ended AC-coupled** analog signals, verify that shunts are installed on pins 1-2 on jumpers JU1–JU6. Verify that resistors R5 and R6 are open. Connect the output of the anti-aliasing filter to the S/E_INA+ and S/E_INB+ connectors
    c) To evaluate **single-ended DC-coupled** analog signals, verify that shunts are installed on pins 1-2 on jumpers JU2 and JU3, and no shunts are installed on jumpers JU1, JU4, JU5, and JU6. Remove capacitors C2 and C3 and resistors R2 and R3. Install 0Ω resistors at R5 and R6. Connect the outputs of the anti-aliasing filters to the S/E_INA± and S/E_INB± SMA connectors.
    d) To evaluate **differential DC-coupled** analog signals, verify that shunts are installed on pins 1-2 on jumpers JU2 and JU3, and no shunts installed on jumpers JU1, JU4, JU5, and JU6. Remove capacitors C2 and C3 and resistors R2 and R3. Install 0Ω resistors at R5 and R6. Connect the outputs of the anti-aliasing filters to the S/E_INA+/- and S/E_INB+/- SMA connectors.
11) Enable the function generators. Set the clock function generator for output amplitude of 2.4V_{P-P} (+11.6dBm) and a frequency (f_{CLK}) of ≤ 10MHz. Set the analog input-signal generators to the desired output-test signal amplitudes and frequencies. The clock and input signal function generators should be phase-locked to each other.
12) Channel A data is presented on the falling edge and channel B data is presented on the rising edge of the logic analyzer clock.
13) Enable the logic analyzer and begin collecting data.

_Detailed Description of Hardware

The MAX19192 EV kit is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX19192 dual, 8-bit ADC. The ADC provides digitized data of its two input channels in multiplexed fashion on a single 8-bit bus. The EV kit comes with the MAX19192ETI+ installed, which can be evaluated with a maximum clock frequency (f_{CLK}) of 10MHz. The ADC accepts differential or single-ended analog input signals. With the proper board configuration, the input signal can be AC- or DC-coupled.

The EV kit is based on a four-layer PCB design to optimize the performance of the ADC. Separate analog and digital power planes minimize noise coupling between analog and digital signals. The EV kit is configured with 3V and 1.8V power supplies applied to analog and digital power planes, respectively. However, the digital plane can be operated from 1.8V to 3.3V without compromising performance. See the *Power Supplies* section for additional information. The logic analyzer's threshold must be adjusted accordingly.

Access to the digital outputs is provided through header J1 for channels A and B. The 0.1in 20-pin header easily interfaces with a user-supplied logic analyzer (Samtec connector J2, which is located on the bottom side the EV kit board).

Power Supplies

The EV kit operates from a single 3.3V to 6V DC power supply applied at the VIN and OGND PCB pads. The EV kit requires separate analog and digital power supplies for best performance. VIN provides the power necessary for operating two 3V LDO regulators (U4, U5) and two 1.8V LDO regulators (U6, U7) used for on-board regulation of the analog and digital power rails. The EV kit also provides the option of using external power supplies to power the analog and digital power rails independently.

Regulator U4 (3V) powers the ADC VDD input and its corresponding analog circuitry. To power the ADC VDD input and the analog circuitry using regulator U4, install a shunt on jumper JU12. To power the ADC VDD input and analog circuitry using an external supply, remove the shunt on JU12 and apply a power source of 2.7V to 3.6V at the VDD_ADC and GND PCB pads. See Table 1 for proper JU12 configuration.

Regulator U5 (3V) powers the EV kit on-board clock-shaping circuit. To power the clock-shaping circuit using regulator U5, install a shunt on jumper JU13. To power the circuitry using an external supply, remove the shunt on JU13 and apply an external voltage of 2.7V to 3.6V at the VCC_CLOCK and GND PCB pads. When applying an external supply at the VCC_CLOCK and GND PCB pads, the minimum voltage should be equal to or less than the VDD_ADC voltage. See Table 2 for proper JU13 configuration.

Regulator U6 (1.8V) powers the ADC OVDD input and its corresponding digital circuitry. To power the ADC OVDD input and its corresponding digital circuitry, install a shunt on jumper JU14. To power the digital circuitry using an external supply, remove the shunt on JU14 and apply an external voltage of 1.8V to 3.6V at the OVDD_ADC and GND PCB pads. See Table 3 for proper JU14 configuration.

Regulator U7 (1.8V) powers the EV kit CMOS buffer/driver IC (U3). To power the buffer/driver IC, install a shunt on jumper JU15. To power the buffer/driver IC using an external supply, remove the shunt on JU15 and apply an external voltage of 1.8V to 3.6V at the VCC_BUFFER and OGND PCB pads. See Table 4 for proper JU15 configuration.

Table 1. VDD Input Power Configuration (JU12)

SHUNT POSITION	VDD_ADC INPUT SOURCE
Installed	3V LDO (U4) powers the ADC VDD input and analog circuitry.
Not installed	External supply applied at the VDD_ADC and GND PCB pads.

Table 2. Clock Circuitry Input Power Configuration (JU13)

SHUNT POSITION	VCC_CLOCK INPUT SOURCE
Installed	3V LDO (U5) powers the clock circuitry.
Not installed	External supply applied at the VCC_CLOCK and GND PCB pads.

Table 3. OVDD Input Power Configuration (JU14)

SHUNT POSITION	OVDD_ADC DIGITAL CIRCUITRY INPUT SOURCE
Installed	1.8V LDO (U6) output powers the ADC OVDD input.
Not installed	External supply applied at the OVDD_ADC and OGND PCB pads.

Table 4. VCC_BUFFER Circuitry Input Power Configuration (JU15)

SHUNT POSITION	VCC_BUFFER INPUT SOURCE
Installed	1.8V LDO (U7) output powers the buffer/driver IC.
Not installed	External supply applied at the VCC_BUFFER and OGND PCB pads to power the buffer/driver IC.

Clock

An on-board clock-shaping circuit generates a clock signal from an AC sine-wave signal applied to the CLKIN SMA connector. The input signal magnitude and frequency should not exceed 2.6V_{P-P} (+12.3dBm) and 10MHz, respectively. The frequency of the sinusoidal input signal determines the sampling frequency of the ADC. Differential line receiver U2 processes the input signal to generate the CMOS clock signal. The signal's duty cycle can be adjusted with potentiometer R16. A clock signal with a 50% duty cycle (recommended) can be achieved by adjusting R16 until 1.24V (40% of the analog power supply) is produced across test point TP1 and GND when the analog supply voltage is set to 3V. The clock signal is available at header pin J1-11, which can be used as a clock source for the logic analyzer. Additionally, header pin J1-11 (A/$\overline{B}$) is an image of the clock signal.

Input Signals

The ADC accepts differential or single-ended AC- or DC-coupled analog input signals. The EV kit accepts input signals with full-scale amplitude of less than 1.024V_{P-P} (+4dBm). See Table 5 for proper jumper configuration. **Note:** When a differential signal is applied to the ADC, the positive and negative input pins of the ADC each receive half of the input signal supplied at SMA connectors D/E_INA and D/E_INB with a DC offset voltage of VADUT/2.

Table 5. Single-Ended/Differential, AC-/DC-Coupled Jumper Configuration

JUMPER	SHUNT POSITION	PIN CONNECTION	EV KIT OPERATION
JU1	1-2	INA- pin connected to the COM pin through R11.	Analog input signal is applied to **channel A**. **Single-ended input, AC-coupled**. • R5 open (default)
JU2	1-2	INA+ pin AC-coupled to SMA connector S/E_INA+ through R12 and C2.	
JU5	Installed	INA+ pin assumes the DC offset at the REFP and REFN common.	
JU1	Not installed	Place DC offset of analog source at the S/E_INA- SMA connector.	Analog input signal is applied to **channel A**. **Single-ended input, DC-coupled**. • R5 shorted (0Ω) • Remove C2 • Remove R2
JU2	1-2	INA+ pin DC-coupled to SMA connector S/E_INA+ through R12 and R5.	
JU5	Not installed	INA+ pin assumes the DC offset from the analog input source.	
JU1	2-3	INA- pin connected to the low side of transformer T1 through R11.	Analog input signal is applied to **channel A**. **Differential input, AC-coupled**.
JU2	2-3	INA+ pin connected to the high side of transformer T1 through R12.	
JU1	Not installed	INA- pin DC-coupled to SMA connector S/E_INA- through R11.	Analog input signal is applied to **channel A**. **Differential input, DC-coupled**. • R5 shorted (0Ω) • Remove C2 • Remove R2
JU2	1-2	INA+ pin DC-coupled to SMA connector S/E_INA+ through R12 and R5.	
JU5	Not installed	INA+ pin assumes the DC offset from the analog input source.	

Table 5. Single-Ended/Differential, AC-/DC-Coupled Jumper Configuration (continued)

JUMPER	SHUNT POSITION	PIN CONNECTION	EV KIT OPERATION
JU3	1-2	INB- pin AC-coupled to SMA connector S/E_INB+ through R13 and C3.	Analog input signal is applied to **channel B**. **Single-ended input, AC-coupled**. R6 open (default)
JU4	1-2	INB- pin connected to the COM in through R14.	
JU6	Installed	INB+ pin assumes the DC offset at the REFP and REFN common.	
JU3	1-2	INB+ pin DC-coupled to SMA connector S/E_INB+ through R13 and R6.	Analog input signal is applied to **channel B**. **Single-ended input, DC-coupled**. • R6 shorted (0Ω) • Remove C3 • Remove R3
JU4	Not installed	Place DC offset of analog source at the S/E_INB SMA connector.	
JU6	Not installed	INB+ pin assumes the DC offset from the analog input source.	
JU3	2-3	INB+ pin connected to high side of transformer T2 through R13.	Analog input signal is applied to **channel B**. **Differential input, AC-coupled**.
JU4	2-3	INB- pin connected to low side of transformer T2 through R14.	
JU3	1-2	INB+ pin DC-coupled to SMA connector S/E_INB+ through R13 and R6.	Analog input signal is applied to **channel B**. **Differential input, DC-coupled**. • R6 shorted (0Ω) • Remove C3 • Remove R3
JU4	Not installed	INB- pin DC-coupled to SMA connector S/E_INB- through R14.	
JU6	Not installed	INB+ pin assumes the DC offset from the analog input source.	

Power-Down, Standby, Idle, and Operating Modes

The EV kit also features jumpers that allow the user to enable or disable certain functions of the data converter. Jumpers JU7 and JU8 control the power-down, standby, idle, and operating modes of the EV kit. See Table 6 for jumper settings.

Reference Modes

The EV kit provides three modes of reference operation: internal reference, buffered external reference, and unbuffered external reference. In internal reference mode, the REFIN PCB pad is connected to VADUT. In buffered external reference mode, an external reference voltage of 1.024V can be connected at the REFIN PCB pad. In unbuffered external reference mode, REFIN is connected to GND, and three external reference voltages should be used to drive REFP, REFN, and COM. Jumper JU11 selects the reference modes of the EV kit. See Table 7 for jumper settings.

Digital Output Format

The ADC features a single 8-bit CMOS-compatible digital output bus. Channel A is available at the output during A/$\overline{B}$ high. Channel B is available at the output during A/$\overline{B}$ low. The channel selection signal (A/$\overline{B}$) is an image of the clock that can be used to synchronize the output data. Refer to the MAX19192 IC data sheet for more information.

A driver is used to buffer the ADC's digital outputs. This buffer is able to drive large capacitive loads that may be present at the logic analyzer connection, without compromising the digital output signals. The outputs of the buffers are connected to header J1 located on the right side of the EV kit, where the user can connect a logic analyzer. See Table 8 for the ADC output channel bit locations on header J1.

All even-number pins on header J1 are connected to OGND.

Table 6. Power-Down, Standby, Idle, and Operating Modes Configuration (JU7, JU8)

SHUNT POSITION		PIN CONNECTION	EV KIT OPERATION
JU7	JU8		
1-2	1-2	PD0 connected to OGND PD1 connected to OGND	MAX19192 in power-down mode: ADC off, ref off, output three stated.
1-2	2-3	PD0 connected to OGND PD1 connected to VODUT	MAX19192 in standby mode: ADC off, ref on, output three stated.
2-3	1-2	PD0 connected to VODUT PD1 connected to OGND	MAX19192 in idle mode: ADC on, ref on, output three stated.
2-3	2-3	PD0 connected to VODUT PD1 connected to VODUT	MAX19192 in operating mode: ADC on, ref on, output enabled.
Not installed	Not installed	External control source (TTL/CMOS-compatible) applied at the PD0 and PD1 PCB pads.	PD0, PD1 = 00 (power-down mode) PD0, PD1 = 01 (standby mode) PD0, PD1 = 10 (idle mode) PD0, PD1 = 11 (operating mode)

Table 7. Reference Modes Configuration (JU11)

SHUNT POSITION	REFIN PIN CONNECTION	EV KIT OPERATION
1-2	Connected to VADUT	Internal reference mode: $V_{REF} = V_{REFP} - V_{REFN} = 0.512V$
2-3	Connected to GND	Unbuffered external reference mode: REFP, REFN, COM driven by external sources
—	Connected to an external reference source (+1.024V)	Buffered external reference mode: $V_{REF} = V_{REFP} - V_{REFN} = 0.512V$

Table 8. Header J1 Output Bit Location

CHANNEL	$A/\overline{B}$	BIT D0	BIT D1	BIT D2	BIT D3	BIT D4	BIT D5	BIT D6	BIT D7
A (CLK ↓)*	1	J1-3 (A0)	J1-5 (A1)	J1-7 (A2)	J1-9 (A3)	J1-13 (A4)	J1-15 (A5)	J1-17 (A6)	J1-19 (A7)
B (CLK ↑)*	0	J1-3 (B0)	J1-5 (B1)	J1-7 (B2)	J1-9 (B3)	J1-13 (B4)	J1-15 (B5)	J1-17 (B6)	J1-19 (B7)

**Trigger signal for the logic analyzer.*

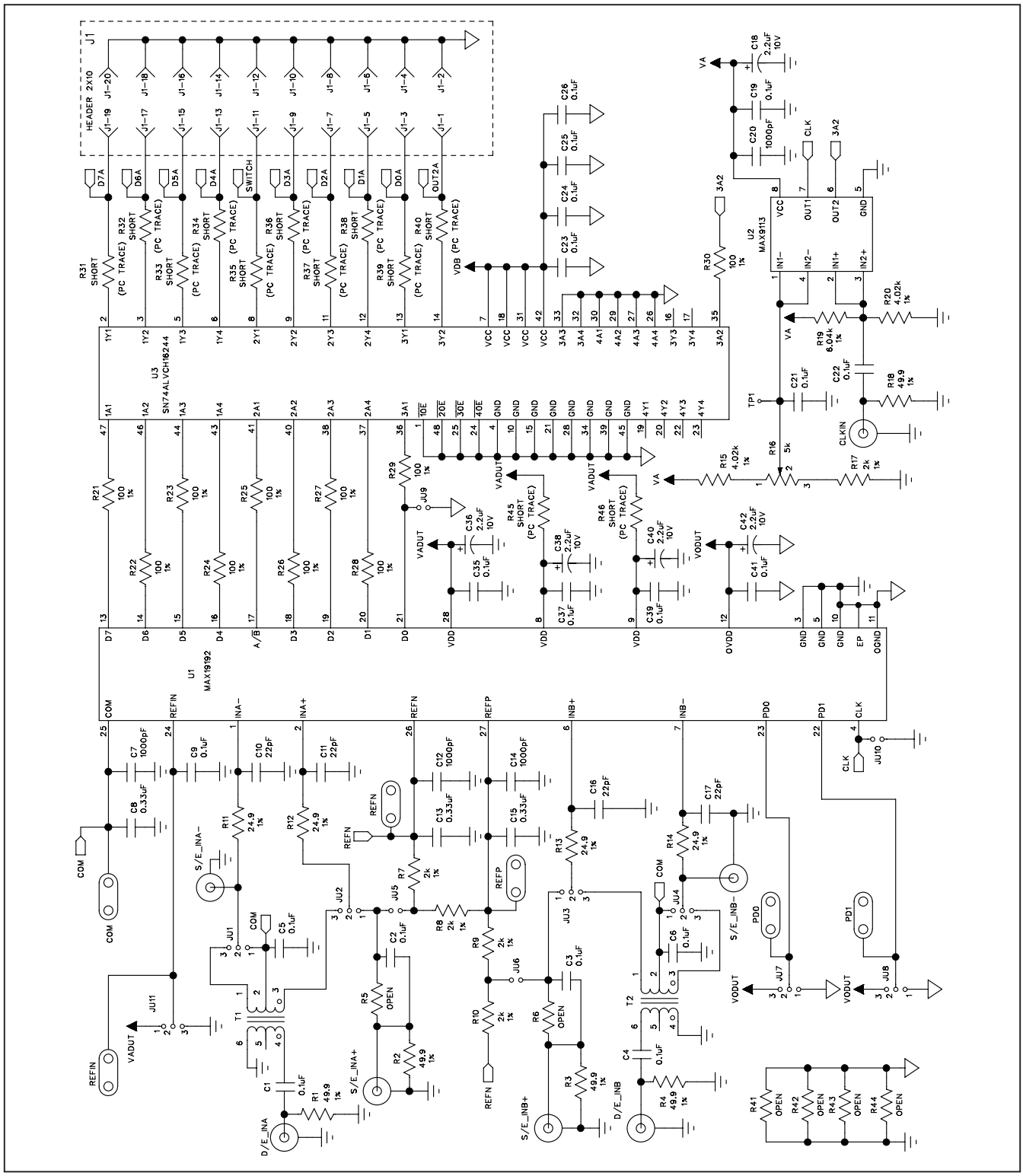

Figure 1a. MAX19192 EV Kit Schematic (Sheet 1 of 2)

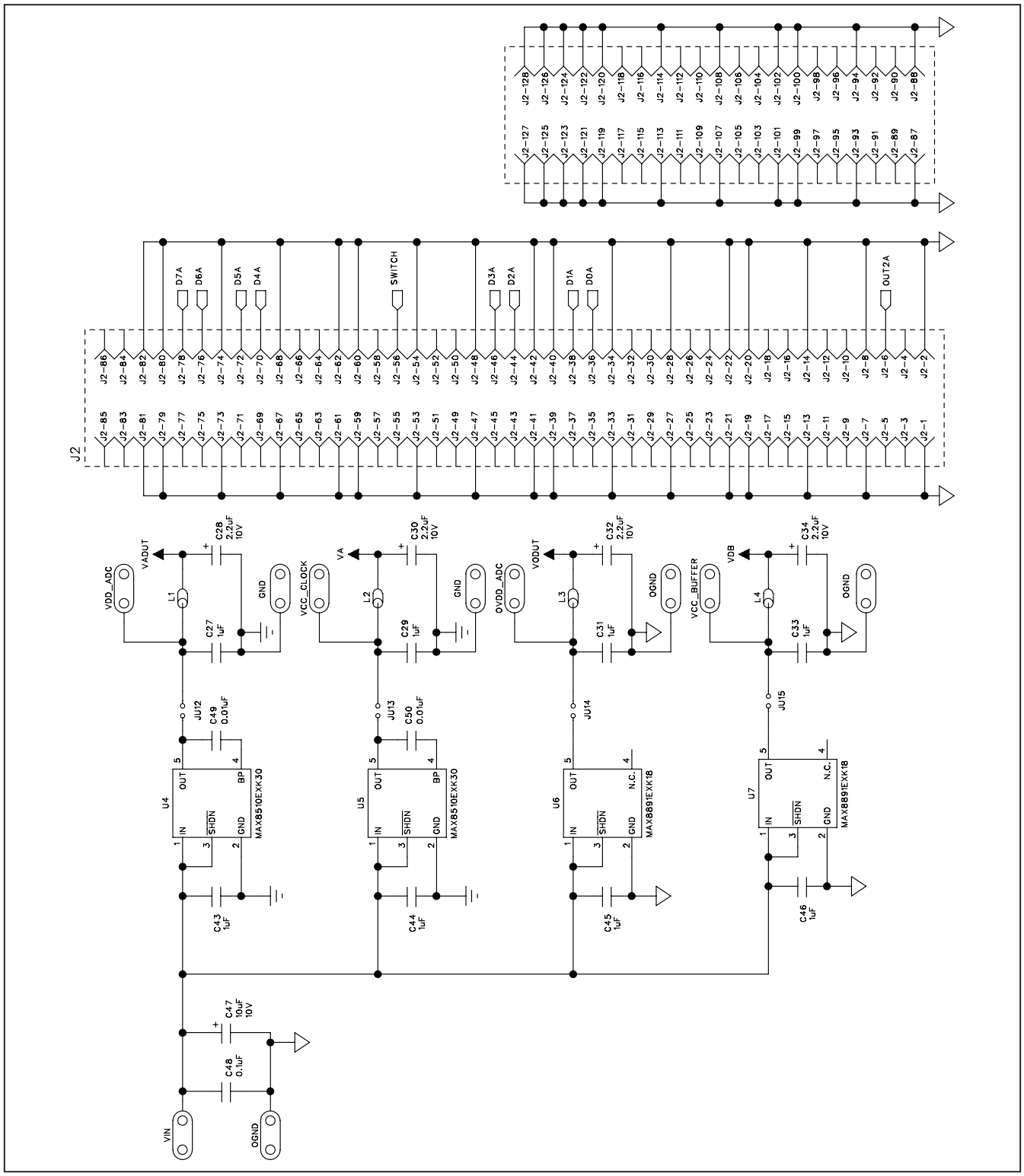

Figure 1b. MAX19192 EV Kit Schematic (Sheet 2 of 2)

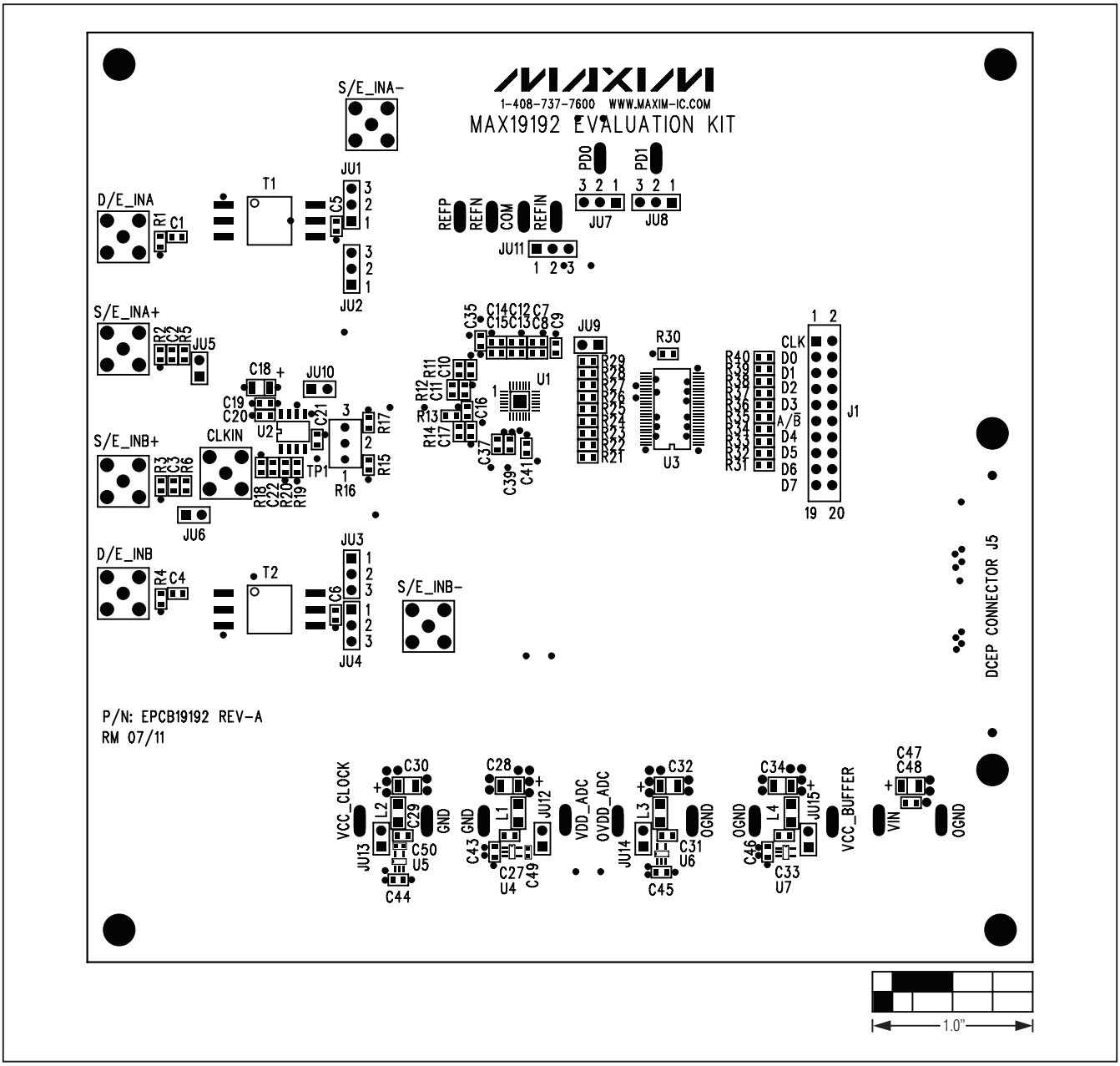

Figure 2. MAX19192 EV Kit Component Placement Guide—Component Side

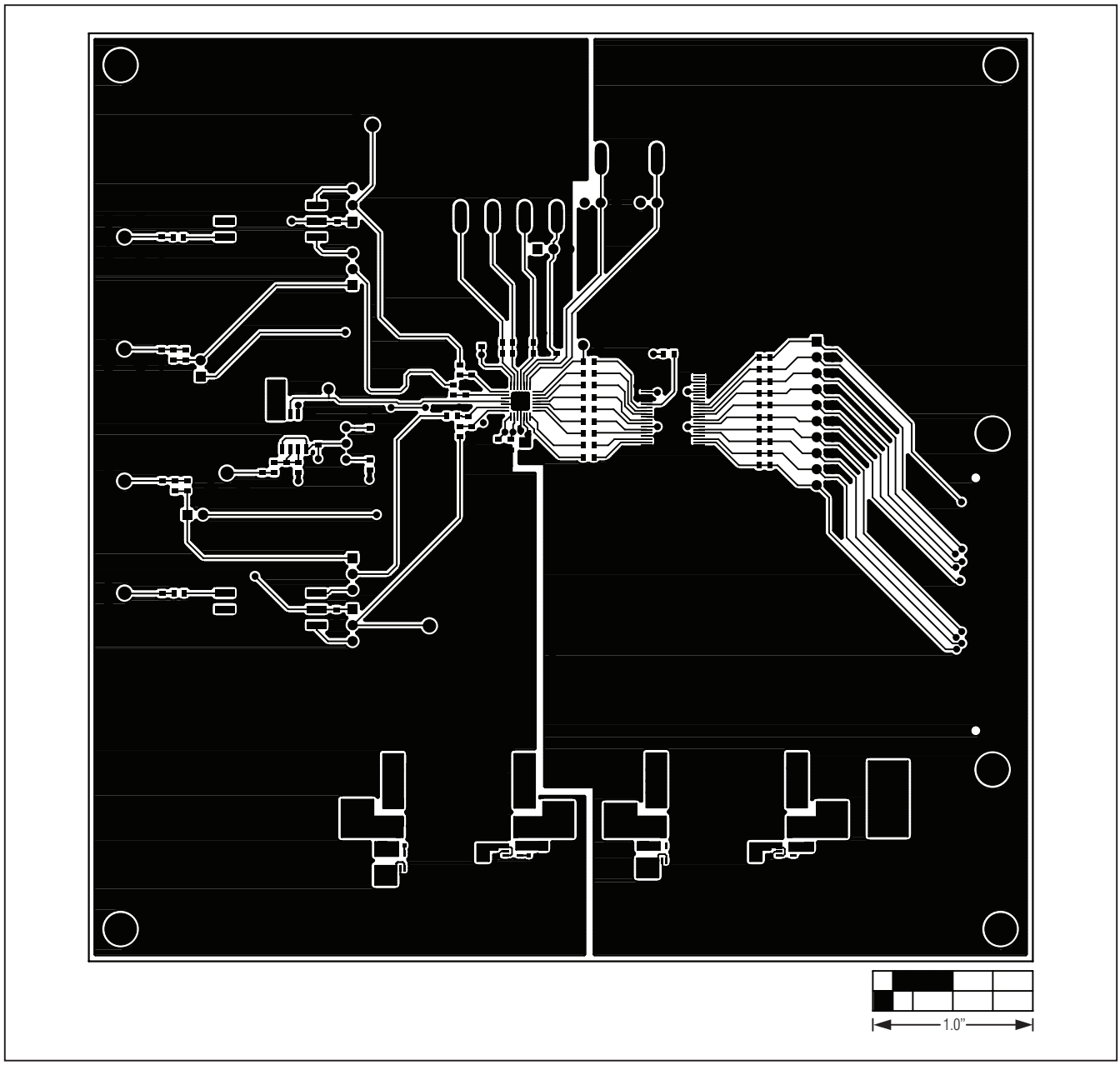

Figure 3. MAX19192 EV Kit PCB Layout—Component Side

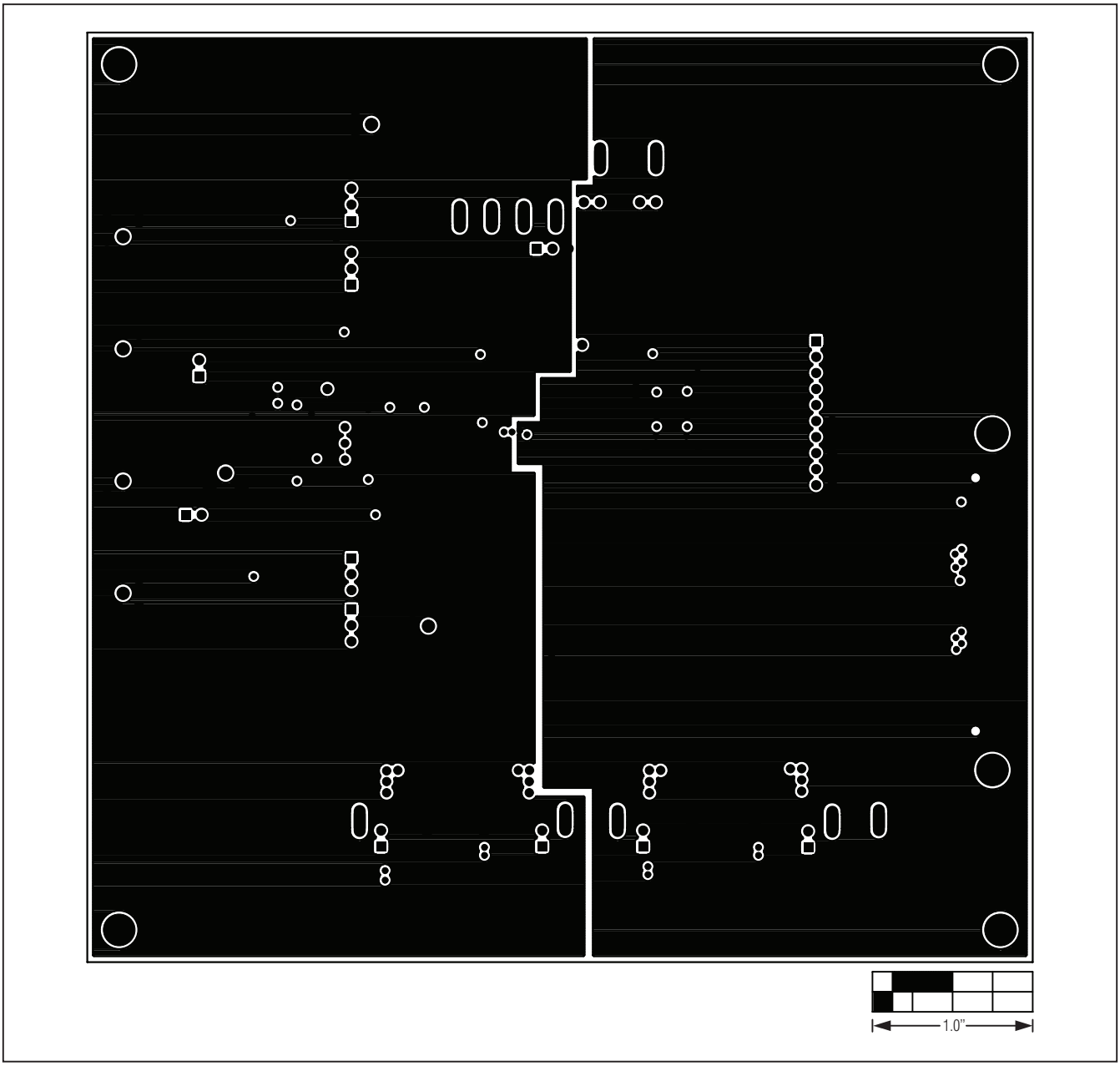

Figure 4. MAX19192 EV Kit PCB Layout—Ground Planes

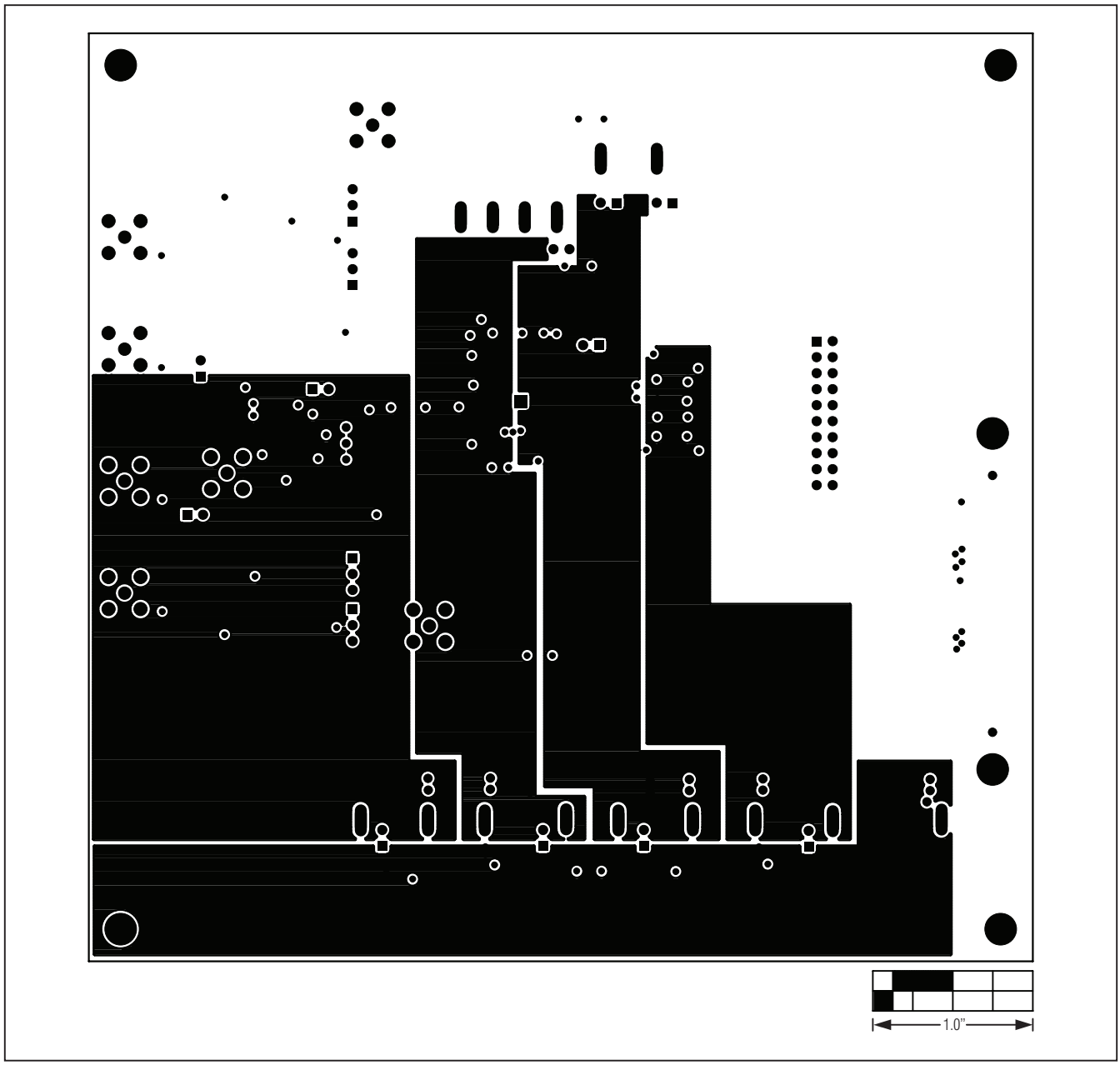

Figure 5. MAX19192 EV Kit PCB Layout—Power Planes

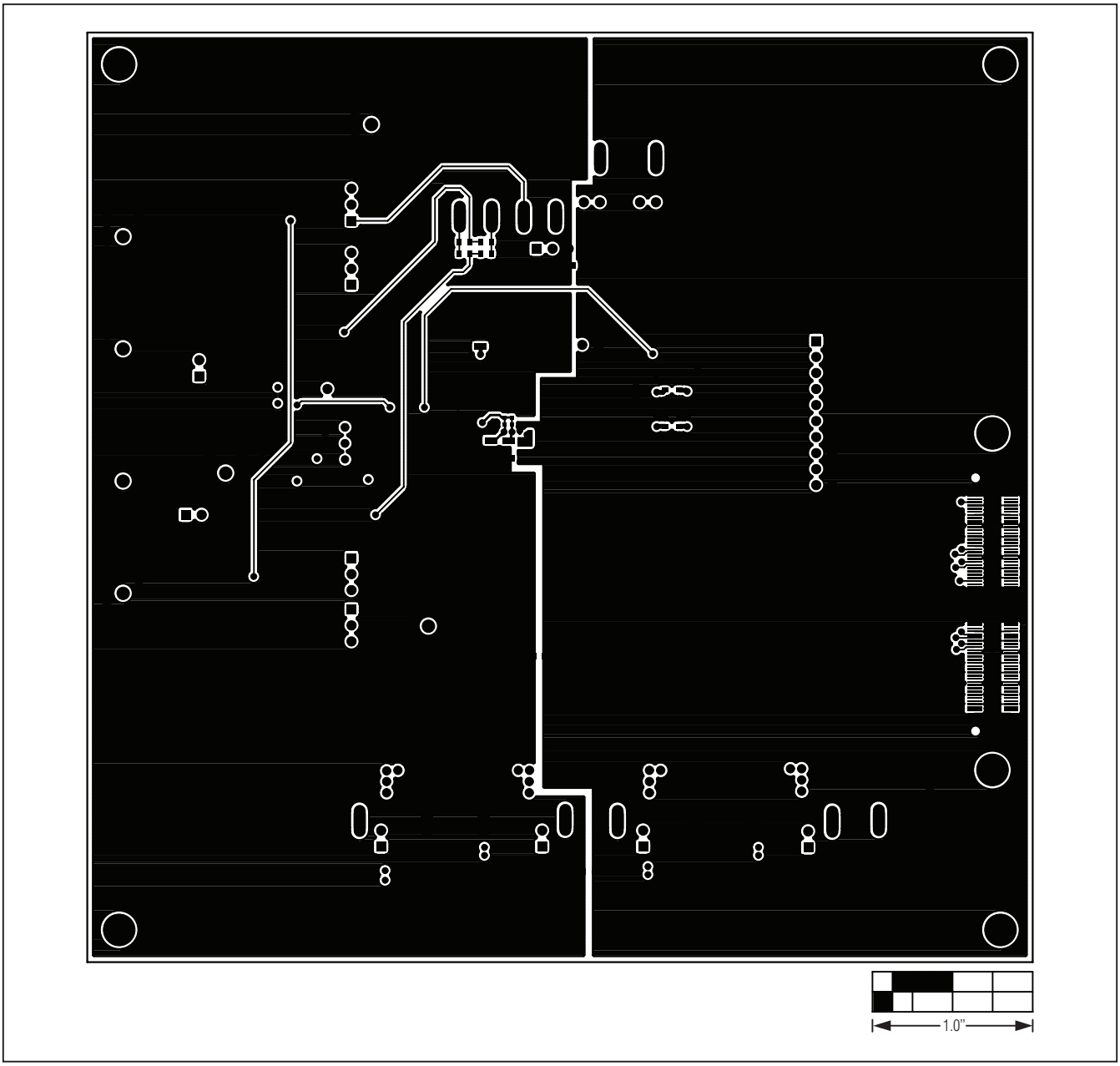

Figure 6. MAX19192 EV Kit PCB Layout—Solder Side

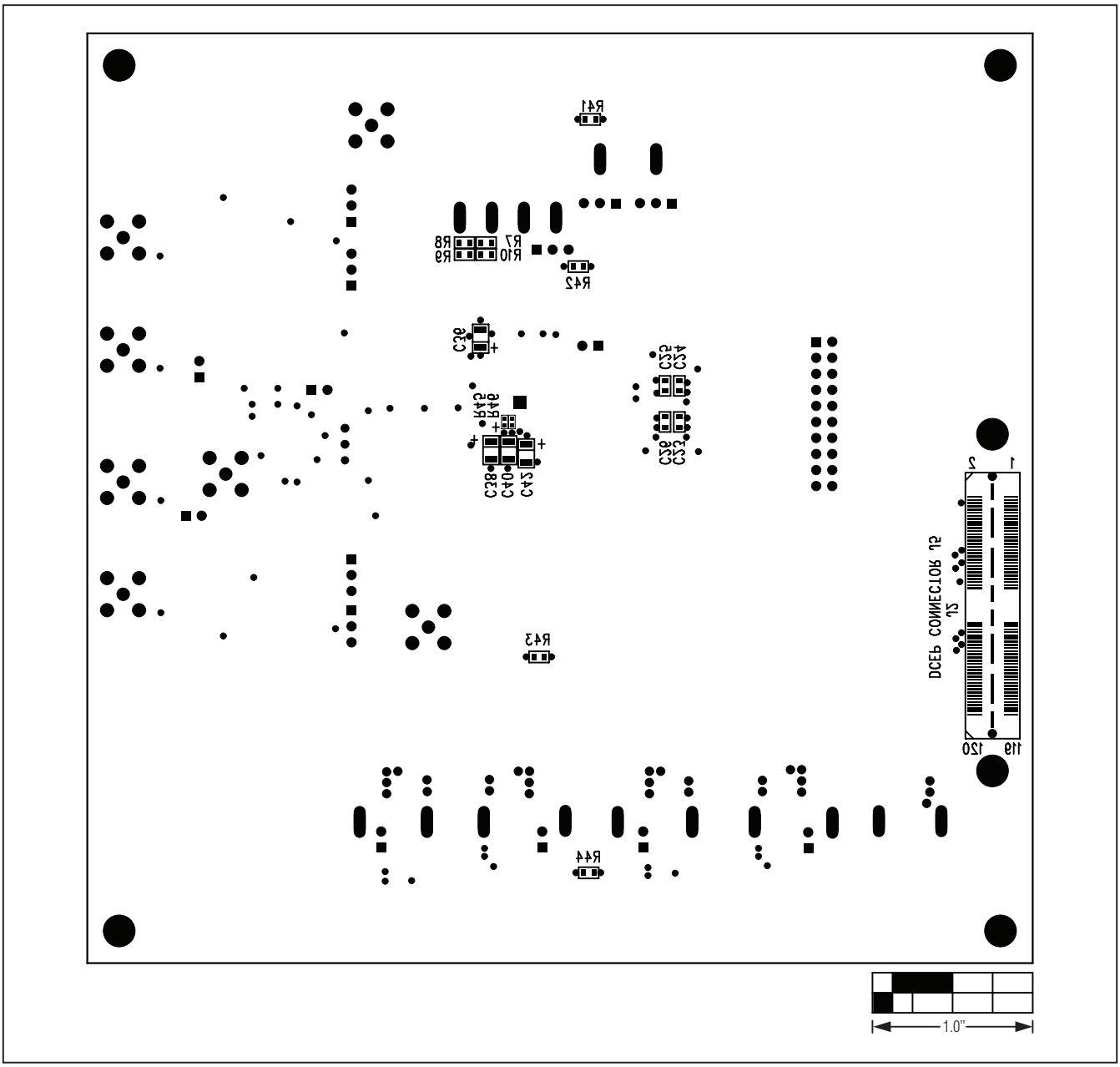

Figure 7. MAX19192 EV Kit Component Placement Guide—Solder Side

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/11	Initial release	—