*Click **here** to ask an associate for production status of specific part numbers.*

MAX20408/MAX20410

Automotive 36V, 8A/10A Fully-Integrated Buck Converter with 10µA Quiescent Current and Dual-Phase Capability

General Description

The MAX20408/MAX20410 are automotive, highly-integrated synchronous buck converters with internal high-side and low-side switches. The ICs deliver up to 8A/10A with input voltages from 3.0V to 36V. The voltage quality can be monitored by the PGOOD signal. The MAX20408/MAX20410 can operate in the dropout mode by running at 99% duty cycle, making them ideal for automotive and industrial applications.

The MAX20408/MAX20410 offer programmable or fixed output voltage options. High switching frequency at 2.1MHz and 400kHz options allow for small external components, reduced output ripple, and guarantee no AM interference. SYNC input programmability enables three modes for optimized performance: forced PWM mode, skip mode with ultra-low quiescent current, and synchronization to an external clock. The spread-spectrum option minimizes EMI radiated emissions.

The MAX20408/MAX20410 also come with dual-phase capability, allowing up to 20A designs. Two ICs can be configured as a master and slave with dynamic current sharing and 180º out-of-phase operation.

The MAX20408/MAX20410 are available in a small 3.5mm x 3.75mm, 17-pin FC2QFN package. They are pin-to-pin compatible with the MAX20404/MAX20405/MAX20406 (4A to 6A) family of products.

Applications

- Automotive Supplies
  - Infotainment Systems
  - Advanced Driver-Assistance Systems (ADAS)
- Industrial Supplies
- General Purpose Buck Converters

Benefits and Features

- High-Power DC/DC Converter in Small Solution Size
  - 3.0V to 36V Operating Input Voltage Range
  - Integrated High-Side and Low-Side FETs
  - 8A/10A Maximum Output Current
  - 400kHz and 2.1MHz Fixed Frequency Options
  - Fixed 2.5ms Soft-Start Time
  - 34ns Minimum On-Time
  - Programmable 0.8V to 10V Output with 400kHz, 0.8V to 6V Output with 2.1MHz, or Fixed Output Options
  - ±1.8% Output Voltage Accuracy
  - Symmetric and Balanced SUP and PGND Pinout Placement for Superior EMI Performance
  - Thermally-Enhanced 3.5mm x 3.75mm, 17-Pin FC2QFN Package
- High Efficiency at All Load Ranges
  - 10µA Quiescent Current in Skip Mode
  - Up to 94.3% Efficiency at $12V_{IN}/5V_{OUT}$/2.1MHz
  - Up to 95.6% Efficiency at $12V_{IN}/5V_{OUT}$/400kHz
- Dual-Phase Operation up to 20A Load Capability
  - Frequency Synchronization Input/Output
  - 180º Out-of-Phase Between Master and Slave
  - Dynamic Current Sharing
- Robust for Automotive Environment
  - Forced PWM and Skip-Mode Operation
  - 99% Duty Cycle Operation with Low Dropout Voltage
  - Supports 42V Load Dump
  - Spread-Spectrum Option
  - Power Good Indicator
  - Overtemperature and Short-Circuit Protection
  - -40°C to +125°C Automotive Temperature Range
  - AEC-Q100 Qualified
- Scalable Power Solution
  - Footprint Compatible with MAX20404/MAX20405/MAX20406

Ordering Information appears at end of data sheet.

19-101036; Rev 5; 3/22

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Simplified Block Diagram

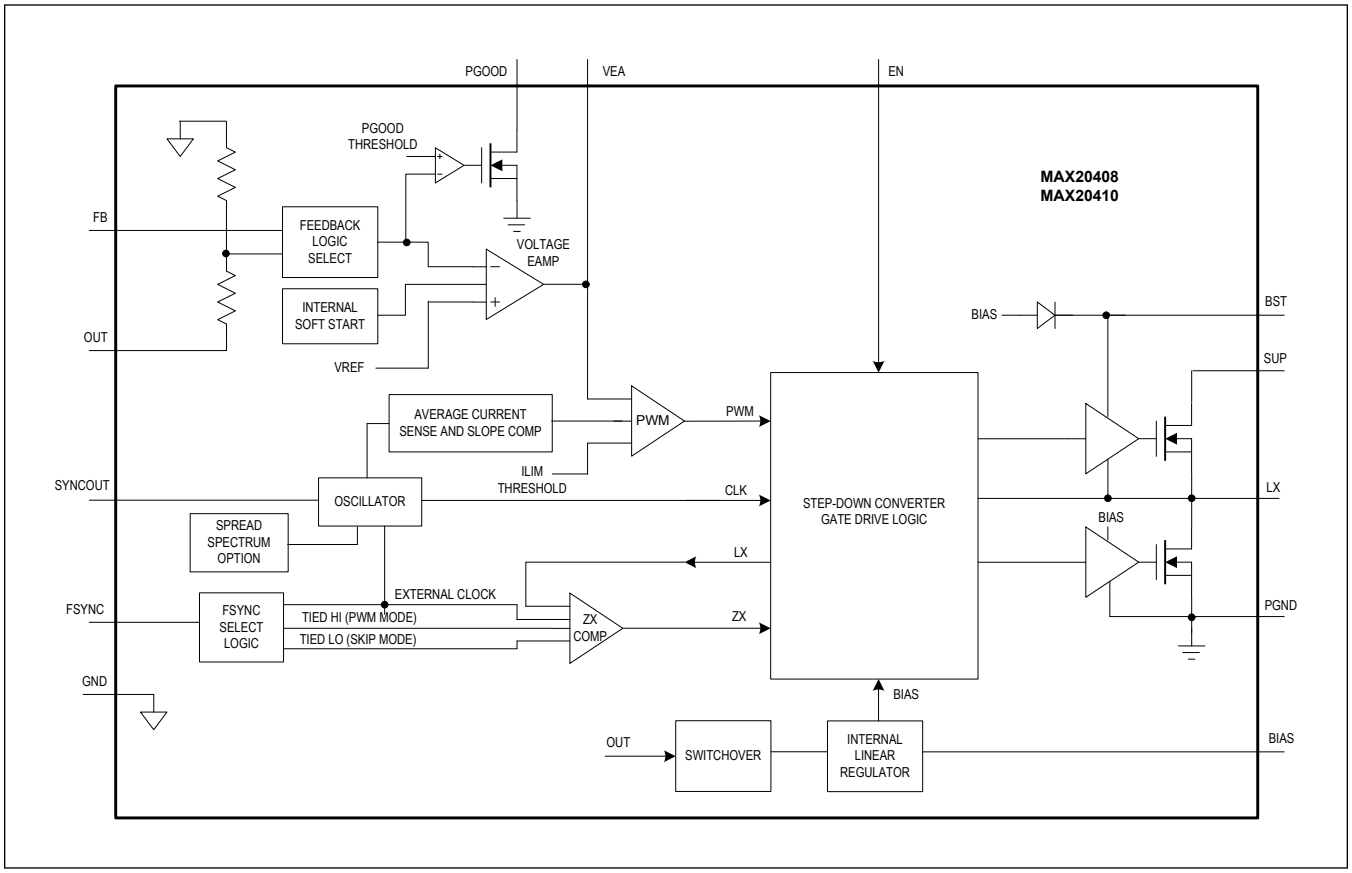


TABLE OF CONTENTS

General Description . . . 1
Applications . . . 1
Benefits and Features . . . 1
Simplified Block Diagram . . . 2
Absolute Maximum Ratings . . . 6
Recommended Operating Conditions . . . 6
Package Information . . . 6
  17L FC2QFN . . . 6
Electrical Characteristics . . . 6
Typical Operating Characteristics . . . 9
Pin Configuration . . . 13
  MAX20408/MAX20410 . . . 13
Pin Description . . . 13
Detailed Description . . . 15
  Linear Regulator Output (BIAS) . . . 15
  Synchronization Input (SYNC) . . . 15
  Enable Input (EN) . . . 15
  Soft-Start . . . 15
  Short-Circuit Protection . . . 15
  Power Good Indicator (PGOOD) . . . 15
  Spread-Spectrum Option . . . 16
  Thermal Shutdown Protection . . . 16
  Dual-Phase Operation . . . 16
  Low-Iq Operation in Dual-Phase . . . 16
Applications Information . . . 17
  Setting the Output Voltage . . . 17
  Setting the Output Voltage . . . 17
  Input Capacitor . . . 18
  Selecting the Inductor . . . 19
  Output Capacitor . . . 19
  PCB Layout Guidelines . . . 19
Typical Application Circuits . . . 22
  MAX20408 Configuration: 2.1MHz, 8A, Fixed Output Voltage . . . 22
  MAX20410 Configuration: 400kHz, 10A, Adjustable Output Voltage . . . 23
  MAX20408 Dual-Phase Configuration: 2.1MHz, 16A, Fixed Output Voltage . . . 24
  MAX20410 Dual-Phase Configuration: 400kHz, 20A, Adjustable Output Voltage . . . 25
Ordering Information . . . 26
Revision History . . . 27

LIST OF FIGURES

Figure 1. Typical Application Circuit for Dual-Phase Configuration with External Resistor-Divider 18

LIST OF TABLES

Table 1. Configurations for Low-Iq Operation 16
Table 2. Recommended Component Selection 17
Table 3. Recommended Inductor and Output Capacitor 19

Absolute Maximum Ratings

SUP, EN to PGND ..... -0.3V to +42V
BST to LX ..... -0.3V to +2.2V
BST to BIAS ..... -0.3V to 42V
BST to PGND ..... -0.3V to +44V
LX to PGND ..... -0.3V to SUP + 0.3V
SYNC, SYNCOUT, PGOOD to GND ..... -0.3V to 6V
FB, VEA to GND ..... -0.3V to BIAS + 0.3V
OUT to GND ..... -0.3V to 16V
PGND to GND ..... -0.3V to 0.3V
BIAS to GND ..... -0.3V to +2.2V
LX Continuous RMS Current 10A
SUP Continuous RMS Current 5A
Continuous Power Dissipation (TA = +70°C, derate 37mW/°C above +70°C) 2963mW
Operating Junction Temperature ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to 125	ºC

Note: These limits are not guaranteed.

Package Information

17L FC2QFN

Package Code	F173A3FY+4
Outline Number	21-100294
Land Pattern Number	90-100104
THERMAL RESISTANCE, JEDEC BOARD	
Junction-to-Ambient (θ_{JA})	38.6°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	7.7°C/W
THERMAL RESISTANCE, FOUR-LAYER EVKIT BOARD	
Junction-to-Ambient (θ_{JA})	27°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.5°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted. (*Note 1*, *Note 2*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}		3.0		36	V

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted. (*Note 1*, *Note 2*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{SUP_SHDN}	V_{EN} = 0, T_A = +25°C		4	6	µA
	I_{SUP}	V_{EN} = 1, V_{OUT} = 3.3V, V_{FB} = V_{BIAS}, no load, switching		10		µA
SUP Undervoltage Lockout		Rising	2.9	3.0	3.2	V
		Falling	2.6	2.7	2.9	
BIAS Voltage		+2.5V ≤ V_{SUP} ≤ +36V		1.8		V
BIAS Undervoltage Lockout	V_{BIAS_UVLO}	Rising	1.58	1.63	1.68	V
	$V_{BIAS_UVLO_HYS}$	Hysteresis		50		mV
BUCK CONVERTER						
Output Voltage Accuracy	$V_{OUT_SKIP_5V}$	V_{OUT} = 5.0V, skip mode, no load	4.92	5	5.05	V
	$V_{OUT_PWM_5V}$	V_{OUT} = 5.0V, PWM mode, no load	4.93	5	5.06	
	$V_{OUT_SKIP,4V}$	V_{OUT} = 4.0V, skip mode, no load	3.93	4	4.04	V
	$V_{OUT_PWM,4V}$	V_{OUT} = 4.0V, PWM mode, no load	3.94	4	4.04	
	$V_{OUT_SKIP_3V3}$	V_{OUT} = 3.3V, skip mode, no load	3.23	3.3	3.34	V
	$V_{OUT_PWM_3V3}$	V_{OUT} = 3.3V, PWM mode, no load	3.24	3.3	3.35	
Adjustable Output Voltage Range		fsw = 2.1MHz	0.8		6	V
		fsw = 400kHz	0.8		10	
FB Voltage Accuracy	V_{FB_PWM}	PWM mode, no load	0.788	0.800	0.812	V
FB Leakage Current	I_{FB}	V_{FB} = 0.8V, T_A = +25°C			100	nA
High-Side Switch On Resistance	R_{DSON_HS}	V_{BIAS} = 1.8V, I_{LX} = 5A		25	50	mΩ
Low-Side Switch On Resistance	R_{DSON_LS}	V_{BIAS} = 1.8V, I_{LX} = 5A		12	24	mΩ
High-Side Switch Current Limit Threshold	I_{LIM}	MAX20408	10	12	14	A
		MAX20410	11.9	14	16	
Low-Side Switch Negative Current Limit Threshold	I_{NEG}			-4		A
LX Leakage Current	I_{LX_LKG}	V_{SUP} = 36V, V_{LX} = 0V or V_{LX} = 36V, T_A = +25°C	-5		5	µA
Soft-Start Ramp Time	t_{SS}			2.5		ms
Minimum On-Time (Note 3)	T_{ON}			34	60	ns
Maximum Duty Cycle		Dropout mode	98	99		%

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted. (*Note 1*, *Note 2*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING FREQUENCY						
PWM Switching Frequency	f_{SW}	2.1MHz	1.925	2.1	2.275	MHz
		400kHz	360	400	440	kHz
SYNC External Clock Frequency	f_{SYNC}	f_{SW} = 2.1MHz	1.7		2.6	MHz
		f_{SW} = 400kHz	360		600	kHz
Spread Spectrum Range		Percentage of f_{SW}		±3		%
PGOOD OUTPUT						
PGOOD Threshold	V_{PGOOD_R}	Percentage of V_{OUT}, rising	92	94	96	%
	V_{GOOD_F}	Percentage of V_{OUT}, falling	91	93	95	
PGOOD Debounce	T_{DEB}	PWM mode, 2.1 MHz option, falling		50		µs
PGOOD High Leakage Current	I_{PGOOD_LKG}	T_A = +25°C			1	µA
PGOOD Low Voltage Level	V_{PGOOD_LOW}	Sinking 1mA			0.4	V
LOGIC LEVELS						
EN High Voltage Level	V_{EN_HIGH}		1.2			V
EN Low Voltage Level	V_{EN_LOW}				0.5	V
EN Input Current	I_{EN}	V_{EN} = V_{SUP} = 36V, T_A = +25°C			1	µA
SYNC High Voltage Level	V_{SYNC_HIGH}		1.4			V
SYNC Low Voltage Level	V_{SYNC_LOW}				0.4	V
SYNC Input Current	$I_{IN,SYNC}$	TA = +25°C			1	µA
SYNCOUT Output Voltage Level	$V_{SYNCOUT}$	No load	2.6	3.3	3.9	V
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			175		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}			20		°C

Note 1: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design and characterization.

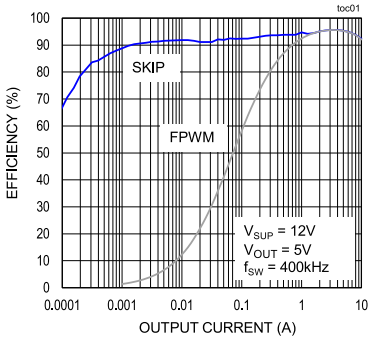
Note 2: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150º for 5,000 hours.

Note 3: Guaranteed by design, not production tested.

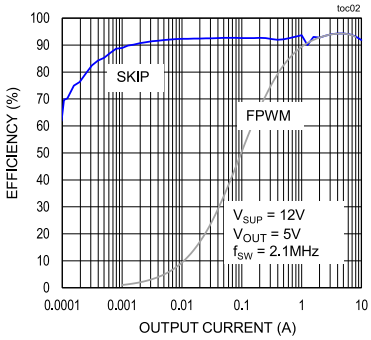
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

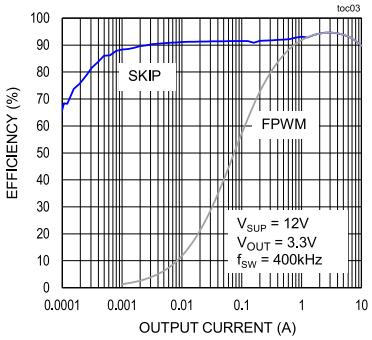
EFFICIENCY vs OUTPUT CURRENT (MAX20410AFOA)



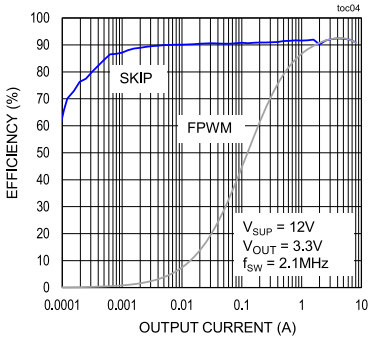
EFFICIENCY vs OUTPUT CURRENT (MAX20408AFOA)



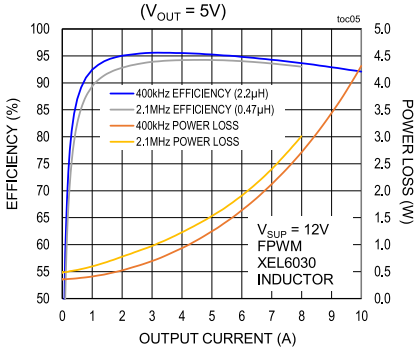
EFFICIENCY vs OUTPUT CURRENT (MAX20410AFOB)



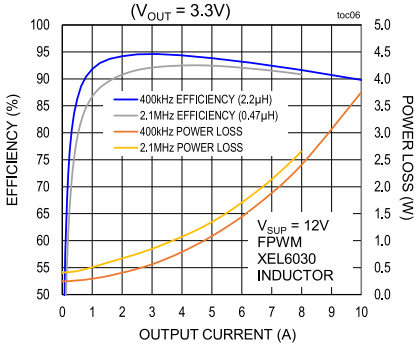
EFFICIENCY vs OUTPUT CURRENT (MAX20408AFOB)



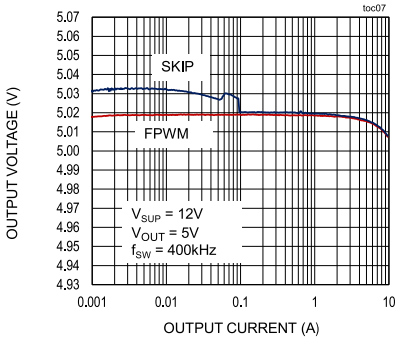
EFFICIENCY & POWER LOSS vs OUTPUT CURRENT (V_{OUT} = 5V)



EFFICIENCY & POWER LOSS vs OUTPUT CURRENT (V_{OUT} = 3.3V)



OUTPUT LOAD REGULATION (MAX20410AFOA)



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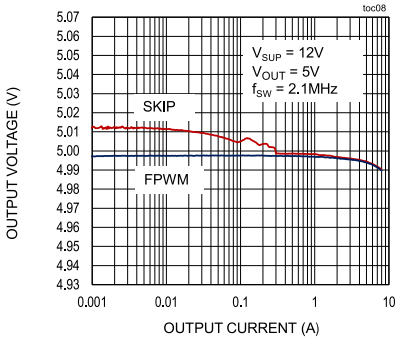

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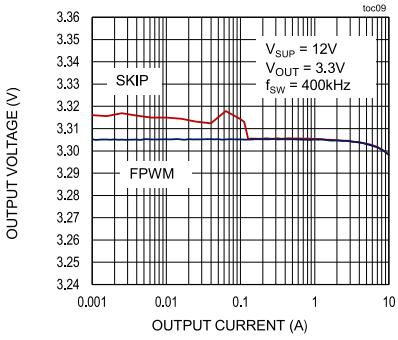
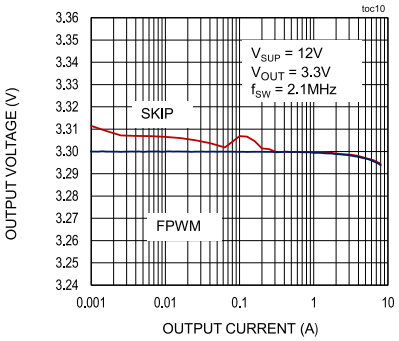


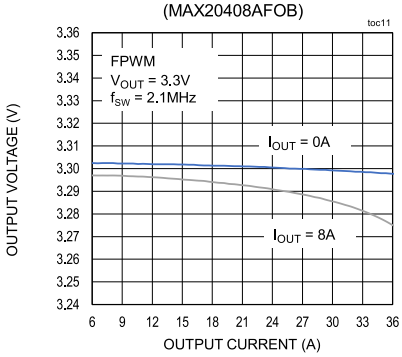
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

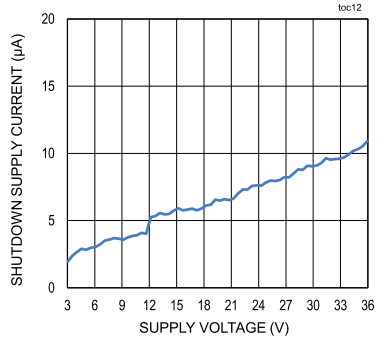
OUTPUT LOAD REGULATION (MAX20408AFOB)



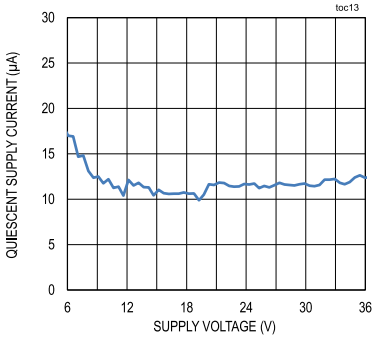
OUTPUT LINE REGULATION (MAX20408AFOB)



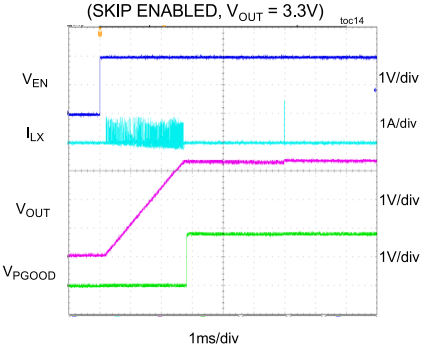
SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE



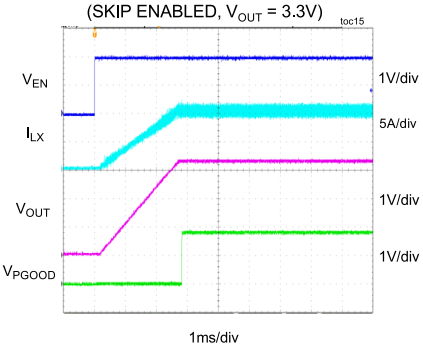
QUIESCENT CURRENT vs SUPPLY VOLTAGE



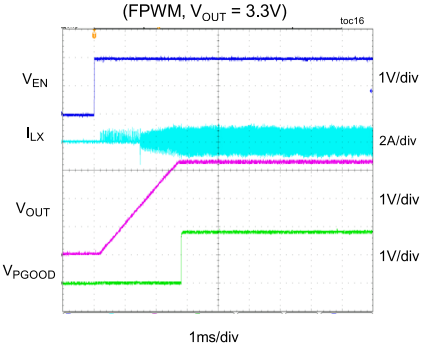
START UP INTO NO LOAD (SKIP ENABLED, VOUT = 3.3V)



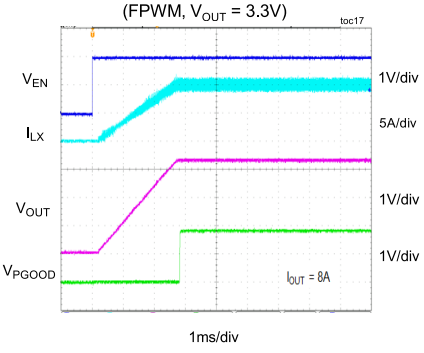
START UP INTO FULL LOAD (SKIP ENABLED, VOUT = 3.3V)



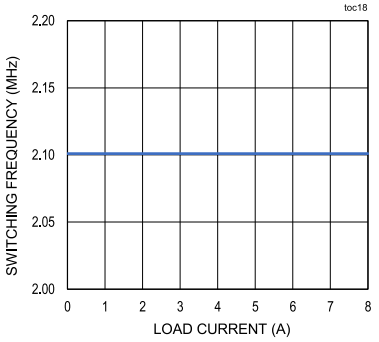
START UP INTO NO LOAD (FPWM, VOUT = 3.3V)



START UP INTO FULL LOAD (FPWM, VOUT = 3.3V)



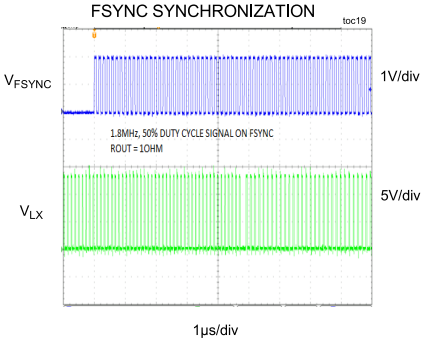
SWITCHING FREQUENCY vs LOAD CURRENT



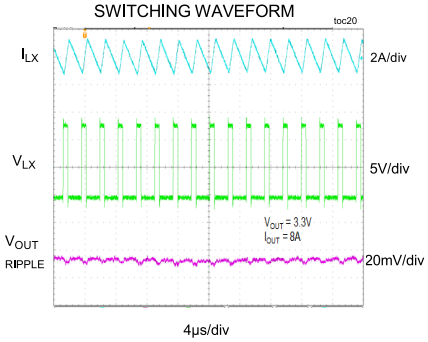
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

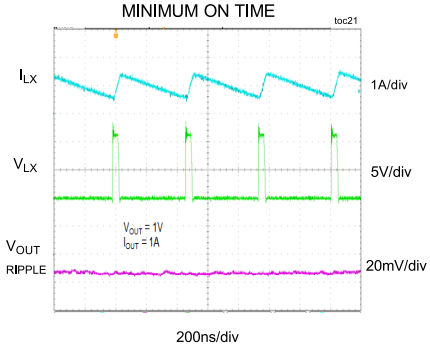
FSYNC SYNCHRONIZATION



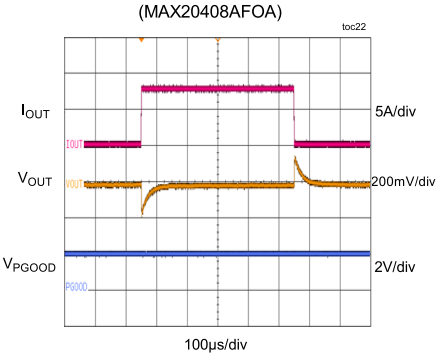
STEADY STATE SWITCHING WAVEFORM



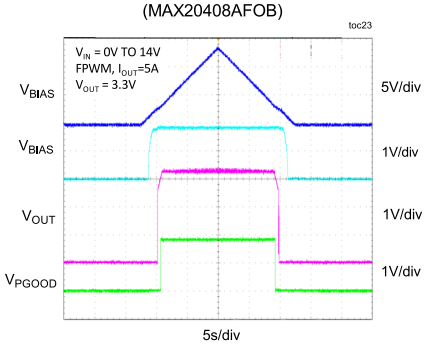
MINIMUM ON TIME



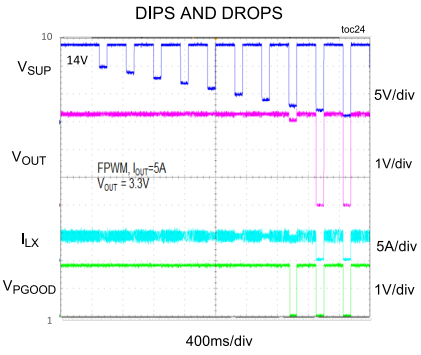
LOAD TRANSIENT RESPONSE (MAX20408AFOA)



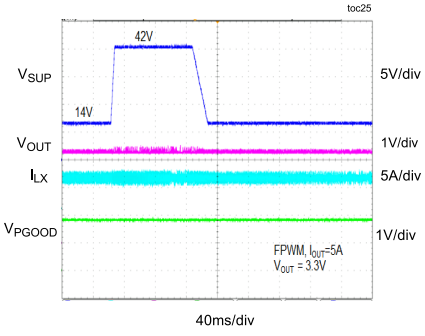
SLOW INPUT VOLTAGE RISING (MAX20408AFOB)



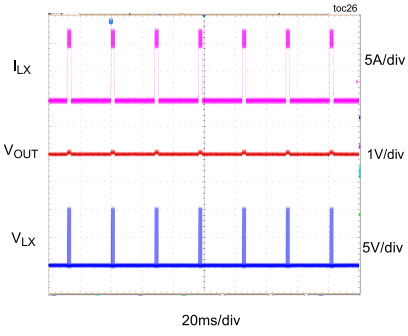
DIPS AND DROPS



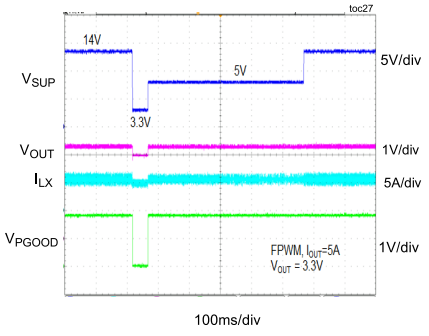
DIPS AND DROPS



OUTPUT SHORT TO GROUND



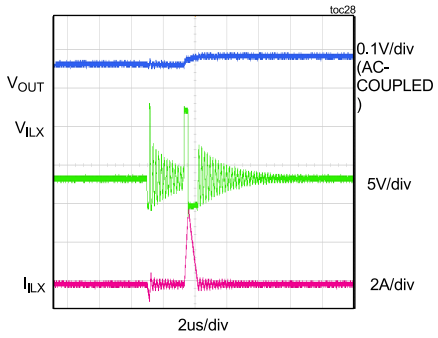
COLD CRANK



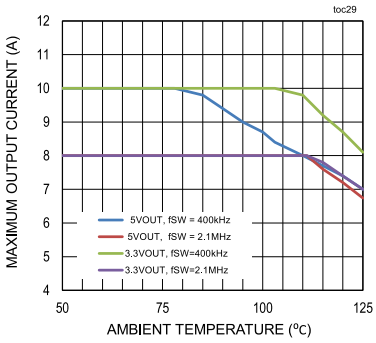
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

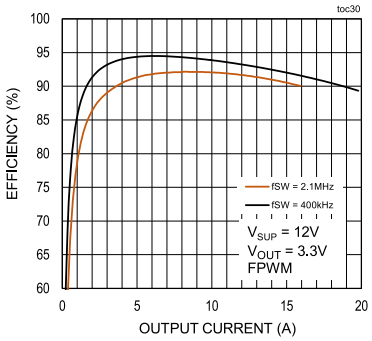
SKIP MODE / NO LOAD OPERATION



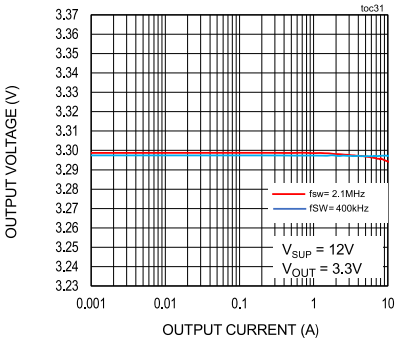
THERMAL DERATING CURVE



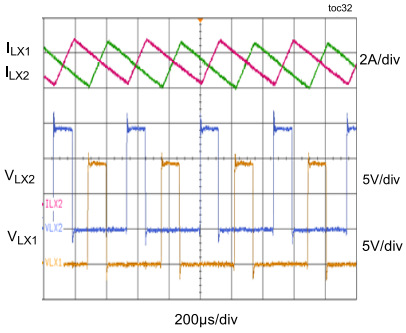
EFFICIENCY vs OUTPUT CURRENT (DUAL PHASES)



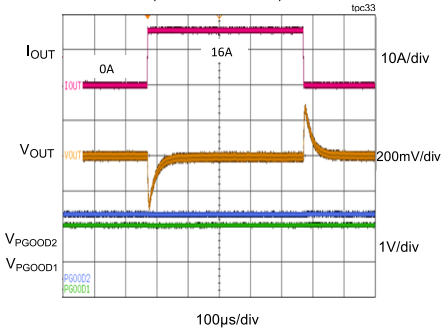
OUTPUT LOAD REGULATION (DUAL PHASES)



DUAL PHASE CURRENT SHARING (I_{OUT} = 16A)

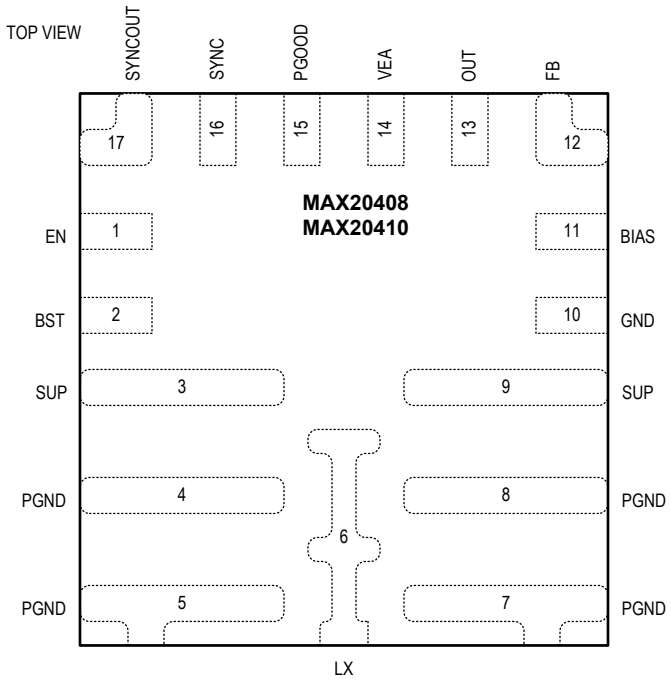


LOAD TRANSIENT RESPONSE (DUAL PHASES)



Pin Configuration

MAX20408/MAX20410



17 FC2QFN
3.5mm x 3.75mm

Pin Description

PIN	NAME	FUNCTION
1	EN	High Voltage Compatible Enable Input. Drive EN high to enable the buck converter.
2	BST	High-Side Gate Driver Supply. Connect a 0.1µF ceramic capacitor between BST and LX.
3	SUP	IC Supply Input and Internal High-Side Switch Supply Input. Bypass SUP to PGND with 0.1µF and 4.7µF ceramic capacitors as close as possible. Both SUP pins are internally connected.
4, 5	PGND	Power Ground. Connect all PGND pins together.
6	LX	Buck Inductor Connection. Connect an inductor from LX to the buck output. LX is high impedance when the IC is disabled.
7, 8	PGND	Power Ground. Connect all PGND pins together.
9	SUP	IC Supply Input and Internal High-Side Switch Supply Input. Bypass SUP to PGND with 0.1µF and 4.7µF ceramic capacitors as close as possible. Both SUP pins are internally connected.
10	GND	Analog Ground. Connect GND and PGND through start connection to the PCB ground plane.
11	BIAS	1.8V Internal Linear Regulator Output. Connect BIAS to ground with a minimum of 2.2µF ceramic capacitor.
12	FB	Feedback Input. Connect FB to a resistor divider between OUT and GND to adjust the output voltage between 0.8V and 10V. Connect FB to BIAS for fixed output voltage.
13	OUT	Output Voltage Sense Input. The buck converter uses OUT to sense output voltage when FB is connected to BIAS.

Pin Description (continued)

PIN	NAME	FUNCTION
14	VEA	Internal Voltage Loop Error Amplifier Output. Connect VEA of the master and slave together in dual-phase operation. Leave VEA open for single-phase operation.
15	PGOOD	Open Drain Power Good Output. The PGOOD is low if the buck output voltage falls below 93% (typ) of regulation voltage. The PGOOD becomes high impedance when the buck output voltage rises above 94% (typ) of its regulation voltage. The PGOOD asserts low during soft-start. Connect PGOOD to BIAS or a positive voltage lower than 5.5V with a pullup resistor to indicate buck output status.
16	SYNC	External Clock Synchronization Input. Connect SYNC low to enable skip-mode operation. Connect SYNC high for forced PWM operation. Connect a valid external clock signal to SYNC to enable external clock synchronization.
17	SYNCOUT	180° Out-of-Phase Clock Output. In dual-phase operation, connect SYNCOUT to BIAS to configure the IC as a slave, and connect SYNCOUT of the master to SYNC of the slave. Leave SYNC open in single-phase operation.

Detailed Description

The MAX20408/MAX20410 are small, synchronous buck converters with integrated high-side and low-side switches. The ICs are designed to deliver up to 8A/10A current with input voltages from 3V to 36V while using only 10µA quiescent current at no load condition. Voltage quality can be monitored by the PGOOD signal. The ICs can operate in dropout by running at 99% duty cycle, making them ideal for automotive and industrial applications.

The MAX20408/MAX20410 offer fixed output voltages or adjustable output voltage programmed by an external resistor divider. Frequency is internally fixed with 2.1MHz and 400kHz options, which allow for small external components, reduced output ripple, and guarantee no AM interference. The signal at SYNC programs the ICs in skip enable, FPWM, or when synchronizing to the external clock. The spread-spectrum option minimizes EMI-radiated emissions. Average current-mode control with 34ns minimum ON time allows for large input/output step-down ratios without skipping cycles.

The MAX20408/MAX20410 can also be configured in dual-phase to supply up to 20A load. The average current-mode control provides noise immunity and accurate dynamic current sharing during transients.

The FC2QFN package lowers the package parasitic impedance and improves thermal performance. Symmetrical pinout placement of SUP and PGND provides balanced current loop around the ICs and further improves their EMI performance.

Linear Regulator Output (BIAS)

The devices include a 1.8V linear regulator (V_{BIAS}) that provide power to the internal circuit blocks. Connect a 2.2uF ceramic capacitor from BIAS to GND. During start-up, the bias regulator draws power from the input and switches over to the output after the start-up is completed (if V_{OUT} > 2.5V).

Synchronization Input (SYNC)

The MAX20408/20410 provide an internal oscillator with 400kHz and 2.1MHz options. Drive SYNC high for forced PWM (FPWM) operation with 400kHz or 2.1MHz switching frequency. Drive SYNC low to enable skip-mode for better efficiency improvement at light load. The ICs can be synchronized to the external clock with a valid external clock present at SYNC.

Enable Input (EN)

An Enable Input (EN) enables the ICs from shutdown mode. The EN is high-voltage compatible with input from automotive battery level down to 3V. Drive EN high to enable the ICs. Drive EN low to disable the ICs into shutdown mode. The quiescent current is reduced to 4µA (typ) during shutdown.

Soft-Start

Drive EN high to enable the ICs. The soft-start circuitry gradually ramps up the reference voltage during soft-start time (2.5ms typ) to reduce the input inrush currents during start-up.

Short-Circuit Protection

The ICs feature a cycle-by-cycle current limit and hiccup-mode to protect against short-circuit or overload condition. In overload conditions, the high-side FET remains on until the inductor current reaches the current limit threshold, I_{LIM}. Then the converter turns off the high-side FET and turns on the low-side FET to allow the inductor current to ramp down. Once the inductor current decreases to the valley current limit, the converter turns on the high-side FET again. This cycle repeats until the overload condition is removed.

A short-circuit is detected when the output voltage falls below the preset threshold voltage while the inductor current hits the current limit. The threshold voltage is 50% of the output regulation voltage for fixed output voltage, or 25% of output regulation voltage for adjustable output voltage. During hiccup-mode, the ICs turn off the buck converter for 25ms (10x soft-start time), and then restart it if the overcurrent or short-circuit condition is removed. The hiccup repeats when the short-circuit is continuously present.

Power Good Indicator (PGOOD)

The ICs feature an open-drain Power Good (PGOOD) output to indicate the output voltage status. The PGOOD goes low to high impedance when the converter output voltage rises above 94% (typ) of its nominal regulation voltage. The

PGOOD goes low when the output voltage drops below 93% (typ) of the nominal regulation voltage. Connect PGOOD to the converter output or BIAS voltage through a pullup resistor The PGOOD asserts low during soft-start.

Spread-Spectrum Option

The ICs feature enhanced EMI performance with the spread-spectrum option. The spread-spectrum is available as a factory option. When the spread-spectrum is enabled, the operating frequency is varied ±3% centered at switching frequency. The modulation signal is a triangular wave with 4.5kHz frequency at 2.1MHz. Therefore, switching frequency ramps down 3% and back to 2.1MHz in 110µs, and also ramps up 3% and back to 2.1MHz in 110µs, after which the cycle repeats. For operations at 400kHz, the modulation signal scales proportionally to 0.4/2.1.

The internal spread-spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock on SYNC and pass any modulation (including spread-spectrum) present on the driving external clock.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the ICs. When the junction temperature exceeds +170°C, an internal sensor shuts down the ICs, allowing them to cool. The thermal sensor turns on the ICs again after the junction temperature cools by 20°C.

Dual-Phase Operation

Two MAX20408/MAX20410s can be configured in dual-phase to provide higher output current up to 20A. To operate in dual-phase, one IC is programmed as a slave by connecting its SYNCOUT to BIAS, and the other IC is treated as a master. The SYNCOUT of the master is connected to the SYNC of the slave to have both ICs switch in 180° out-of-phase. Therefore, with present SYNCOUT signal from the master, FPWM is recommended for dual-phase operation.

The VEA nodes of the master and slave are connected together to ensure balanced current sharing between two phases. Also, by doing this, the master's voltage control loop is shared with the slave. Therefore, both FB nodes can be connected to the respective BIAS for fixed output voltage options. For adjustable output voltage option, instead of connecting FB nodes together, separate resistor dividers are used for each phase.

Low-Iq Operation in Dual-Phase

The MAX20408/MAX20410 come with dual-phase capability, where each IC can be either configured as master or slave. The SYNCOUT pin of the master outputs 180-degree out-of-phase clock when SYNC is tied high (FPWM mode). For low-Iq mode, pull the SYNC pin of the master low (skip-mode). In this mode, there is no clock present on the SYNCOUT pin of the master and the master IC enters the skip-mode. The internal circuit of the slave IC remains ON during this time and actively looks for the SYNCOUT signal from the master. As the slave IC is ON, the quiescent current is slightly higher, even though both the ICs skip pulses.

To improve the light-load efficiency and further reduce the Iq, pull the slave EN low. This disables the slave and its internal circuits, further reducing the Iq. Table 1 summarizes the truth table for low-Iq operation.

Table 1. Configurations for Low-Iq Operation

MASTER	SLAVE	MODE
EN = High, SYNC=BIAS	EN = High	FPWM (high Iq)
EN = High, SYNC=Low	EN = High	Skip mode (low Iq)
EN = High, SYNC=Low	EN = Low	Standby mode (ultra-low Iq)
EN = Low	EN = High	Not allowed

Applications Information

Setting the Output Voltage

Connect FB to BIAS to select the fixed output voltage set by the internal resistor divider between OUT and GND. Contact the factory for fixed output voltage options. To externally program the output voltage between 0.8V and 10V for 400kHz switching frequency, and between 0.8V and 6V for 2.1MHz switching frequency, connect a resistor divider from the buck converter output to FB, and then to GND. Select R_{FB2} between FB and GND in Typical Application Circuits less than 20kΩ. Calculate R_{FB1} between buck output and FB with the following equation:

$$R_{FB1} = R_{FB2} \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where, V_{FB} = 0.8V, and R_{FB2} is less than 20 kΩ.

The following table provides components selection recommendation for each output range (CFF is recommended based on R_{FB2} = 10 kΩ).

Table 2. Recommended Component Selection

SWITCHING FREQUENCY (kHz)	V_{OUT} (V)	INDUCTOR (µH)	OUTPUT CAPACITOR (µF)	CFF (pF)
400	0.8 to 1.8	0.68	752	N/A
400	1.8 to 3.3	1	611	N/A
400	3.3 to 5	2.2	420	220pF
400	5 to 7	2.2	287	180pF
400	7 to 10	2.2	134	47pF
2100	0.8 to 1.8	0.22	376	N/A
2100	1.8 to 3.3	0.22	423	N/A
2100	3.3 to 5	0.47	88	39pF
2100	5 to 6	0.47	83	15pF

Setting the Output Voltage

To set the output voltage to the internal fixed voltage, order the same fixed V_{OUT} setting for both master and slave ICs, and connect the FB pin to its respective BIAS. DO NOT connect the FB pins of the master and slave together.

To set the output voltage to a value other than the available fixed V_{OUT} options, connect a resistor-divider between OUT, FB, and GND as shown in Figure 1. Use an identical but separate resistor-divider for master and slave.

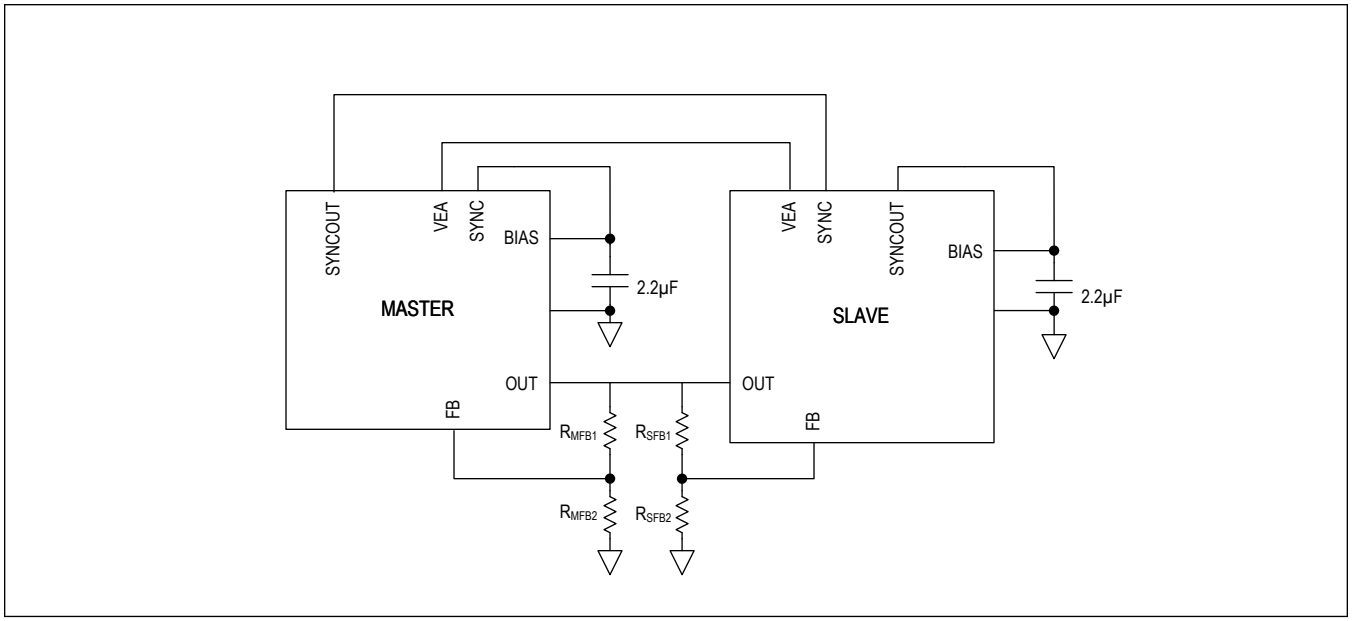


Figure 1. Typical Application Circuit for Dual-Phase Configuration with External Resistor-Divider

Input Capacitor

The input capacitors reduce peak current drawn from the power source, and improve noise and voltage ripple on the SUP nodes caused by the buck converter switching cycles. Use two ceramic input capacitors with 0.1µF and 4.7µF capacitance in parallel at each side of the IC for proper buck operation.

Place a 0.1 µF ceramic capacitor with 0402 or 0603 size next to SUP and PGND at each side of the IC to reduce input noise and improve EMI performance. A 4.7µF ceramic capacitor after 0.1µF capacitor is required on each input side to reduce input voltage ripple. Additional buck capacitor might be required if high impedance exists in the input supply or traces.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \times \left(\frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}} \right)$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$V_{SUP} = 2 \times V_{OUT}$

Therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability. The input-voltage ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{LOAD(MAX)} + \Delta I_L / 2}$$

$$C_{IN} = \frac{I_{LOAD(MAX)} \cdot D(1 - D)}{\Delta V_Q \cdot f_{SW}}$$

where

$$\Delta I_L = \frac{\left(V_{SUP} - V_{OUT}\right) \cdot V_{OUT}}{V_{SUP} \cdot f_{SW} \cdot L}$$

$$D = \frac{V_{OUT}}{V_{SUP}}$$

and $I_{LOAD(MAX)}$ is the maximum output current, ΔI_L is peak-to-peak inductor current, f_{SW} is switching frequency, and D is the duty cycle.

Selecting the Inductor

Inductor selection is a compromise between component size, efficiency, control loop bandwidth, and loop stability. Insufficient inductance increases the inductor current ripple, conduction losses, and output voltage ripple, and causes loop instability in the worst case. A large inductor reduces the inductor current ripple by sacrificing component size and slow response. See Table 2 for optimized inductor values at 400kHz and 2.1MHz switching frequency. The nominal standard value selected should be within ±50% of the specified inductance.

Table 3. Recommended Inductor and Output Capacitor

SWITCHING FREQUENCY	RECOMMENDED INDUCTANCE (µH)	RECOMMENDED OUTPUT CAPACITANCE (µF)
400kHz	2.2	4 x 47
2.1MHz	0.47	4 x 22

Output Capacitor

The output capacitor is a critical component for switching regulators. It is selected to meet output voltage ripple, load transient response, and loop stability requirements.

The output voltage ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low ESR ceramic capacitors. Assume the contribution to the output ripple voltage from ESR and the capacitor discharge to be equal. Use the following equations to get the output capacitance and ESR for a specified output voltage ripple.

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{p-p}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \cdot \Delta V_Q \cdot f_{SW}}$$

$$\Delta I_{P-P} = \frac{\left(V_{SUP} - V_{OUT}\right) \cdot V_{OUT}}{V_{SUP} \cdot f_{SW} \cdot L}$$

$$V_{OUT_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

where, ΔI_{P-P} is the peak-to-peak inductor current, and f_{SW} is the switching frequency.

During a load step, the output capacitors supply the load current before the converter loop responses with higher duty cycle, which causes output voltage undershoot. To keep the maximum output voltage deviations below the tolerable limits of the electronics being powered, calculate the output capacitance with the following equation:

$$C_{OUT} = \frac{\Delta I_{LOAD}}{\Delta V \cdot 2\pi \cdot f_C}$$

where, ΔI is the load step, ΔV is the allowed output voltage undershoot, and f_C is the loop crossover frequency, which can be assumed to be the lesser of $f_{SW}/10$ or 100kHz. The calculated C_{OUT} is the actually capacitance after considering capacitance tolerance, temperature effect, and voltage derating. See Table 3 for recommended output capacitance.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses, low EMI, and clean, stable operation. See the following

figure for an example layout.

Place the input bypass capacitors CBP and CIN as close as possible to each SUP and PGND on both sides of the IC. CBP should be placed right next to the SUP and PGND node on the same layer to provide best EMI rejection and minimize the input noise on SUP. The symmetrical CIN and CBP arrangements generate the SUP loops with opposite orientation to cancel the magnetic fields and help EMI mitigation.

Minimize the connection from the buck output capacitor's ground terminal to the input capacitor's ground terminal. Keep buck high-current path, and power traces wide and short. Minimize the traces from LX node to the inductor and then to the output capacitors. This minimizes the buck current loop area, and minimizes LX trace resistance and stray capacitance to achieve optimal efficiency.

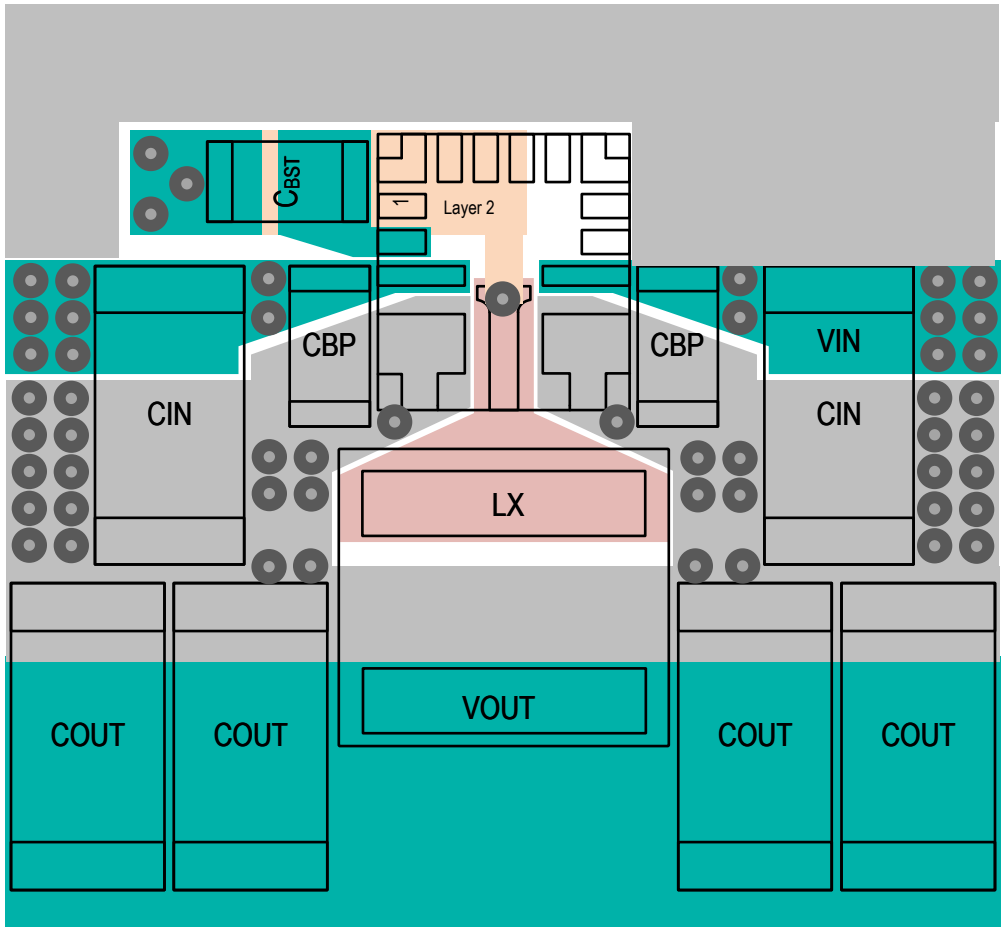
Place the bootstrap capacitor CBST close to the IC. Use short and wide traces from BST and LX, and minimize this routing parasitic impedance. High parasitic impedance from BST to LX impacts the switching speed, further increases switching losses, and high dV/dt noise. See Figure 1 for BST to LX routing.

Place the BIAS capacitor as close to the BIAS node as possible. Noise coupling into BIAS can disturb the reference and bias circuitry if this capacitor is installed away from the IC.

Keep the sensitive analog signals (FB/VEA) away from noisy switching nodes (LX and BST) and high current loops.

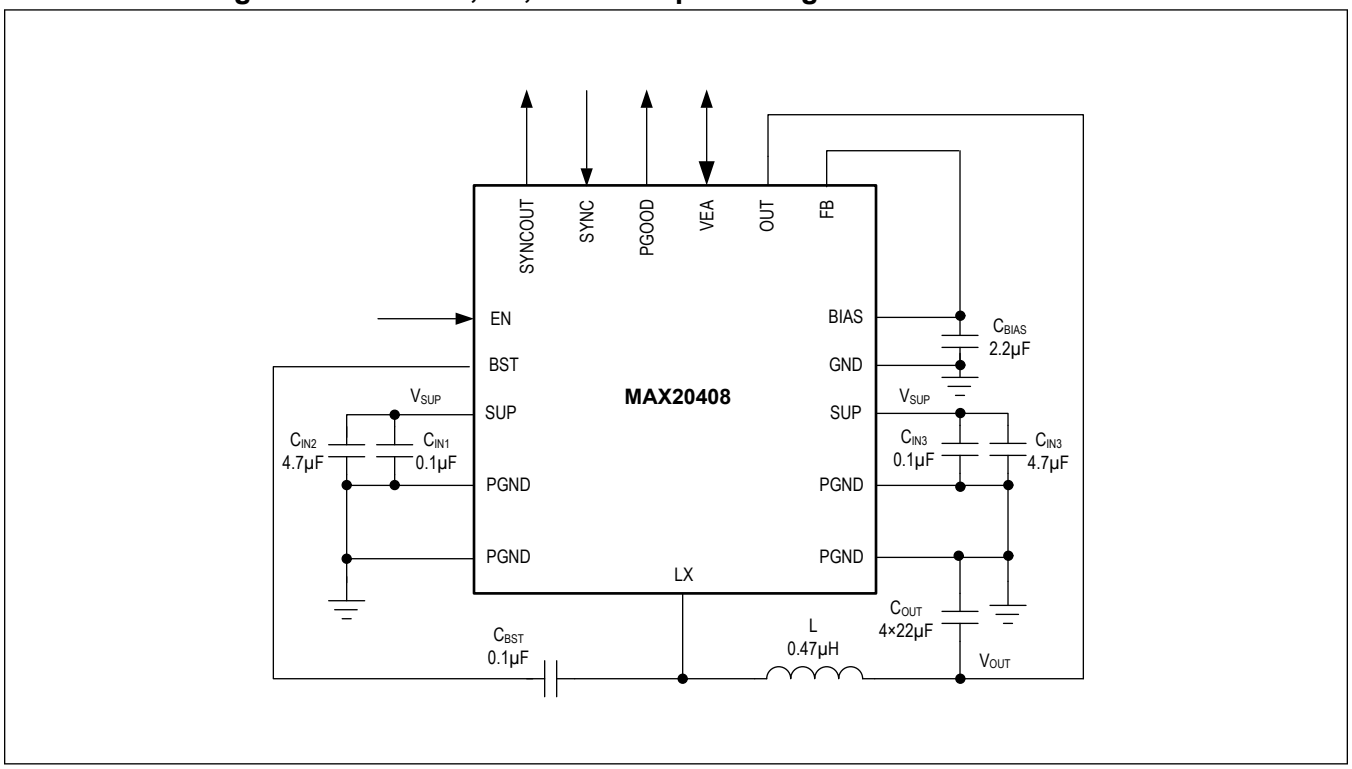
Ground is the return path for the full-load currents flowing into and out of the IC. It is also the common reference voltage for all the analog circuits. Improper ground routing can bring extra resistance and inductance into the current loop, causing different voltage reference and worsening voltage ringing or spikes. Place a solid ground plane layer under the power loop components layer to shield the switching noise from other sensitive traces. Connect the analog ground GND and power grounds PGND together at a single point in a star ground connection.

The PCB layout also plays an important role in power dissipation and thermal performance. The PGND nodes are the main power connection area between the IC and outside the IC. Place the ground copper area as much as as possible around the PGND area to ensure efficient heat transfer. Place vias as many as possible around the PGND nodes to further transfer the heat down the internal ground plane and other layers to further improve the thermal resistance from the IC package to the ambient.


CBST
1
Layer 2
CBP
CBP
VIN
CIN
CIN
LX
VOUT
COUT
COUT
COUT
COUT

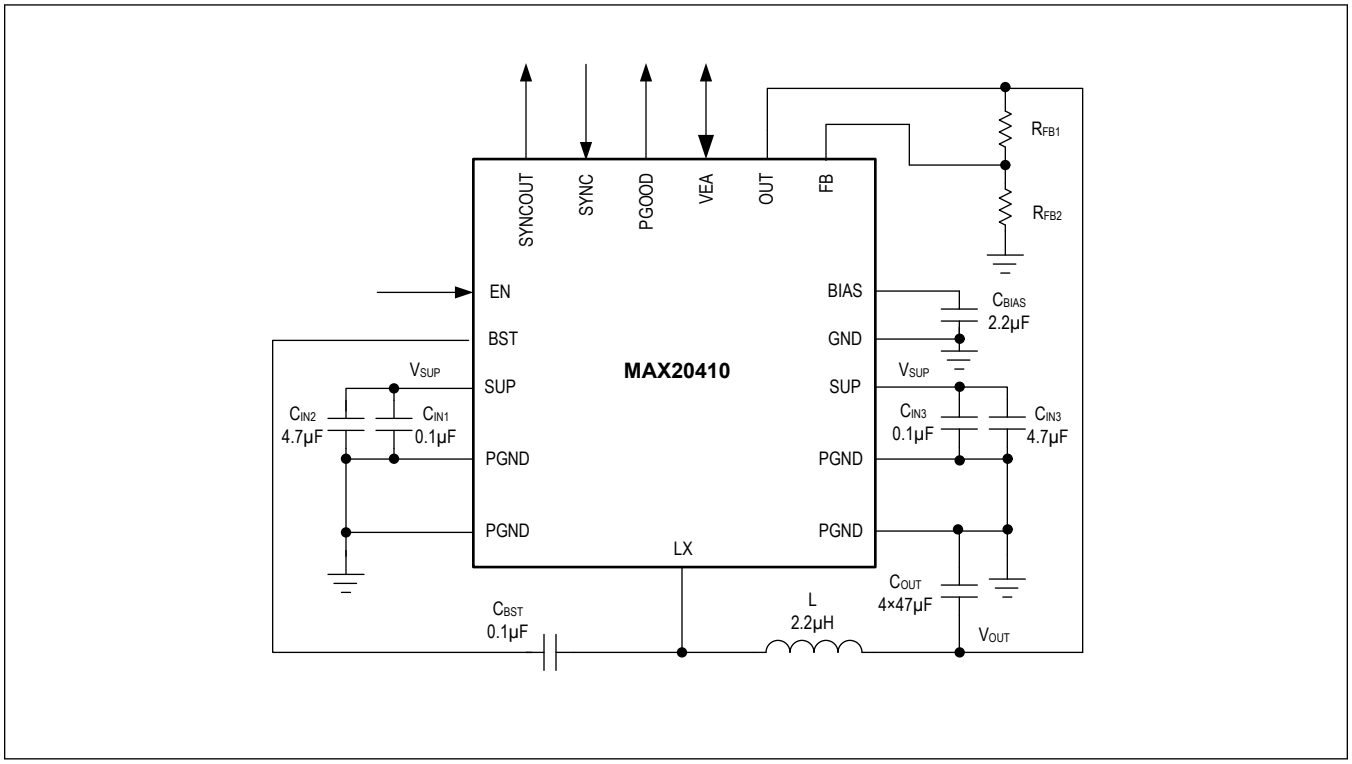
Typical Application Circuits

MAX20408 Configuration: 2.1MHz, 8A, Fixed Output Voltage



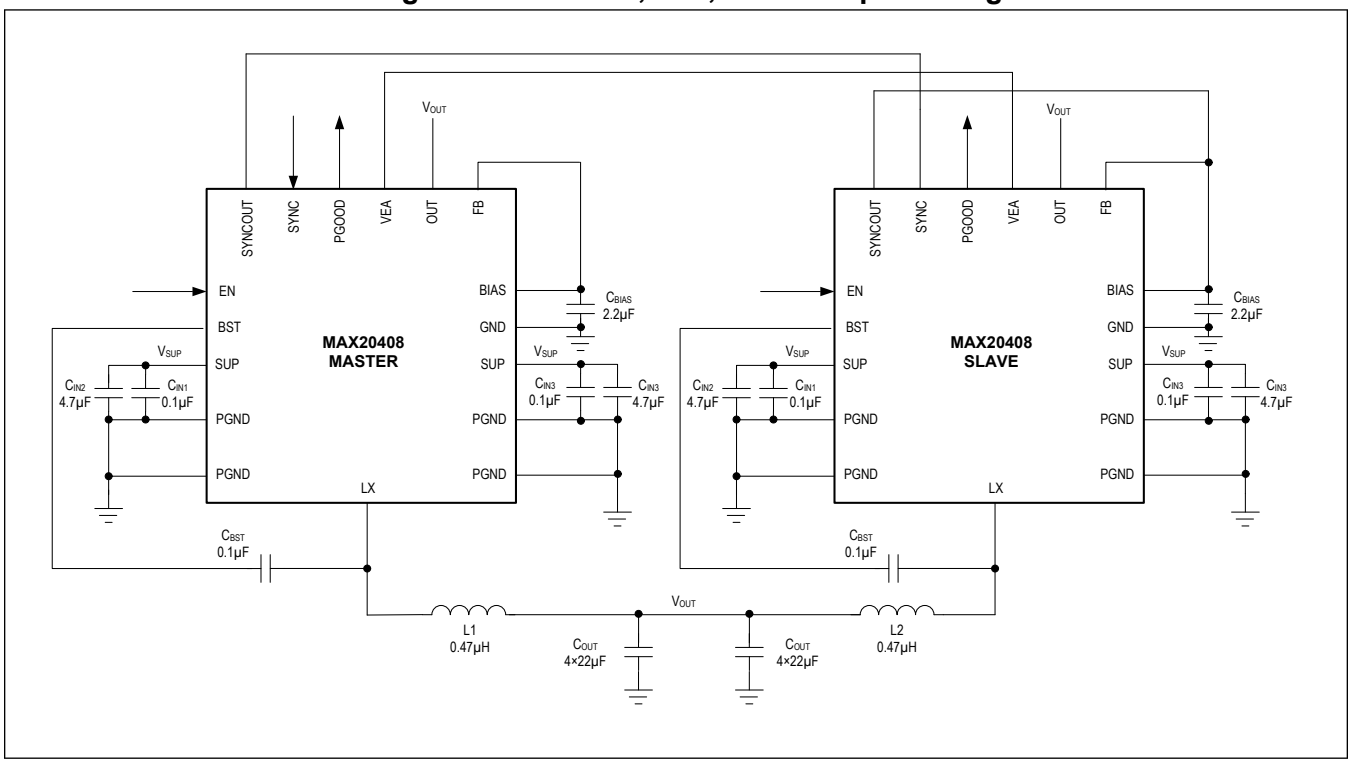
Typical Application Circuits (continued)

MAX20410 Configuration: 400kHz, 10A, Adjustable Output Voltage



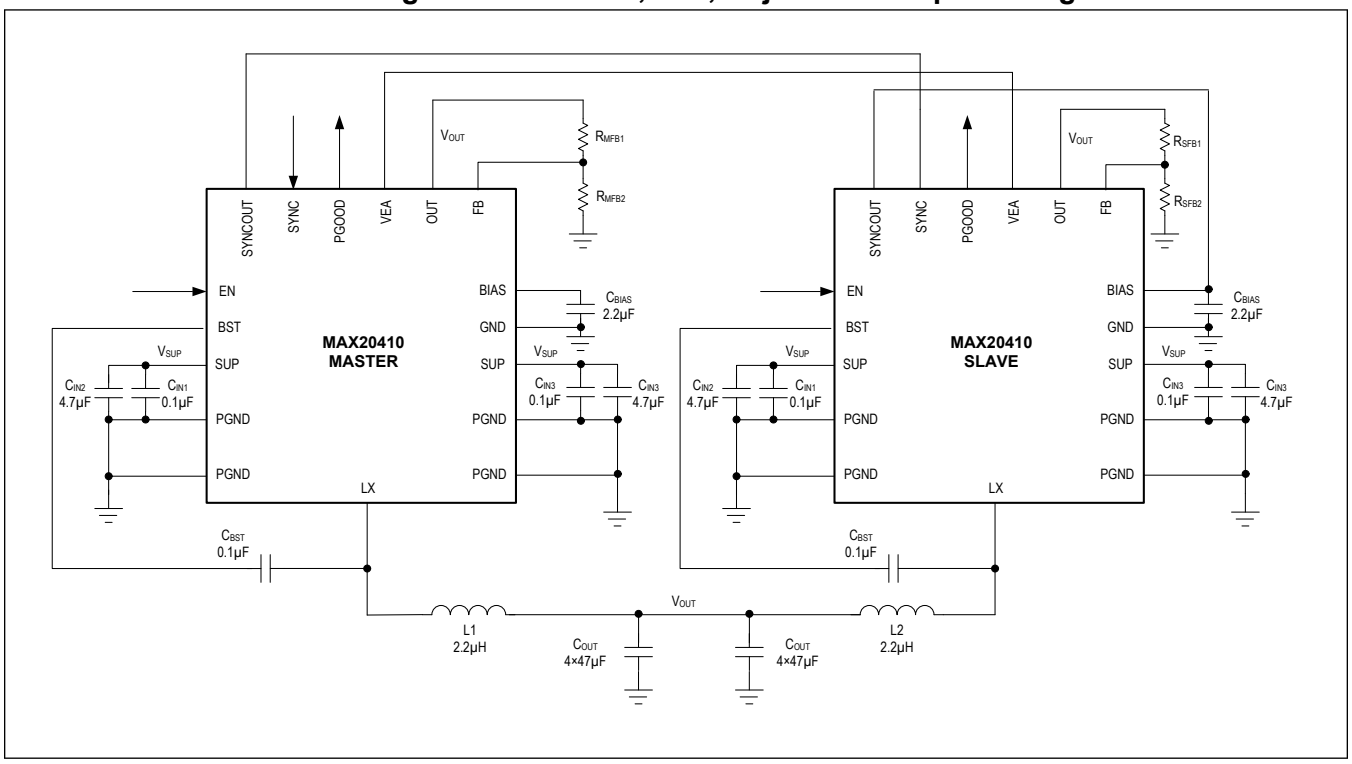
Typical Application Circuits (continued)

MAX20408 Dual-Phase Configuration: 2.1MHz, 16A, Fixed Output Voltage



Typical Application Circuits (continued)

MAX20410 Dual-Phase Configuration: 400kHz, 20A, Adjustable Output Voltage



Ordering Information

PART NUMBER	FIXED V_{OUT} (V)	ADJUSTABLE V_{OUT} (V)	MAXIMUM OPERATING CURRENT (A)	FREQUENCY (kHz)	SPREAD-SPECTRUM
MAX20408AFOA/VY+	5	0.8 to 6	8	2100	OFF
MAX20408AFOB/VY+**	3.3	0.8 to 6	8	2100	OFF
MAX20408AFOC/VY+	5	0.8 to 6	8	2100	ON
MAX20408AFOD/VY+	3.3	0.8 to 6	8	2100	ON
MAX20408AFOE/VY+	4	0.8 to 6	8	2100	ON
MAX20408AFOF/VY+	5	0.8 to 10	8	400	ON
MAX20408AFOG/VY+	3.3	0.8 to 10	8	400	ON
MAX20410AFOA/VY+	5	0.8 to 10	10	400	OFF
MAX20410AFOB/VY+	3.3	0.8 to 10	10	400	OFF
MAX20410AFOC/VY+	5	0.8 to 10	10	400	ON
MAX20410AFOD/VY+**	3.3	0.8 to 10	10	400	ON
MAX20410AFOE/VY+**	5	0.8 to 6	10	2100	ON
MAX20410AFOF/VY+**	3.3	0.8 to 6	10	2100	ON

For variants with different options, contact the factory.

*** Future product - contact the factory for availability.*

/VY+ denotes a side-wettable, automotive-qualified package.

/V denotes an AEC-Q100, automotive-qualified part.

+ denotes a lead(Pb)-free/RoHS-compliant package.

T denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/21	Release for Market Intro	—
1	6/21	Updated the *Absolute Maximum Ratings* table and added *Table 1* for Component Selection	5, 16
2	8/21	Updated *Ordering Information* table	24
3	9/21	Updated *Ordering Information* table	24
4	1/22	Added *Dual-Phase Operation, Low-Iq Operation in Dual-Phase* Sections, and *Table 1. Configurations for Low-Iq Operation*, Updated *Ordering Information* table	16, 26
5	3/22	Updated *Ordering Information* table	26

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