*Click **here** to ask an associate for production status of specific part numbers.*

MAX20481

Four- to Seven-Input Automotive Power-System Monitor Family

General Description

The MAX20481 is a complete ASIL-compliant SoC power system monitor with up to seven voltage-monitor inputs. Each input has factory OTP programmable OV/UV thresholds of between 2.5% and 10% with ±1% accuracy. Two of the inputs have a separate remote ground-sense input for use with high-current SoC supplies.

The MAX20481 contains a factory-programmable windowed watchdog with digital input pins for both refreshing and disabling the watchdog. The $\overline{\text{RESET}}$ pin of the device can be set at the factory to assert under a variety of conditions.

The MAX20481 significantly reduces system size and component count while improving reliability compared to separate ICs or discrete components. The MAX20481 meets ASIL B reliability levels in a standalone application. The device is designed to operate from -40°C to +125°C ambient temperature.

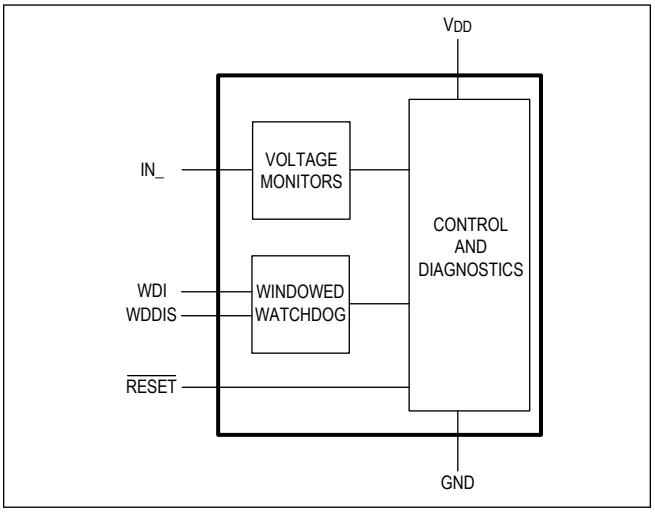
Applications

- ADAS
- Autonomous Driving Processing Systems
- Remote Sensor Modules
- Power System Supervision and MCU/SoC Montioring

Benefits and Features

- Small Solution
  - 2.35V to 5.50V Operating Supply Voltage
  - No External Components Needed
  - 150µA Operating Current
- High Precision
  - Selectable 102.5% to 110% OV Monitors
  - Selectable 97.5% to 90% UV Monitors
  - ±1% Accuracy
  - 0.5% Step Size
  - ASIL B Compliance
- Highly Integrated
  - Five Fixed-Voltage Monitoring Inputs
  - Two Differential-Voltage Monitoring Inputs with Remote GND Sense
  - Windowed Watchdog with Disable Pin for SoC Programming
  - Error-Correcting Code (ECC) on Internal OTP
  - Factory-Programmable $\overline{\text{RESET}}$ Pin
- 16-Pin, Side-Wettable TQFN with Exposed Pad (3mm x 3mm)
- AEC-Q100 Qualified
- -40°C to +125°C Operating Temperature

Simplified Block Diagram



***Ordering Information** appears at end of data sheet.*

19-100608; Rev 6; 12/21

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Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V to +6V
IN1–IN5 to GND ..... -0.3V to +6V
INP6–INP7 to GND ..... -0.3V to +6V
INM to GND ..... -0.3V to 0.3V
$\overline{RESET}$ to GND ..... -0.3V to +6V
WDI to GND ..... -0.3V to +6V
WDDIS to GND ..... -0.3V to VDD + 0.3V

Continuous Power Dissipation (T_A = +70°C)
16-TQFN (derate 22.5mW/°C > 70°C) 1797.8mW
Operating Temperature ..... -40°C to +125°C
Junction Temperature ..... +150ºC
Storage Temperature Range ..... -65ºC to +150ºC
Lead Temperature Range ..... +300ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16-TQFN-EP

Package Code	T1633Y+5
Outline Number	21-100150
Land Pattern Number	90-100064
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	44.5°C/W
Junction to Case (θ_{JC})	5.9°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted, Typical values are at T_A = 25°C under normal conditions, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Fully operational	2.35		5.5	V
		$\overline{RESET}$ output guaranteed low	1.2			
UVLO	V_{UVLO}	V_{DD} Voltage Rising	1.85	2.05	2.25	V
		V_{DD} Voltage Falling	1.75	1.95	2.15	
Internal Oscillator	f_{OSC}		1.15	1.28	1.40	MHz
IN1–IN4						
Input Current	$I_{IN\_}$	$V_{IN\_}$ ≤ 3.3V		1	1.5	µA
Set-Point Range			0.5		3.6875	V
Set-Point Resolution		12.5mV/step		8		Bits
OV/UV Threshold Range			2.5		10	%
OV/UV Threshold Resolution		0.5%/step		4		Bits

Electrical Characteristics (continued)

(V_{DD} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted, Typical values are at T_A = 25°C under normal conditions, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OV/UV Threshold Accuracy		(IN1 through IN4) ≥ 1.0V. Factory-trimmed thresholds.	-1		1	%
		(IN1 through IN4) < 1.0V. Factory-trimmed thresholds.	-10		10	mV
OFF Threshold	V_{OFF}	(IN1 through IN4) voltage falling	0.23	0.25	0.27	V
		(IN1 through IN4) voltage rising	0.28	0.3	0.32	
UV Comparator Filter Time	t_{UV}	2% below threshold		5		µs
OV Comparator Filter Time	t_{OV}	2% above threshold		5		µs
IN5						
Input Current	I_{IN5}	V_{IN5} ≤ 5V		1.5	2.3	µA
Set-Point Range			0.5		5.5	V
Set-Point Resolution		20mV/step		8		Bits
OV/UV Threshold Resolution		0.5%/step		4		Bits
OV/UV Threshold Accuracy		IN5 ≥ 1.0V. Factory-trimmed thresholds.	-1		1	%
		IN5 < 1.0V. Factory-trimmed thresholds.	-10		10	mV
OFF Threshold	V_{OFF}	IN5 voltage falling	0.23	0.25	0.27	V
		IN5 voltage rising	0.28	0.3	0.32	
UV Comparator Filter Time	t_{UV}	2% below threshold		5		µs
OV Comparator Filter Time	t_{OV}	2% above threshold		5		µs
OV/UV Threshold Range			2.5		10	%
IN6P–IN7P, INM						
INM Range	V_{INM}		-0.1		0.1	V
Input Current	$I_{IN\_}$	$V_{IN\_}$ ≤ 1.8V		1.4	2.2	µA
Set-Point Range		Relative to INM	0.5		1.775	V
Set-Point Resolution		5mV/step		8		Bits
Set-Point Accuracy		(IN6P, IN7P) ≥ 1.0V	-1		1	%
		(IN6P, IN7P) < 1.0V	-10		10	mV
OFF Threshold	V_{OFF}	(IN6P, IN7P) voltage falling, relative to INM	0.23	0.25	0.27	V
		(IN6P, IN7P) voltage rising, relative to INM	0.28	0.3	0.32	
UV Comparator Filter Time	t_{UV}	2% below threshold		5		µs
OV Comparator Filter Time	t_{OV}	2% above threshold		5		µs

Electrical Characteristics (continued)

(V_{DD} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted, Typical values are at T_A = 25°C under normal conditions, unless otherwise noted. (Note 1)

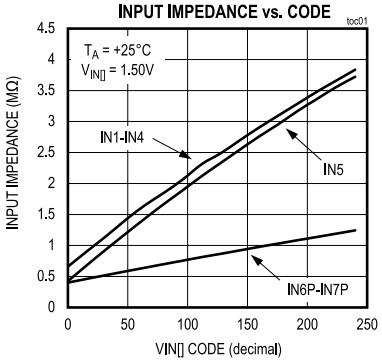
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WDI, WDDIS INPUTS						
Input High Level	V_{IH}	Input Voltage Rising	1.3			V
Input Low Level	V_{IL}	Input Voltage Falling			0.4	V
Hysteresis				0.1		V
DIGITAL OUTPUT ($\overline{RESET}$)						
Digital Output Low Level	V_{RL}	V_{DD} = 2.35V, I_{SINK} = 2mA			0.2	V
Digital Output Leakage	I_{R-LKG}	$\overline{RESET}$ = 5.0V			1	µA
Active Timeout Period	t_{HOLD}	RHLD[1:0] = 00		6		µs
		RHLD[1:0] = 01	7.2	8	8.8	ms
		RHLD[1:0] = 10	14.4	16	17.6	
		RHLD[1:0] = 11	28.8	32	35.2	

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

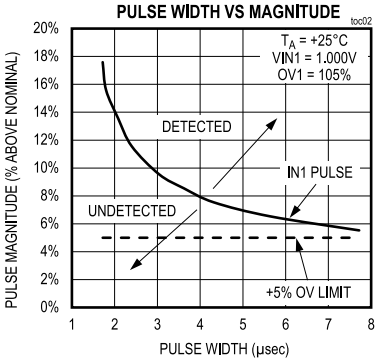
Typical Operating Characteristics

(V_{DD} = 3.3V, T_A = +25°C)

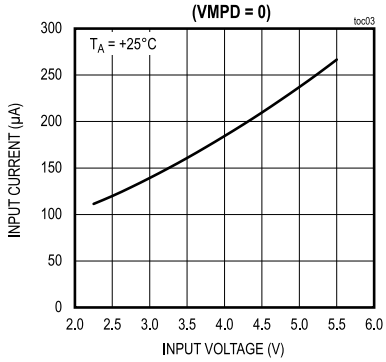
INPUT IMPEDANCE vs. CODE



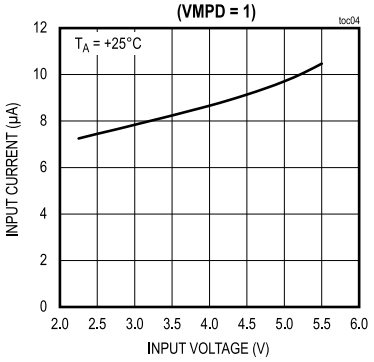
IN[] VOLTAGE PULSE THRESHOLD OF DETECTION PULSE WIDTH VS MAGNITUDE



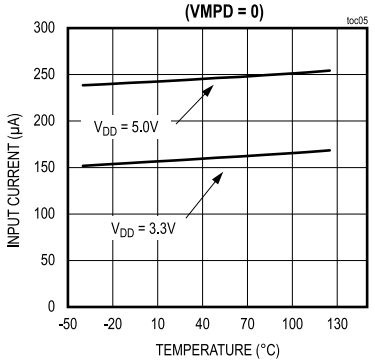
SUPPLY CURRENT vs. VOLTAGE NORMAL MODE (VMPD = 0)



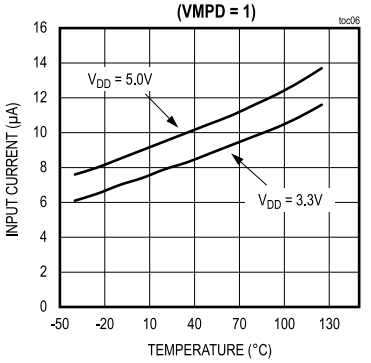
SUPPLY CURRENT vs. VOLTAGE POWER-DOWN MODE (VMPD = 1)



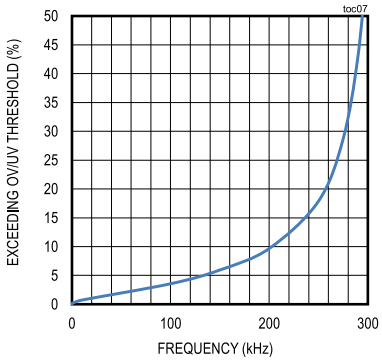
SUPPLY CURRENT vs. TEMP NORMAL MODE (VMPD = 0)



SUPPLY CURRENT vs. TEMP POWER-DOWN MODE (VMPD = 1)

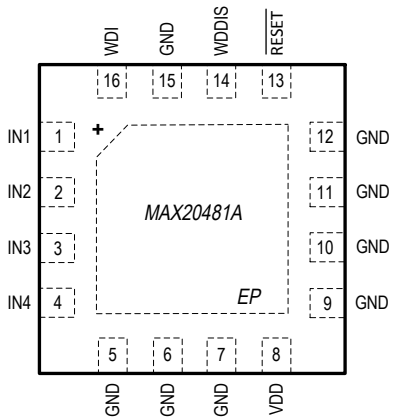


OV/UV FREQUENCY RESPONSE

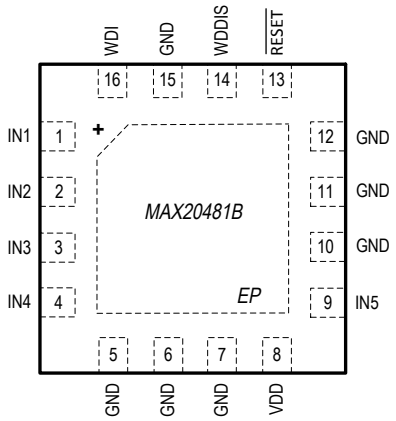


Pin Configurations

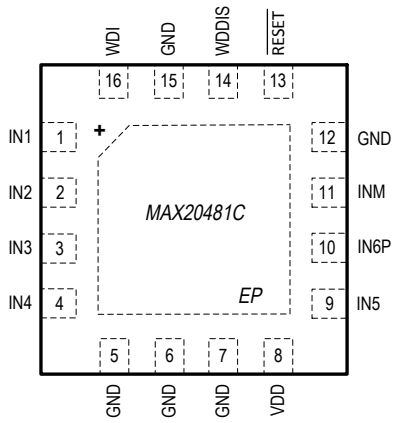
MAX20481A: 4-Channel Monitor



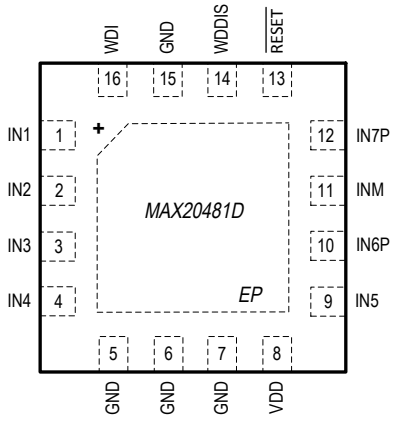
MAX20481B: 5-Channel Monitor



MAX20481C: 6-Channel Monitor



MAX20481D: 7-Channel Monitor



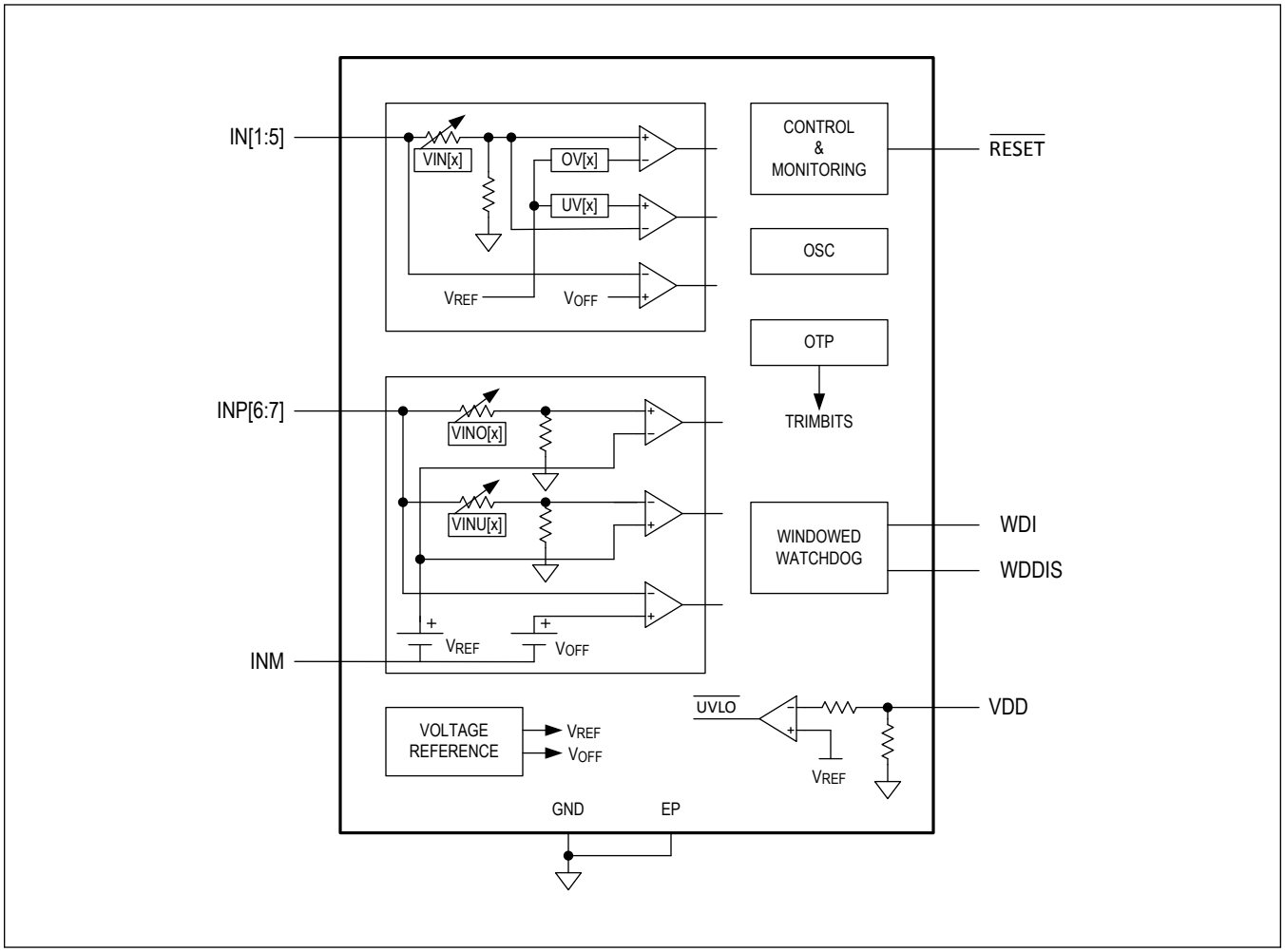
Pin Description

PIN				NAME	FUNCTION
MAX20481A	MAX20481B	MAX20481C	MAX20481D		
MAX20481					
1	1	1	1	IN1	Input Voltage Monitor 1
2	2	2	2	IN2	Input Voltage Monitor 2
3	3	3	3	IN3	Input Voltage Monitor 3
4	4	4	4	IN4	Input Voltage Monitor 4
5, 6, 7	5, 6, 7	5, 6, 7	5, 6, 7	GND	Ground. Connect all grounds together at the EP.

Pin Description (continued)

PIN				NAME	FUNCTION
MAX20481A	MAX20481B	MAX20481C	MAX20481D		
8	8	8	8	VDD	Input Supply Voltage. Connect a 0.1µF capacitor between V_{DD} and GND and place close to the IC.
9	-	-	-	GND	Ground. Connect all grounds together at the EP.
-	9	9	9	IN5	Input Voltage Monitor 5
10	10	-	-	GND	Ground. Connect all grounds together at the EP.
–	–	10	10	IN6P	Differential Input Voltage Monitor 6
11	11	–	–	GND	Ground. Connect all grounds together at the EP.
–	–	11	11	INM	Common Negative Input for Voltage Monitors 6 and 7.
12	12	12	–	GND	Ground. Connect all grounds together at the EP.
–	–	–	12	IN7P	Differential Input Voltage Monitor 7
13	13	13	13	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output. Open-drain output that signals a status change. Can be mapped to any combination of input monitors to indicate that they are within nominal operating range. Connect to logic supply with a pullup resistor.
14	14	14	14	WDDIS	Watchdog Disable. Connect to GND to enable windowed watchdog. Connect to V_{DD} to disable watchdog.
15	15	15	15	GND	Ground. Connect all grounds together at the EP.
16	16	16	16	WDI	Watchdog Input. A low-to-high transition will refresh the watchdog. This pin is only available on the MAX20481 version.
-	-	-	-	EP	Exposed Pad. Connect to ground. Does not serve as a substitute for a proper GND pin connection.

Functional Diagrams



Detailed Description

The MAX20481 is an ASIL B-compliant SoC power-system monitor. It has up to 7 channels voltage monitors to supervise system power rails, and a windowed watchdog for SoC/MCU monitoring. The system features numerous checks and redundancies to maintain a high performance level and meet ASIL B reliability specifications.

Voltage Monitor

The MAX20481 IC has up to seven voltage-monitor channels available for system power rails. Five of the monitors have single-ended inputs. For these channels, a nominal voltage is set first and OV/UV thresholds (as a percentage of that nominal voltage setting) are set second. The remaining two monitors have differential inputs and share a remote ground-sense pin (INM). Unlike the other monitors, which have a nominal voltage + %OV/UV configuration, the two differential inputs have completely independent OV and UV comparators. Each comparator can be configured with a separate reference voltage.

Monitor channels IN1 through IN5 have the single-ended configuration, with OV/UV thresholds independently configurable from ±2.5% to ±10% in 0.5% steps. IN1 through IN4 have a nominal voltage set-point range of 0.50V to 3.6875V, while IN5 has an extended range of 0.50V to 5.50V. IN6P and IN7P have the differential configuration. Their OV and UV set points can range from 0.50V to 1.775V; these measurements are with respect to the voltage difference between the INxP supply and INM remote ground-sense pins. Every monitor channel also has an OFF comparator that asserts when the monitor input voltage falls below 0.25V (typ).

Modern SoCs and processors can require a large amount of supply current, which may cause small offsets in ground voltages (even when using multiple large ground planes). To account for this when using the differential channels, route the INM pin separately from ground and connect to a point near where the IN6P and IN7P lines are connected. If this feature is not necessary, the INM pin can be grounded directly at the IC. The comparators on the voltage monitors are designed to respond quickly for applications that require rapid response to voltage fluctuations. If a slower response is desired, an RC filter can be added between the IC pin and the monitored voltage rail. If an RC filter is implemented, the value of the resistor should be kept low to avoid artificial voltage shift at the IC pins. Because each IN_ pin draws a few microamperes of current, the filter resistor value should be 1kΩ or less.

Windowed Watchdog and Reset Control

The IC also contains a windowed watchdog for external SoC monitoring. The closed and open windows are independently configurable, as well as the main watchdog clock (which can range from 200µs/tick to 12.8ms/tick). Because the watchdog is meant to supervise a processor system, it features an extended first-update window: when the IC $\overline{\text{RESET}}$ pin deasserts, the watchdog window is immediately opened and extended to provide extra time for an SoC to finish any boot sequences before being required to update the watchdog. (The specific length of the extended first-update window is configurable as well.) The watchdog is refreshed through a dedicated pin on the IC (the WDI pin). A low-to-high transition triggers a refresh of the watchdog. For system programming at the factory, there is also an active-high watchdog disable pin (WDDIS). Pulling the pin high disables the watchdog functionality while leaving the voltage monitors fully active. The watchdog will trigger an error signal on both too-early or too-late update faults. It can be configured to assert $\overline{\text{RESET}}$ on every update violation, or only after encountering two consecutive violations. The watchdog is inactive while the $\overline{\text{RESET}}$ pin is asserted low (for any fault condition).

Watchdog Window Settings

A regular watchdog window consists of two parts: an initial (closed) window during which updates are not allowed, and a second (open) window during which updates are accepted. For a given watchdog clock rate t_{WDCLK} (set according to the WDCDIV register), the two window lengths are as follows:

$t_{CLO} = t_{WDCLK} \times 8 \times$ WDCFG1.CLO[3 : 0]

$t_{OPN} = t_{WDCLK} \times 8 \times$ WDCFG1.OPN[3 : 0]

If a refresh is sent to the IC during the closed window, the IC asserts a fault and restarts the watchdog once RESET deasserts. When the IC receives a valid refresh, it will immediately transition to a new closed window. It will not finish the existing open window. The first cycle encountered once the watchdog starts (either on power-on reset or once $\overline{\text{RESET}}$ deasserts) is different from the typical closed/open cycle. It has no closed window, and is longer than a normal cycle.

This is to allow for an SoC or MCU to run through a boot sequence that may take longer than the usual watchdog cycle. The length of the first update window is an odd multiple of the sum of the normal closed and open windows: $t_{1UD} = (t_{OPN} + t_{CLO}) \times (1 + 2 \times WDCFG2.1UD[2 : 0])$

$\overline{\text{RESET}}$ Output

The device features an open-drain interrupt/reset output that asserts low when any mapped fault conditions occur. $\overline{\text{RESET}}$ remains asserted for a fixed timeout period after all triggering fault conditions are removed. The fixed timeout period can be set to 6µs, 8ms, 16ms, or 32ms. The $\overline{\text{RESET}}$ pin works as an open-drain output. To obtain a logic signal, place a pullup resistor between the $\overline{\text{RESET}}$ pin and system I/O voltage (10kΩ to 100kΩ recommended for reduced current consumption). Mapping of this pin to selected fault sources is fully programmable.

Register Map

Top Level

ADDRESS	NAME	MSB							LSB
General Configuration									
0x01	CONFIG1[7:0]	–	–	–	–	–	–	MBST	–
Voltage Monitor System									
0x04	RSTMAP[7:0]	PARM	IN7	IN6	IN5	IN4	IN3	IN2	IN1
0x08	VIN1[7:0]	D[7:0]							
0x09	VIN2[7:0]	D[7:0]							
0x0A	VIN3[7:0]	D[7:0]							
0x0B	VIN4[7:0]	D[7:0]							
0x0C	VIN5[7:0]	D[7:0]							
0x0D	VINO6[7:0]	D[7:0]							
0x0E	VINU6[7:0]	D[7:0]							
0x0F	VINO7[7:0]	D[7:0]							
0x10	VINU7[7:0]	D[7:0]							
0x11	OVUV1[7:0]	OV[3:0]				UV[3:0]			
0x12	OVUV2[7:0]	OV[3:0]				UV[3:0]			
0x13	OVUV3[7:0]	OV[3:0]				UV[3:0]			
0x14	OVUV4[7:0]	OV[3:0]				UV[3:0]			
0x15	OVUV5[7:0]	OV[3:0]				UV[3:0]			
Watchdog and $\overline{\text{RESET}}$ Control									
0x27	WDCDIV[7:0]	–	–	WDIV[5:0]					
0x28	WDCFG1[7:0]	CLO[3:0]				OPN[3:0]			
0x29	WDCFG2[7:0]	–	–	–	–	WDEN	1UD[2:0]		
0x2C	RSTCTRL[7:0]	–	–	–	–	–	MR1	RHLD[1:0]	

Register Details

CONFIG1 (0x01)

Configuration Register 1

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MBST	–
Reset	–	–	–	–	–	–	OTP	–
Access Type	–	–	–	–	–	–	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
MBST	1	Built-In Self-Test Mapping. When set, any comparator that fails BIST will cause the $\overline{\text{RESET}}$ pin to be asserted.	0: BIST for OV/UV/OFF comparators not mapped to $\overline{\text{RESET}}$ pin 1: BIST for OV/UV/OFF comparators mapped to $\overline{\text{RESET}}$ pin

RSTMAP (0x4)

Interrupt Mapping

BIT	7	6	5	4	3	2	1	0
Field	PARM	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Reset	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PARM	7	Parity $\overline{\text{RESET}}$ Mapping. Defines whether or not a parity check failure will assert the $\overline{\text{RESET}}$ pin.	0: Parity faults are not mapped to the $\overline{\text{RESET}}$ pin. 1: Any parity fault will cause the $\overline{\text{RESET}}$ pin to be asserted.
IN7	6	$\overline{\text{RESET}}$ Mapping. Defines whether or not OV/UV assertions will cause the $\overline{\text{RESET}}$ pin to trigger.	0: OV/UV faults are not mapped to the $\overline{\text{RESET}}$ pin. 1: OV/UV faults are mapped to the $\overline{\text{RESET}}$ pin.
IN6	5	$\overline{\text{RESET}}$ Mapping. Defines whether or not OV/UV assertions will cause the $\overline{\text{RESET}}$ pin to trigger.	0: OV/UV faults are not mapped to the $\overline{\text{RESET}}$ pin. 1: OV/UV faults are mapped to the $\overline{\text{RESET}}$ pin.
IN5	4	$\overline{\text{RESET}}$ Mapping. Defines whether or not OV/UV assertions will cause the $\overline{\text{RESET}}$ pin to trigger.	0: OV/UV faults are not mapped to the $\overline{\text{RESET}}$ pin. 1: OV/UV faults are mapped to the $\overline{\text{RESET}}$ pin.
IN4	3	$\overline{\text{RESET}}$ Mapping. Defines whether or not OV/UV assertions will cause the $\overline{\text{RESET}}$ pin to trigger.	0: OV/UV faults are not mapped to the $\overline{\text{RESET}}$ pin. 1: OV/UV faults are mapped to the $\overline{\text{RESET}}$ pin.
IN3	2	$\overline{\text{RESET}}$ Mapping. Defines whether or not OV/UV assertions will cause the $\overline{\text{RESET}}$ pin to trigger.	0: OV/UV faults are not mapped to the $\overline{\text{RESET}}$ pin. 1: OV/UV faults are mapped to the $\overline{\text{RESET}}$ pin.
IN2	1	$\overline{\text{RESET}}$ Mapping. Defines whether or not OV/UV assertions will cause the $\overline{\text{RESET}}$ pin to trigger.	0: OV/UV faults are not mapped to the $\overline{\text{RESET}}$ pin. 1: OV/UV faults are mapped to the $\overline{\text{RESET}}$ pin.
IN1	0	$\overline{\text{RESET}}$ Mapping. Defines whether or not OV/UV assertions will cause the $\overline{\text{RESET}}$ pin to trigger.	0: OV/UV faults are not mapped to the $\overline{\text{RESET}}$ pin. 1: OV/UV faults are mapped to the $\overline{\text{RESET}}$ pin.

VIN1 (0x8)

IN1 Nominal Voltage Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	Nominal Rail Voltage	V_{NOM} = 500mV + 12.5mV x D[7:0] (0.5V to 3.6875V)

VIN2 (0x9)

IN2 Nominal Voltage Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	Nominal Rail Voltage	V_{NOM} = 500mV + 12.5mV x D[7:0] (0.5V to 3.6875V)

VIN3 (0xA)

IN3 Nominal Voltage Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	Nominal Rail Voltage	V_{NOM} = 500mV + 12.5mV x D[7:0] (0.5V to 3.6875V)

VIN4 (0xB)

IN4 Nominal Voltage Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	Nominal Rail Voltage	V_{NOM} = 500mV + 12.5mV x D[7:0] (0.5V to 3.6875V)

VIN5 (0xC)

IN5 Nominal Voltage Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	Nominal Rail Voltage	V_{NOM} = 500mV + 20mV x D[7:0] (0.5V to 5.6V)

VINO6 (0xD)

IN6 Overvoltage Threshold Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	OV Threshold	V_{OV6} = 500mV + 5mV x D[7:0] (0.5V to 1.775V)

VINU6 (0xE)

IN6 Undervoltage Threshold Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	UV Threshold	V_{UV6} = 500mV + 5mV x D[7:0] (0.5V to 1.775V)

VINO7 (0xF)

IN7 Overvoltage Threshold Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	OV Threshold	V_{OV7} = 500mV + 5mV x D[7:0] (0.5V to 1.775V)

VINU7 (0x10)

IN7 Undervoltage Threshold Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	UV Threshold	V_{UV7} = 500mV + 5mV x D[7:0] (0.5V to 1.775V)

OVUV1 (0x11)

IN1 Overvoltage and Undervoltage Thresholds

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	IN1 Overvoltage Threshold	OV (%) = 102.5% + 0.5% x OV[3:0]
UV	3:0	IN1 Undervoltage Threshold	UV (%) = 97.5% - 0.5% x UV[3:0]

OVUV2 (0x12)

IN2 Overvoltage and Undervoltage Thresholds

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	IN2 Overvoltage Threshold	OV (%) = 102.5% + 0.5% x OV[3:0]
UV	3:0	IN2 Undervoltage Threshold	UV (%) = 97.5% - 0.5% x UV[3:0]

OVUV3 (0x13)

IN3 Overvoltage and Undervoltage Thresholds

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	IN3 Overvoltage Threshold	OV (%) = 102.5% + 0.5% x OV[3:0]
UV	3:0	IN3 Undervoltage Threshold	UV (%) = 97.5% - 0.5% x UV[3:0]

OVUV4 (0x14)

IN4 Overvoltage and Undervoltage Thresholds

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	IN4 Overvoltage Threshold	OV (%) = 102.5% + 0.5% x OV[3:0]
UV	3:0	IN4 Undervoltage Threshold	UV (%) = 97.5% - 0.5% x UV[3:0]

OVUV5 (0x15)

IN5 Overvoltage and Undervoltage Thresholds

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	IN5 Overvoltage Threshold	OV (%) = 102.5% + 0.5% x OV[3:0]
UV	3:0	IN5 Undervoltage Threshold	UV (%) = 97.5% - 0.5% x UV[3:0]

WDCDIV (0x27)

Watchdog Mode and Clock Divider

BIT	7	6	5	4	3	2	1	0
Field	–	–	WDIV[5:0]					
Reset	–	–	OTP					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
WDIV	5:0	Watchdog Clock Divider. The main oscillator is divided by 32 and supplied to the watchdog subsystem. This field controls further dividing of the clock.	t_{WDCLK} = (WDIV[5:0] + 1) x 25µs x 8

WDCFG1 (0x28)

Watchdog Configuration Register 1

BIT	7	6	5	4	3	2	1	0
Field	CLO[3:0]				OPN[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CLO	7:4	Watchdog Closed Window. Sets the length of the first portion of a watchdog period, where updates are rejected.	t_{CLO} = (CLO[3:0] + 1) x 8 x t_{WDCLK}
OPN	3:0	Watchdog Open Window. Sets the length of the second portion of a watchdog period, where updates are accepted.	t_{OPN} = (OPN[3:0] + 1) x 8 x t_{WDCLK}

WDCFG2 (0x29)

Watchdog Configuration Register 2

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	WDEN	1UD[2:0]		
Reset	–	–	–	–	OTP	OTP		
Access Type	–	–	–	–	Read Only	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
WDEN	3		
1UD	2:0	First Update Extension. Sets the length of the first open window after $\overline{\text{RESET}}$ deassertion.	$t_{1OPN} = (t_{CLO} + t_{OPN}) \times (1UD[2:0] \times 2 + 1)$

RSTCTRL (0x2C)

$\overline{\text{RESET}}$ Control

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MR1	RHLD[1:0]	
Reset	–	–	–	–	–	OTP	OTP	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MR1	2	Watchdog Violation Count for $\overline{\text{RESET}}$ Assertion. This determines whether the $\overline{\text{RESET}}$ pin is asserted on any single watchdog violation, or after two consecutive violations.	0: $\overline{\text{RESET}}$ will assert after any watchdog violation. 1: $\overline{\text{RESET}}$ will assert only after two consecutive violations. Valid updates will reset the violation counter if one violation has been encountered.
RHLD	1:0	$\overline{\text{RESET}}$ Hold/Active Timeout Time. This is the amount of time that the $\overline{\text{RESET}}$ pin remains low after the removal of any event that would cause the $\overline{\text{RESET}}$ pin to assert low.	00: 0ms (6µs typ, used for interrupt-style functionality) 01: 8ms 10: 16ms 11: 32ms

Applications Information

Diagnostics

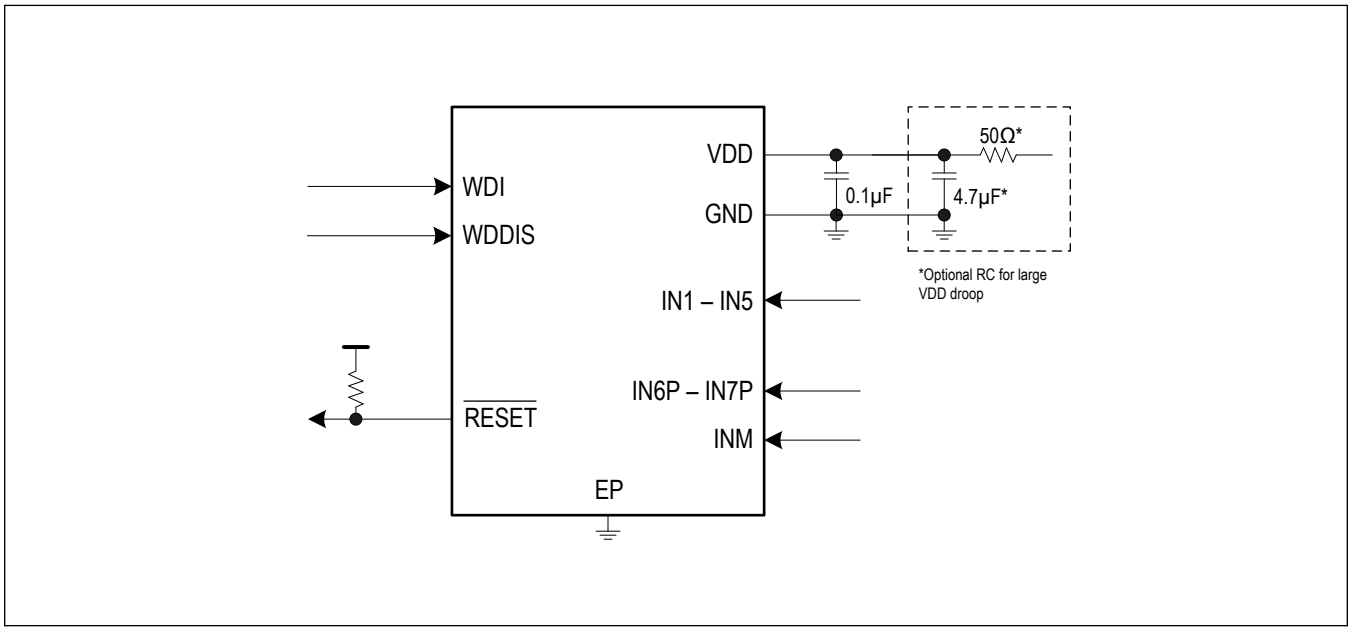
The MAX20481 is ASIL B-compliant in a standalone monitor role. In addition to out-of-bounds voltage rails and watchdog faults, the IC can also use the $\overline{\text{RESET}}$ pin to communicate various internal faults, including register parity-check failures, oscillator faults, and comparator BIST results. Internal OTP configuration information is protected by an automatic single-error-correcting coding scheme. For full safety-related information, contact Maxim Integrated.

Table 1. Diagnostics

FAULT	DIAGNOSTIC COVERAGE
Short to GND/V_{DD} on IN[x] pins	OV/UV comparators assert depending on voltage
Open on IN[x] pins	UV/OFF comparators assert
IN[x] comparator fault	Built-in self-test operates at power-on and can communicate faults through $\overline{\text{RESET}}$ pin
Short to GND on V_{DD} pin	$\overline{\text{RESET}}$ is pulled low (if connected to same supply as IC)
Open on V_{DD} pin	Can be detected through host-induced test
Open GND pin	$\overline{\text{RESET}}$ can still assert down to one body diode above system ground. Persistent UV conditions will occur if monitored rails are operational.
Short to V_{DD} on $\overline{\text{RESET}}$	Can be detected through host-induced test
Open on $\overline{\text{RESET}}$ pin	Can be detected through host-induced test
Internal watchdog block failure	Can be detected through host-induced test

Typical Application Circuits

Circuit 1



Ordering Information

PART	Ch1 (V)	Ch2 (V)	Ch3 (V)	Ch4 (V)	CH5 (V)	Ch6 OV (V)	Ch6 UV (V)	Ch7 OV (V)	Ch7 UV (V)
MAX20481AATEB/VY+*	1.8000	2.8000	0.5000	0.5000	—	—	—	—	—
MAX20481AATEC/VY+	3.3000	1.8000	1.1500	0.5000	—	—	—	—	—
MAX20481BATEA/VY+	1.0250	1.8000	1.3500	3.3000	1.2000	—	—	—	—
MAX20481CATEA/VY+	3.300	1.8000	2.5000	0.5000	1.1000	1.0050	0.8350	—	—

Y denotes a side-wettable package.

/V+ denotes an automotive-qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Future product—contact factory for availability.*

For variants with different options, contact the factory.

Devices are also available in tape-and-reel packaging. Specify tape and reel by adding "T" to the part number when ordering.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/19	Initial release	—
1	8/19	Added *Typical Operating Characteristics*	7
2	1/20	Updated *General Description*, *Benefits and Features*, *Pin Configurations*, and *Detailed Description*	1, 8, 9, 13
3	9/20	Updated *Electrical Characteristics* and *Functional Diagrams*	6, 11
4	5/21	Updated *Package Information*	3
5	6/21	Updated *Ordering Information* table	13
6	12/21	Added Register Map, *ASIL Diagnostics* section, and MAX20481BATEA/VY+ to *Ordering Information* table	14–20, 21, 22