*MAXIM*

# 3.3GHz to 3.9GHz
# Wireless Broadband RF Transceiver

**MAX2838**

## General Description

The MAX2838 direct-conversion, zero-IF, RF transceiver is designed specifically for 3.3GHz to 3.9GHz wireless broadband systems. The MAX2838 completely integrates all circuitry required to implement the RF transceiver function, providing RF-to-baseband receive path, baseband-to-RF transmit path, VCO, frequency synthesizer, and baseband/control interface. The device includes a fast-settling sigma-delta RF synthesizer with smaller than 29Hz frequency steps. The MAX2838 supports 2Tx, 2Rx MIMO applications with a master device providing coherent LO to the slave device. The transceiver IC also integrates circuits for on-chip DC-offset cancellation, I/Q error, and carrier-leakage detection circuits. Only an RF bandpass filter (BPF), TCXO, RF switch, PA, and a small number of passive components are needed to form a complete wireless broadband RF radio solution.

The MAX2838 completely eliminates the need for an external SAW filter by implementing on-chip monolithic filters for both the receiver and transmitter. The baseband filters along with the Rx and Tx signal paths are optimized to meet the stringent noise figure and linearity specifications. The device supports up to 2048-FFT OFDM and implements programmable channel filters for 1.5MHz to 28MHz RF channel bandwidths. The transceiver requires only 2μs Tx-Rx switching time. The IC is available in a small 48-pin thin QFN package measuring only 6mm x 6mm x 0.8mm.

## Applications

802.16-2004/802.16d Fixed WiMAX™

802.16e MIMO Mobile WiMAX

WiMAX Pico and Femto Basestations

NLOS Wireless Broadband Systems

*WiMAX is a trademark of the WiMAX Forum.*
*SPI is a trademark of Motorola, Inc.*

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX2838ETM+T | -40°C to +85°C | 48 TQFN-EP* |

*EP = Exposed paddle.*
*+Denotes a lead-free package.*
*T = Tape and reel.*

## Features

♦ **3.3GHz to 3.9GHz Wide-Band Operation**
♦ **Master-Slave Modes with Coherent LO for MIMO**
♦ **Complete RF Transceiver, and PA Driver**
  **0dBm Linear OFDM Transmit Power**
  **-70dBr Tx Spectral Emission Mask**
  **2.8dB Rx Noise Figure**
  **Tx/Rx I/Q Error and LO Leakage Detection and Adjustment**
  **Automatic Rx DC Offset Correction**
  **Monolithic Low-Noise VCO with -39dBc Integrated Phase Noise**
  **Programmable Rx I/Q Lowpass Channel Filters**
  **Programmable Tx I/Q Lowpass Anti-Aliasing Filter**
  **Sigma-Delta Fractional-N PLL with 29Hz Step Size**
  **60dB Tx Gain Control Range with 1dB Step Size, Digitally Controlled**
  **94dB Rx Gain Control Range with 2dB Step Size, Digitally Controlled**
  **60dB Analog RSSI Instantaneous Dynamic Range**
  **4-Wire SPI™ Digital Interface**
  **I/Q Analog Baseband Interface**
  **Digital Tx/Rx/Shutdown Mode Control**
  **Low-Power CLOCKOUT Mode**
  **On-Chip Digital Temperature Sensor Readout**
♦ **+2.7V to +3.6V Transceiver Supply**
♦ **Low-Power Shutdown Mode**
♦ **Small 48-Pin Thin QFN Package (6mm x 6mm x 0.8mm)**

## Pin Configuration
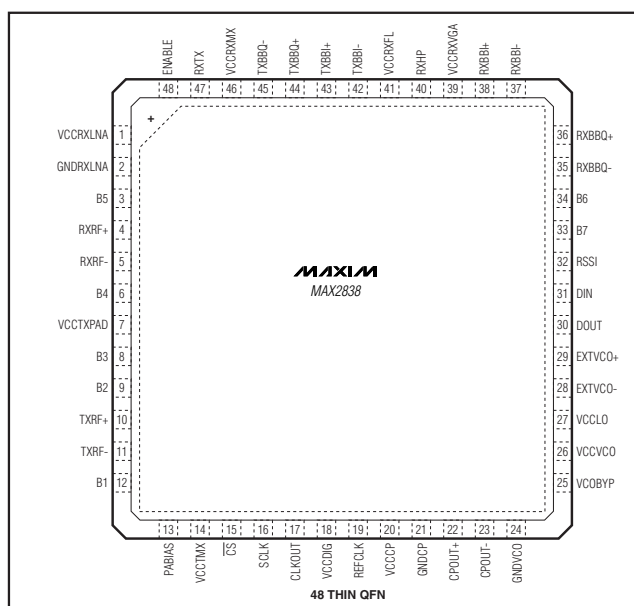


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# 3.3GHz to 3.9GHz Wireless Broadband RF Transceiver

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## ABSOLUTE MAXIMUM RATINGS

V<sub>CC_</sub> Pins to GND..................................................-0.3V to +3.6V

RF Inputs: RXRF+, RXRF-, EXTVCO+,
  EXTVCO- to GND ...............................................-0.3V to +3.6V

RF Outputs: TXRF+, TXRF-, EXTVCO+,
  EXTVCO- to GND ...............................................-0.3V to +3.6V

Analog Inputs: TXBBI+, TXBBI-, TXBBQ+,
  TXBBQ-, REFCLK to GND ...................................-0.3V to +3.6V

Analog Outputs: RXBBI+, RXBBI-, RXBBQ+,
  RXBBQ-, RSSI, VCOBYP, CPOUT+, CPOUT-,
  PABIAS to GND...................................................-0.3V to +3.6V

Digital Inputs: ENABLE, RXTX, $\overline{CS}$, SCLK,
  DIN, RXHP B1–B7 to GND .................................-0.3V to +3.6V

Digital Outputs: DOUT, CLKOUT to GND ............-0.3V to +3.6V

Short-Circuit Duration
  Analog Outputs: RXBBI+, RXBBI-, RXBBQ+,
    RSSI, VCOBYP,RXBBQ-, CPOUT+, CPOUT-,
    PABIAS, TXRF-, TXRF+ ....................................................10s
  Digital Outputs: DOUT, CLKOUT ........................................10s

RF Input Power: RXRF+, RXRF- ....................................+15dBm

RF Output Differential Load VSWR: TXRF+, TXRF- .................6:1

Continuous Power Dissipation (T<sub>A</sub> = +70°C)
  48-Pin Thin QFN (derate 37mW/°C above +70°C) ...... > 2.96W

Operating Temperature Range ..........................-40°C to +85°C

Junction Temperature.....................................................+150°C

Storage Temperature Range ............................-65°C to +160°C

Lead Temperature (soldering, 10s) ................................+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

⚠ **CAUTION!** ESD SENSITIVE DEVICE

## DC ELECTRICAL CHARACTERISTICS

(MAX2838 Evaluation Kit, V<sub>CC_</sub> = 2.7V to 3.6V, T<sub>A</sub> = -40°C to +85°C, ENABLE and RXTX set according to operating mode, $\overline{CS}$ = high, SCLK = DIN = low, transmitter and receiver in maximum gain, no input signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open. 90mV<sub>RMS</sub> differential I and Q signals (1MHz) applied to I and Q baseband inputs of transmitter in transmit mode, all registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at V<sub>CC</sub> = 2.8V, f<sub>LO</sub> = 3.6GHz, and T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 1)

| PARAMETERS | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | V<sub>CC_</sub> | | 2.7 | 2.8 | 3.6 | V |
| Supply Current | Shutdown mode | T<sub>A</sub> = +25°C | | 12 | | µA |
| | Standby mode, see Tables 1 and 2 | Single configuration | | 35 | 52 | mA |
| | | MIMO master configuration | | 44 | | |
| | | MIMO slave configuration | | 11 | | |
| | Rx mode, see Tables 1 and 2 | Single configuration | | 103 | 133 | |
| | | MIMO master configuration | | 112 | | |
| | | MIMO slave configuration | | 80 | | |
| | Tx mode, see Tables 1 and 2 | Single configuration | | 152 | 186 | |
| | | MIMO master configuration | | 160 | | |
| | | MIMO slave configuration | | 128 | | |
| | Rx calibration mode, see Tables 1 and 2 | Single configuration | | 142 | 182 | |
| | | MIMO master configuration | | 151 | | |
| | | MIMO slave configuration | | 119 | | |
| | Tx calibration mode, see Tables 1 and 2 | Single configuration | | 111 | 145 | |
| | | MIMO master configuration | | 120 | | |
| | | MIMO slave configuration | | 88 | | |
| Rx I/Q Output Common-Mode Voltage | D9:D8 = 00 in A4:A0 = 00100 | | 0.8 | 1.0 | 1.2 | V |
| | D9:D8 = 01 in A4:A0 = 00100 | | | 1.1 | | |
| | D9:D8 = 10 in A4:A0 = 00100 | | | 1.2 | | |
| | D9:D8 = 11 in A4:A0 = 00100 | | | 1.35 | | |

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## DC ELECTRICAL CHARACTERISTICS (continued)

(MAX2838 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, $T_A$ = -40°C to +85°C, ENABLE and RXTX set according to operating mode, $\overline{CS}$ = high, SCLK = DIN = low, transmitter and receiver in maximum gain, no input signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open. 90mV$_{RMS}$ differential I and Q signals (1MHz) applied to I and Q baseband inputs of transmitter in transmit mode, all registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at $V_{CC}$ = 2.8V, $f_{LO}$ = 3.6GHz, and $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETERS | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Tx Baseband Input Common-Mode Voltage Operating Range | DC-coupled | 0.5 | | 1.2 | V |
| Tx Baseband Input Bias Current | Source current | | 8 | 20 | µA |
| **LOGIC INPUTS: ENABLE, RXTX, SCLK, DIN, $\overline{CS}$, B1:B7, RXHP** | | | | | |
| Digital Input Voltage High, $V_{IH}$ | | $V_{CC}$ - 0.4 | | | V |
| Digital Input Voltage Low, $V_{IL}$ | | | | 0.4 | V |
| Digital Input Current High, $I_{IH}$ | | -1 | | +1 | µA |
| Digital Input Current Low, $I_{IL}$ | | -1 | | +1 | µA |
| **LOGIC OUTPUTS: DOUT** | | | | | |
| Digital Output Voltage High, $V_{OH}$ | Sourcing 100µA | $V_{CC}$ - 0.4 | | | V |
| Digital Output Voltage Low, $V_{OL}$ | Sinking 100µA | | | 0.4 | V |

## AC ELECTRICAL CHARACTERISTICS—Rx MODE

(MAX2838 Evaluation Kit, $V_{CC\_}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{RF}$ = 3.601GHz, receiver baseband I/Q outputs at 90mV$_{RMS}$, $f_{REF}$ = 40MHz, $\overline{CS}$ = ENABLE = RXTX = high, SCLK = DIN = low, channel bandwidth BW = 7MHz, with power matching for the RF inputs using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated. Rx I/Q differential output load impedance = 10kΩ ll 8pF.) (Note 1)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **RECEIVER SECTION: LNA RF INPUT TO BASEBAND I/Q OUTPUTS** | | | | | | |
| RF Input Frequency Range | | | 3.3 | | 3.9 | GHz |
| Peak-to-Peak Gain Variation over RF Input Frequency Range | Tested at band edges and band center | | | 1.8 | | dB |
| RF Input Return Loss | All LNA settings | | | 10 | | dB |
| Total Voltage Gain | $T_A$ = -40°C to +85°C | Maximum gain, B7:B1 = 0000000 | 88 | 98 | | dB |
| | | Minimum gain, B7:B1 = 1111111 | | 5 | 10 | |
| RF Gain Steps | From max RF gain to max RF Gain - 8dB | | | 8 | | dB |
| | From max RF gain to max RF gain - 16dB | | | 16 | | |
| | From max RF gain to max RF gain - 32dB | | | 32 | | |
| Gain Change Settling Time | Any RF or baseband gain change; gain settling to within ±1dB of steady state; RXHP = 1 | | | 200 | | ns |
| | Any RF or baseband gain change; gain settling to within ±0.1dB of steady state; RXHP = 1 | | | 500 | | |
| Baseband Gain Range | From maximum baseband gain (B5:B1 = 00000) to minimum baseband gain (B5:B1 = 11111) | | | 62 | | dB |
| Baseband Gain Minimum Step Size | | | | 2 | | dB |

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## AC ELECTRICAL CHARACTERISTICS—Rx MODE (continued)

(MAX2838 Evaluation Kit, $V_{CC\_}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{RF}$ = 3.601GHz, receiver baseband I/Q outputs at 90mV$_{RMS}$, $f_{REF}$ = 40MHz, $\overline{CS}$ = ENABLE = RXTX = high, SCLK = DIN = low, channel bandwidth BW = 7MHz, with power matching for the RF inputs using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated. Rx I/Q differential output load impedance = 10kΩ ll 8pF.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| DSB Noise Figure | Voltage gain ≥ 65dB with max RF gain (B7:B6 = 00) | | 2.9 | | dB |
| | Voltage gain = 50dB with max RF gain - 8dB (B7:B6 = 01) | | 7.9 | | |
| | Voltage gain = 45dB with max RF gain - 16dB (B7:B6 = 10) | | 13.7 | | |
| | Voltage gain = 15dB with max RF gain - 32dB (B7:B6 = 11) | | 31.4 | | |
| In-Band Input P-1dB | Max RF gain (B7:B6 = 00) | | -35 | | dBm |
| | Max RF gain - 8dB (B7:B6 = 01) | | -27 | | |
| | Max RF gain - 16dB (B7:B6 = 10) | | -19 | | |
| | Max RF gain - 32dB (B7:B6 = 11) | | -3 | | |
| Maximum Output Signal Level | Over passband frequency range; at any gain setting; 1dB compression point, differential output | | 2.5 | | V$_{P-P}$ |
| Out-of-Band Input IP3 (Note 2) | Max RF gain (B7:B6 = 00), AGC set for -65dBm wanted signal | | -10 | | dBm |
| | Max RF gain - 8dB (B7:B6 = 01), AGC set for -55dBm wanted signal | | -5 | | |
| | Max RF gain - 16dB (B7:B6 = 10), AGC set for -40dBm wanted signal | | -4 | | |
| | Max RF gain - 32dB (B7:B6 = 11), AGC set for -30dBm wanted signal | | +23 | | |
| I/Q Phase Error | 1MHz baseband output; 1 σ variation, $T_A$ = +25°C | | 0.15 | | Degrees |
| I/Q Gain Imbalance | 1MHz baseband output; 1 σ variation, $T_A$ = +25°C | | 0.05 | | dB |
| I/Q Output DC Droop | After completion of default power-on on-chip DC cancellation, 1 σ variation | | ±1 | | V/s |
| I/Q Static DC Offset | No RF input signal; B7:B1 = 0000000, after completion of default power-on on-chip DC cancellation, 1 σ variation | | ±1.0 | | mV |
| Loopback Gain (for Receiver I/Q Calibration) | Transmitter I/Q input to receiver I/Q output; transmitter B6:B1 = 000011, receiver B5:B1 = 10011 programmed through SPI | -7.0 | -2 | +2.5 | dB |
| **RECEIVER BASEBAND FILTERS** | | | | | |
| Baseband Highpass Filter Corner Frequency | Corner frequency 1 | | 600 | | kHz |
| | Corner frequency 2 | | 100 | | |
| | Corner frequency 3 | | 30 | | |
| | Corner frequency 4 | | 1 | | |
| | Corner frequency 5 | | 0.1 | | |

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## AC ELECTRICAL CHARACTERISTICS—Rx MODE (continued)

(MAX2838 Evaluation Kit, $V_{CC\_}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{RF}$ = 3.601GHz, receiver baseband I/Q outputs at 90mV$_{RMS}$, $f_{REF}$ = 40MHz, $\overline{CS}$ = ENABLE = RXTX = high, SCLK = DIN = low, channel bandwidth BW = 7MHz, with power matching for the RF inputs using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated. Rx I/Q differential output load impedance = 10kΩ ‖ 8pF.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| RF Channel BW Supported by Baseband Filter | A4:A0 = 00010 serial bits D7:D4 = 0000 | | 1.5 | | MHz |
| | A4:A0 = 00010 serial bits D7:D4 = 0001 | | 1.75 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 0010 | | 3.5 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 0011 | | 5.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 0100 | | 5.5 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 0101 | | 6.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 0110 | | 7.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 0111 | | 8.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 1000 | | 9.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 1001 | | 10.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 1010 | | 12.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 1011 | | 14.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 1100 | | 15.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 1101 | | 20.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 1110 | | 24.0 | | |
| | A4:A0 = 00010 serial bits D7:D4 = 1111 | | 28.0 | | |
| Baseband Gain Ripple | 0 to 3.2MHz for BW = 7MHz | | 1 | | dB$_{P-P}$ |
| Baseband Group Delay Ripple | 0 to 3.2MHz for BW = 7MHz | | 65 | | ns$_{P-P}$ |
| Baseband Filter Rejection for 7MHz RF Channel BW | At 4.67MHz | | 7 | | dB |
| | At > 10.5MHz | | 53 | | |
| | At > 14MHz | | 75 | | |
| | At > 29.4MHz | | 75 | | |
| **RSSI** | | | | | |
| RSSI Minimum Output Voltage | $R_{LOAD}$ ≥ 10kΩ | | 0.65 | | V |
| RSSI Maximum Output Voltage | $R_{LOAD}$ ≥ 10kΩ | | 2.4 | | V |
| RSSI Slope | | | 30 | | mV/dB |
| RSSI Output Settling Time | To within 3dB of steady state | +32dB signal step | | 200 | | ns |
| | | -32dB signal step | | 800 | | |

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## AC ELECTRICAL CHARACTERISTICS—Tx MODE

(MAX2838 Evaluation Kit, $V_{CC\_}$ = 2.8V, $T_A$ = +25°C, $f_{RF}$ = 3.601GHz , $f_{LO}$ = 3.6GHz. $f_{REF}$ = 40MHz, ENABLE = $\overline{CS}$ = high, and RXTX = SCLK = DIN = low, with power matching for the differential RF pins using the *Typical Operating Circuit*. Lowpass filter is set to 7MHz RF channel BW, 90mV$_{RMS}$ sine and cosine signal (or 90mV$_{RMS}$ 64QAM 1024-FFT OFDMA FUSC I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter (differential DC-coupled). Registers set to recommended settings and corresponding test mode, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **TRANSMIT SECTION: Tx BASEBAND I/Q INPUTS TO RF OUTPUTS** | | | | | |
| RF Output Frequency Range | | 3.3 | | 3.9 | GHz |
| Peak-to-Peak Gain Variation over RF Band | | | 2.6 | | dB |
| Total Voltage Gain | Maximum gain; at unbalanced 50Ω matched output | | 8 | | dB |
| Maximum Output Power over Frequency | OFDM signal conforming to spectral emission mask and -36dB EVM after I/Q imbalance calibration by modem (Note 3) | | 0 | | dBm |
| RF Output Return Loss | All gain settings | | 7 | | dB |
| RF Gain Control Range | | | 60 | | dB |
| RF Gain Control Binary Weights | B1 | | 1 | | dB |
| | B2 | | 2 | | |
| | B3 | | 4 | | |
| | B4 | | 8 | | |
| | B5 | | 16 | | |
| | B6 | | 32 | | |
| Unwanted Sideband Suppression | Without calibration by modem, and excludes modem I/Q imbalance; $P_{OUT}$ = 0dBm | | -40 | | dBc |
| Carrier Leakage | Relative to 0dBm output power; without calibration by modem | | -40 | | dBc |
| Tx I/Q Input Impedance (R ‖ C) | Minimum differential resistance | | 60 | | kΩ |
| | Maximum differential capacitance | | 0.5 | | pF |
| Baseband Frequency Response for 7MHz RF Channel BW | 0 to 4.67MHz | | -8 | | dB |
| | At > 13.23MHz | | -45 | | |
| Baseband Group Delay Ripple | 0 to 4.9MHz (BW = 7MHz) | | 15 | | ns$_{P-P}$ |

## AC ELECTRICAL CHARACTERISTICS—FREQUENCY SYNTHESIS

(MAX2838 Evaluation Kit, $V_{CC}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{REF}$ = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 180kHz, charge-pump comparison frequency = 40MHz, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **FREQUENCY SYNTHESIZER** | | | | | |
| RF Channel Center Frequency | | 3.3 | | 3.9 | GHz |
| Channel Center Frequency Programming Minimum Step Size | | | 29 | | Hz |
| Charge-Pump Comparison Frequency | | 11 | 40 | | MHz |
| Reference Frequency Range | | 11 | 40 | 80 | MHz |
| Reference Frequency Input Levels | AC-coupled to REFCLK pin | 800 | | | mV$_{P-P}$ |

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## AC ELECTRICAL CHARACTERISTICS—FREQUENCY SYNTHESIS (continued)

(MAX2838 Evaluation Kit, $V_{CC}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{REF}$ = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 180kHz, charge-pump comparison frequency = 40MHz, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Programmable Reference Divider Values | A4:A0 = 10100, D2:D1 = 00 | | | 1 | | |
| | A4:A0 = 10100, D2:D1 = 01 | | | 2 | | |
| Closed-Loop Integrated Phase Noise | Loop BW = 180kHz, integrate phase noise from 200Hz to 5MHz | | | -39 | | dBc |
| Charge-Pump Output Current | On each differential side | | | 0.8 | | mA |
| Close-In Spur Level | $f_{OFFSET}$ = 0 to 1.8MHz | | | -45 | | dBc |
| | $f_{OFFSET}$ = 1.8MHz to 7MHz | | | -70 | | |
| | $f_{OFFSET}$ > 7MHz | | | -80 | | |
| Reference Spur Level | $f_{OFFSET}$ ≥ 40MHz | | | -73 | | dBc |
| Turnaround LO Frequency Error | Relative to steady state; measured 35µs after Tx-Rx or Rx-Tx switching instant, and 4µs after any receiver gain changes | | | ±50 | | Hz |
| Temperature Range over which VCO Maintains Lock | Relative to the initial ambient temperature $T_A$, as long as the final temperature is within operating temperature range | | | $T_A$ ± 40 | | °C |
| CLKOUT Frequency Divider Values | A4:A0 = 10100, D6:D5 = 01 (Note 4) | | | 2 | | |
| CLKOUT Output Swing | R = 10kΩ, C = 10pF | Low drive | | 1.6 | | $V_{P-P}$ |
| | | High drive | | 2.4 | | |
| External VCO Input Power | MIMO slave mode only | | | -10 | | dBm |
| External VCO Output Power | MIMO master mode only | | | -8 | | dBm |

## AC ELECTRICAL CHARACTERISTICS—MISCELLANEOUS BLOCKS

(MAX2838 Evaluation Kit, $V_{CC}$ = 2.8V, $f_{REF}$ = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, and $T_A$ = +25°C, unless otherwise noted) (Note 1)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PA BIAS DAC: CURRENT MODE** | | | | | | |
| Numbers of bits | | | | 6 | | |
| Minimum Output Sink Current | D5:D0 = 000000 in A4:A0 = 11100 | | | 0 | | µA |
| Maximum Output Sink Current | D5:D0 = 111111 in A4:A0 = 11100 | | | 310 | | µA |
| Compliance Voltage Range | | | 0.8 | | | V |
| Turn-On Time | Excludes programmable delay of 0 to 7µs in steps of 0.5µs | | | 200 | | ns |
| DNL | | | | 1 | | LSB |
| **PA BIAS DAC: VOLTAGE MODE** | | | | | | |
| Output High Level | 10mA source current | | | $V_{CC}$ - 0.2 | | V |
| Output Low Level | 10mA sink current | | | 0.1 | | V |
| Turn-On Time | Excludes programmable delay of 0 to 7µs in steps of 0.5µs | | | 200 | | ns |
| **ON-CHIP TEMPERATURE SENSOR** | | | | | | |
| Digital Output Code | Read-out at DOUT pin through SPI A4:A0 = 00111, D4:D0 | $T_A$ = +25°C | | 01111 | | |
| | | $T_A$ = +85°C | | 11001 | | |
| | | $T_A$ = -40°C | | 00100 | | |
| Temperature Step Size | | | | 5 | | °C |

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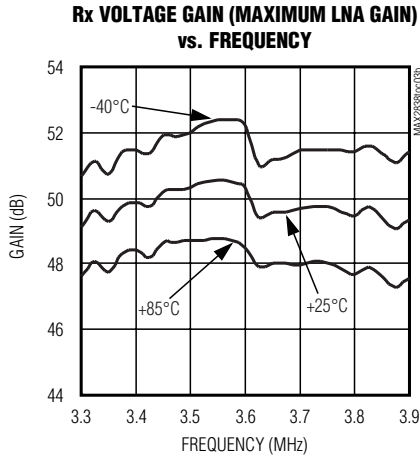# 3.3GHz to 3.9GHz
# Wireless Broadband RF Transceiver

## AC ELECTRICAL CHARACTERISTICS—TIMING

(MAX2838 Evaluation Kit, $V_{CC}$ = 2.8V, $f_{LO}$ = 3.6GHz, $f_{REF}$ = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 180kHz, and $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **SYSTEM TIMING** | | | | | | | |
| Channel Switching Time | Frequency error settles to ±50Hz | Automatic VCO sub-band selection | | | 2 | | ms |
| | | Manual VCO sub-band selection | | | 56 | | µs |
| Turnaround Time | | Measured from Tx or Rx enable rising edge, signal settling to within 0.5dB of steady state | Rx to Tx | | 2 | | µs |
| | | | Tx to Rx | | 2 | | |
| Tx Turn-On Time (from Standby Mode) | | Measured from Tx enable rising edge, signal settling to within 0.5dB of steady state | | | 2 | | µs |
| Tx Turn-Off Time (to Standby Mode) | | From Tx-enable falling edge | | | 0.1 | | µs |
| Rx Turn-On Time (from Standby Mode) | | Measured from Rx enable rising edge, signal settling to within 0.5dB of steady state | | | 2 | | µs |
| Rx Turn-Off Time (to Standby Mode) | | From Rx-enable falling edge | | | 0.1 | | µs |
| **4-WIRE SERIAL INTERFACE TIMING (See Figure 1)** | | | | | | | |
| SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time | $t_{CSO}$ | | | | 6 | | ns |
| Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time | $t_{CSS}$ | | | | 6 | | ns |
| DIN to SCLK Setup Time | $t_{DS}$ | | | | 6 | | ns |
| DIN to SCLK Hold Time | $t_{DH}$ | | | | 6 | | ns |
| SCLK Pulse-Width High | $t_{CH}$ | | | | 6 | | ns |
| SCLK Pulse-Width Low | $t_{CL}$ | | | | 6 | | ns |
| Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$ or Clock to Load Enable Setup Time | $t_{CSH}$ | | | | 6 | | ns |
| $\overline{CS}$ High Pulse Width | $t_{CSW}$ | | | | 20 | | ns |
| Time Between Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK | $t_{CS1}$ | | | | 6 | | ns |
| Clock Frequency | $f_{CLK}$ | | | | | 45 | MHz |
| Rise Time | $t_R$ | | | | $f_{CLK}$ / 10 | | ns |
| Fall Time | $t_F$ | | | | $f_{CLK}$ / 10 | | ns |
| SCLK Falling Edge to Valid DOUT | $t_D$ | | | | 12.5 | | ns |

**Note 1:** Min and max limits are guaranteed by test above $T_A$ = +25°C and are guaranteed by design and characterization at $T_A$ = -40°C. The power-on register settings are not guaranteed. Recommended register setting must be loaded after $V_{CC}$ is supplied.
**Note 2:** Two tones at +20MHz and +39MHz offset with -35dBm/tone. Measure IM3 at 1MHz.
**Note 3:** Gain adjusted over max gain and max gain - 3dB.
**Note 4:** $V_{CC}$ rise time (0V to 2.7V) must be less than 1ms.

*MAXIM*
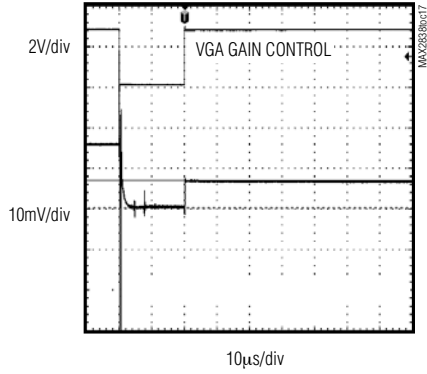
## Typical Operating Characteristics

($V_{CC}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{REF}$ = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 7MHz, using the MAX2838 Evaluation Kit.)
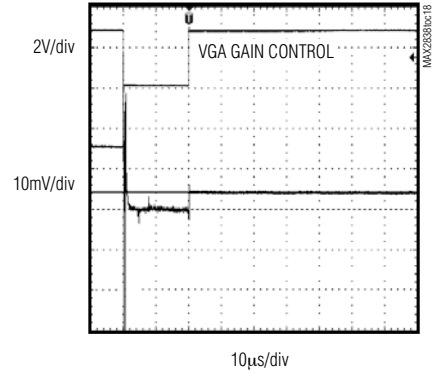
### RECEIVER
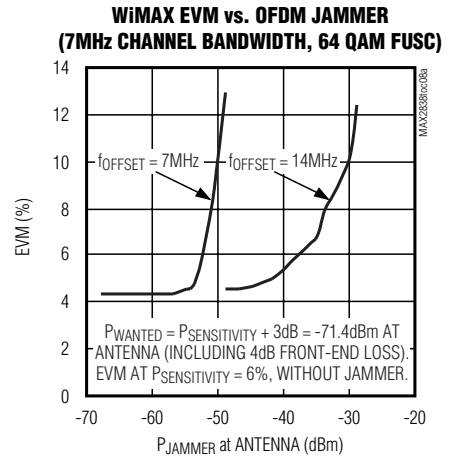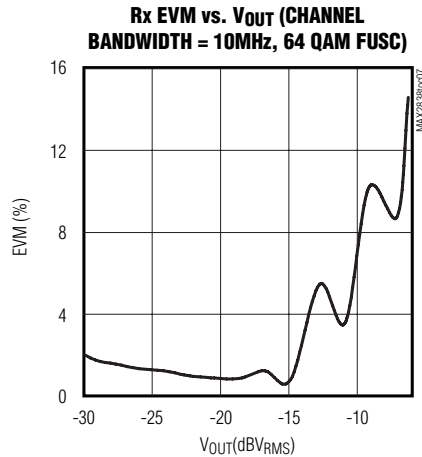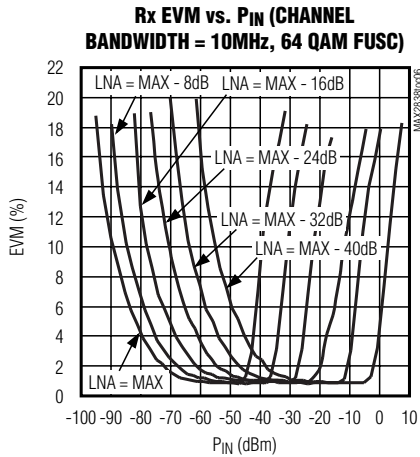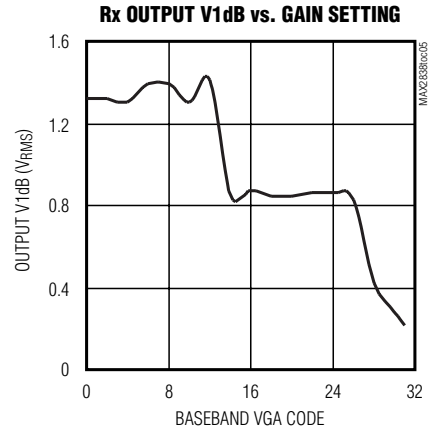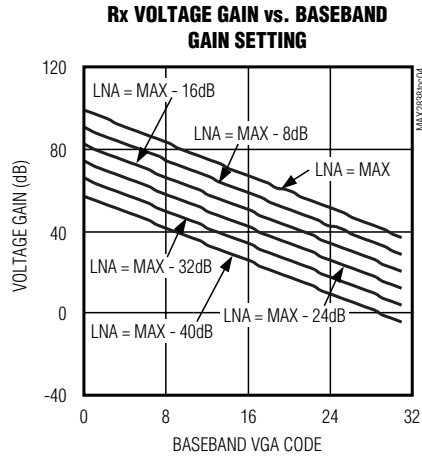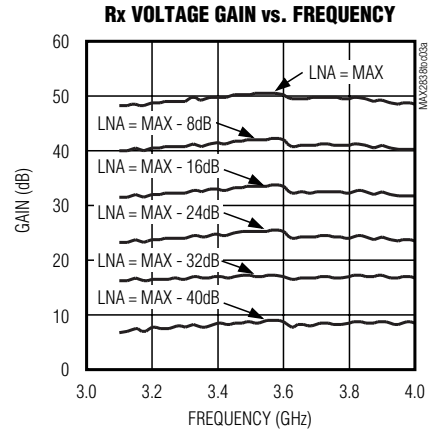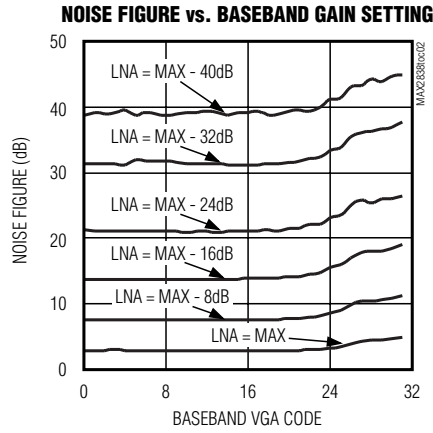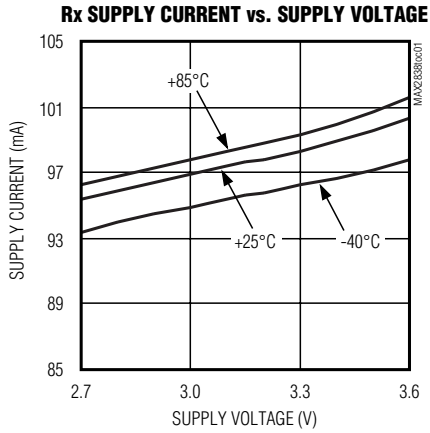
**Rx SUPPLY CURRENT vs. SUPPLY VOLTAGE**

**NOISE FIGURE vs. BASEBAND GAIN SETTING**

**Rx VOLTAGE GAIN vs. FREQUENCY**

**Rx VOLTAGE GAIN (MAXIMUM LNA GAIN) vs. FREQUENCY**

**Rx VOLTAGE GAIN vs. BASEBAND GAIN SETTING**

**Rx OUTPUT V1dB vs. GAIN SETTING**

**Rx EVM vs. P$_{IN}$ (CHANNEL BANDWIDTH = 10MHz, 64 QAM FUSC)**

**Rx EVM vs. V$_{OUT}$ (CHANNEL BANDWIDTH = 10MHz, 64 QAM FUSC)**

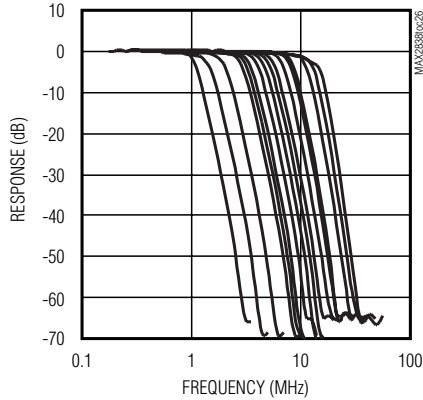**WiMAX EVM vs. OFDM JAMMER (7MHz CHANNEL BANDWIDTH, 64 QAM FUSC)**

**MAX2838**

## Typical Operating Characteristics (continued)

($V_{CC}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{REF}$ = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 7MHz, using the MAX2838 Evaluation Kit.)
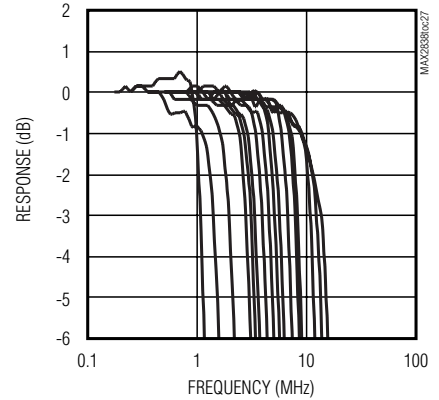


WiMAX EVM vs. OFDM JAMMER
(10MHz CHANNEL BANDWIDTH, 64 QAM FUSC)
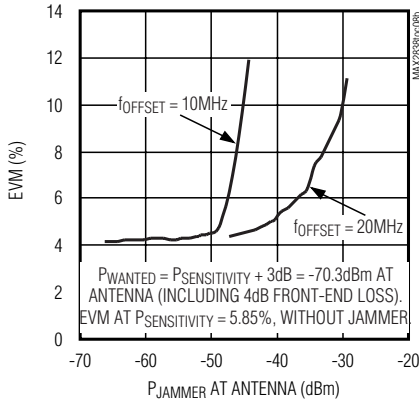


Rx EMISSION SPECTRUM, LNA INPUT
(Tx OFF, LNA = MAX)
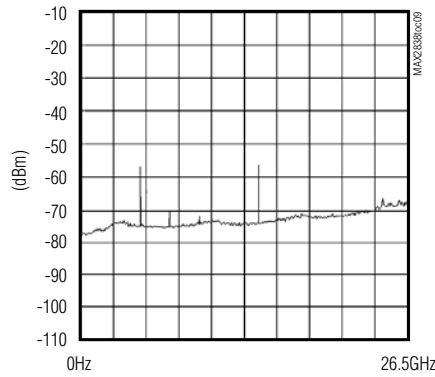


Rx INPUT DIFFERENTIAL IMPEDANCE
vs. FREQUENCY
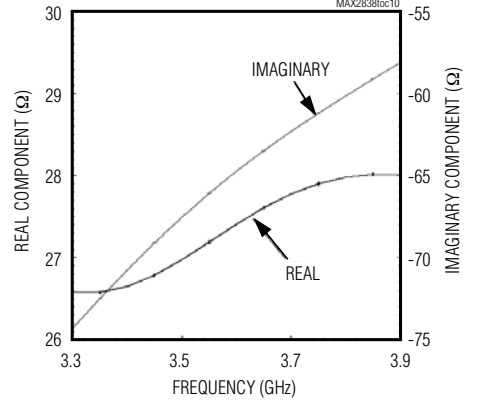


Rx INPUT RETURN LOSS vs. FREQUENCY
(LNA = MAX)
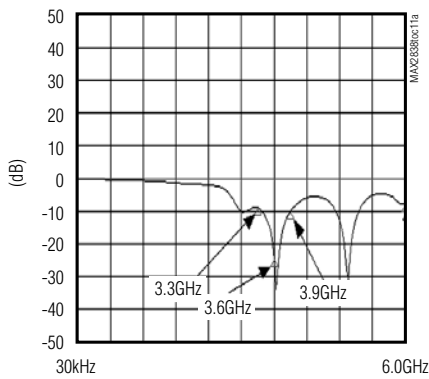


Rx INPUT RETURN LOSS vs. FREQUENCY
(LNA = MAX - 32dB)
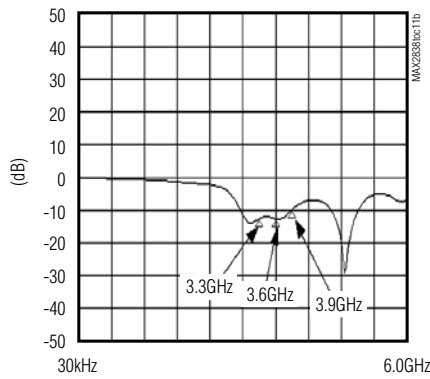


RSSI VOLTAGE vs. INPUT POWER
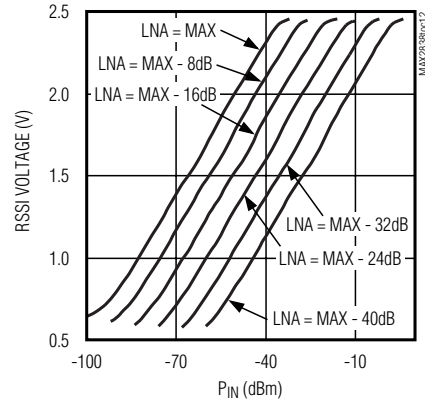


Rx RSSI STEP RESPONSE
(+40dB SIGNAL STEP)
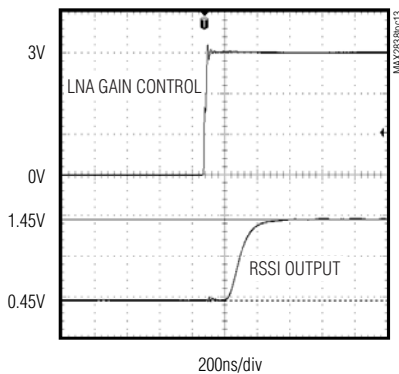


Rx RSSI STEP RESPONSE
(-40dB SIGNAL STEP)
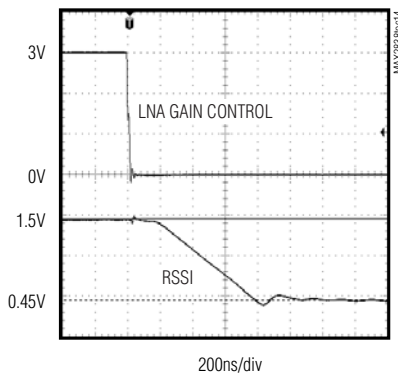


Rx LPF GROUP DELAY vs. FREQUENCY
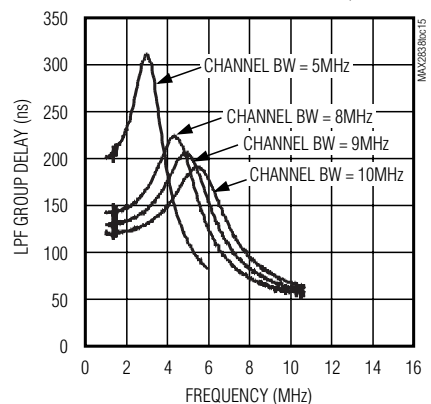
**MAXIM**

**MAX2838**

_____Typical Operating Characteristics (continued)

($V_{CC}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{REF}$ = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 7MHz, using the MAX2838 Evaluation Kit.)
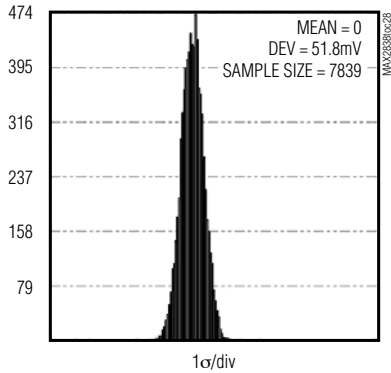
**Rx DC OFFSET SETTLING RESPONSE**
**(+8dB BB VGA GAIN STEP)**

VGA GAIN CONTROL

2V/div

10mV/div

10μs/div

**Rx DC OFFSET SETTLING RESPONSE**
**(-8dB BB VGA GAIN STEP)**

VGA GAIN CONTROL

2V/div

10mV/div

10μs/div
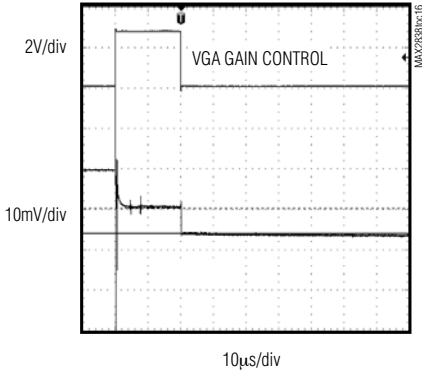
**Rx DC OFFSET SETTLING RESPONSE**
**(-16dB BB VGA GAIN STEP)**

VGA GAIN CONTROL

2V/div

10mV/div

10μs/div

**Rx DC OFFSET SETTLING RESPONSE**
**(-32dB BB VGA GAIN STEP)**

VGA GAIN CONTROL

2V/div

10mV/div

10μs/div
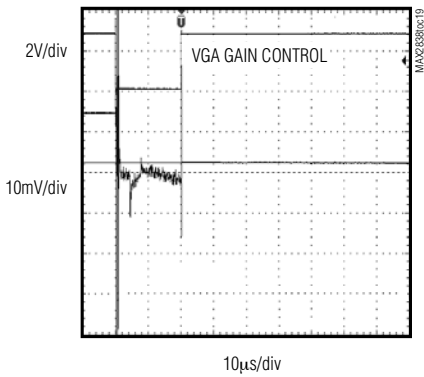
**Rx BBVGA SETTLING RESPONSE**
**(+8dB GAIN STEP)**

100mV/div

2V/div

VGA GAIN CONTROL

200ns/div

**Rx BBVGA SETTLING RESPONSE**
**(-8dB BB VGA GAIN STEP)**

100mV/div

2V/div

VGA GAIN CONTROL

200ns/div
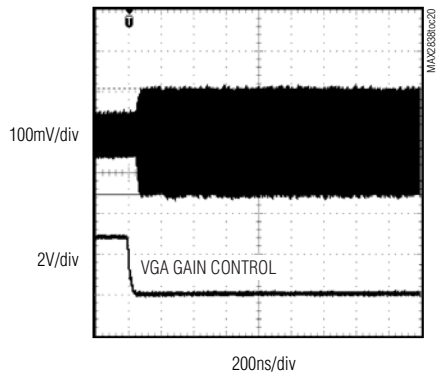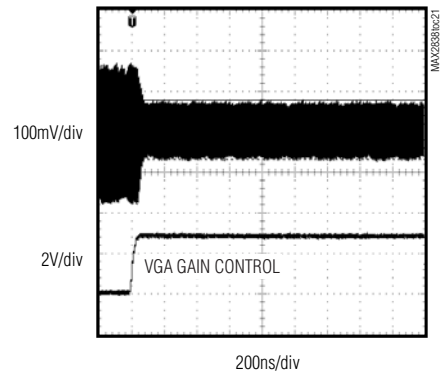
**Rx BBVGA SETTLING RESPONSE**
**(-16dB GAIN STEP)**

500mV/div

2V/div

VGA GAIN CONTROL

200ns/div
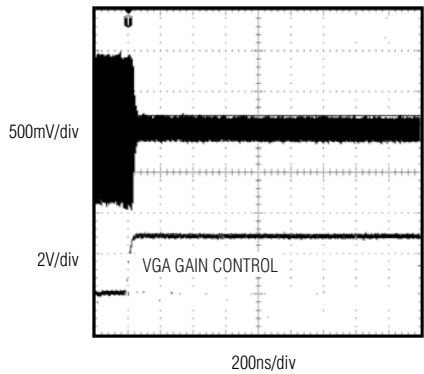
**Rx BBVGA SETTLING RESPONSE**
**(-32dB GAIN STEP)**
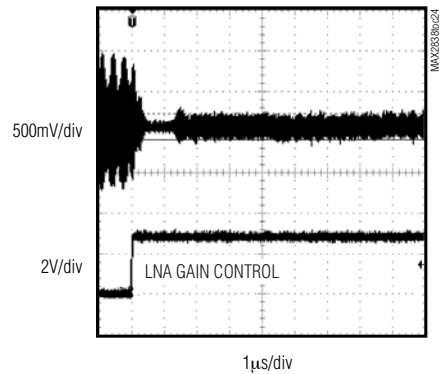
1V/div

2V/div

VGA GAIN CONTROL

200ns/div

**Rx LNA SETTLING RESPONSE**
**(MAX TO MAX - 8dB)**

500mV/div

2V/div

LNA GAIN CONTROL

1μs/div

**MAX2838**

## _____Typical Operating Characteristics (continued)

($V_{CC}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{REF}$ = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 7MHz, using the MAX2838 Evaluation Kit.)

**Rx LNA SETTLING RESPONSE
(MAX TO MAX - 16dB)**
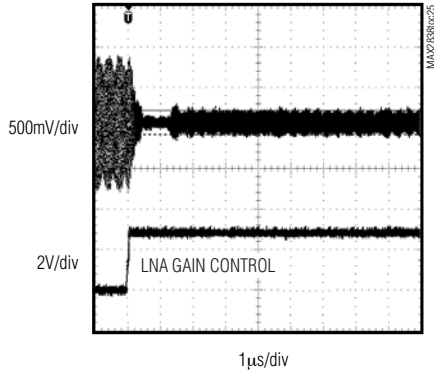
**Rx BB FREQUENCY RESPONSE**

**Rx BB FREQUENCY RESPONSE**

**HISTOGRAM: IQ GAIN IMBALANCE**

MEAN = 0
DEV = 51.8mV
SAMPLE SIZE = 7839

**HISTOGRAM: Rx PHASE IMBALANCE**

MEAN = 0
DEV = 0.11878°
SAMPLE SIZE = 7841
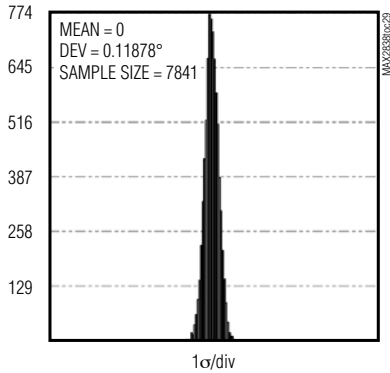
**HISTOGRAM: Rx STATIC DC OFFSET**

MEAN = 0
DEV = 0.23981mV
SAMPLE SIZE = 7841
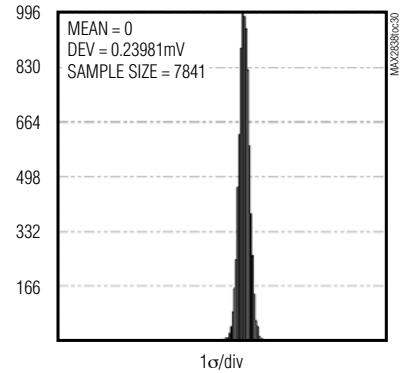
**TRANSMITTER**

**POWER-ON DC OFFSET CANCELLATION
WITH INPUT SIGNAL**
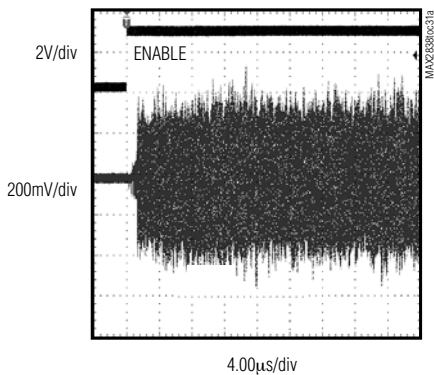
**POWER-ON DC OFFSET CANCELLATION
WITHOUT INPUT SIGNAL**
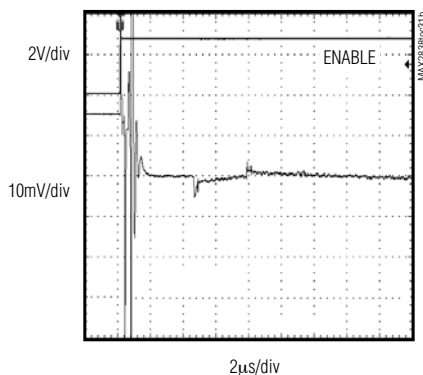
**Tx SUPPLY CURRENT vs. SUPPLY VOLTAGE**
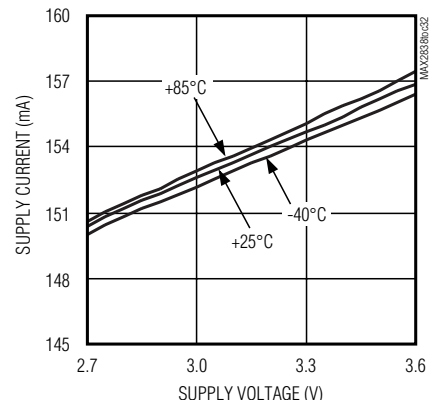
***MAXIM***

## Typical Operating Characteristics (continued)

($V_{CC}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{REF}$ = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 7MHz, using the MAX2838 Evaluation Kit.)

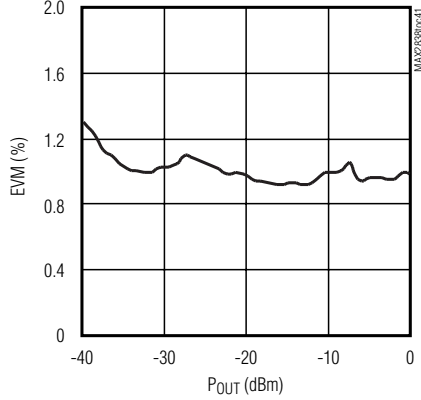**Tx BASEBAND FREQUENCY RESPONSE**



**Tx BASEBAND FREQUENCY RESPONSE**



**Tx OUTPUT POWER vs. FREQUENCY**



**Tx OUTPUT POWER vs. GAIN SETTING**



**Tx OUTPUT SPECTRUM**



**Tx CARRIER SUPPRESSION vs. FREQUENCY**



**Tx CARRIER SUPPRESSION vs. GAIN SETTING**



**Tx SIDEBAND SUPPRESSION vs. FREQUENCY**



**Tx SIDEBAND SUPPRESSION vs. GAIN SETTING**
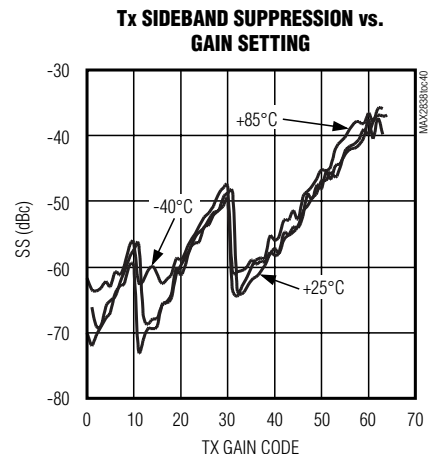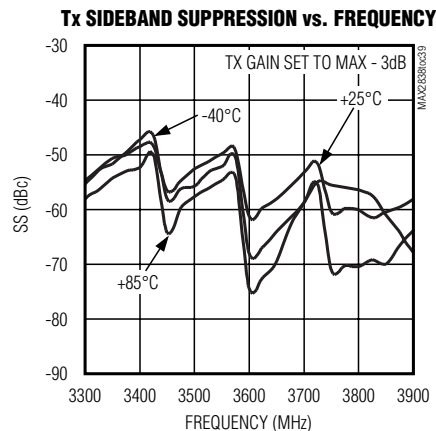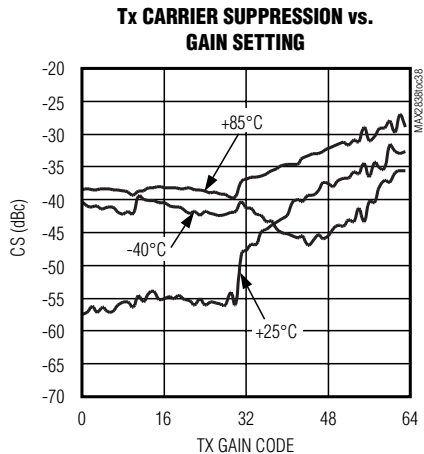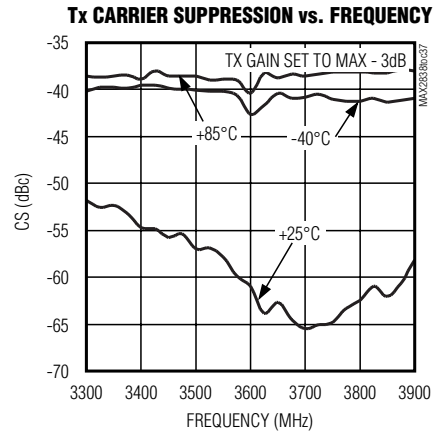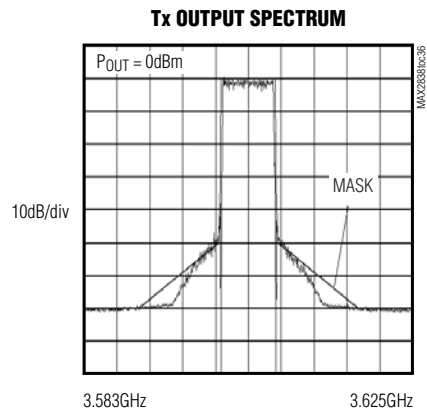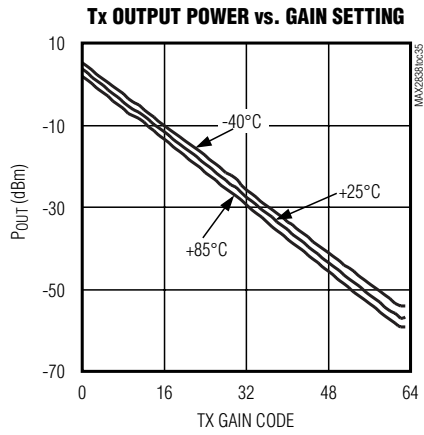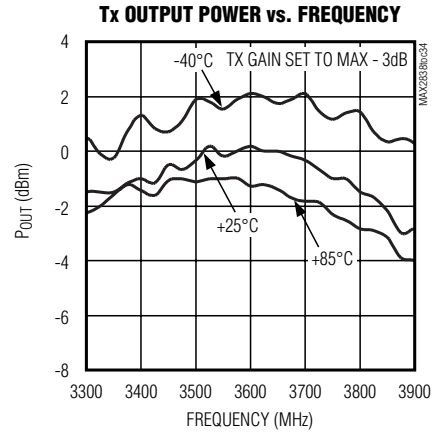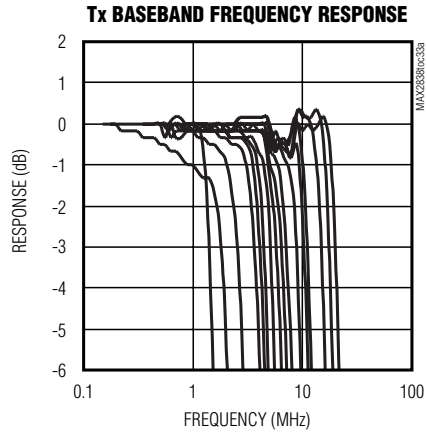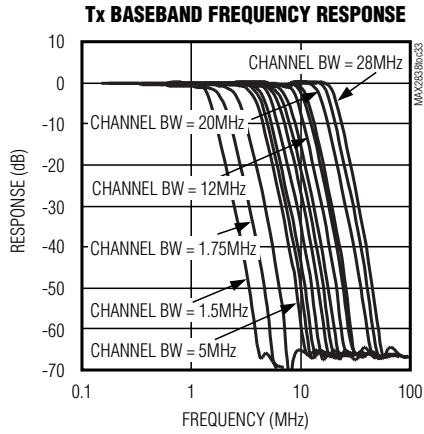
*MAX2838*

_____*Typical Operating Characteristics (continued)*

(V<sub>CC</sub> = 2.8V, T<sub>A</sub> = +25°C, f<sub>LO</sub> = 3.6GHz, f<sub>REF</sub> = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 7MHz, using the MAX2838 Evaluation Kit.)
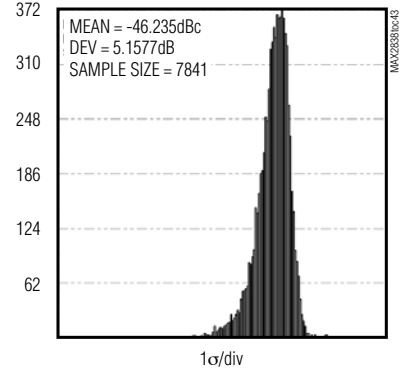
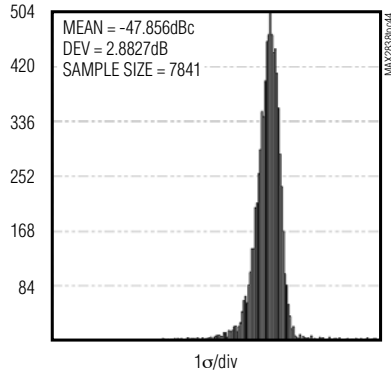**EVM vs. Tx OUTPUT POWER (64 QAM FUSC, 10MHz CHANNEL BANDWIDTH)**
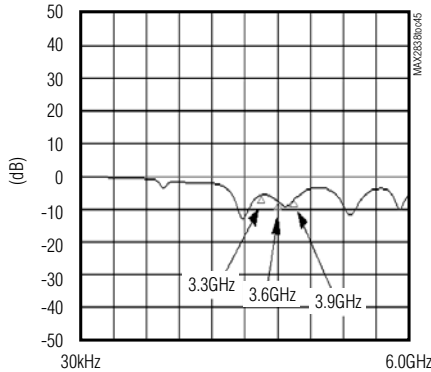
**Tx OUTPUT EMISSION SPECTRUM**

**HISTOGRAM: Tx LO LEAKAGE**

MEAN = -46.235dBc
DEV = 5.1577dB
SAMPLE SIZE = 7841
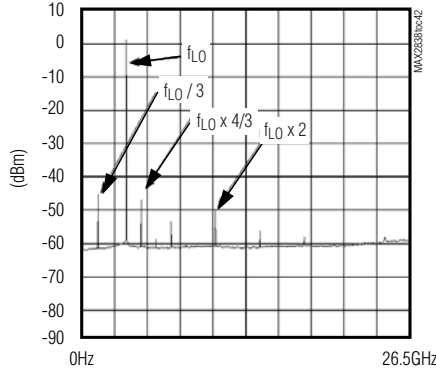
**SYNTHESIZER**

**HISTOGRAM: Tx SIDEBAND SUPPRESSION**

MEAN = -47.856dBc
DEV = 2.8827dB
SAMPLE SIZE = 7841
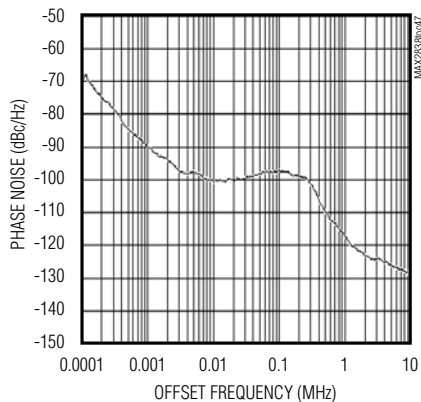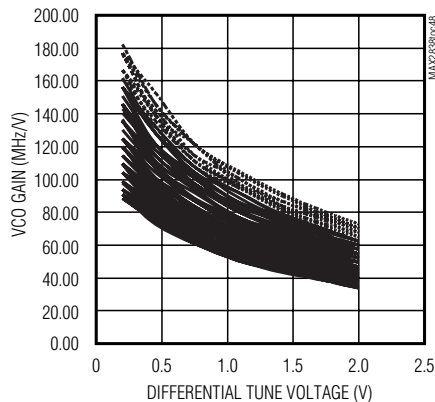
**Tx OUTPUT RETURN LOSS vs. FREQUENCY**

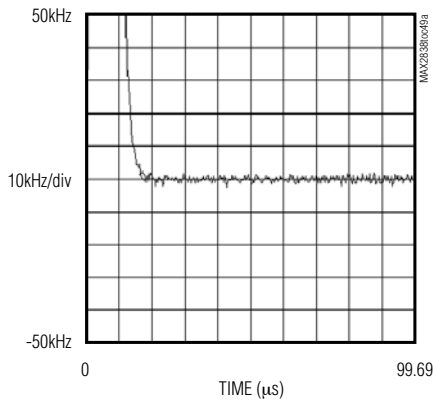**LO FREQUENCY vs. DIFFERENTIAL TUNE VOLTAGE**
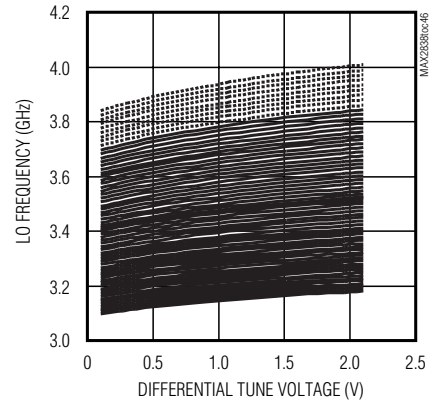
**PHASE NOISE vs. OFFSET FREQUENCY**

**VCO GAIN vs. DIFFERENTIAL TUNE VOLTAGE**

**CHANNEL-SWITCHING FREQUENCY SETTLING (3.3GHz TO 3.9GHz, MANUAL VCO SUB-BAND SELECTION)**

***MAXIM***

# 3.3GHz to 3.9GHz
# Wireless Broadband RF Transceiver

## Typical Operating Characteristics (continued)

($V_{CC}$ = 2.8V, $T_A$ = +25°C, $f_{LO}$ = 3.6GHz, $f_{REF}$ = 40MHz, $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RF BW = 7MHz, using the MAX2838 Evaluation Kit.)

CHANNEL-SWITCHING FREQUENCY SETTLING
(3.9GHz TO 3.3GHz, MANUAL VCO SUB-BAND SELECTION)
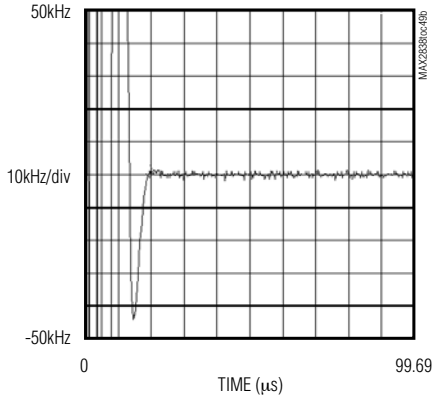
CHANNEL-SWITCHING FREQUENCY SETTLING
(3.9GHz TO 3.3GHz, AUTOMATIC VCO
SUB-BAND SELECTION)
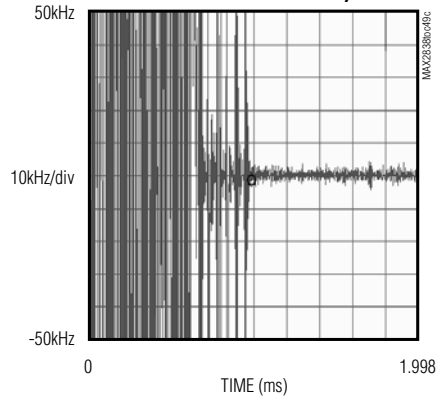
CHANNEL-SWITCHING FREQUENCY SETTLING
(3.3GHz TO 3.9GHz, AUTOMATIC VCO
SUB-BAND SELECTION)

Rx-TO-Tx TURNAROUND FREQUENCY
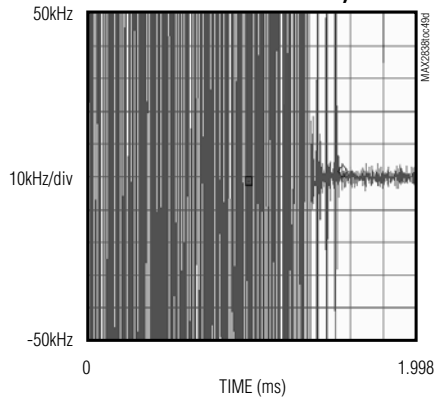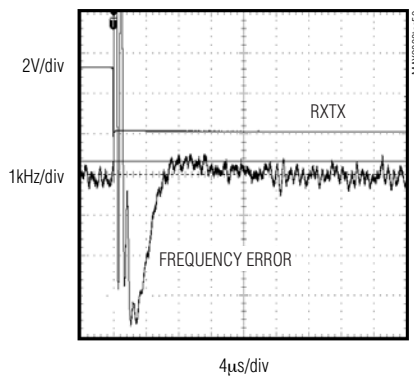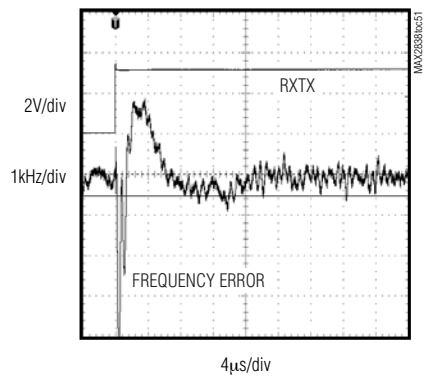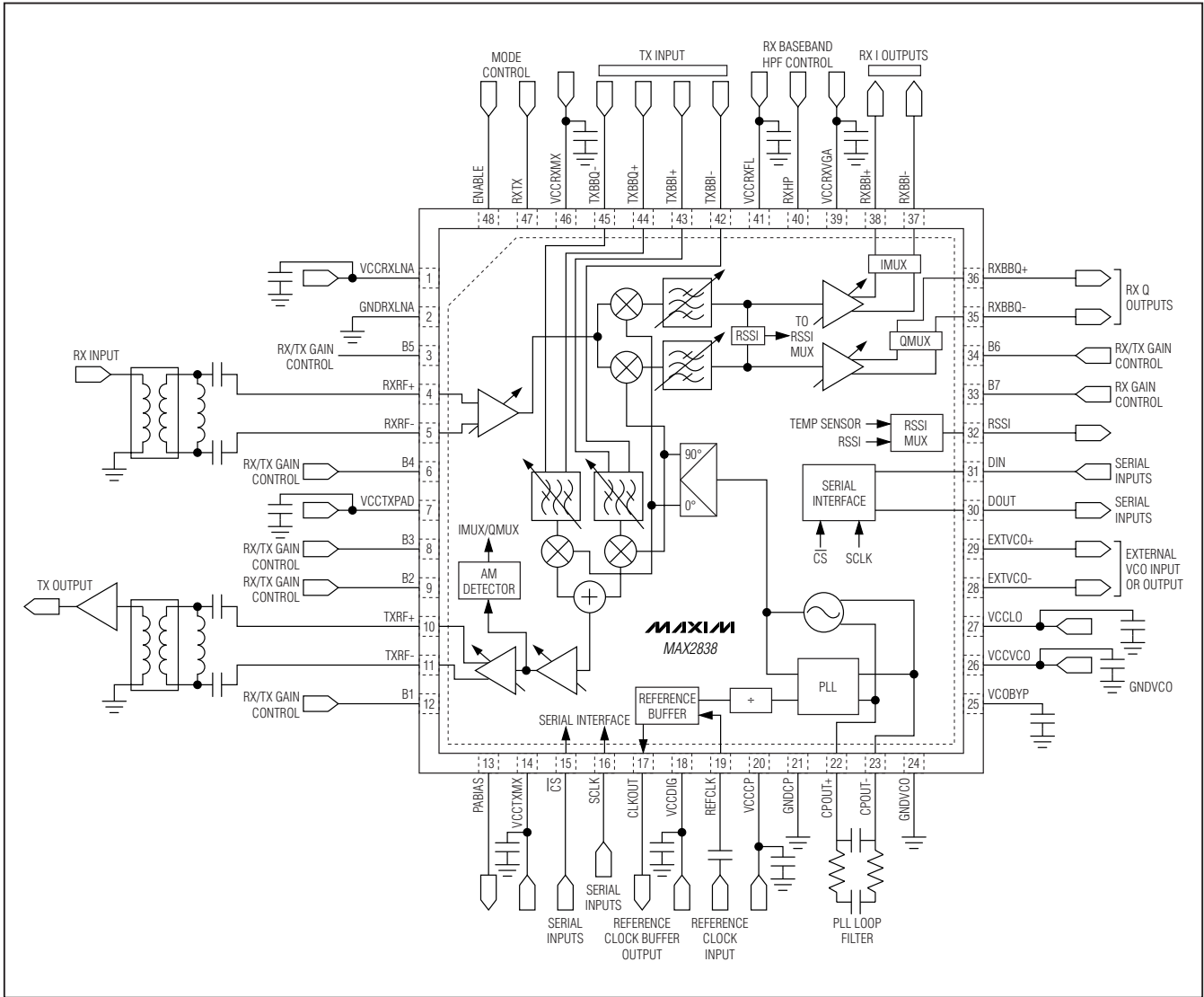GLITCH SETTLING

Tx-TO-Rx TURNAROUND FREQUENCY
GLITCH SETTLING

# 3.3GHz to 3.9GHz
# Wireless Broadband RF Transceiver

## Typical Operating Circuit

**МАХIМ**

**MAX2838**

## Pin Description

| PIN | NAME | FUNCTION |
|-----|------|----------|
| 1 | VCCRXLNA | LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin. |
| 2 | GNDRXLNA | LNA Ground |
| 3 | B5 | Receiver and Transmitter Gain-Control Logic Input Bit 5 |
| 4 | RXRF+ | LNA Differential Inputs. Inputs are internally DC-coupled. Two external series capacitors and one shunt inductor match the inputs to 100Ω differential. |
| 5 | RXRF- | |
| 6 | B4 | Receiver and Transmitter Gain-Control Logic Input Bit 4 |
| 7 | VCCTXPAD | Supply Voltage for Power-Amplifier Driver. Bypass with a capacitor as close as possible to the pin. |
| 8 | B3 | Receiver and Transmitter Gain-Control Logic Input Bit 3 |
| 9 | B2 | Receiver and Transmitter Gain-Control Logic Input Bit 2 |
| 10 | TXRF+ | Power-Amplifier Driver Differential Output. Outputs are internally DC-coupled. Two external series capacitors and one shunt inductor match the outputs to 100Ω differential. |
| 11 | TXRF- | |
| 12 | B1 | Receiver and Transmitter Gain-Control Logic Input Bit 1 |
| 13 | PABIAS | Transmit PA Bias DAC Output |
| 14 | VCCTXMX | Transmitter Upconverter Supply Voltage. Bypass with a capacitor as close as possible to the pin. |
| 15 | $\overline{CS}$ | Chip-Select Logic Input of 4-Wire Serial Interface (See Figure 1) |
| 16 | SCLK | Serial-Clock Logic Input of 4-Wire Serial Interface (See Figure 1) |
| 17 | CLKOUT | Reference Clock Divided Output |
| 18 | VCCDIG | Digital Circuit Supply Voltage. Bypass with a capacitor as close as possible to the pin. |
| 19 | REFCLK | Reference Clock Input |
| 20 | VCCCP | PLL Charge-Pump Supply Voltage. Bypass with a capacitor as close as possible to the pin. |
| 21 | GNDCP | Charge-Pump Circuit Ground |
| 22 | CPOUT+ | Differential Charge-Pump Output. Connect the frequency synthesizer's loop filter between CPOUT+ and CPOUT- (see the *Typical Operating Circuit*). |
| 23 | CPOUT- | |
| 24 | GNDVCO | VCO Ground |
| 25 | VCOBYP | On-Chip VCO Regulator Output Bypass. Bypass with a 1µF capacitor to GND. Do not connect other circuitry to this point. |
| 26 | VCCVCO | VCO Supply Voltage. Bypass with a capacitor as close as possible to the pin. |
| 27 | VCCLO | LO Generation Supply Voltage. Bypass with a capacitor as close as possible to the pin. |
| 28 | EXTVCO- | External VCO Differential Input or Output. Input for slave configuration and output for master configuration. Leave unconnected for single configuration. |
| 29 | EXTVCO+ | |
| 30 | DOUT | Data Logic Output of 4-Wire Serial Interface (See Figure 1) |
| 31 | DIN | Data Logic Input of 4-Wire Serial Interface (See Figure 1) |
| 32 | RSSI | RSSI or Temperature Sensor Multiplexed Analog Output |
| 33 | B7 | Receiver Gain-Control Logic Input Bit 7 |
| 34 | B6 | Receiver and Transmitter Gain-Control Logic Input Bit 6 |
| 35 | RXBBQ- | Receiver Baseband Q-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband detector outputs. |
| 36 | RXBBQ+ | |
| 37 | RXBBI- | Receiver Baseband I-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband detector outputs. |
| 38 | RXBBI+ | |
| 39 | VCCRXVGA | Receiver VGA Supply Voltage. Bypass with a capacitor as close as possible to the pin. |

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| PIN | NAME | FUNCTION |
|---|---|---|
| 40 | RXHP | Receiver Baseband AC-Coupling Highpass Corner Frequency Control Logic Input. Connect to ground if not being used. |
| 41 | VCCRXFL | Receiver Baseband Filter Supply Voltage. Bypass with a capacitor as close as possible to the pin. |
| 42 | TXBBI- | Transmitter Baseband I-Channel Differential Inputs |
| 43 | TXBBI+ | |
| 44 | TXBBQ+ | Transmitter Baseband Q-Channel Differential Inputs |
| 45 | TXBBQ- | |
| 46 | VCCRXMX | Receiver Downconverters Supply Voltage. Bypass with a capacitor as close as possible to the pin. |
| 47 | RXTX | Mode Control Logic Input. See Table 1 for operating modes. |
| 48 | ENABLE | Mode Control Logic Input. See Table 1 for operating modes. |
| — | EP | Exposed Paddle. Connect to the ground plane with multiple vias for proper operation and heat dissipation. Do not share with any other pin grounds and bypass capacitors' ground. |

### Table 1. Operating Mode for MIMO Master and Single Configuration (Note 5)

| MODE | MODE CONTROL LOGIC INPUTS | | | CIRCUIT BLOCK STATES | | | | |
|---|---|---|---|---|---|---|---|---|
| | SPI REG 16, D1:D0 (Note 6) | ENABLE PIN | RXTX PIN | Rx PATH | Tx PATH | PLL, VCO | CLOCK OUT | CALI-BRATION SECTIONS ON |
| **SHUTDOWN** | xx | 0 | 0 | Off | Off | Off | Off | None |
| **STANDBY (Note 7)** | 01 | 0 | 1 | Off | Off | On | On | None |
| **CLOCK OUT** | 00 (Note 11) | 0 | 1 | Off | Off | Off | On | None |
| **Rx** | 01 | 1 | 1 | On | Off (Note 8) | On | On | None |
| **Tx** | 01 | 1 | 0 | Off | On | On | On | None |
| **Tx CALIBRATION (Note 9)** | 11 | 1 | 0 | Off | On (except PA driver) | On | On | AM detector + RX I,Q buffers |
| **Rx CALIBRATION (Note 10)** | 11 | 1 | 1 | On (except LNA) | On (except PA driver) | On | On | Loopback |

**Note 5:** Set SPI Reg 24 D1:D0 = "00" for single-transceiver mode of operation. Set SPI Reg 16 D4:D3 = "11," Reg 24 D8 = "1," Reg 24 D1:D0 = "01" for MIMO master configuration.
**Note 6:** Unused states of SPI Reg 16, D1:D0 above are not tested, and therefore, should not be used.
**Note 7:** Parts of transceiver may be selectively enabled.
**Note 8:** PA bias DAC may be kept active in these non-transmit mode(s) by SPI programming.
**Note 9:** Set SPI Reg 5 D5 = "1" to mux AM detector output to RXBB pins.
**Note 10:** Set SPI Reg 26 D3 = "1."
**Note 11:** CLKOUT signal is active independent of the states of SPI Reg 16, D1:D0, and is only dependent on the states of ENABLE and RXTX pins. However, to ensure that the rest of the chip is off when the CLKOUT is active in the clock-out mode, set SPI Reg 16, D1:D0 to "00" as shown above.

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**Table 2.** Operating Mode for MIMO Slave Configuration (Note 12)

| MODE | MODE CONTROL LOGIC INPUTS | | | CIRCUIT BLOCK STATES | | | | |
|---|---|---|---|---|---|---|---|---|
| | SPI REG 16, D1:D0 (Note 4) | ENABLE PIN | RXTX PIN | Rx PATH | Tx PATH | PLL, VCO | CLOCK OUT | CALI-BRATION SECTIONS ON |
| **SHUTDOWN** | xx | 0 | 0 | Off | Off | Off | Off | None |
| **STANDBY (Note 7)** | 01 | 0 | 1 | Off | Off | Off | On | None |
| **CLOCK OUT** | 00 (Note 11) | 0 | 1 | Off | Off | Off | On | None |
| **Rx** | 01 | 1 | 1 | On | Off (Note 8) | Off | On | None |
| **Tx** | 01 | 1 | 0 | Off | On | Off | On | None |
| **Tx CALIBRATION (Note 9)** | 11 | 1 | 0 | Off | On (except PA driver) | Off | On | AM detector + RX I,Q buffers |
| **Rx CALIBRATION (Note 10)** | 11 | 1 | 1 | On (except LNA) | On (except PA driver) | Off | On | Loop-back |

**Note 12:** Set SPI Reg 16 D4:3 = "00," Reg 24 D8 = "0," Reg 24 D1:0 = "10" to select the MIMO slave configuration.

# Detailed Description

## Configurations

The MAX2838 can be configured in a) single mode, for non-MIMO or SISO applications, b) MIMO master mode, and c) MIMO slave mode. Options b) and c) are for MIMO applications where a coherent LO is required for all transmitters and all receivers.

## Modes of Operation

The modes of operation for the MAX2838 are clock-out, shutdown, standby, Tx, Rx, Tx calibration, and Rx calibration. See Table 1 for a summary of the modes of operation. The logic input pins—RXTX (pin 47) and ENABLE (pin 48)—control the various modes.

## Shutdown Mode (Complete IC Power-Down)

All circuit blocks are powered down, except the 4-wire serial bus and its internal programmable registers. Current drain is the minimum possible with the supply voltages applied. If the digital supply voltage is applied at the VCCDIG pin, the registers can be loaded.

## Standby Mode

PLL, VCO, and LO generation blocks are ON, so that Tx or Rx modes can be quickly enabled from this mode. These and other blocks may be selectively enabled in this mode.

## Rx Mode

All Rx circuit blocks are powered on and active. Antenna signal is applied; RF is downconverted, filtered, and buffered at Rx BB I & Q outputs.

## Tx Mode

All Tx circuit blocks are powered on. The external PA is powered on after a programmable delay.

## Clock-Out Only

Only the clock-out signal is active on the CLKOUT pin. The clock output divider is also functional. The rest of the transceiver is powered down.

## Rx Calibration

Part of the Rx and Tx circuit blocks except the LNA and PA driver are powered on and active. The transmitter IQ input signal is upconverted to RF and at the output of the Tx gain control (VGA). It is fed to the receiver at the input of the downconverter. Either or both of the two receiver channels can be connected to the transmitter and powered on. The I/Q lowpass filters are not present in the transmitter signal path (they are bypassed).

## Tx Calibration

All Tx circuit blocks except the PA driver and external PA are powered on and active. The AM detector and receiver I/Q channel buffers are also on, along with multiplexers in receiver side to route this AM detector's signal to each I and Q differential lines.

# 3.3GHz to 3.9GHz
# Wireless Broadband RF Transceiver

### Programmable Registers and
### 4-Wire SPI-Interface

The MAX2838 includes 32 programmable 16-bit registers. The most significant bit (MSB) is the read/write selection bit. The next 5 bits are register addresses. The 10 least significant bits (LSBs) are register data. Register data is loaded through the 4-wire SPI/MICROWIRE™-compatible serial interface. Data at the DIN pin is shifted in MSB first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active, and input data is shifted at the rising edge of the clock. During the read mode, register data selected by address bits is shifted out to the DOUT pin at the falling edges of the clock. At $\overline{CS}$ rising edge, the 10-bit data bits are latched into the register selected by address bits. See Figure 1.
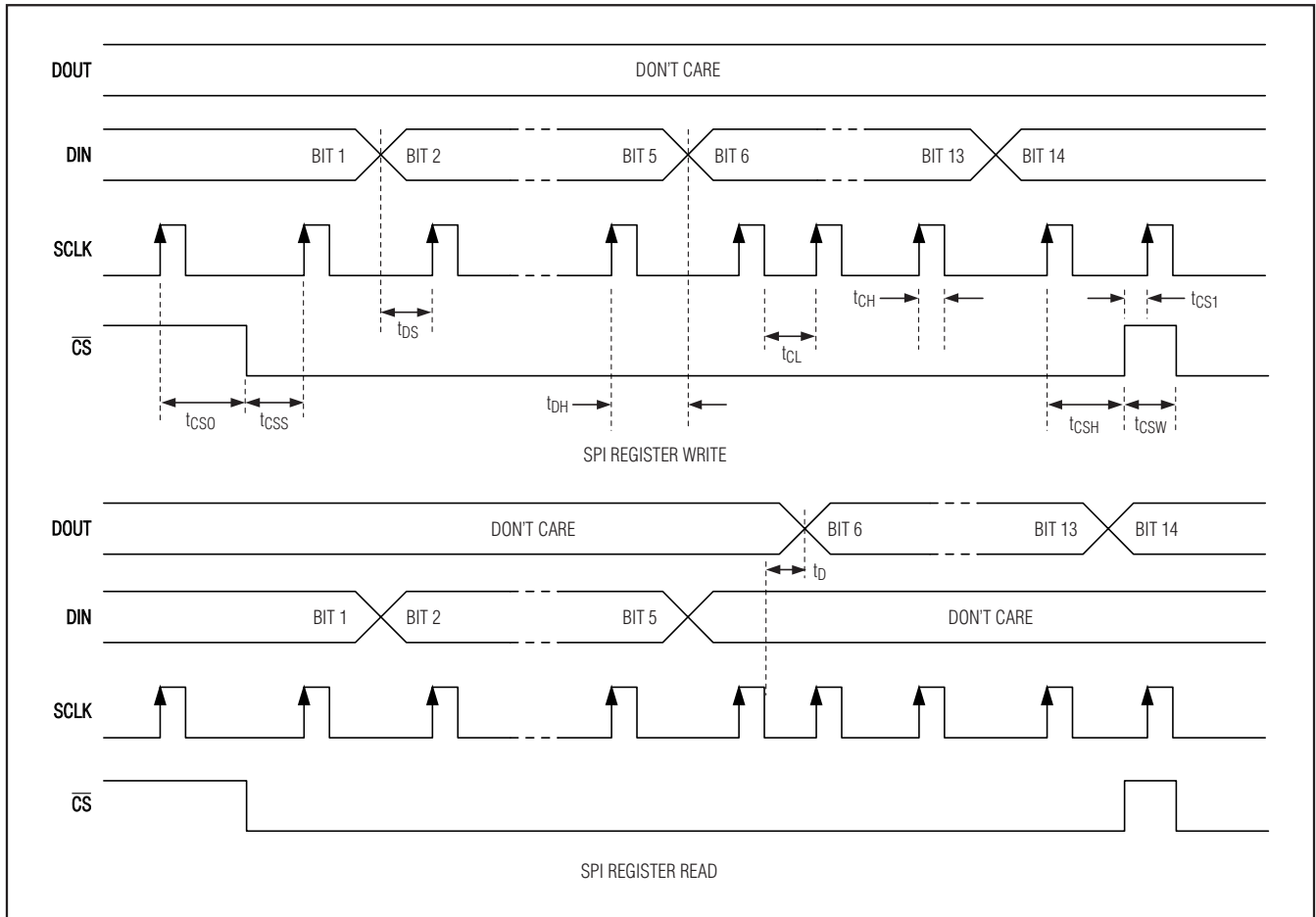
*MICROWIRE is a trademark of National Semiconductor Corp.*

### Chip Information

PROCESS: BiCMOS



*Figure 1. 4-Wire SPI Serial-Interface Timing Diagram*

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## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|:---:|:---:|:---:|
| 48 TQFN-EP | T4866+2 | **21-0141** |

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# 3.3GHz to 3.9GHz
# Wireless Broadband RF Transceiver

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 10/07 | Initial release | — |
| 1 | 8/08 | Removed CLKOUT frequency divide-by-1 ratio in *AC Electrical Characteristics—Frequency Synthesis* table | 7 |