MAX32665/MAX32666 ERRATA SHEET

Revision A1 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc. may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Maxim has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the topside of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the Maxim website at ***www.maximintegrated.com/errata****.*

1) SPIXF BUS IDLE FEATURE CANNOT BE DISABLED

Description:
The SPIXF bus idle feature cannot be disabled. The SPIXF will unexpectedly force the start of a new transaction, requiring resending of the SPI transaction header, if two consecutive reads of the cache both generate a cache miss. (14358)

Workaround:
Set the SPIXF_BUS_IDLE.busidle to 0x1 to approximate the operation of the SPIXF when the bus idle feature is disabled. This will have minimal effect on sequential code execution.

2) QSPI IN SLAVE MODE 0 OR MODE 2 DOES NOT OPERATE AS EXPECTED IF Tx FIFO IS FULL

Description:
When the QSPIn_SS0 signal transitions to its active state, the first bit of the first byte of the MISO signal is always 0 if the transaction starts when the Tx FIFO is full. (14354)

Workaround:
Ensure that the number of bytes in the Tx FIFO is always less than 32 (*QSPIn_DMA.tx_fifo_cnt* < *32*).

3) EXTERNAL CAPACITORS REQUIRED FOR RTC OPERATION

Description:
External capacitors are required to meet the loading requirements for RTC accuracy. (14416)

Workaround:
Specific values are based on PCB and internal oscillator capacitances. Contact factory for details on the characterization procedure.

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4) AUDIO SYSTEM CLOCK AND SAMPLE RATE ACCURACIES GOVERNED BY HSCLK SPECIFICATION

Description:
The HSCLK clock is the source for the digital audio peripheral that has an accuracy of approximately ±2.5%. Refer to the MAX32665–MAX32668 data sheet *Electrical Characteristics* table for guaranteed minimum and maximum values of f_{HSCLK}. (14416)

Workaround:
Ensure the application can tolerate audio clock and sample rate frequencies derived from the HSCLK.

5) SPI MODE 1 AND MODE 3 OPERATION MAY BE AFFECTED WHEN QSPIn_CLK_CFG.*SCALE* = 0

Description:
The following settings are invalid when operation the SPI is operating in mode 1 or mode 3:
SCALE=0, CLOCKHI=0, CLOCKLO=0
SCALE=0, CLOCKHI=1, CLOCKLO=1

Workaround:
Do not use the invalid settings. The operating speeds generated by all other field combinations are valid.

6) UART RECEIVER REQUIRES ONE EXTRA BIT TIME BETWEEN STOP AND START BITS

Description:
The UART requires an external transmitter to send at least one more stop bit than specified in the UARTn_CTRL0.stop field. (10650)

Workaround:
There are two workarounds:
1) Configure the transmitter to send at least one additional stop bit than specified in the UARTn_CTRL0.stop field.
2) Ensure the transmitter generates at least one idle bit time between byte transmissions.

7) DO NOT USE UART Tx AND Rx FUNCTIONALITY SIMULTANEOUSLY

Description:
The peripheral does not operate as expected if both the receive and transmit functions are used simultaneously. (10685)

Workaround:
There are two workarounds:
1) Use flow control to prevent an external UART from transmitting while the peripheral is transmitting.
2) Assign the transmit and receive functionality to different peripherals if full-duplex operation is required.

8) UART TRANSMITTER GENERATES SPURIOUS PULSE WHEN USING 7.3728MHz CLOCK SOURCE

Description:
The UART generates a negative pulse two PCLK periods wide on the UART_TX line one bit period before the falling edge of the start bit. (10689)

Workaround:
There are two workarounds:
1) Use PCLK as the clock source when transmitting.
2) Ensure the external receiver will reject the spurious pulse.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—
1	12/20	Updated erratum 1, deleted erratum 3, added erratum 5	1, 2
2	8/21	Added errata 6–9	2, 3
3	3/22	Removed erratum 9, updated part numbers to match data sheet	All