



# MAX32670/MAX32671 ERRATA SHEET

## Revision B2 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the topside of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the Maxim website at [www.maximintegrated.com/errata](http://www.maximintegrated.com/errata).

### 1) STANDARD DMA OPERATIONS INVOLVING ECC-ENABLED SYSTEM RAM INSTANCES MAY TRANSFER INCORRECT DATA

#### Description:

Incorrect data may be transferred if operations are performed on system RAM instances with their ECC enabled. (21206)

#### Workaround:

Use a secondary DMA channel in conjunction with a primary DMA channel to perform DMA operations to and from ECC-enabled memory.

Considerations:

- The secondary DMA channel must be enabled before the primary DMA channel.
- The value of DMA\_CHn\_CNT.cnt for the secondary channel must be:

$$(4 \times \text{number\_of\_primary\_bursts}) + 1$$

For example, if both DMA\_CHn\_CNT.cnt = 2048 and DMA\_CHn\_CTRL.burst\_size = 32 for the primary channel, then 64 bursts are required. DMA\_CHn\_CNT.cnt for the secondary channel is therefore:

$$(4 \times 64) + 1 = 257$$

Use the following steps to configure both the secondary and primary DMA channels:

1. Configure a secondary DMA channel for a dummy transfer of data. The destination is an unused location in the memory map, so this use of the secondary channel does not affect any usable memory.
  - a) Set DMA\_CHn\_SRC.addr to 0x4000 0000.
  - b) Set DMA\_CHn\_DST.addr to 0x4000 0200.
  - c) Clear DMA\_CHn\_CTRL.srcinc to 0 to disable the source automatic incrementing.
  - d) Clear DMA\_CHn\_CTRL.dstinc to 0 to disable the destination automatic incrementing.

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- e) Set DMA\_CHn\_CTRL.srcwd to 0b10.
- f) Set DMA\_CHn\_CTRL.dstwd to 0b10.
- g) Set DMA\_CHn\_CTRL.burst\_size to 0b00011.
- h) Configure DMA\_CHn\_CTRL.pri of the secondary DMA channel to the same value as DMA\_CHn\_CTRL.pri of the primary DMA channel.
- i) Configure DMA\_CHn\_CNT.cnt to the value calculated above.

2. Configure the primary DMA channel based on the transfer width. The source and destination address of the primary DMA channel must be aligned to a 32-bit boundary.

- For a transfer width of 4 bytes:
  - a) DMA\_CHn\_CNT.cnt must be a multiple of 4.
  - b) DMA\_CHn\_CTRL.burst\_size must be a multiple of 4 bytes.
- For a transfer width of 2 bytes:
  - a) DMA\_CHn\_CNT.cnt must be a multiple of 8.
  - b) DMA\_CHn\_CTRL.burst\_size must be a multiple of 8 bytes.
  - c) Set GCR\_MEMCTRL.ramws\_en to 1 to enable SRAM wait states.
- For a transfer width of 1 byte:
  - a) DMA\_CHn\_CNT.cnt must be a multiple of 4.
  - b) DMA\_CHn\_CTRL.burst\_size must be a multiple of 4 bytes.
  - c) Set GCR\_MEMCTRL.ramws\_en to 1 to enable SRAM wait states.

### 2) GPIO0\_INEN AND GPIO0\_PS RESET VALUES ARE INCORRECT

**Description:**

For all reset events, the reset values are:

GPIO0\_INEN = 0xFFFFFFFF

GPIO0\_PS = 0x00000000

**Workaround:**

None.

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### Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/22	Initial release	—

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