*Click **here** to ask an associate for production status of specific part numbers.*

MAX32674C

Ultra-Low-Power Biometric Algorithm/Sensor Hub

General Description

The MAX32674C is an algorithm/sensor hub with embedded software and world-class algorithms for the fitness and medical wearables market meant to interface directly with Analog Devices' optical sensors. The MAX32674C processes raw data and outputs biometric measurements when configured as an algorithm hub. When configured as a sensor hub, the MAX32674C seamlessly enables customer-desired sensor functionality, including driver communication with Analog Devices optical sensor solutions and delivering raw or calculated data to the outside world. The MAX32674C optimizes system power consumption by sleeping when idle.

Analog Devices provides software algorithms developed by data scientists and machine learning experts for a complete solution—taking raw ADC data and turning it into usable data such as heart rate and SpO_2. The device is delivered unprogrammed. The host microcontroller interfaces to an internal bootloader through an I^2C slave interface for initial programming or in-field upgrades.

The MAX32674C supports the MAX86176 for wrist-based algorithm hub and sensor hub applications. The sensor hub uses the master mode SPI interface to communicate with the sensors.

The wearable algorithms in the MAX32674C support a directly connected accelerometer when used as a sensor hub. It also supports an indirect connection where the accelerometer is instead connected to the host microcontroller. This architecture provides robust detection and compensation of motion artifacts in captured samples.

The device is packaged in a tiny form factor: 2.50mm x 1.75mm, 0.4mm pitch, 24-pin WLP.

Applications

- Wearable Fitness
- Hearables
- Wearable Medical
- Portable Medical
- Mobile Devices

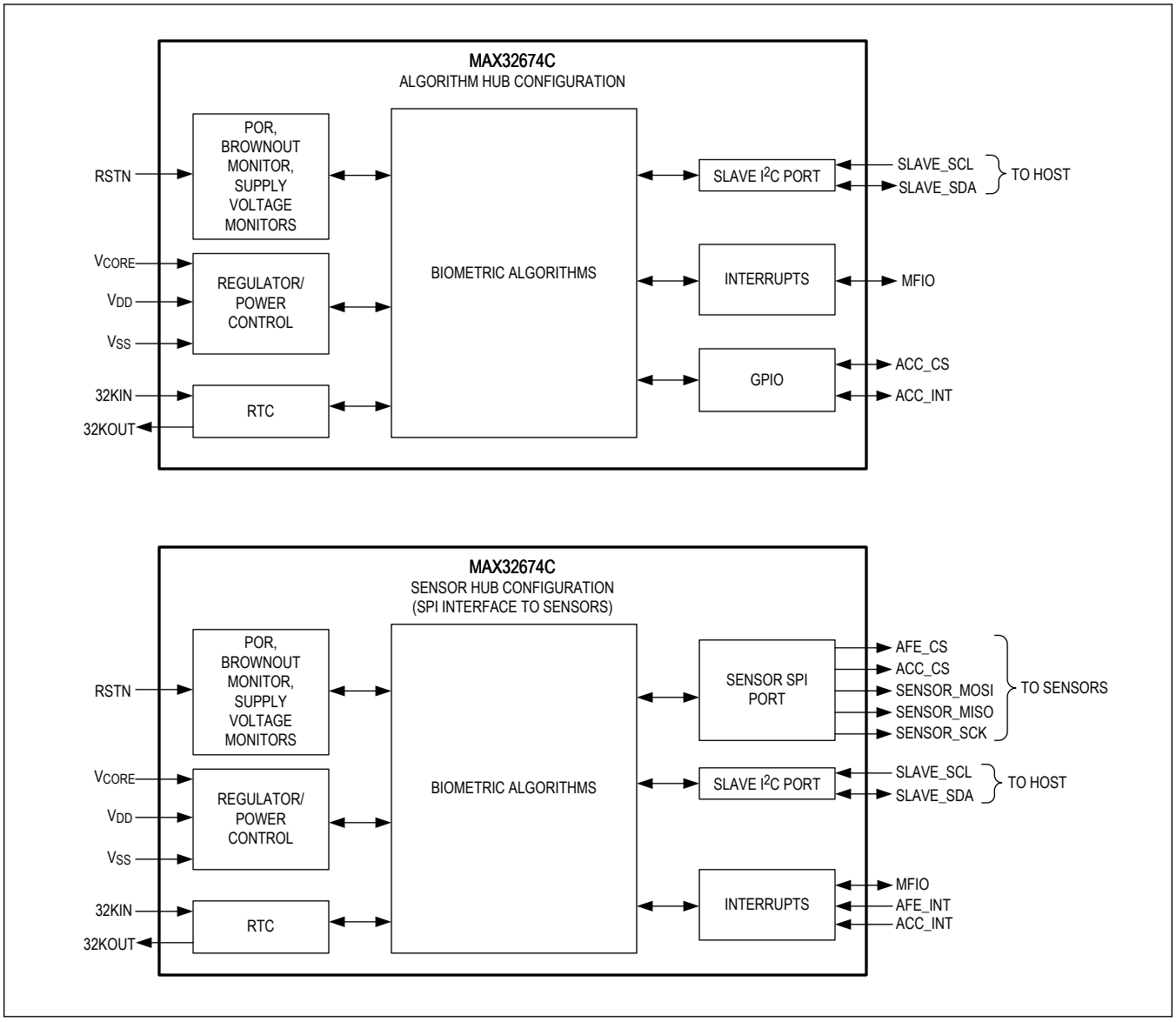
Benefits and Features

- Analog Devices Supplied Software Enables Faster Time to Market:
  - Embedded Algorithms
  - Example Host Microcontroller Source Code
  - Complex Sensor Management and Synchronization Handled by the Sensor Hub
    - Reduces Host Interactions
- Wrist-Based Algorithms Measure:
  - Pulse Heart Rate
  - Pulse Blood Oxygen Saturation (SpO_2)
  - Heart Rate Variability
  - Skin Contact Detection
  - Activity Tracking
- Automatic Exposure Control (AEC) Is a Multidimensional Improvement to Automatic Gain Control (AGC) that Optimizes:
  - Analog Front-End LED Currents
  - Sampling Rate
  - Pulse Width
  - Integration Time
  - Power Consumption and Performance
- Both Raw and Processed Data Are Available
- Software/Algorithm Upgradeable
- FIFO Provides Minimal Host Interaction
- Bootloader Facilitates Secure, Authenticated Software Upgrades

Ordering Information appears at the end of the data sheet.

19-101487; Rev 1; 6/22

Simplified Block Diagram



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LIST OF FIGURES

Absolute Maximum Ratings

(All voltages with respect to V_{SS}, unless otherwise noted.).....
V_{CORE} ..... -0.3V to +1.21V
V_{DD} ..... -0.3V to +3.63V
32KIN, 32KOUT ..... -0.3V to V_{DD} + 0.3V
RSTN, SLAVE_SCL, SLAVE_SDA, MFIO, SENSOR_MISO, AFE_INT, ACC_INT ..... -0.3V to V_{DD} + 0.3V
Total Current into All GPIO Combined (sink) 100mA
V_{SS} 100mA
Output Current (sink) by Any of SLAVE_SDA, MFIO, AFE_CS, ACC_CS, SENSOR_MOSI, SENSOR_SCK 25mA
Output Current (source) by Any of SLAVE_SDA, MFIO, AFE_CS, ACC_CS, SENSOR_MOSI, SENSOR_SCK ..... -25mA
Continuous Package Power Dissipation 24 WLP (multilayer board, T_A = +70°C, derate 18.85mW/°C above +70°C) .1037mW
Operating Temperature Range .....-40°C to +105°C
Storage Temperature Range .....-65°C to +125°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 WLP

Package Code	W241A2+1
Outline Number	21-100625
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	53.04°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Supply Voltage	V_{DD}		1.71	1.8	3.63	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD}	1.58		1.71	V
Power-on-Reset (POR) Voltage	V_{POR}	Monitors V_{DD}		1.4		V
DIGITAL I/O						
Input Low Voltage for RSTN, SLAVE_SCL, SLAVE_SDA, MFIO, SENSOR_MISO, ACC_INT, AFE_INT	V_{IL}				0.3 × V_{DD}	V
Input High Voltage for RSTN, SLAVE_SCL, SLAVE_SDA, MFIO, SENSOR_MISO, ACC_INT, AFE_INT	V_{IH}		0.7 × V_{DD}			V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage for SENSOR_SDA, SENSOR_SCL	V_{OL_I2C}	V_{DD} = 1.71V, I_{OL} = 2mA		0.2	0.4	V
Output High Voltage for SENSOR_SDA, SENSOR_SCL	V_{OH_I2C}	V_{DD} = 1.71V, I_{OH} = 2mA	V_{DD} - 0.4			V
Output Low Voltage for AFE_CS, ACC_CS, SENSOR_MOSI, SENSOR_SCK, MFIO	V_{OL}	V_{DD} = 1.71V, I_{OL} = 1mA		0.2	0.4	V
Output High Voltage for AFE_CS, ACC_CS, SENSOR_MOSI, SENSOR_SCK, MFIO	V_{OH}	V_{DD} = 1.71V, I_{OH} = 1mA	V_{DD} - 0.4			V
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				100	mA
Combined I_{OH}, All GPIO	I_{OH_TOTAL}		-100			mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input/Output Pin Capacitance for All Pins	C_{IO}			4		pF
Input Leakage Current Low	I_{IL}	V_{IN} = 0V	-500		+500	nA
Input Leakage Current High	I_{IH}	V_{IN} = 3.6V	-500		+500	nA
Input Pull-Up Resistor to RSTN	R_{PU_VDD}	Pull-up to V_{DD} = V_{RST}, RSTN at V_{IH}		18.7		kΩ
		Pull-up to V_{DD} = 3.63V, RSTN at V_{IH}		10.0		
CLOCKS						
System Clock Frequency	f_{SYS_CLK}			100		MHz
External RF Oscillator (ERFO)	f_{ERFO}	Required crystal characteristics: C_L = 12pF, ESR ≤ 50Ω, C_0 ≤ 7pF, temperature stability ±20ppm, initial tolerance ±20ppm	16		32	MHz
External RTC Oscillator (ERTCO)	f_{ERTCO}	32.768kHz watch crystal, C_L = 6pF, ESR < 90kΩ, C_0 < 2pF		32.768		kHz
RTC Operating Current	I_{RTC}	All power modes, RTC enabled		0.35		µA
RTC Power-Up Time	t_{RTC_ON}			250		ms
FLASH MEMORY						
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +125°C	10			years

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency	f_{MCK}	f_{SYS_CLK} = 100MHz, $f_{MCK(MAX)} = f_{SYS\_CLK}/2$			50	MHz
SPI Master SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCK}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns

Electrical Characteristics—I²C

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAST MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs

Note 1: GPIO Drive Strength: When using a GPIO bias voltage of 2.97V, the drive current capability of the GPIO is 2x that of its drive strength when using a GPIO bias voltage of 1.71V.

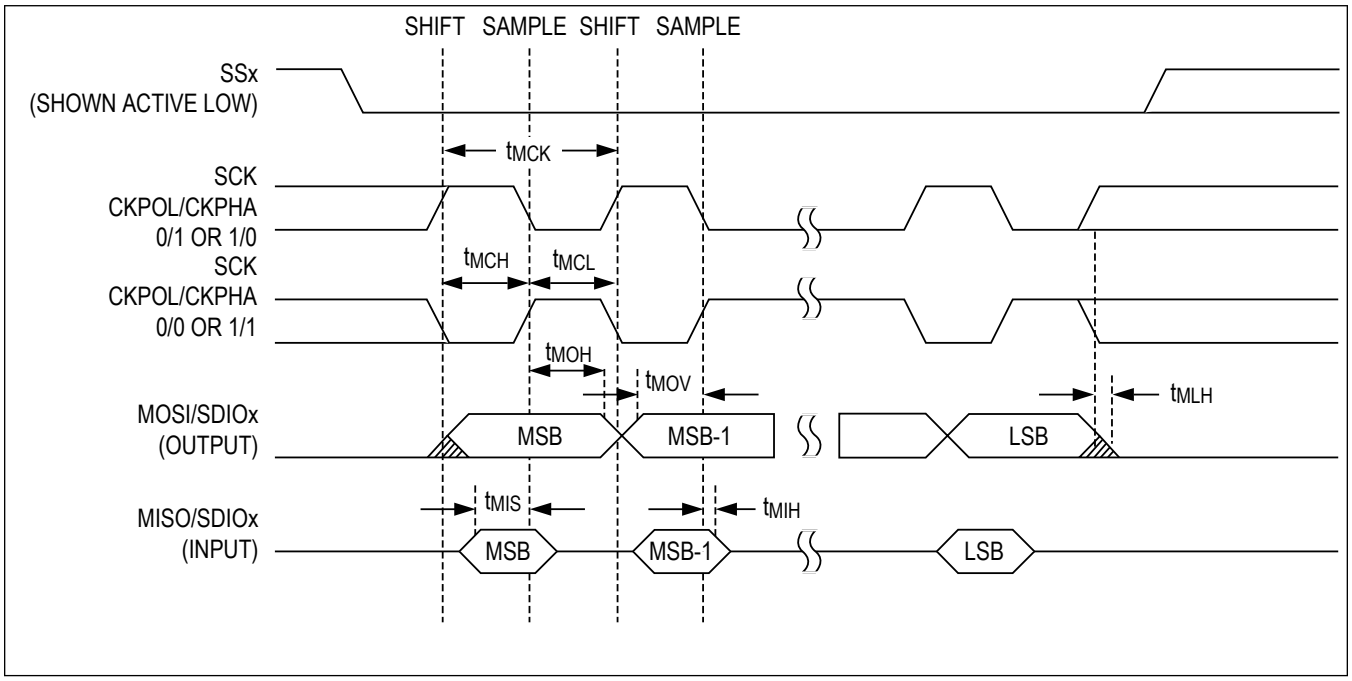


Figure 1. SPI Master Mode Timing Diagram

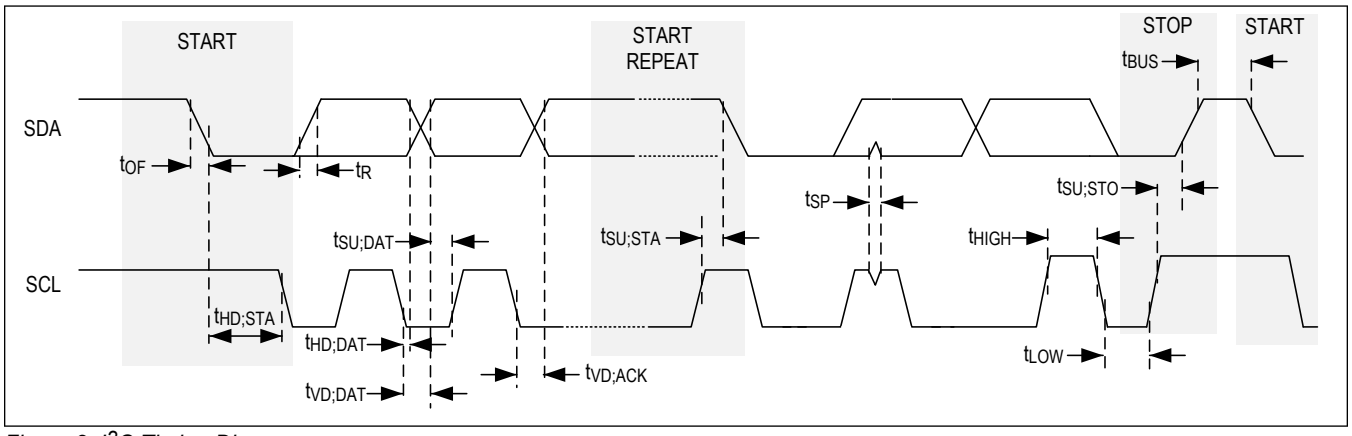
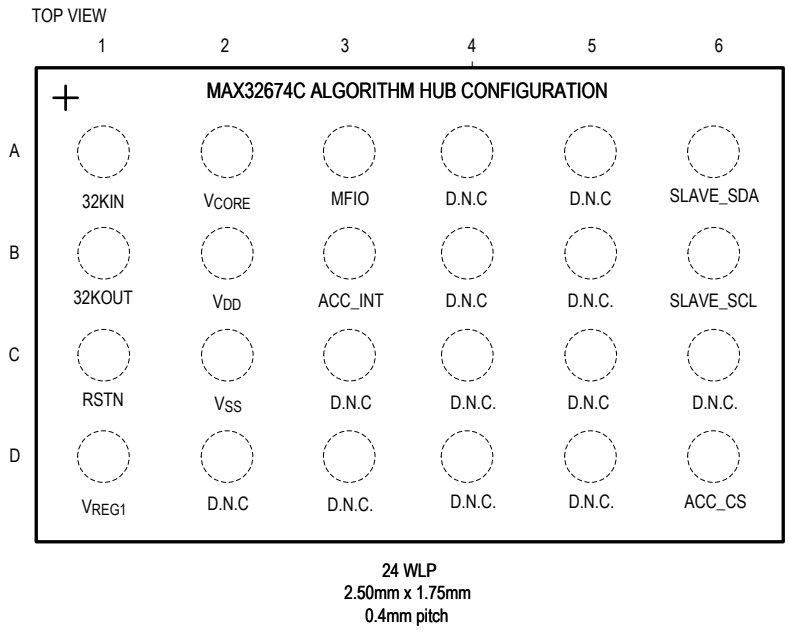


Figure 2. I²C Timing Diagram

Pin Configuration

Algorithm Hub Configuration



Pin Descriptions

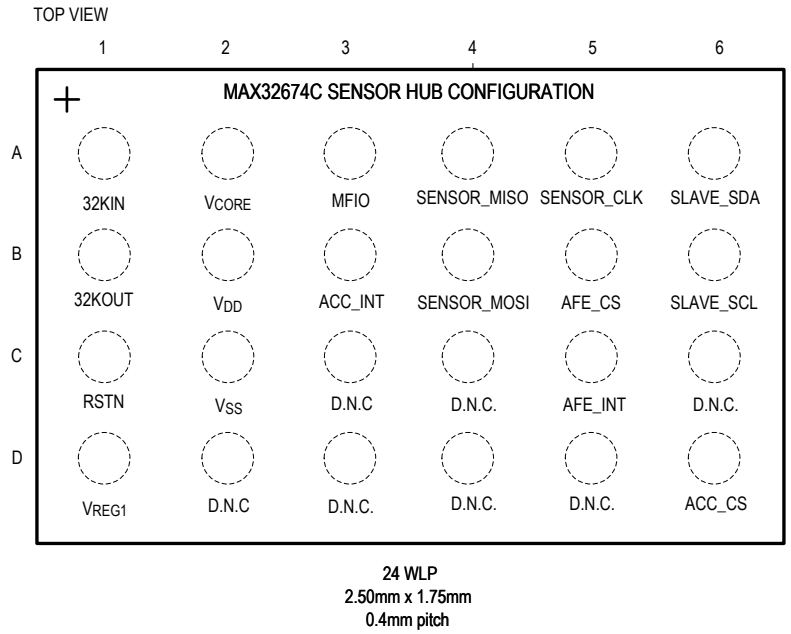
PIN	NAME	FUNCTION MODE Primary Signal (Default)	FUNCTION
POWER (See the *Applications Information* section for bypass capacitor recommendations.)			
A2	V_{CORE}	Digital Power-Supply Input	Bypass with 100nF to V_{SS} and 1µF with 10mΩ to 150mΩ ESR to V_{SS}. Do not connect this device pin to any other external circuitry.
D1	V_{REG1}	Internal Regulator	Bypass with 4.7nF to V_{SS}. Do not connect this device pin to any other external circuitry.
B2	V_{DD}	Power Supply Input	Bypass with 100nF to V_{SS} and 1µF with 10mΩ to 150mΩ ESR to V_{SS}.
C2	V_{SS}	Ground	Ground
RESET AND CONTROL			
C1	RSTN	Reset	Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pull-up to the V_{DD} supply.
B3	ACC_INT	Control 1	This device pin controls the behavior of the device when exiting a reset event. This pin must be high when exiting a reset. Add an external 10kΩ pull-up resistor that is connected to V_{DD}.

Algorithm Hub Configuration

PIN	NAME	FUNCTION MODE	FUNCTION
		Primary Signal (Default)	
D6	ACC_CS	Control 2	This device pin controls the behavior of the device when exiting a reset event. This pin must be high when exiting a reset. Add an external 10kΩ pull-up resistor that is connected to V_{DD}.
CLOCK			
B1	32KOUT	32kHz Crystal Oscillator Output	Refer to the *MAX32670/MAX32671 User Guide* to determine the required external stability capacitors.
A1	32KIN	32kHz Crystal Oscillator Input	Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Refer to the *MAX32670/MAX32671 User Guide* to determine the required external stability capacitors. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
I²C			
B6	SLAVE_SCL	I²C Slave Clock	The I²C slave SCL should be connected to the host I²C master SCL.
A6	SLAVE_SDA	I²C Slave Data	The I²C slave SDA should be connected to the host I²C master SDA.
INTERRUPTS			
A3	MFIO	Multifunction Input/ Output	MFIO acts as an input and, when held low during a reset, the algorithm hub enters bootloader mode. The host asserts MFIO low when it needs to communicate with the algorithm hub.
DO NOT CONNECT			
A4, A5, B4, B5, C3, C4, C5, C6, D2, D3, D4, D5	D.N.C.	Do Not Connect	This pin is internally connected. Do not make any electrical connection, including V_{SS}, to this pin.

Pin Configuration

Sensor Hub Configuration



Pin Descriptions

PIN	NAME	FUNCTION MODE	FUNCTION
		Primary Signal (Default)	
POWER (See the *Applications Information* section for bypass capacitor recommendations.)			
A2	V_{CORE}	Digital Power-Supply Input	Bypass with 100nF to V_{SS} and 1µF with 10mΩ to 150mΩ ESR to V_{SS}.
D1	V_{REG1}	Internal Regulator	Bypass with 4.7nF to V_{SS}. Do not connect this device pin to any other external circuitry.
B2	V_{DD}	Power Supply Input	Bypass with 100nF to V_{SS} and 1µF with 10mΩ to 150mΩ ESR to V_{SS}.
C2	V_{SS}	Ground	Ground
RESET			
C1	RSTN	Reset	Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pull-up to the V_{DD} supply.
CLOCK			
B1	32KOUT	32kHz Crystal Oscillator Output	Refer to the *MAX32670/MAX32671 User Guide* to determine the required external stability capacitors.

Sensor Hub Configuration

PIN	NAME	FUNCTION MODE	FUNCTION
		Primary Signal (Default)	
A1	32KIN	32kHz Crystal Oscillator Input	Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Refer to the *MAX32670/MAX32671 User Guide* to determine the required external stability capacitors. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
I²C			
B6	SLAVE_SCL	I²C Slave Clock	The I²C slave SCL should be connected to the host I²C master SCL.
A6	SLAVE_SDA	I²C Slave Data	The I²C slave SDA should be connected to the host I²C master SDA.
SPI			
A5	SENSOR_SCK	SPI Master Clock	The SPI master clock should be connected to the sensor SPI SCK.
B4	SENSOR_MOSI	SPI Master Out Slave In	The SPI MOSI should be connected to the sensor SPI data input pin.
A4	SENSOR_MISO	SPI Master In Slave Out	The SPI MISO should be connected to the sensor SPI data output pin.
B5	AFE_CS	Analog Front-End Sensor Chip Select	The SPI master analog front-end sensor chip-select output should be connected to the SPI slave PPG sensor chip-select input.
D6	ACC_CS	Accelerometer Chip Select	The SPI master accelerometer chip-select output should be connected to the SPI slave accelerometer chip-select input. An external 10kΩ pull-up resistor (which is connected to V_{DD}) is required. This pin or ACC_INT must be high when exiting reset.
INTERRUPTS			
C5	AFE_INT	Analog Front-End Interrupt Input	The analog front-end sensor interrupt input connects to the PPG sensor interrupt output.
B3	ACC_INT	Accelerometer Interrupt Input	The accelerator interrupt input connects to the accelerometer sensor interrupt output. An external 10kΩ pull-up resistor (which is connected to V_{DD}) is required. This pin or ACC_CS must be high when exiting reset.
A3	MFIO	Multifunction Input/ Output	MFIO acts as an input and, when held low during a reset, the sensor hub enters bootloader mode. The host asserts MFIO low when it needs to communicate with the sensor hub.
DO NOT CONNECT			
C3, C4, C6, D2, D3, D4, D5	D.N.C.	Do Not Connect	This pin is internally connected. Do not make any electrical connection, including V_{SS}, to this pin.

Detailed Description

The MAX32674C supports embedded biometric algorithms in wearable devices. It seamlessly enables customer-desired sensor functionality, including communication with ADI's optical sensor solutions and delivering raw or calculated data to the outside world. This performance is achieved while keeping overall system power consumption in check. The device family interfaces to a microcontroller host through a Fast-mode slave I^2C interface for access to processed biometric data and field updates. The algorithm automatically adjusts the sampling to minimize power consumption and can be configured by the user as needed.

Algorithm Hub Configuration

The algorithm hub configuration should be used when the system requirements require that ECG and PPG run simultaneously or when it is necessary to have accel, ECG, and PPG data time-synchronized. The algorithm hub mode requires more host integration effort for AFE, accelerometer register settings, piping in the PPG and accel data to the MAX32674C, and creating the host code that responds to the algorithm hub requests to update the AFE PPG register settings. The total system power will be more for algorithm hub configuration. The host must handle the dynamic management of the PPG AFE and accelerometer sensors.

Sensor Hub Configuration

The sensor hub configuration should be used when the system requirements do not require that ECG and PPG run simultaneously—ECG and PPG are run in stand-alone modes. The sensor hub mode requires less host integration effort since the MAX32674C includes specific drivers to retrieve the PPG data from the MAX86176 and the accelerometer data from the LIS2DS12 accelerometer. The total system power will be less for sensor hub configuration since there will be less host communication. The dynamic management of the PPG AFE and the accelerometer is offloaded to the power-optimized MAX32674C.

Algorithm Updates

The production version of the MAX32674C is factory-programmed with a bootloader that accepts the flashing of encrypted files that contain the biometric algorithms provided by Analog Devices (.msbl files). The MAX32674C does not come preprogrammed with the biometric algorithms. The host microcontroller must flash the algorithm using bootloader mode to modify the device to use P0.0 as the MFIO pin and then flash the software using I^2C commands. The latest .msbl files are available from the *MAXREFDES104#* webpage.

Algorithm Encryption Keying

The .msbl file is encrypted and released in the Z and C keyed versions of the files. The Z keyed .msbl file and the Z version device are used in the Analog Devices reference designs and evaluation kits. Customers should use the C version of the MAX32674 and the C keyed .msbl file.

Interface to Host

The interface to the host is the I^2C interface. The MAX32674 supports one slave interface with a 7-bit address of 0x55. The features for this interface are:

- One slave for communication with a host
- RESTART condition
- Fast mode: 400kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes
- Software bootloader

Interface to Sensors

For sensor hub configuration, the interface to the sensors is a master SPI.

Applications Information

Bypass Capacitors

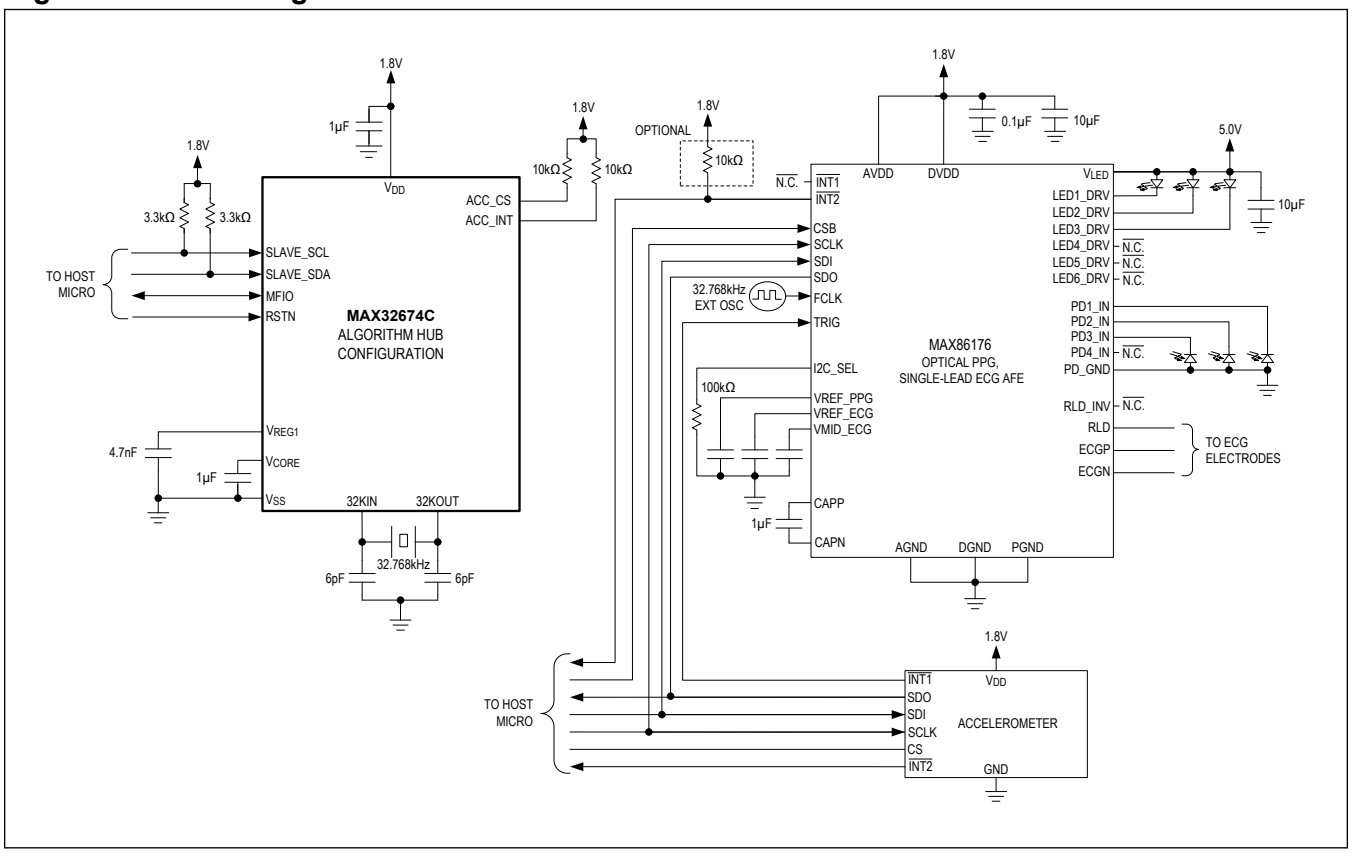
The proper use of bypass capacitors reduces the noise generated by the IC into the ground plane. The *Pin Descriptions* table indicates which pins should be connected to bypass capacitors and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the *Pin Descriptions* table shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Capacitors should be placed as close as possible to their corresponding device pins. When more than one value of capacitor per pin is recommended, the capacitors should be placed in parallel starting with the lowest value capacitor closest to the pin.

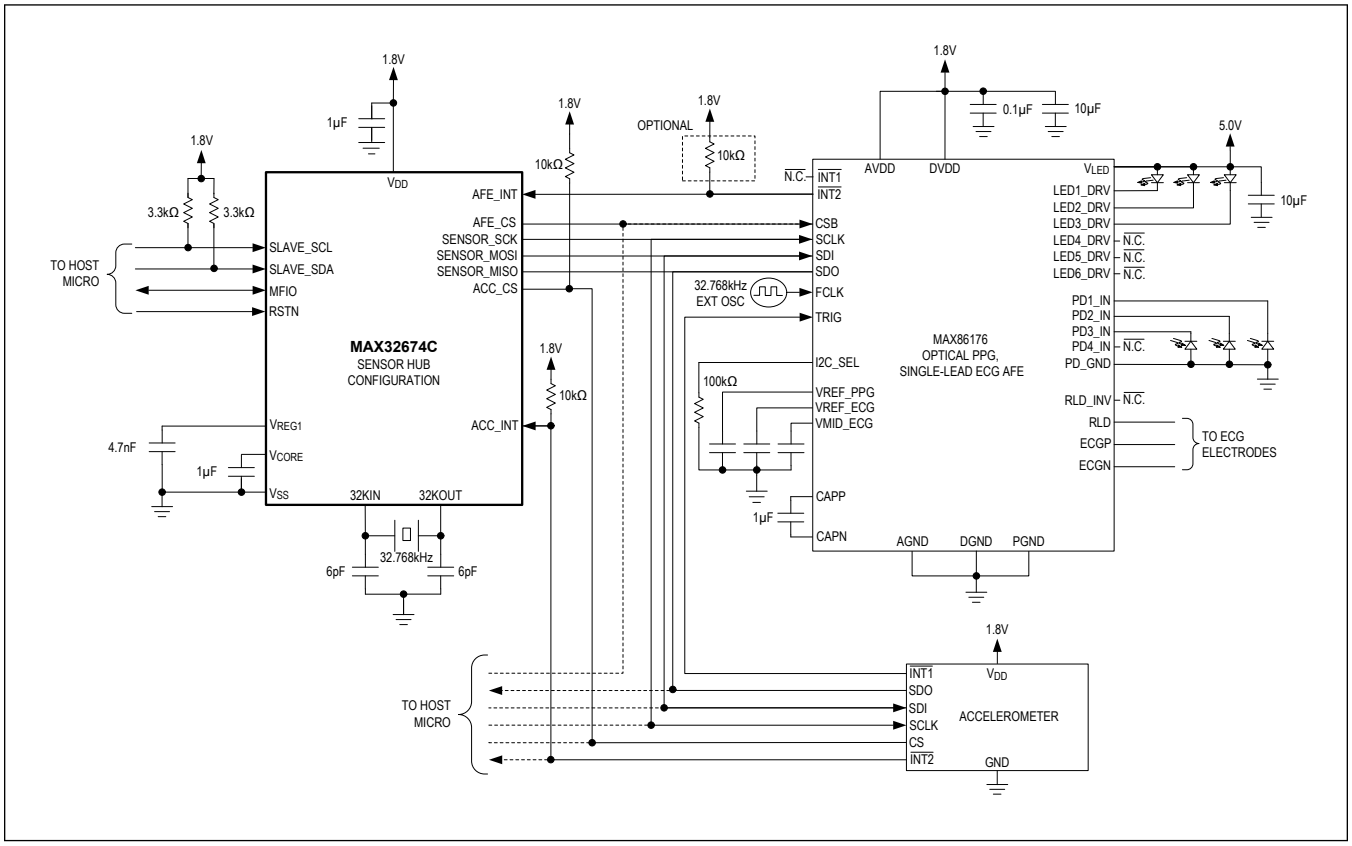
Typical Application Circuits

Algorithm Hub Configuration



Typical Application Circuits (continued)

Sensor Hub Configuration



References

Refer to the *MAX86176* data sheet for the detailed application circuit and additional notes.

Refer to the *MAX32670/MAX32671 data sheet* for detailed information regarding active power consumption.

Ordering Information

PART	DESCRIPTION	APPLICATION ALGORITHM PRELOADED	COMPATIBLE SENSOR	BOOT LOADER	PIN-PACKAGE
MAX32674CGWG+	Algorithm/ sensor hub (C version)	No	MAX86176	Yes	24 WLP (2.5mm x 1.75mm x 0.65mm) 0.4mm pitch
MAX32674CGWG+T	Algorithm/ sensor hub (C version)	No	MAX86176	Yes	24 WLP (2.5mm x 1.75mm x 0.65mm) 0.4mm pitch
MAX32674CGWGZ+	Evaluation version	No	MAX86176	Yes	24 WLP (2.5mm x 1.75mm x 0.65mm) 0.4mm pitch

T = Tape and reel. Full reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/22	Initial release	—
1	6/22	Updated *Benefits and Features* and *Ordering Information*	1, 16