Click here to ask an associate for production status of specific part numbers.

MAX33072E/
MAX33073E

+3.3V and +5.0V, Polarity Invert RS-485 Half-Duplex Transceiver with ±65V Fault Protection, ±40V CMR, and ±40kV ESD

General Description

The MAX33072E/MAX33073E are a family of fault-protected RS-485/RS-422 transceivers with high ±65V protection for overvoltage conditions on the communication bus lines, ensuring robust protection in harsh industrial environments. Both devices have ±40V of common-mode range (CMR) within V_{CCH} (+4.5V to +5.5V), exceeding the RS-485 standard of -7V to +12V, suitable for electrically noisy environments where different systems have shifting ground levels relative to each other. They also incorporate a high ESD protection circuit capable of protecting against ±40kV of ESD HBM (human body model) for driver outputs and receiver inputs (A and B data lines). Each device contains one driver and one receiver and operates with +3.3V or +5V supply, making it convenient for designers to use one part with either +3.3V or +5V supply voltages across multiple end equipment.

These devices feature a polarity selection input (POL) that swaps the A and B data lines, allowing for software correction of cross-wired field cables.

The MAX33072E features slew-rate-limited outputs for data rates up to 500kbps, while the MAX33073E is rated up to 2Mbps for applications requiring higher bandwidth. These transceivers are optimized for robust communication in noisy environments. A true failsafe feature guarantees a logic-high on the receiver output when the inputs are open or shorted. Driver outputs are protected against short-circuit conditions. The receivers feature a 1/8 unit load input impedance, allowing up to 256 transceivers on a bus. The MAX33072E/MAX33073E are available in 8-pin SOIC and operate over the -40°C to +125°C temperature range.

Applications

- Industrial Automation Equipment
- Home and Building Automation
- Agriculture and Heavy Machinery
- Power Supply and UPS
- Elevator Control
- Motion Controllers

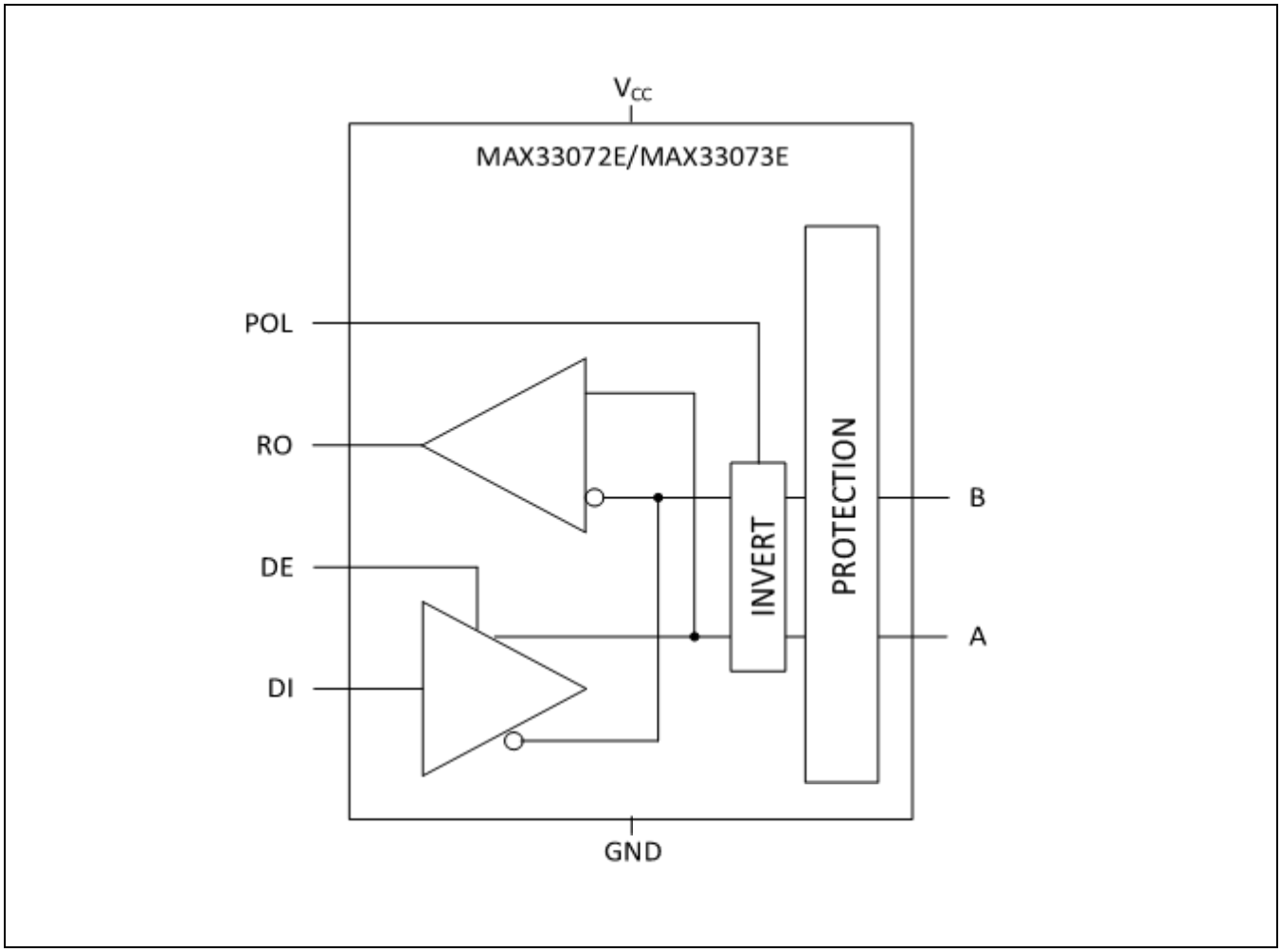
Benefits and Features

- Integrated Protection for Robust Communication
  - Protection on Driver Outputs/Receiver Inputs (A, B Data Lines)
    - ±65V Fault Protection Range on Driver Outputs/Receiver Inputs
    - ±40V Common-Mode Range on Driver Outputs/Receiver Inputs
    - ±40kV Human Body Model (JEDEC JS-001-2017) ESD Protection
    - ±15kV Air Gap Discharge (IEC 61000-4-2) ESD Protection
    - ±10kV Contact Discharge (IEC 61000-4-2) ESD Protection
  - Hot-Swap Protection
  - Short Circuit Protection
  - Thermal Shutdown
  - True Fail-Safe Guarantees Known Receiver Output State
  - Wide Operating Temperature Range from -40ºC to +125ºC
- High-Performance Transceiver Enables Flexible Designs
  - Compliant with RS-485 EIA/TIA-485 Standard
  - 500kbps (MAX33072E), 2Mbps (MAX33073E) Maximum Data Rate
  - 3V to 5.5V Supply Range
  - 1/8 Unit Load for up to 256 Devices on the Bus

***Ordering Information* appears at end of data sheet.**

19-100766; Rev 1; 12/21

Simplified Block Diagram



Absolute Maximum Ratings

V_{CC} .....-0.3V to +6V

RO.....-0.3V to V_{CC} + 0.3V

DE, DI, POL.....-0.3V to +6V

A, B (Continuous) .....-70V to +70V

Short-Circuit Duration (RO, A, B)..... Continuous

Continuous Power Dissipation

8-Pin SOIC +70°C (derate 7.6mW/°C above +70°C)606.1mW

Operating Temperature Range.....-40°C to +125°C

Junction Temperature .....+150°C

Storage Temperature Range.....-65°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

SOIC

Package Code	S8+4
Outline Number	*21-0041*
Land Pattern Number	*90-0096*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	132°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	38°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC} = 3.0V to 3.6V and V_{CC} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5.0V and T_A = +25°C. POL = 0V (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage	V_{CCL}	Low range	3		3.6	V
	V_{CCH}	High range	4.5		5.5	
Supply Current	I_{CC}	DE = high, no load, no switching		6		mA
DRIVER						
Differential Driver Output	$\|V_{OD}\|$	Figure 1a, R_L = 54Ω	1.5			V
		Figure 1a, R_L = 100Ω	2.0			
		Figure 1b	1.5			
External Common Mode Voltage	V_{CM}	Figure 1b, V_{CC} = V_{CCL}	-25		+25	V
		Figure 1b, V_{CC} = V_{CCH}	-40		+40	
Change in Magnitude of Differential Driver Output Voltage	ΔV_{OD}	R_L = 54Ω or 100Ω, Figure 1a (Note 2)	-0.2		+0.2	V

(V_{CC} = 3.0V to 3.6V and V_{CC} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5.0V and T_A = +25°C. POL = 0V (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Common-Mode Output Voltage	V_{OC}	R_L = 54Ω or 100Ω, Figure 1a		1	V_{CC}/2	3	V
Change in Magnitude of Common Mode Voltage	ΔV_{OC}	R_L = 54Ω or 100Ω, Figure 1a (Note 2)		-0.1		+0.1	V
Single-Ended Driver Output Voltage High	V_{OH}	A or B output, output is high, I_{SOURCE} = 3mA		2.4	V_{CC}-0.2		V
Single-Ended Driver Output Voltage Low	V_{OL}	A or B output, output is low, I_{SINK} = 3mA				0.2	V
Driver Short-Circuit Output Current	I_{SC_DR}	-65V ≤ (V_A or V_B) < 0V or V_{CC} < (V_A or V_B) ≤ +65V (Note 3) (Note 5, not production tested)				450	mA
Average Driver Short-Circuit Output Current	I_{AVG_SCDR}	0V ≤ (V_A or V_B) ≤ V_{CC}				450	mA
RECEIVER							
Input Current (A, B)	I_A, I_B	DE = low, 0V ≤ V_{CC} ≤ 5.5V	V_{CM} = +40V			410	μA
			V_{CM} = -40V	-424			
Receiver Input Resistance	R_{IN}	Over V_{CM} range		96			kΩ
Common Mode Voltage Range	V_{CM}	V_{CC} = V_{CCL}		-25		+25	V
		V_{CC} = V_{CCH}		-40		+40	
Receiver Differential Threshold Voltage Rising	V_{TLH}	Over V_{CM} range				-50	mV
Receiver Differential Threshold Voltage Falling	V_{THL}	Over V_{CM} range		-200			mV
Receiver Input Hysteresis	ΔV_{TH}				100		mV
Differential Input Capacitance	C_{A_B}	(Note 5, not production tested)	Measured between A and B, f = 1MHz		50		pF
LOGIC OUTPUT							
RO Output Logic-High Voltage	V_{OH}	I_{SOURCE} = 3mA, (V_A - V_B) ≥ -50mV		V_{CC} - 0.4			V
RO Output Logic-Low Voltage	V_{OL}	I_{SINK} = 3mA, (V_A - V_B) ≤ -200mV				0.4	V
RO Leakage Current	I_{OZR}	RE = V_{IH}, 0V ≤ V_{RO} ≤ V_{CC}		-1		+1	μA
RO Short-Circuit Current	I I_{OSR} I	0 ≤ (V_A - V_B) ≤ V_{CC}	V_{CC} = V_{CCL}		90		mA
			V_{CC} = V_{CCH}		190		
LOGIC INPUTS (DE, DI, POL)							
Input Logic-High Voltage	V_{IH}			2			V
Input Logic-Low Voltage	V_{IL}					0.8	V
Input Hysteresis	V_{HYS}				100		mV
Input Leakage Current	I_{IN}	After first transition of DE		-1		+1	μA
DE Input Impedance on First Transition	R_{IN_FT}			1		10	kΩ
PROTECTION							

(V_{CC} = 3.0V to 3.6V and V_{CC} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5.0V and T_A = +25°C. POL = 0V (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Threshold	T_{SHDN}	Temperature rising		+160		ºC
Thermal Shutdown Hysteresis	T_{HYST}			12		ºC
ESD Protection (A, B Pins to GND)		Human Body Model (JEDEC JS-001-2017)		±40		kV
		IEC 61000-4-2 Contact Discharge		±10		
		IEC 61000-4-2 Air Gap		±15		
ESD Protection (All Other Pins)		Human Body Model		±4000		V
		Charge Device Model		±2000		
Fault Protection Range (A, B Pins to GND)		A, B independently or simultaneously	-65		+65	V
		A and B opposite polarity from separate supplies simultaneously (Note 5, not production tested)	-65		+65	
SWITCHING						
DRIVER (Note 4) (Note 5)						
Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF (Figure 2) (Figure 3)		50	1000	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF (Figure 2) (Figure 3)		10	140	ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF (Figure 2) (Figure 3)		30	600	ns
Maximum Data Rate	DR_{MAX}	R_L = 54Ω, C_L = 50pF	0.5			Mbps
Driver Enable to Output High or Output Low	t_{DZH}, t_{DZL}	R_L = 110Ω, C_L = 50pF (Figure 4) (Figure 5)		500		ns
Driver Enable Time	t_D	-40V ≤ V_{CM} ≤ +40V, Figure 1b		3.5		µs
Driver Disable Time from Output Low or Output High	t_{DLZ}, t_{DHZ}	R_L = 110Ω, C_L = 50pF (Figure 4) (Figure 5)		500		ns
RECEIVER (Note 4) (Note 5)						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF (Figure 6) (Figure 7)		130	200	ns
Receiver Output Skew	t_{RSKEW}	C_L = 15pF (Figure 6) (Figure 7)		2	30	ns

Note 1:	All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2:	ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when DI changes state
Note 3:	The short-circuit current is 450mA (max) for a short period (30µs, typ). If the short circuit persists, the outputs are then set to high impedance for 300ms (typ).
Note 4:	Capacitive load includes test probe and fixture capacitance.
Note 5:	Guaranteed by design. Not production tested.

Timing Diagrams

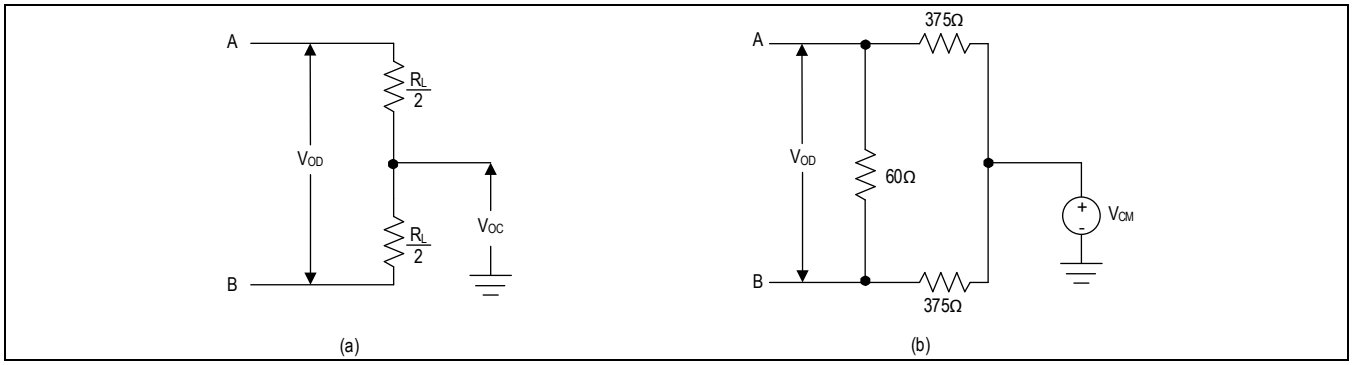


Figure 1. Driver DC Test Load

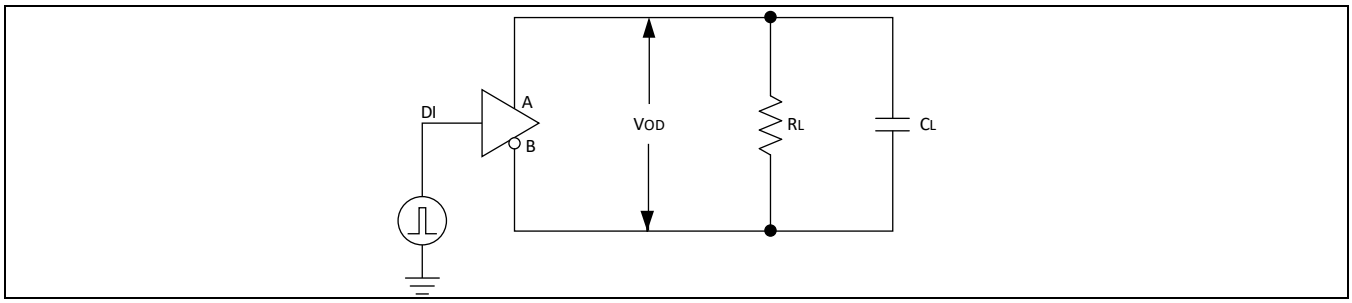


Figure 2. Driver Timer Test Circuit

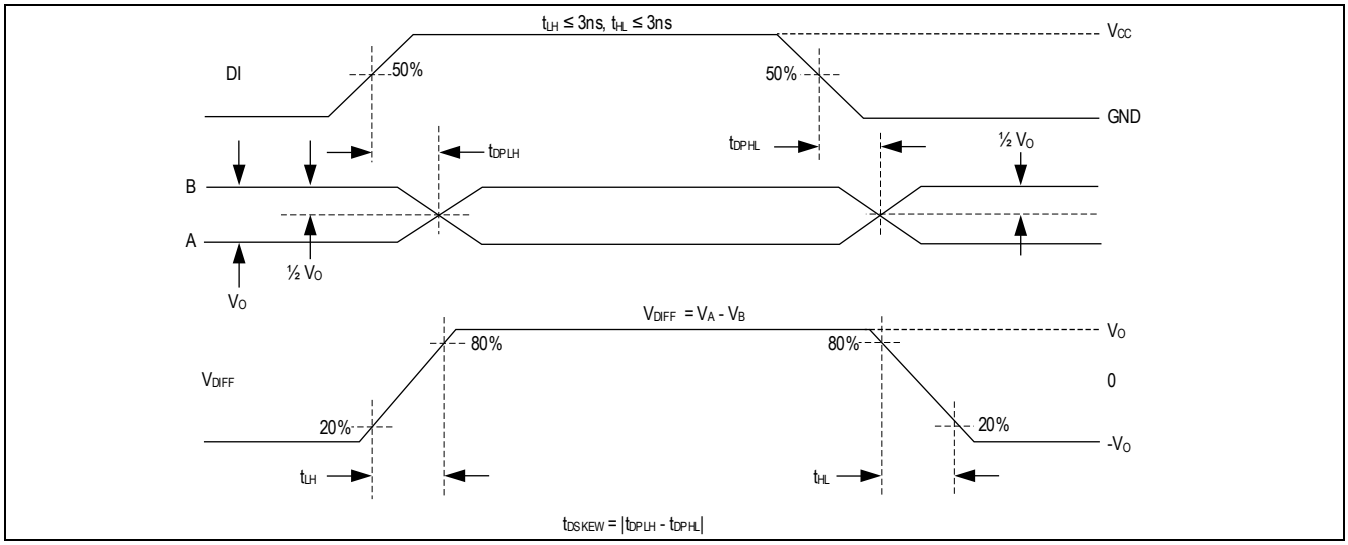


Figure 3. Driver Propagation Delays

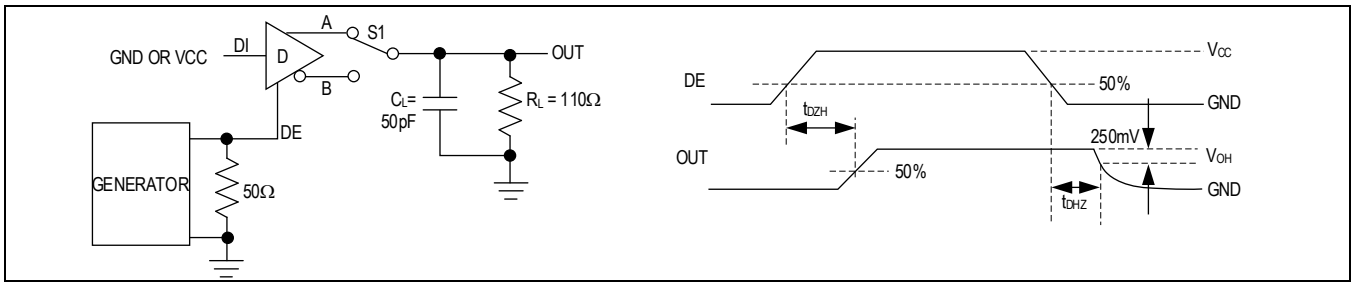


Figure 4. Driver Enable and Disable Times (t_{DHZ}, t_{DZH})

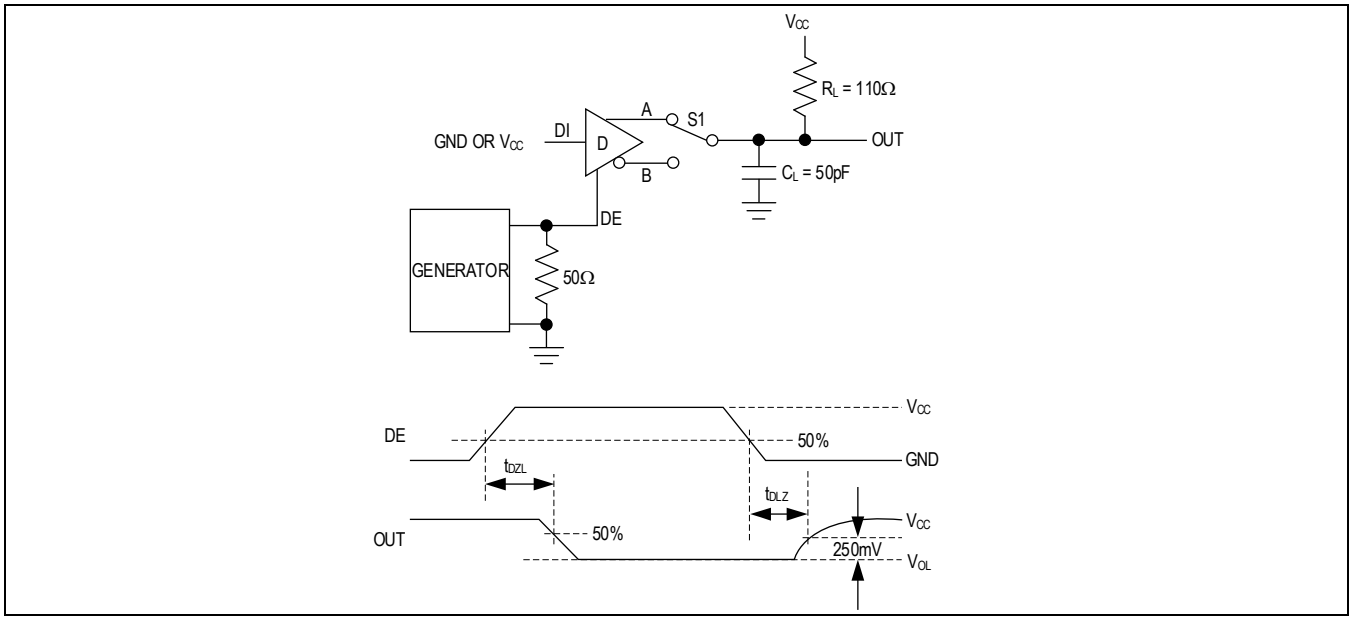


Figure 5. Driver Enable and Disable Times (t_{DZL}, t_{DLZ})

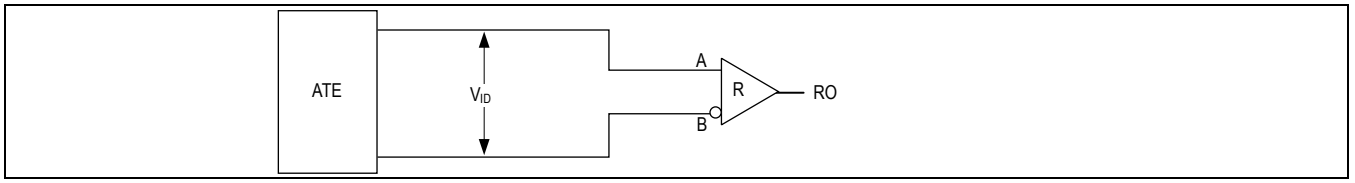


Figure 6. Receiver Propagation Delay Test Circuit

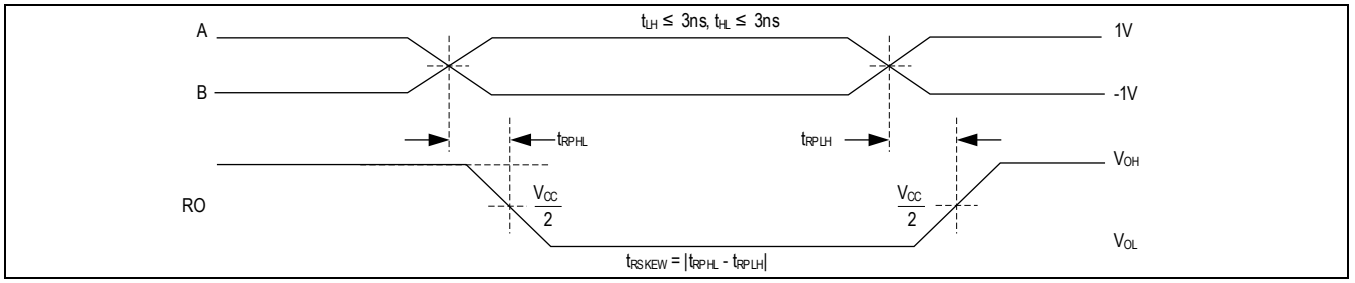
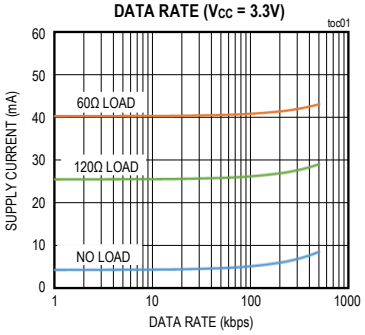


Figure 7. Receiver Propagation Delays

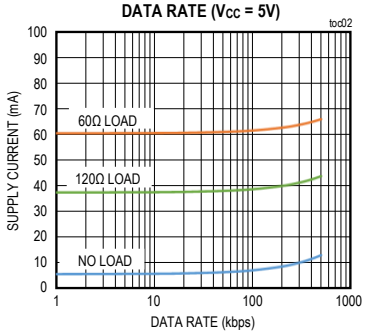
Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

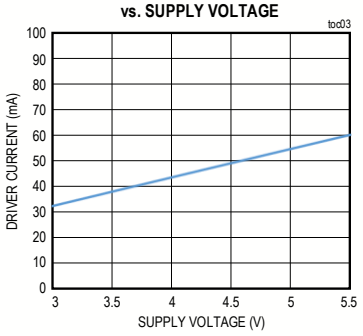
SUPPLY CURRENT vs. DATA RATE (V_{CC} = 3.3V)



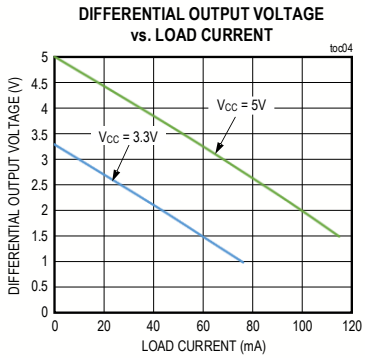
SUPPLY CURRENT vs. DATA RATE (V_{CC} = 5V)



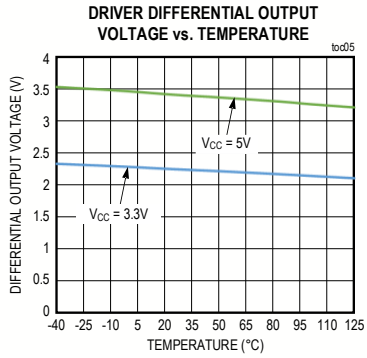
DRIVER CURRENT vs. SUPPLY VOLTAGE



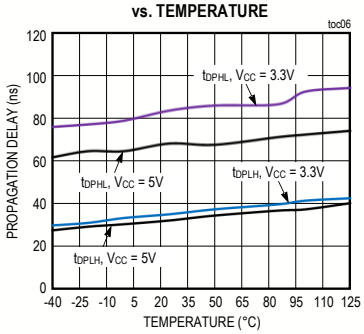
DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD CURRENT



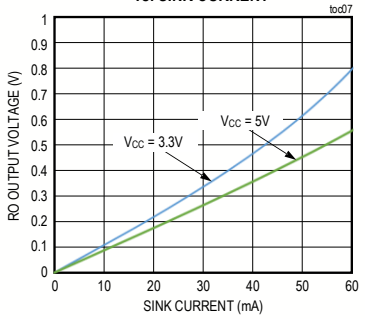
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



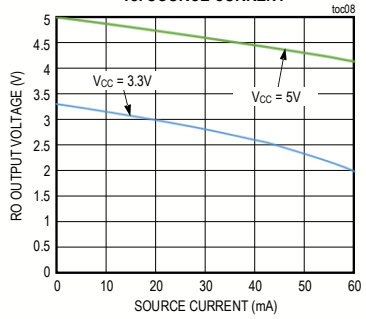
DRIVER PROPAGATION DELAY vs. TEMPERATURE



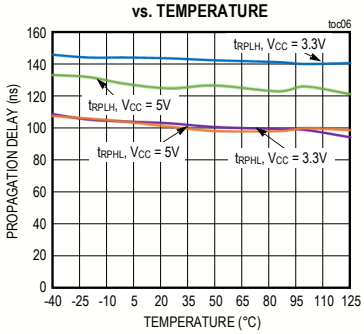
RO OUTPUT LOW vs. SINK CURRENT



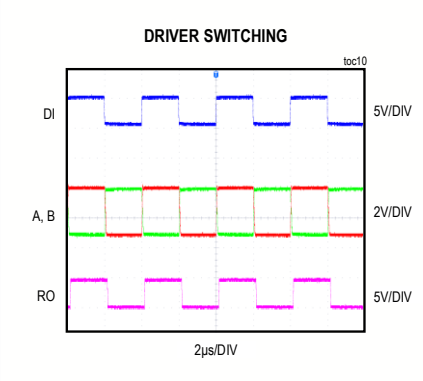
RO OUTPUT HIGH vs. SOURCE CURRENT



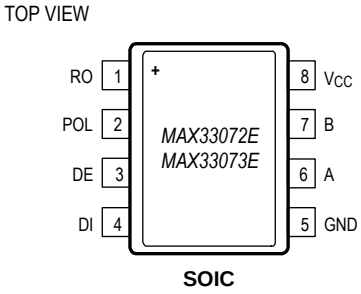
RECEIVER PROPAGATION DELAY vs. TEMPERATURE



(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)



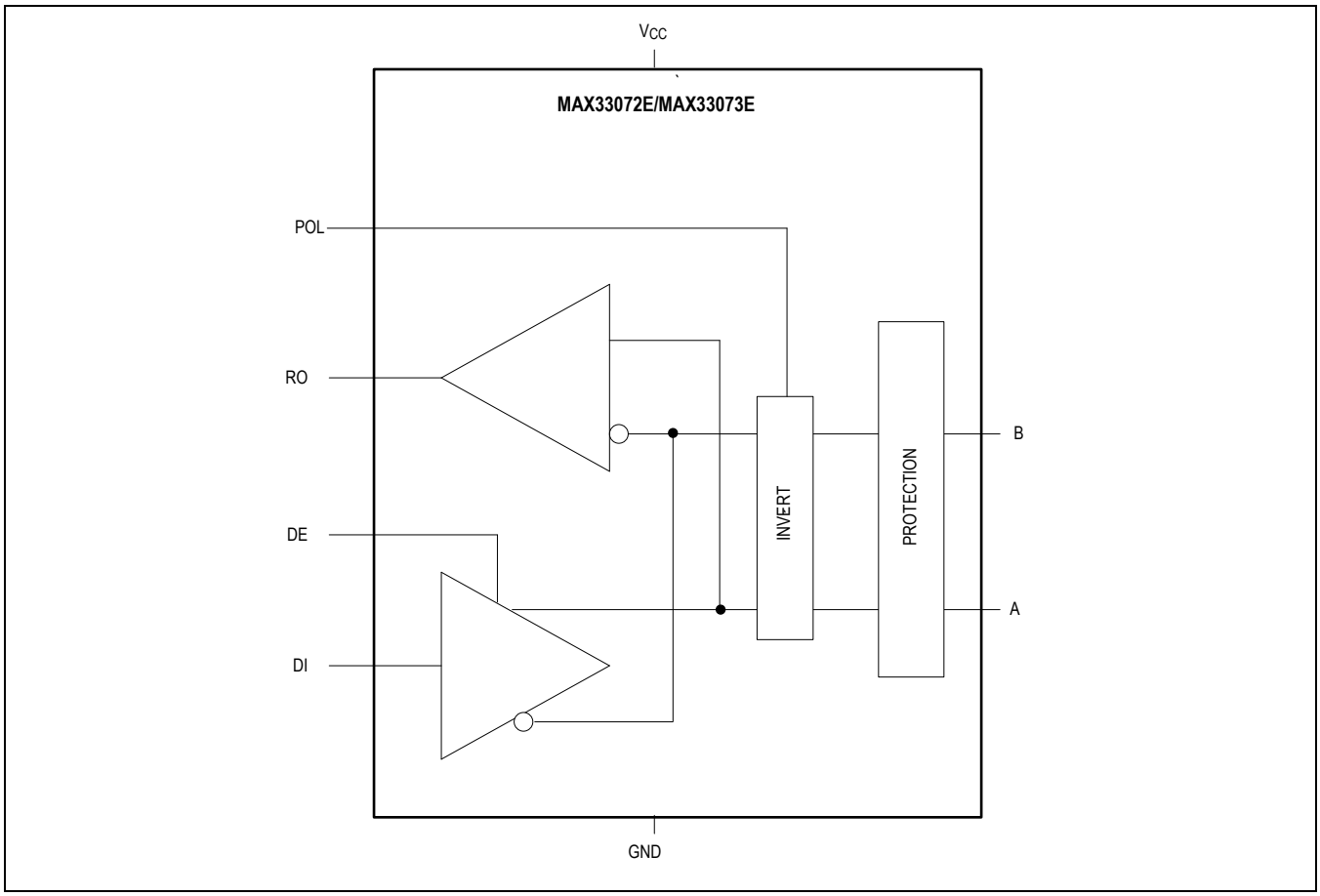
Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION
1	RO	Receiver Data Output. See Receiver Truth Table for more information.
2	POL	Polarity Select Input. Drive POL low for normal A/B operation. Drive POL high to switch A/B operation.
3	DE	Driver Output Enable. Drive DE high to enable the driver. Drive DE low or connect to GND to disable the driver. Receiver is always enabled.
4	DI	Driver Input. See Transmitter Truth Table for more information.
5	GND	Ground
6	A	Noninverting Driver Output/Receiver Input.
7	B	Inverting Driver Output/Receiver Input.
8	VCC	Power Supply Input. Bypass V_{CC} to GND with a 0.1µF capacitor as close as possible to the device.

Functional Diagrams



Detailed Description

The MAX33072E/MAX33073E half-duplex transceivers are optimized for RS-485/RS-422 applications that require ±65V protection from faults on communication bus lines. These devices contain one differential driver and one differential receiver. The devices feature a polarity phase reversal pin which enables a software controlled method of correcting mis-wired A/B data lines. These devices feature a 1/8 unit load, allowing up to 256 transceivers on a single bus. The MAX33072E supports a data rate up to 500kbps and the MAX33073E supports a data rate up to 2Mbps.

Driver

The driver accepts a single-ended, logic-level input (DI) and transfers it to a differential RS-485 level output on the A and B driver outputs. Set the driver enable input (DE) low to disable the driver. A and B are high impedance when the driver is disabled.

Table 1. Transmitter Truth Table

POL	DE	DI	A	B
0	1	0	0	1
0	1	1	1	0
1	1	0	1	0
1	1	1	0	1
X	0	X	High-Z	High-Z

Receiver

The receiver accepts a differential, RS-485 level on the A and B inputs and transfers it to a single-ended, logic-level output (RO). The receiver is always enabled, except during thermal shutdown. The state of the DE pin has no effect on the receiver.

Table 2. Receiver Truth Table

POL	(V_A - V_B)	RO
0	≥ -50mV	1
0	≤ -200mV	0
1	≤ 50mV	1
1	≥ 200mV	0
0	Open/Shorted	1
1	Open/Shorted	0

±65V Fault Protection

The driver outputs/receiver inputs of transceivers connected to an industrial RS-485 network often experience faults when shorted to voltages that exceed the -7V to +12V input range specified in the EIA/TIA-485 standard. Under such circumstances, ordinary RS-485 transceivers that have a typical absolute maximum voltage rating of -8V to +12.5V require costly external protection devices which can compromise the RS-485 performance.

To reduce system complexity and the need for external protection, the driver outputs/receiver inputs of the MAX33072E/MAX33073E are designed to withstand voltage faults of up to ±65V with respect to ground without damage. Protection is guaranteed regardless whether the transceiver is active, in shutdown or without power. When a fault is detected on A or B, the affected driver output is switched into a high-impedance state. After 300ms (typ), the driver output is re-enabled for 30µs (typ). If the fault condition persists, the driver output is again disabled. If the fault has been removed, the driver outputs remain on and the transceiver operates normally.

Driving a non-terminated cable may cause the voltage seen at the driver outputs (A or B) to exceed the absolute maximum voltage rating if the DI input is switched during a ±65V fault on the A or B pins. Therefore, a termination resistor is recommended in order to maximize the overvoltage fault protection while the DI input is being switched. If the DI input does not change state while the fault condition is present, the MAX33072E/MAX33073E will withstand up to ±65V on the RS-485 inputs, regardless of the termination status of the data cable.

±40V Common-Mode Range

RS-485 standards define the common-mode range as -7V to +12V for the receiver. For the MAX33072E and MAX33073E, the common-mode range exceeds the standard with ±40V for both the driver and receiver. This feature was specifically designed for systems where there is a large common-mode voltage present due to either nearby electrically noisy equipment or large ground differences due to different earth grounds or different power transformers. Two-way communication is possible with ±40V high common-mode range where other standard RS-485 transceivers would either fail, not transmit or receive, and/or cause data errors.

True Fail-Safe

The MAX33072E/MAX33073E guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. If the differential receiver input voltage (V_A - V_B) is greater than or equal to -50mV, RO is logic-high when POL is logic-low.

Hot-Swap Inputs

Inserting circuit boards into a hot, or powered backplane may cause voltage transients on DE, and receiver inputs A and B that can lead to data errors. For example, upon initial circuit board insertion, the processor undergoes a power-up sequence. During this period, the high impedance state of the output drivers makes them unable to drive the MAX33072E/MAX33073E DE input to a defined logic level. Meanwhile, leakage currents of up to 10µA from the high-impedance output, or capacitively coupled noise from V_{CC} or GND, could cause an input to drift to an incorrect logic state. To prevent such a condition from occurring, the MAX33072E/MAX33073E features hot-swap input circuitry on DE to safeguard against unwanted driver activation during hot-swap situations. When V_{CC} rises, an internal pulldown circuit holds DE low for at least 10µs. After the first transition on DE, the internal pulldown/pullup circuitry becomes transparent, resetting the hot-swap tolerable inputs.

Thermal Shutdown Protection

The MAX33072E/MAX33073E feature thermal-shutdown protection circuitry to protect the device. When the internal silicon junction temperature exceeds +160°C (typ), the driver outputs are disabled and RO is high impedance. Driver and receiver outputs are re-enabled when the junction temperature falls below +148°C (typ).

Applications Information

256 Transceivers on the Bus

The MAX33072E/MAX33073E transceivers have 1/8 unit load receiver, allowing for up to 256 MAX33072E/MAX33073E transceivers connected in parallel on a shared communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit loads on the line.

Typical Application

The MAX33072E/MAX33073E half-duplex transceivers are designed for bidirectional data communications on multipoint bus transmission lines. The Typical Application Circuit shows a typical network application's circuit. To minimize reflections, the bus should be terminated at the receiver inputs in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

Power Considerations for the MAX33072E/MAX33073E

At high data rates, the power dissipation of a half-duplex transceiver is determined by a number of factors, including:

- The data rate
- The time that the driver is transmitting
- The termination impedance
- The power supply voltage
- The external common-mode voltage

Higher data rates result in higher power dissipation due to switching losses in the transceiver. Switching losses increase even more when capacitance is applied to the A and B pins. External capacitance should be kept to a minimum to help reduce power dissipations at high data rates.

Similarly, the power dissipation in a transceiver is much higher when the driver is transmitting, compared to when the transceiver is receiving. In half-duplex communication, the period of transmission relative to the idle or receiving intervals (i.e., the duty cycle) should be taken into consideration when calculating the average power dissipation.

The line termination resistance/impedance determines the driver's load current during transmission and the differential output voltage (V_{OD}) on the driver is determined by the supply voltage. A higher supply voltage results in a larger differential output voltage at the driver driving the line, which in turn results in a higher current draw from the supply (I_{CC}). The power dissipation in the chip is calculated as the product of supply current times supply voltage, subtracting the power dissipated in the external termination resistor. If there is a common-mode voltage (higher than V_{CC}) present (Figure 1b), the transceiver will pull this voltage down to operating levels by sinking current into the A pin (or B pin, whichever is lower). This is factored into the following equation:

$$P_{DIS} = (V_{CC} \times I_{CC}) - (V_{OD}^2/R_L) + (V_{AB} \times I_{AB})$$

where $I_{AB} = ((V_{CM} – V_{AB})/375) + ((V_{CC}-V_{AB})/R_L)$.

Use the Typical Operation Characteristics to determine the supply current at a given supply voltage and data rate. For example, assuming a data rate of 500kbps with a 5V supply on a fully loaded bus with +40V common mode (Figure 1b), and assuming V_{AB} = 1.5V (the lower of A, B), we can calculate that the power dissipation (at room temperature) is:

$$P_{DIS} = (5V \times 65mA) - (3.4V^2/60\Omega) + (1.5V \times 160mA) = 564mW$$

Ensure that power dissipation of the transceiver is kept below the value listed in the Absolute maximum ratings to protect the device from entering thermal shutdown or from damage.

PCB Layout Considerations

PCB layout can affect the performance of the transceiver in conditions with high common-mode voltage at a high ambient temperature. In order to maximize thermal dissipation, it is recommended to:

1. Use large copper pads for all the pins.
2. Connect the GND pad to a large copper plane on the same layer or through vias to the bottom layer.

ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharge encountered during handling and assembly. The driver outputs and receiver inputs (A and B data lines) of the MAX33072E/MAX33073E have extra protection against static electricity. The ESD structures withstand high ESD in normal operation and when powered down. After an ESD event, the devices keep working without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs (A and B data lines) of the devices are characterized for protection to the cable-side ground (GNDB) to the following limits:

- ±40kV Human Body Model (HBM) per JEDEC JS-001-2017
- ±15kV using the Air Gap Discharge method specified in the IEC 61000-4-2
- ±10kV using the Contact Discharge method specified in the IEC 61000-4-2

The other non-data pins are also ESD protected, but at a lower level per the Electrical Characteristics table.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology and test results.

Human Body Model (HBM)

Figure 8 shows the HBM test model and *Figure 9* shows the current waveform it generates when discharged in a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

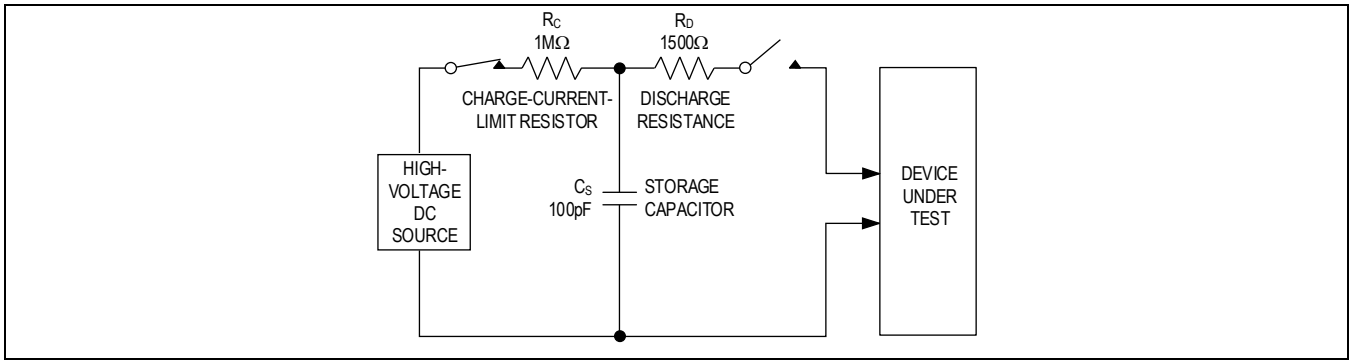


Figure 8. Human Body ESD Test Model

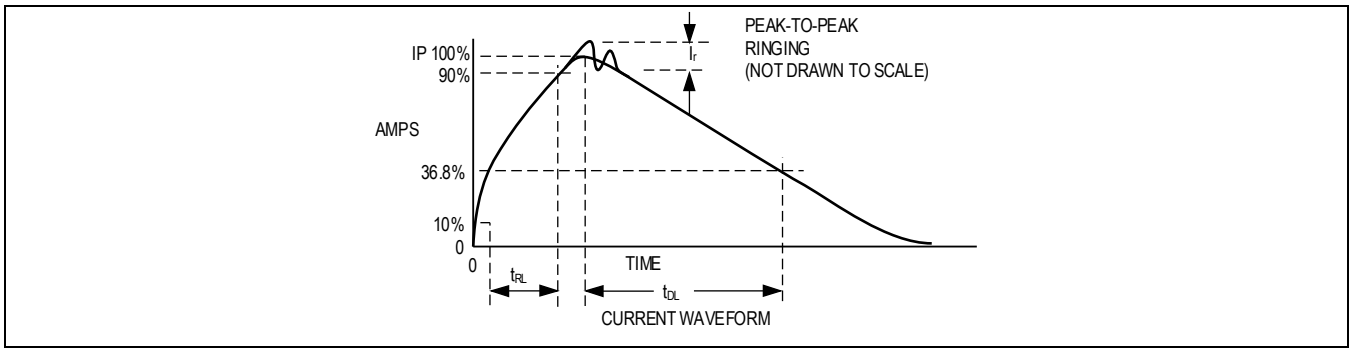


Figure 9. Human Body Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX33072E/MAX33073E help in designing equipment to meet IEC 61000-4-2 without the need for additional ESD protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM. *Figure 10* shows the IEC 61000-4-2 model and *Figure 11* shows the current waveform for IEC 61000-4-2 ESD Contact Discharge and Air Gap tests.

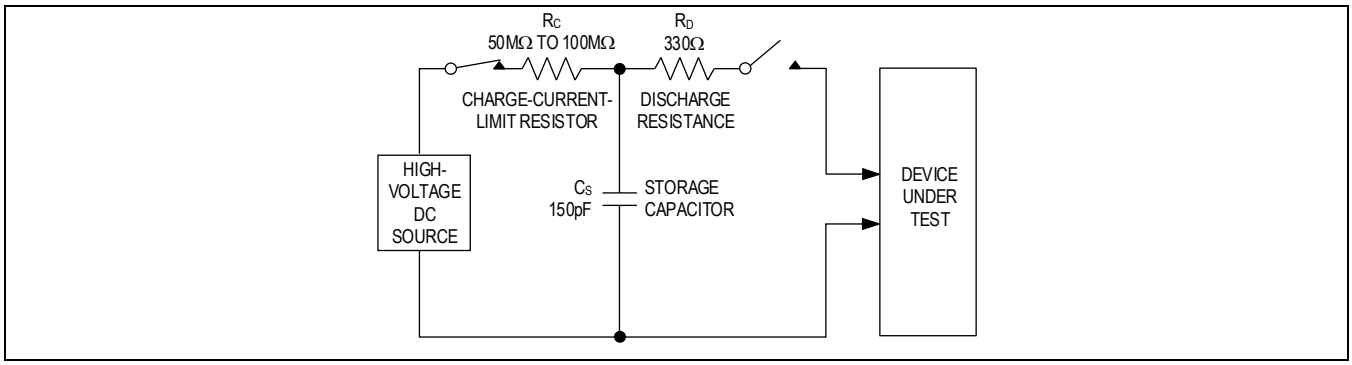


Figure 10. IEC 61000-4-2 ESD Test Model

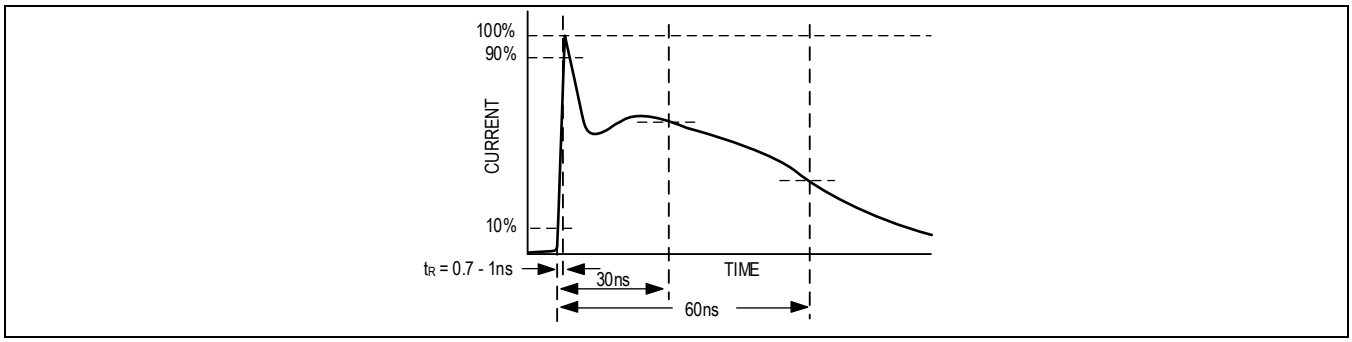
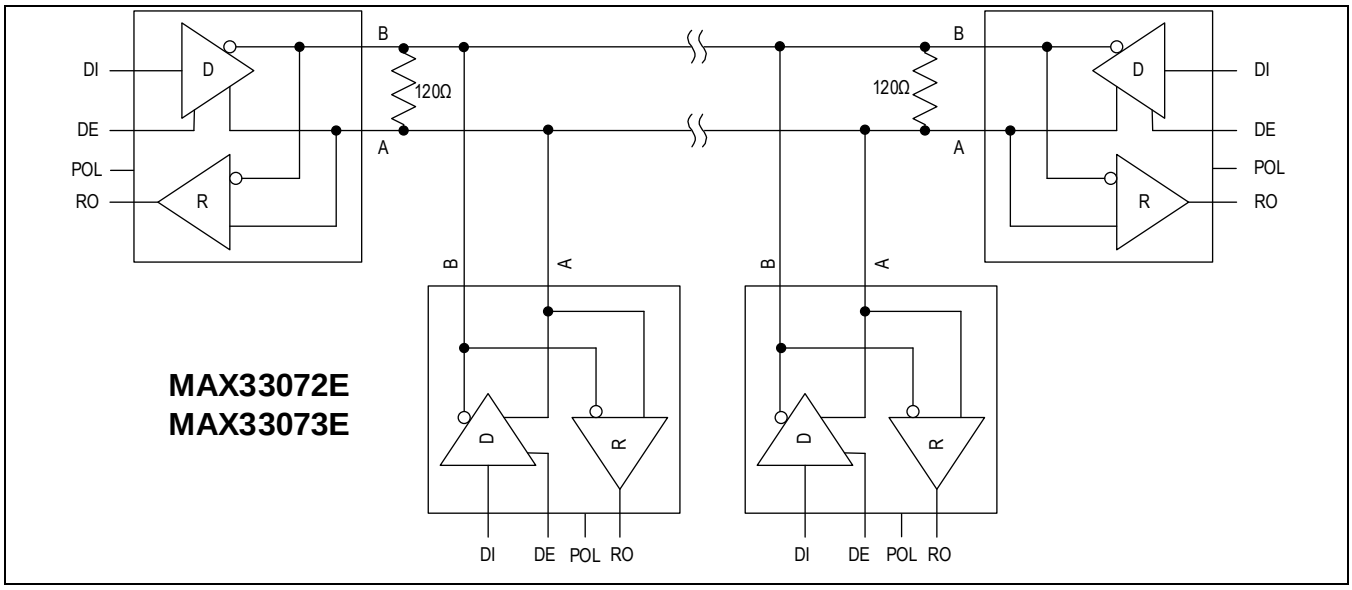


Figure 11. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuits

Typical RS-485 Network



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	MAXIMUM DATA RATE
MAX33072EASA+	-40°C to +125°C	8 SO	500kbps
MAX33072EASA+T	-40°C to +125°C	8 SO	500kbps
MAX33073EASA+*	-40°C to +125°C	8 SO	2Mbps
MAX33073EASA+T*	-40°C to +125°C	8 SO	2Mbps

+ = Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/20	Initial release	—
1	12/21	Updated *General Description*, *Electrical Characteristics* table, and Table 2	1, 4, 5, 11