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MAXIM

+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

General Description

The MAX3691 serializer is ideal for converting 4-bit-wide, 155Mbps parallel data to 622Mbps serial data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts low-voltage differential-signal (LVDS) clock and data inputs for interfacing with high-speed digital circuitry, and delivers a 3.3V PECL serial-data output. A fully integrated PLL synthesizes an internal 622Mbps serial clock from a 155.52MHz reference clock.

The MAX3691 is available in the extended-industrial temperature range (-40°C to +85°C), in a 32-pin TQFP package.

Applications

622Mbps SDH/SONET Transmission Systems
622Mbps ATM/SONET Access Nodes
Add/Drop Multiplexers
Digital Cross Connects

Features

- ◆ Single +3.3V Supply
- ◆ 155Mbps Parallel to 622Mbps Serial Conversion
- ◆ 215mW Power
- ◆ LVDS Parallel Clock and Data Inputs
- ◆ Differential 3.3V PECL Serial-Data Output

MAX3691

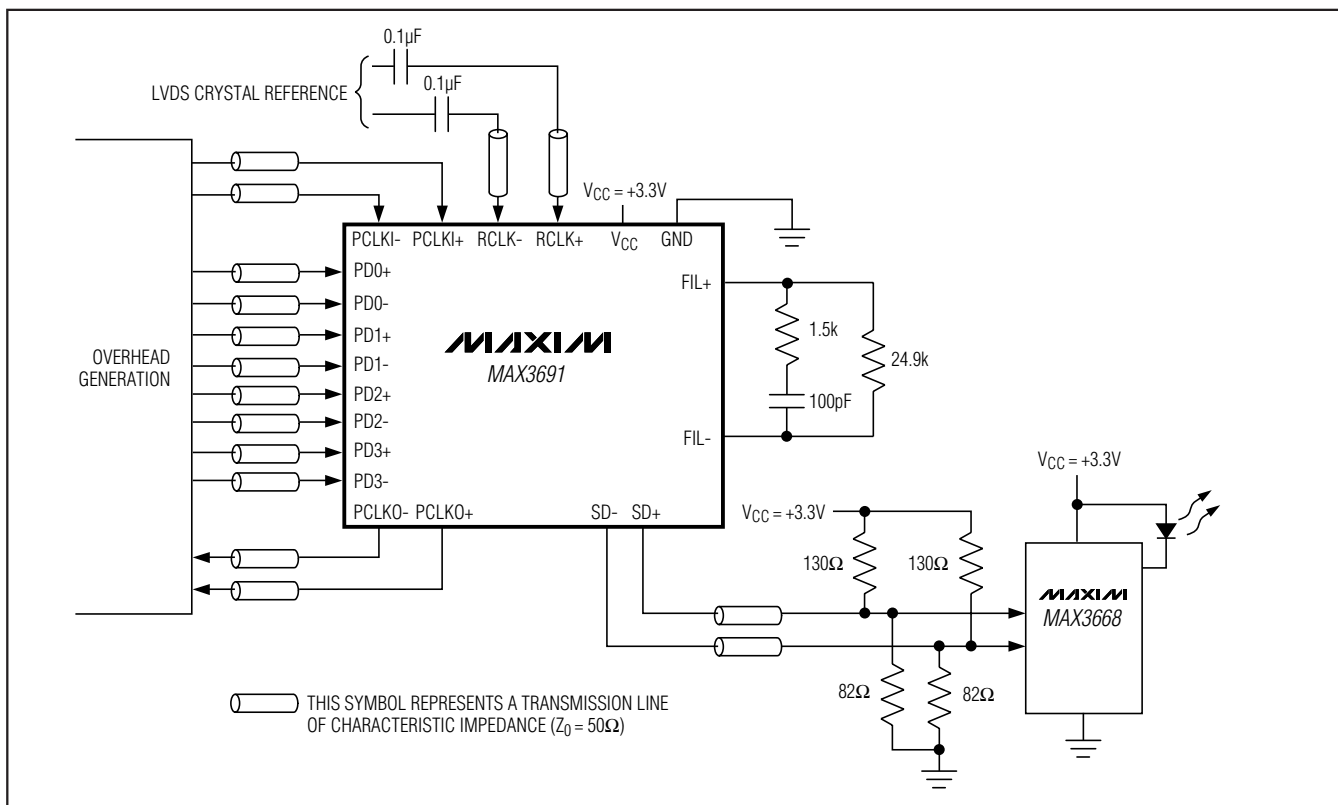
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3691ECJ	-40°C to +85°C	32 TQFP
MAX3691ECJ+	-40°C to +85°C	32 TQFP

+Denotes lead-free package.

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)		Continuous Power Dissipation ($T_A = +85^\circ\text{C}$)
VCC	-0.5V to 5V	TQFP (derate 10.20mW/°C above +85°C).....
All Inputs.....	-0.5V to (VCC + 0.5V)	Operating Temperature Range
Output Current		Storage Temperature Range
LVDS Outputs (PCLKO±).....	10mA	Lead Temperature (soldering, 10s).....
PECL Outputs (SD±).....	50mA	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(VCC = +3.0V to +3.6V, differential LVDS loads = 100Ω ±1%, PECL loads = 50Ω ±1% to (VCC - 2V), TA = -40°C to +85°C, unless otherwise noted. Typical values are at VCC = +3.3V, TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	ICC	PECL outputs unterminated	38	65	100	mA
PECL OUTPUTS (SD±)						
Output High Voltage	VOH	TA = +25°C to +85°C	VCC - 1.03	VCC - 0.88		V
		TA = -40°C	VCC - 1.08	VCC - 0.88		
Output Low Voltage	VOL	TA = +25°C to +85°C	VCC - 1.81	VCC - 1.62		V
		TA = -40°C	VCC - 1.95	VCC - 1.62		
LVDS INPUTS AND OUTPUTS (PCLKI±, RCLK±, PCLKO±, PD_±)						
Input Voltage Range	VI	Differential input voltage = 100mV	0		2.4	V
Differential Input Threshold	VIDTH	Common-mode voltage = 50mV	-100		100	mV
Threshold Hysteresis	VHYST			70		mV
Differential Input Resistance	RIN		85	100	115	Ω
Output High Voltage	VOH				1.475	V
Output Low Voltage	VOL		0.925			V
Differential Output Voltage	VOD		250		400	mV
Change in Magnitude of Differential Output Voltage for Complementary States	ΔVOD				25	mV
Output Offset Voltage	VOS	TA = +25°C	1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	ΔVOS				25	mV
Single-Ended Output Resistance	RO		40	70	140	Ω
Change in Magnitude of Single-Ended Output Resistance for Complementary States	ΔRO			±1	±10	%

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to $+3.6V$, differential LVDS load = $100\Omega \pm 1\%$, PECL loads = $50\Omega \pm 1\%$ to $(V_{CC} - 2V)$ $T_A = +25^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$.) (Note 1)

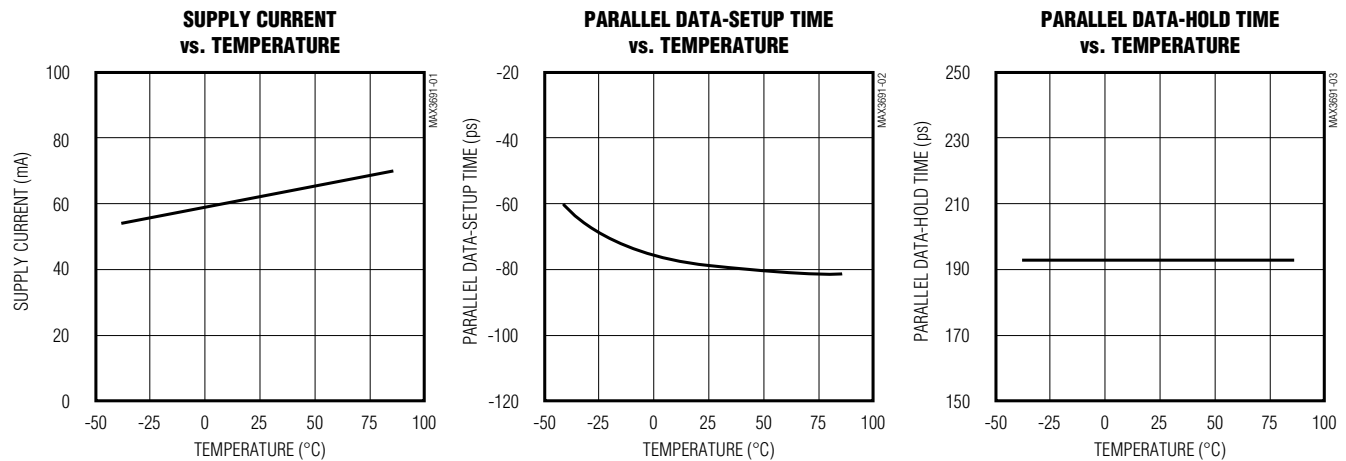
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Rate	f _{SCLK}			622.08		MHz
Parallel Data-Setup Time	t _{SU}		200			ps
Parallel Data-Hold Time	t _H		600			ps
PCLKO to PCLKI Skew	t _{SKEW}		-0.7		+3.3	ns
Output Jitter	Φ_0	$T_A = -40^\circ C$ to $+85^\circ C$ (Note 2)			13	ps _{RMS}
PECL Differential Output Rise/Fall Time	t _R , t _F			400		ps

Note 1: AC characteristics guaranteed by design and characterization.

Note 2: Assumes a 50% duty cycle $\pm 5\%$.

Typical Operating Characteristics

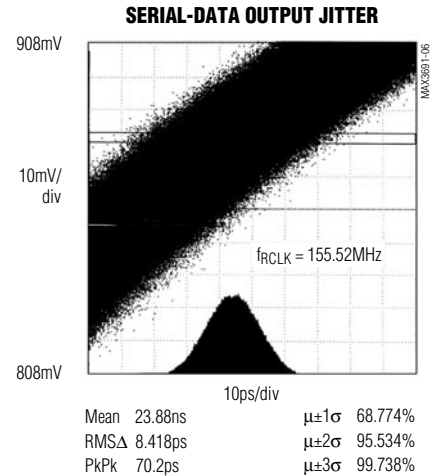
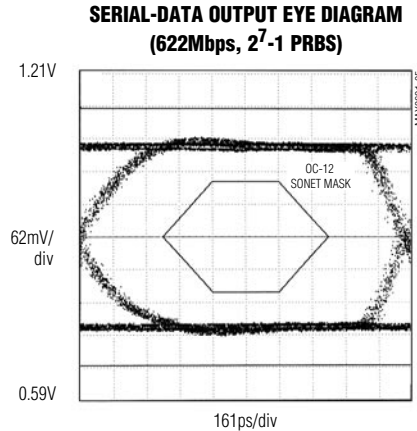
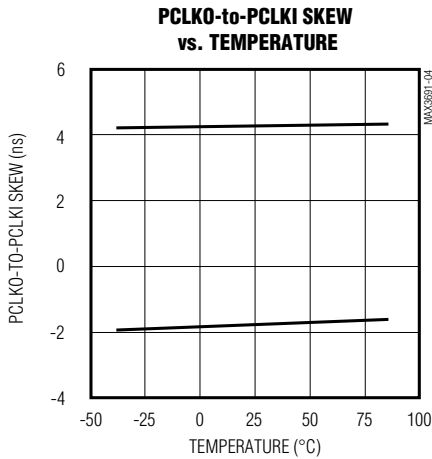
($V_{CC} = +3.0V$ to $+3.6V$, differential LVDS loads = 100Ω , unless otherwise noted.)



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Typical Operating Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, differential LVDS loads = 100Ω, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7	PD0+ to PD3+	Noninverting LVDS Parallel Data Inputs. Data is clocked in on the PCLKI signal's positive transition.
2, 4, 6, 8	PD0- to PD3-	Inverting LVDS Parallel Data Inputs. Data is clocked in on the PCLKI signal's positive transition.
9, 17, 18, 19, 24, 25, 32	GND	Ground
10	PCLKO-	Inverting LVDS Parallel-Clock Output. Use PCLKO to clock the overhead management circuit.
11	PCLKO+	Noninverting LVDS Parallel-Clock Output. Use PCLKO to clock the overhead management circuit.
12, 13, 16, 20, 21, 28, 29	V _{CC}	+3.3V Supply Voltage
14	SD-	Inverting PECL Serial-Data Output
15	SD+	Noninverting PECL Serial-Data Output
22	FIL-	Filter Capacitor Input. See <i>Typical Operating Circuit</i> for external-component connections.
23	FIL+	Filter Capacitor Input. See <i>Typical Operating Circuit</i> for external-component connections.
26	RCLK+	Noninverting LVDS Reference Clock Input. Connect (AC couple) a crystal reference clock (155.52MHz) to the RCLK inputs.
27	RCLK-	Inverting LVDS Reference Clock Input. Connect (AC couple) a crystal reference clock (155.52MHz) to the RCLK inputs.
30	PCLKI+	Noninverting LVDS Parallel Clock Input. Connect the incoming parallel-data-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal.
31	PCLKI-	Inverting LVDS Parallel Clock Input. Connect the incoming parallel-data-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal.

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Detailed Description

The MAX3691 serializer comprises a 4-bit parallel input register, a 4-bit shift register, control and timing logic, a PECL output buffer, LVDS input/output buffers, and a frequency-synthesizing PLL (consisting of a phase/frequency detector, loop filter/amplifier, and voltage-controlled oscillator). This device converts 4-bit-wide, 155Mbps data to 622Mbps serial data (Figure 1).

The PLL synthesizes an internal 622Mbps reference used to clock the output shift register. This clock is generated by locking onto the external 155.52MHz reference-clock signal (RCLK).

The incoming parallel data is clocked into the MAX3691 on the rising transition of the parallel-clock-input signal (PCLKI). The control and timing logic ensure proper operation if the parallel-input register is latched within a window of time that is defined with respect to the parallel-clock-output signal (PCLKO). PCLKO is the synthesized 622Mbps internal serial-clock signal divided by four. The allowable PCLKO-to-PCLKI skew is -0.7ns to +3.3ns. This defines a timing window at about the PCLKO rising edge, during which a PCLKI rising edge may occur. Figure 2 is the timing diagram.

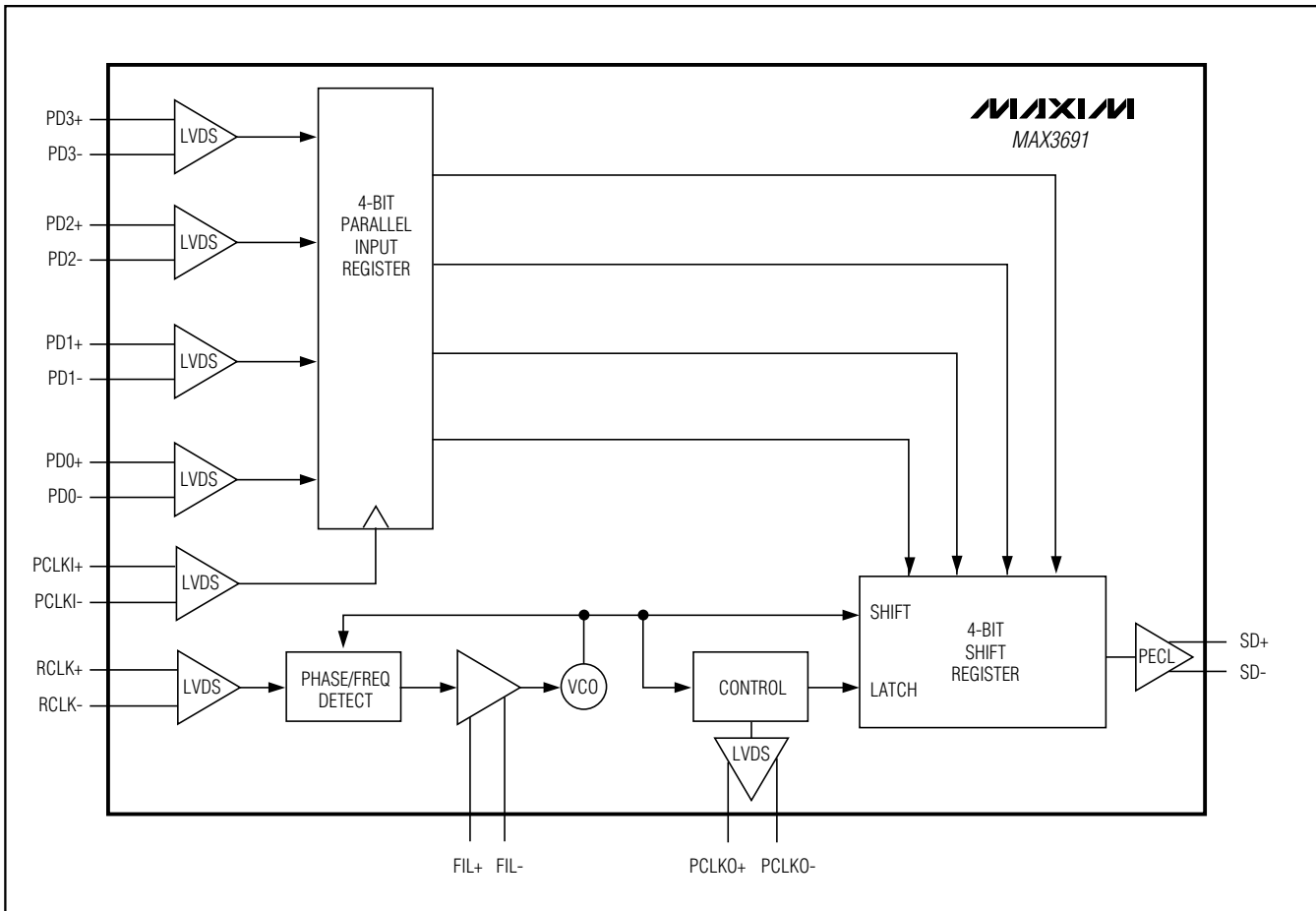


Figure 1. Functional Diagram

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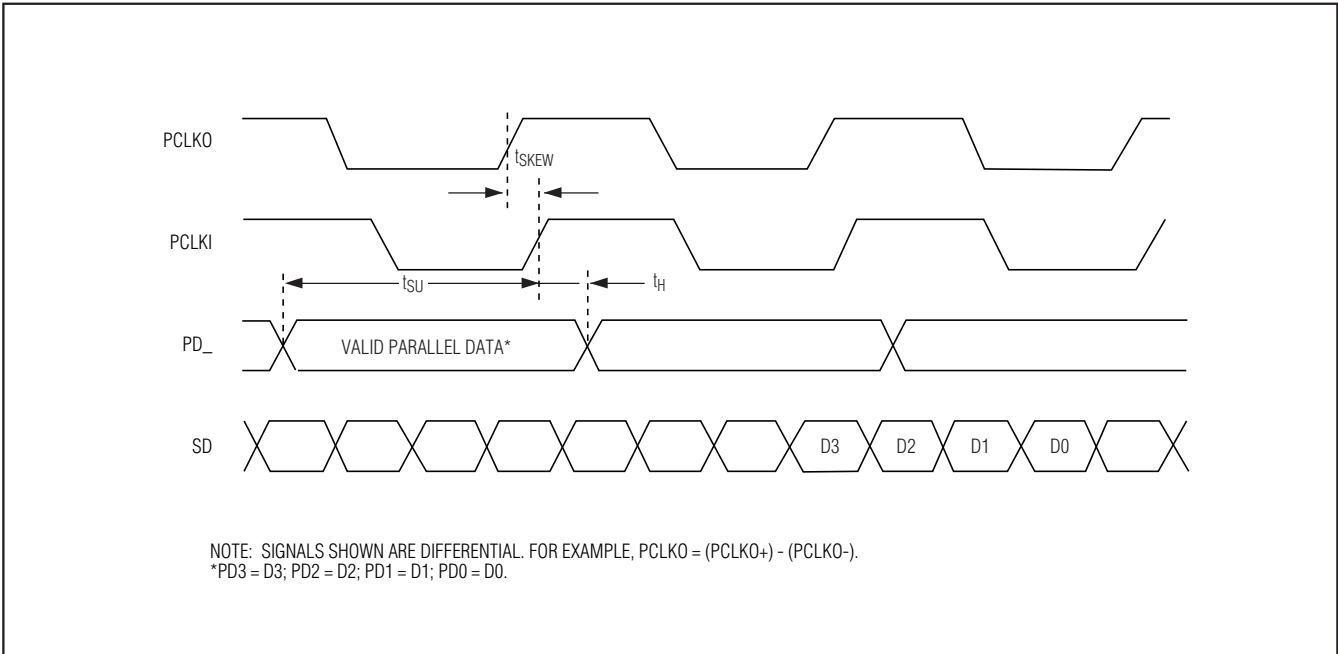


Figure 2. Timing Diagram

Low-Voltage Differential-Signal (LVDS) Inputs and Outputs

The MAX3691 features LVDS inputs and outputs for interfacing with high-speed digital circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses 250mV–400mV differential low-voltage swings to achieve fast transition times, minimized power dissipation, and noise immunity.

For proper operation, the parallel-clock LVDS outputs (PCLKO+, PCLKO-) require 100Ω differential DC termi-

nation between the inverting and noninverting outputs. Do not terminate these outputs to ground.

The parallel data and parallel clock LVDS inputs (PD_+, PD_-, PCLKI+, PCLKI-) are internally terminated with 100Ω differential input resistance, and therefore do not require external termination.

PECL Outputs

The serial-data PECL outputs (SD+, SD-) require 50Ω DC termination to (VCC - 2V). See the *Alternative PECL-Output Termination* section.

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Applications Information

Alternative PECL-Output Termination

Figure 3 shows alternative PECL output-termination methods. Use Thevenin-equivalent termination when a ($V_{CC} - 2V$) termination voltage is not available. If AC coupling is necessary, be sure that the coupling capacitor is placed following the 50Ω or Thevenin-equivalent DC termination.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled-impedance transmission lines to interface with the MAX3691 clock and data inputs and outputs.

Pin Configuration

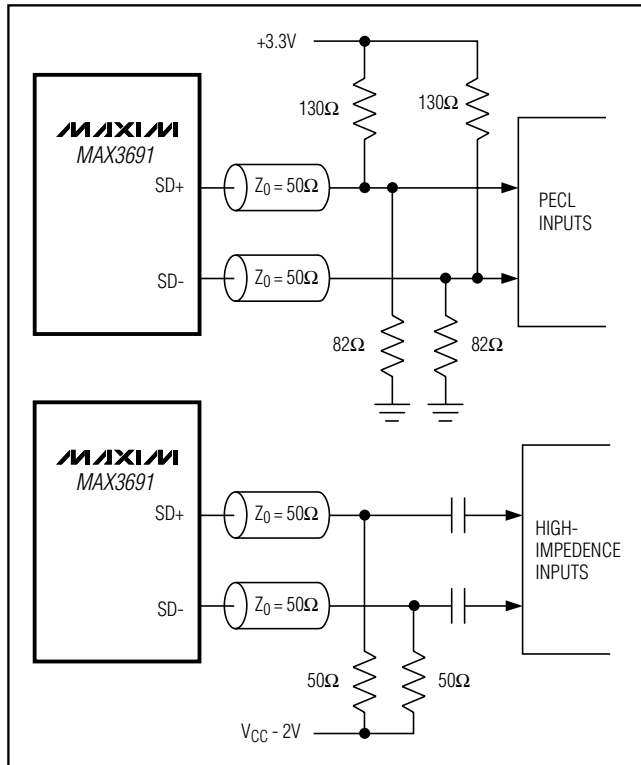
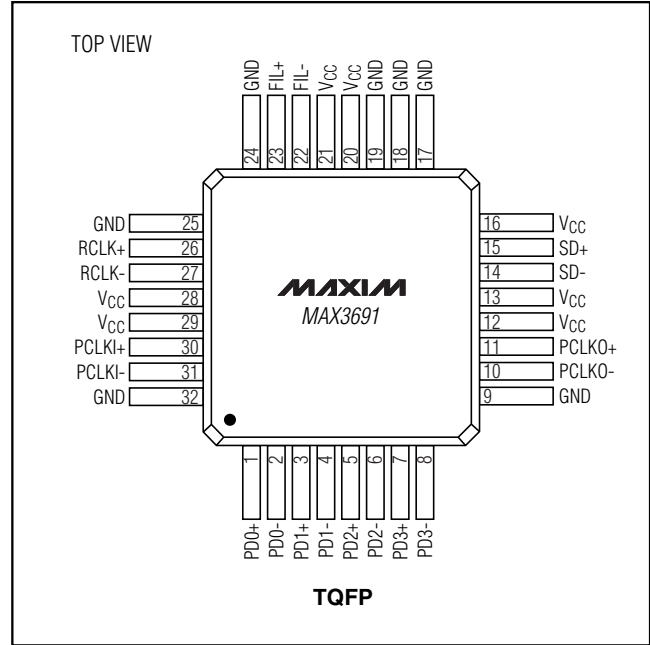


Figure 3. Alternative PECL-Output Termination

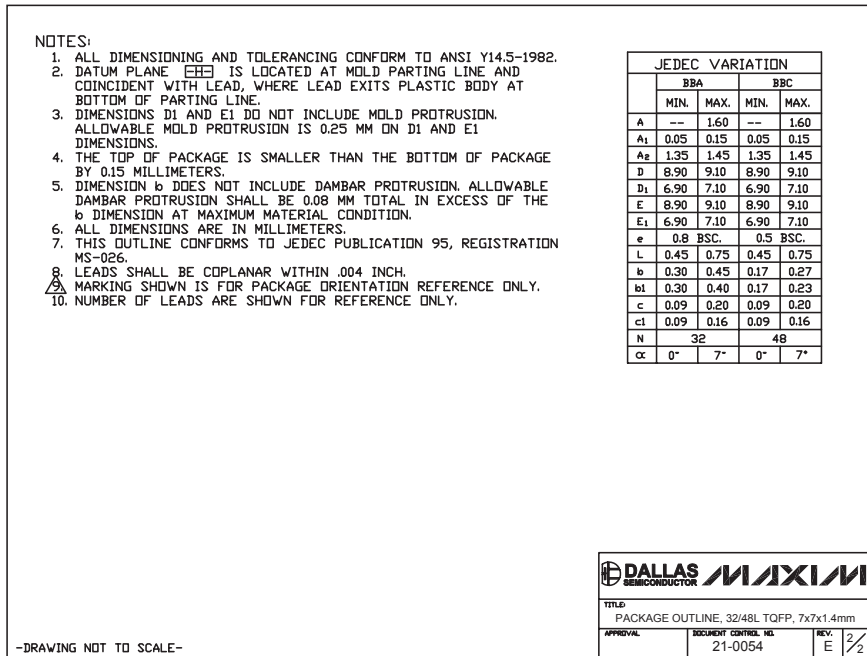
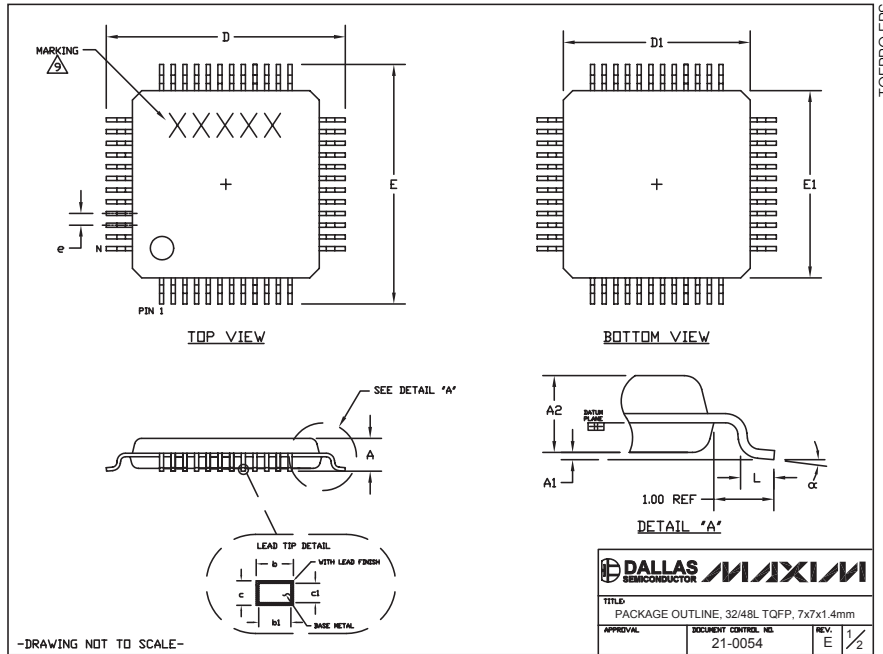
Chip Information

TRANSISTOR COUNT: 1633

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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