MAX38886

2.5V to 5.0V, 0.5A/2.5A, Charge/Discharge Regulator for Supercapacitor Backup Applications

General Description

The MAX38886 is a storage capacitor or capacitor bank backup regulator designed to efficiently transfer power between a storage element and a system supply rail in reversible buck and boost operations using the same inductor.

When the main supply is present and above the minimum system supply voltage, the regulator operates in buck mode and charges the storage element at up to 500mA peak inductor current. Once the storage element is charged, the circuit draws only 2.5µA of current while it maintains the supercapacitor or other storage element in its ready state. When the main supply is removed, the regulator operates in boost mode and prevents the system from dropping below the minimum operating voltage, discharging the storage element at up to 2.5A peak inductor current.

The MAX38886 is externally programmable for minimum and maximum voltage of the storage element, such as supercapacitor, minimum system voltage, and maximum charge and discharge currents. The internal DC-DC converter requires only a 1µH inductor.

Applications

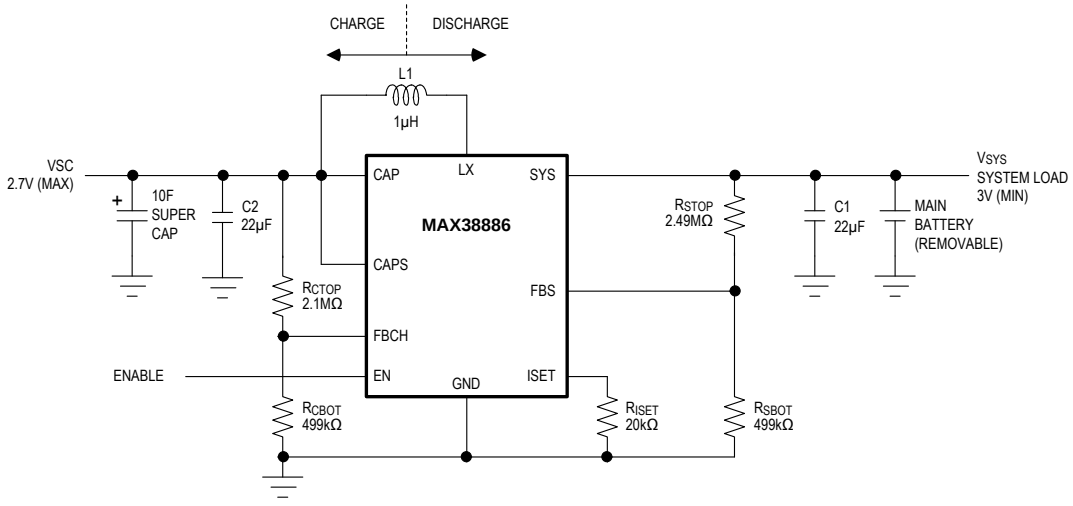
- Handheld Industrial Equipment
- Portable Computers
- Portable Devices with a Removable Battery

Benefits and Features

- 2.5V to 5V System Output Voltage
- Up to 4.5V Capacitor Voltage Range
- Up to 2.5A Peak Inductor Discharge Current
- Programmable Voltage and Current Thresholds
- ±2% Threshold Accuracy
- Up to 95% Efficiency, Charge or Discharge
- 2.5µA Ready Quiescent Current
- Small Solution Size
  - 3mm x 3mm x 0.75mm TDFN Package

***Ordering Information** appears at the end of data sheet.*

Simplified Block Diagram



Absolute Maximum Ratings

CAP, EN, SYS, LX to GND ..... -0.3V to +6V

FBCH to GND ..... -0.3V to CAP +0.3V

FBS, ISET to GND ..... -0.3V to SYS +0.3V

PGND to GND ..... -0.3V to +0.3V

LX RMS Current ..... +2.0A_{RMS}

Continuous Power Dissipation (T_A = +70°C, TDFN, derate 24.4mW/°C above +70°C) 1951.2mW

Output Short-Circuit Duration ..... Continuous

Operating Temperature Range ..... -40ºC to +125ºC

Storage Temperature Range ..... -65ºC to +150ºC

Maximum Junction Temperature ..... +150ºC

Lead Temperature (Soldering,10 seconds) ..... +300ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	T1433+2C
Outline Number	21-0137
Land Pattern Number	90-0063
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W

For the latest package outline information and land patterns (footprints), go to https://www.maximintegrated.com/en/design/packaging.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{SYS} = 3.7V, V_{CAP} = 2.7V, Typical values are at T_J = -40ºC to +125ºC, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS Voltage Range	V_{SYS}		2.5		5	V
CAP Voltage	V_{CAP}				4.5	V
Min CAP Voltage	V_{CAP}			0.5		V
SYS Shutdown Current	I_{SYS_SD}	EN = 0V, T_A = +25ºC		0.01	1	µA
		EN = 0V		0.1		
SYS Charging Supply Current	I_{SYS_CHG}	V_{FBS} = 0.6V, V_{FBCH} = 0.485V		1.5		mA
SYS Backup Supply Current	I_{SYS_BUP}	V_{FBS} = V_{FBCH} = 0.515V, T_A = +25°C		35	65	µA
		V_{FBS} = V_{FBCH} = 0.515V		35		
SYS Ready Supply Current	I_{SYS_RDY}	V_{FBS} = 0.6V, V_{FBCH} = 0.515V, T_A = +25°C		2.5	5	µA
		V_{FBS} = 0.6V, V_{FBCH} = 0.515V		2.5		
CAP Shutdown Current	I_{CAP_SD}	EN = 0V, T_A= +25ºC		0.01	1	µA

(V_{SYS} = 3.7V, V_{CAP} = 2.7V, Typical values are at T_J = -40ºC to +125ºC, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		EN = 0V		0.1		
UVLO Threshold	V_{UVLOF}	V_{VSYS} falling, 100mV typical hysteresis	1.7	1.8	1.9	V
FBS Backup Voltage	V_{FBS}	FBS rising, when discharging stops	-2%	0.5	+2%	V
FBS Charging Threshold	$V_{TH\_FBS\_CHG}$	Above FBS backup voltage, when charging begins, 30mV typical hysteresis	25	60	95	mV
FBCH Threshold	V_{TH_FBCH}	FBCH rising, when charging stops, 25mV typical hysteresis	-2%	0.5	2%	V
EN Threshold	V_{IL}	When LX stops switching, EN falling	225	600		mV
	V_{IH}	EN rising		660	925	
ISET Resistor Range	R_{ISET}	Guaranteed by LX peak current limits	20		100	kΩ
LX Peak Backup Current Limit (Note 1)	I_{DCHG}	Circuit of *Figure 1*, V_{CAP} = 2V, V_{SYS} = 2.9V, R_{ISET} = 20kΩ	2.0	2.5	3.0	A
		Circuit of *Figure 1*, V_{CAP} = 2V, V_{SYS} = 2.9V, R_{ISET} = 100kΩ		0.5		
LX Peak Charge Current Limit (Note 1)	I_{CHG}	Circuit of *Figure 1*, V_{SYS} = 3.7V, V_{CAP} = 2V, R_{ISET} = 20kΩ	400	500	600	mA
		Circuit of *Figure 1*, V_{SYS} =3.7 V, V_{CAP} = 2V, R_{ISET} = 100kΩ		100		
FBS/FBCH Input Bias Current	$I_{FBS/FBCH}$	$V_{FBS/FBCH}$ = 0.5V, T_A = +25°C	-0.1	0.001	0.1	µA
		$V_{FBS/FBCH}$ = 0.5V		0.01		
EN Input Leakage Current	I_{EN}	0V < V_{EN} < 5.5V, T_A = +25°C	-0.1	0.001	0.1	µA
		0V < V_{EN} < 5.5V		0.01		
LX Switching Frequency	f_{SW}	Delivering maximum current from CAP		2		MHz
LX Low-Side FET Resistance	R_{LOW}	V_{SYS} = 3V, LX switched to GND		50	100	mΩ
LX High-Side FET Resistance	R_{HIGH}	V_{SYS} = 3V, LX switched to SYS		80	160	mΩ
LX Leakage Current	I_{LX_LKG}	V_{EN} = 0V, V_{SYS} = 5V, V_{LX} = 0V/5V, T_A = +25°C	-1		1	µA
		V_{EN} = 0V, V_{SYS} = 5V, V_{LX} = 0V/5V		0.1		
Maximum On-Time	t_{ON}	Backup mode, V_{FBS} = 0.485V	320	400	480	ns
Minimum Off-Time	t_{OFF}	Backup mode, V_{FBS} = 0.485V	80	100	120	ns
Overtemperature Lockout Threshold	T_{OTLO}	T_J rising, 15°C typical hysteresis		165		°C
High-Side FET Zero-Crossing (Note 1)	I_{ZXP}	Circuit of *Figure 1*, V_{CAP} = 2V, V_{SYS} = 2.9V	25	50	75	mA
Low-Side FET Zero-Crossing (Note 1)	I_{ZXN}	Circuit of *Figure 1*, V_{SYS} = 3.7V, V_{CAP} = 2V	25	50	75	mA

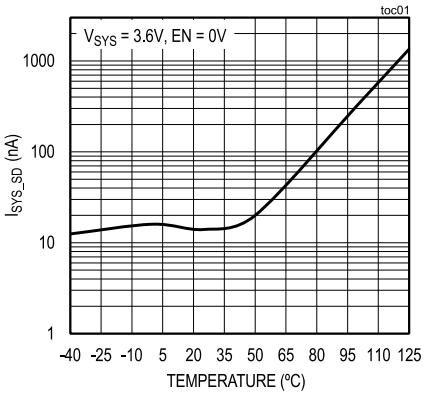
Note 1: DC measurement, actual zero-crossing and peak current accuracy in circuit will be affected by the propagation delay time.

Note 2: Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at T_J = +25ºC only.

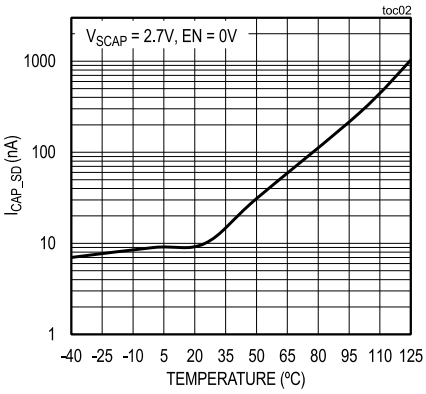
Typical Operating Characteristics

(MAX38886, V_{SYS} = 3.6V, V_{CAP} = 2.0V, C1 = 22µF, C2 = 22µF, T_A = +25°C, unless otherwise noted.)

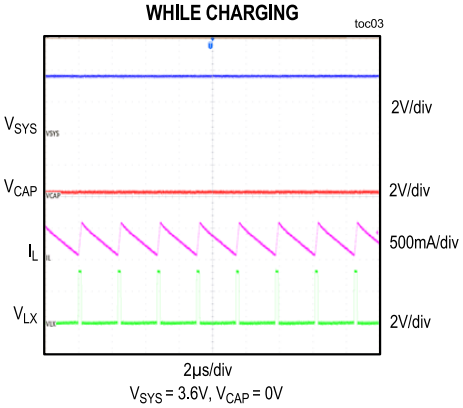
SYS PIN SHUTDOWN CURRENT



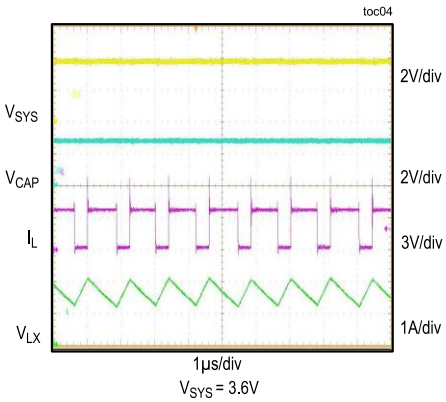
CAP PIN SHUTDOWN CURRENT



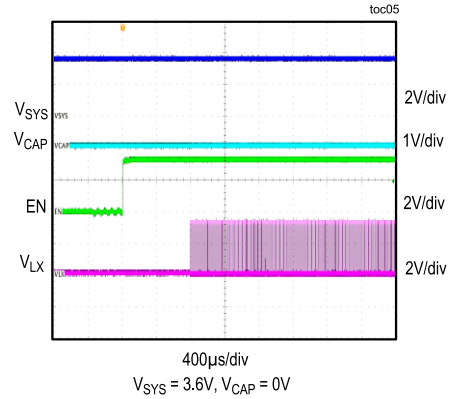
SWITCHING WAVEFORM WHILE CHARGING



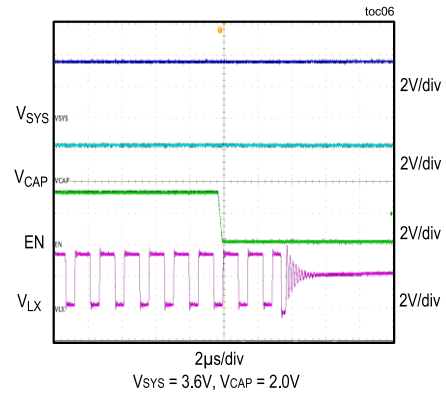
SWITCHING WAVEFORM HEAVY LOAD



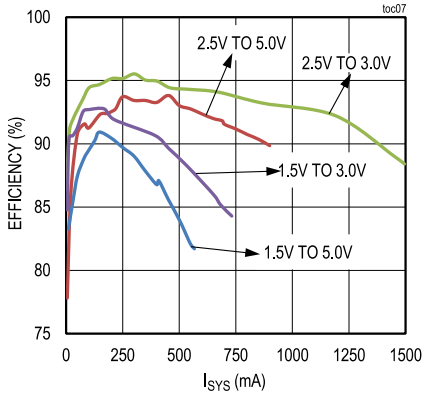
POWER-UP



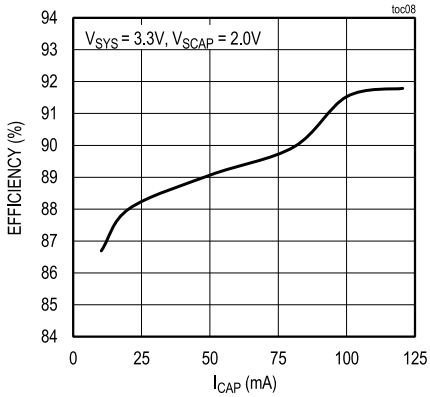
POWER-DOWN



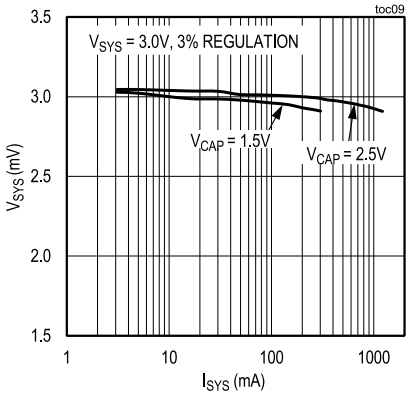
EFFICIENCY DURING BOOST MODE



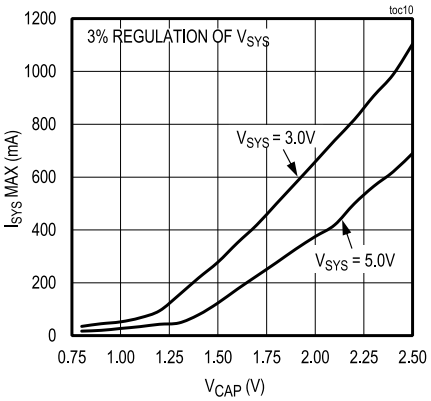
EFFICIENCY DURING BUCK MODE

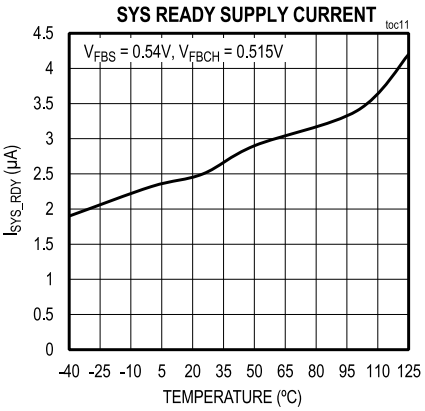


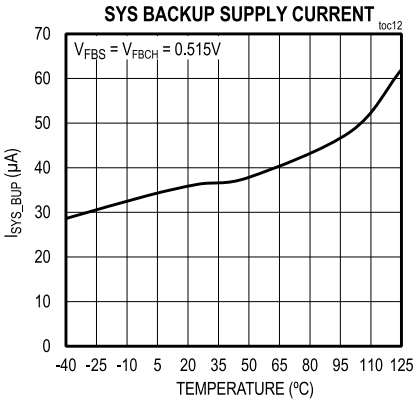
LOAD REGULATION DURING BOOST



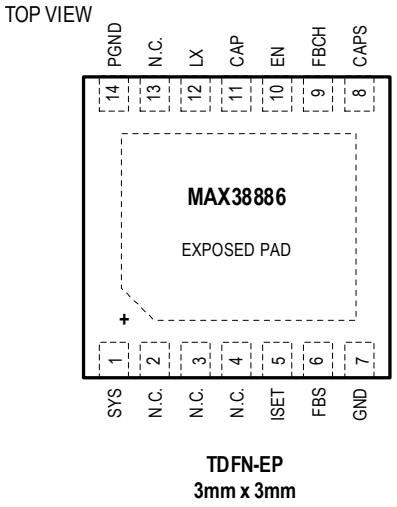
I_{SYS} MAX vs. V_{CAP}







Pin Configurations



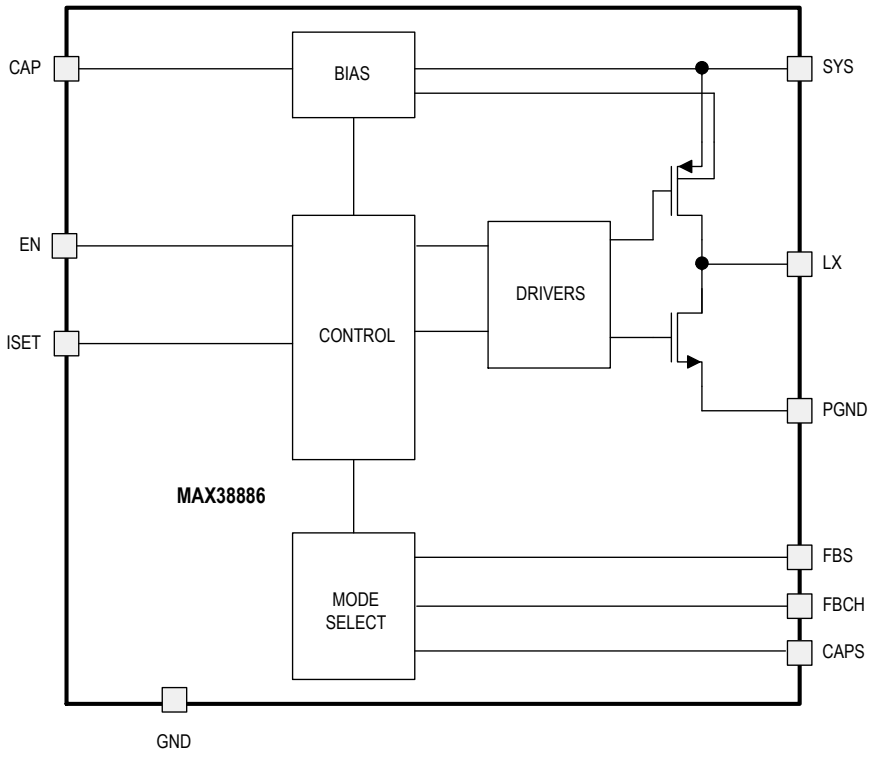
TDFN-EP
3mm x 3mm

Pin Descriptions

PIN	NAME	FUNCTION
1	SYS	System Supply Rail. Connect to a system supply rail or removable battery between 2.5V and 5V and bypass with a 22µF capacitor to GND.
2	NC	No Connect
3	NC	No Connect
4	NC	No Connect
5	ISET	Charge/Discharge Current Select Input. The peak discharge current is set by 50kV/R_{ISET} while the peak charging current is 1/5 the discharging current.
6	FBS	SYS Feedback Input. Connect to the center point of a resistor divider from SYS to GND. SYS will boost to 0.5V x (1 + R_{STOP}/R_{SBOT}) when V_{FBS} < 0.5V.
7	GND	Analog Ground
8	CAPS	CAP Sense Input. Connect to CAP pin.
9	FBCH	CAP Feedback Input. Connect to the lower point of a resistor-divider from CAP to GND.

		CAP will charge to 0.5V x (1 + R_{CTOP}/R_{CBOT}) when V_{FBS} > 0.56V.
10	EN	Enable Input. Force this pin high to enable the regulator or force pin low to disable the part and enter shutdown. If not driven, tie it to the SYS rail.
11	CAP	Super Cap. Connect to a supercapacitor input.
12	LX	Inductor Switching Node. Connect a 1.0µH to 4.7µH inductor from LX to CAP.
13	NC	No Connect
14, EP	PGND	Power Ground

Functional Diagram



Detailed Description

The MAX38886 is a flexible storage capacitor or capacitor bank backup regulator that efficiently transfers power between a storage element and a system supply rail.

When the main supply is present and its voltage above the minimum system supply voltage, the regulator operates in the charging mode of operation and charges the storage element at up to 500mA peak inductor current.

When the main supply is removed, the regulator prevents the system from dropping below the minimum operating voltage, boosting V_{SYS} by discharging the storage element at up to 2.5A peak inductor current. For backup mode functioning, ensure that the supercapacitor is charged up to 2.7V. During this backup mode of operation, the MAX38886 utilizes a fixed on-time, current-limited, pulse-frequency-modulation (PFM) control scheme. When V_{SYS} is applied for the first time, ensure that the supercapacitor is charged to 2.7V to activate backup mode.

The external pins allow a wide range of system and storage element, such as supercapacitor voltage settings, as well as charging and discharging peak inductor current settings.

The MAX38886 implements a True Shutdown™ feature disconnecting V_{SYS} from V_{CAP}, as well as protecting against a SYS short or if $V_{CAP} > V_{SYS}$.

Application Circuit

The typical application of the MAX38886 is shown in *Figure 1*.

Supercapacitor Voltage Configuration

The maximum supercapacitor voltage is set using a resistor-divider from CAP to FBCH to GND. The recommended value for R_{CBOT} is 499kΩ. Because resistor tolerance has a direct effect on voltage accuracy, these resistors should have 1% accuracy or better.

$$R_{CTOP} = R_{CBOT} \times ((V_{CAPMAX}/0.5) - 1)$$

V_{CAP} halts charging when V_{FBCH} reaches 0.5V. The maximum supercapacitor voltage is where the supercapacitor remains after it is completely charged.

The supercapacitor supports backup until the voltage across it reaches 500mV (typ).

The duty cycle limitation of the boosting phase is 80% (typ).

The MAX38886 detects when V_{SYS} falls below V_{CAP}. The device will not enable if V_{SYS} is below V_{CAP}. Raising V_{SYS} above the backup threshold re-initiates charging and backup.

System Voltage Configuration

The minimum system voltage is set using a resistor-divider from SYS to FBS to GND. Recommended value for R_{SBOT} is 499kΩ. Because resistor tolerance has a direct effect on voltage accuracy, these resistors should have 1% accuracy or better.

$$R_{STOP} = R_{SBOT} \times ((V_{SYSMIN}/0.56) - 1)$$

When V_{FBS} is above 0.56V, the DC-DC regulator draws power from the SYS pin to charge the supercapacitor to the maximum voltage set by FBCH and be ready for backup. When the main battery is removed, V_{FBS} drops to 0.5V and the SYS pin is regulated to the programmed minimum voltage with up to 2A of CAP current.

Charge/Discharge Current Configuration

The peak inductor discharge current is set by placing a resistor from ISET to GND. The values of R_{ISET} resistor is calculated by following formula:

$$I_{DISCHARGE} = 2.5A \times (20k\Omega/R_{ISET})$$

The supercapacitor charging current is internally set to 1/5 of the discharge current.

$$I_{CHARGE} = 0.5A \times (20k\Omega/R_{ISET})$$

A value of R_{ISET} between 20kΩ and 100kΩ is recommended to ensure accurate current compliance.

Typical Application Circuits

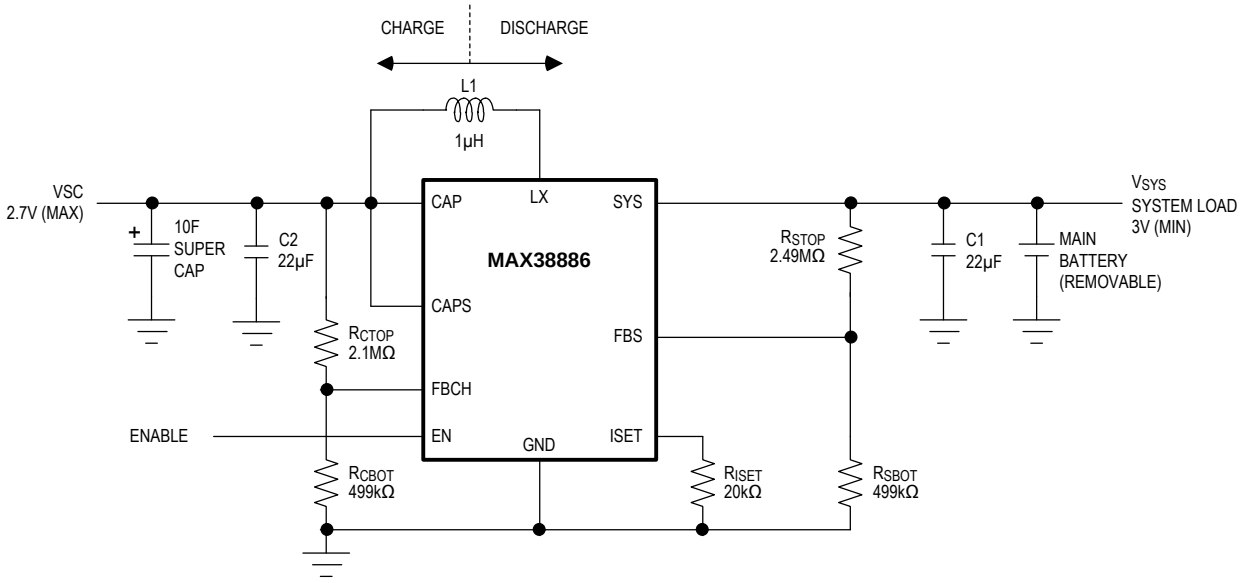


Figure 1. Typical Application

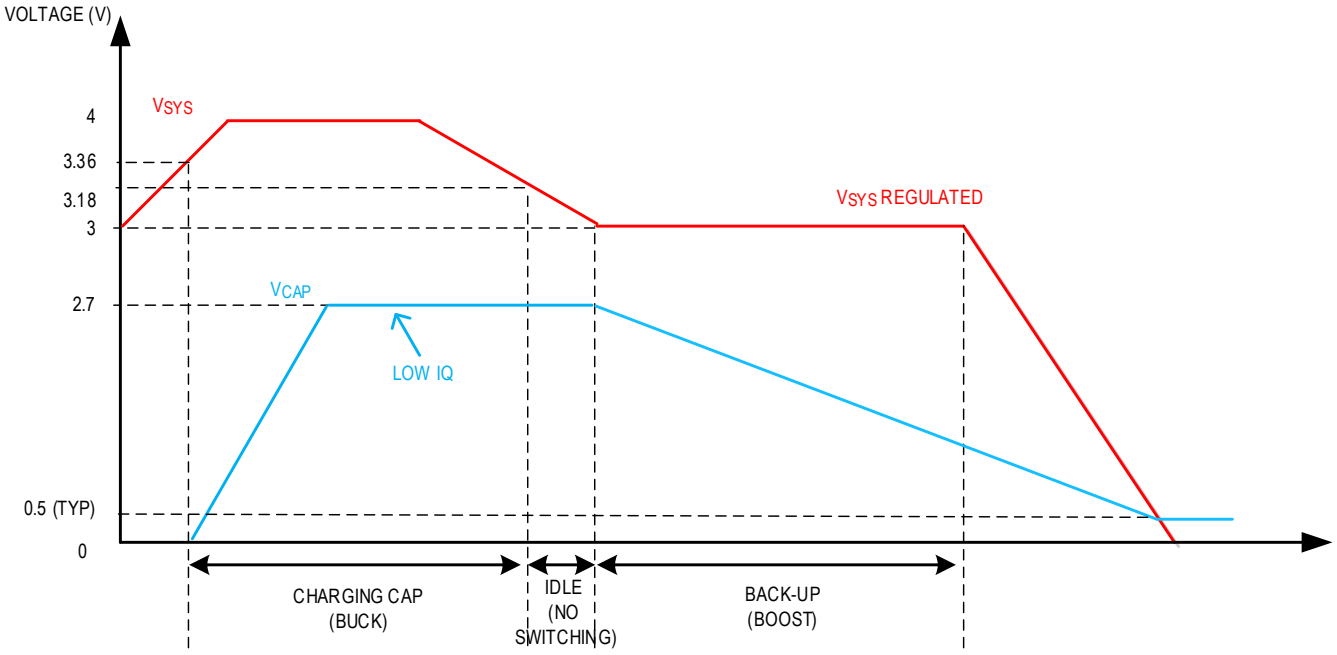


Figure 2. Charging/Discharging Waveforms

Applications Information

Capacitor Selection

Capacitors at SYS and CAP pins reduce current peaks and increase efficiency. Ceramic capacitors are recommended because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. Choose an acceptable dielectric such as X5R or X7R. Due to ceramic capacitors' capacitance derating with DC bias standard 22µF ceramic capacitors are recommended at both pins for most applications.

Supercapacitor Selection

When the power source supplying the V_{SYS} voltage is removed, power to the output is provided by the MAX38886 operating in the backup or boost mode of operation using the supercapacitor as its source. In order to ensure the supply voltage stays in regulation, the amount of power the supercapacitor can deliver at its minimal voltage should be greater than that required by the system. The MAX38886 presents a constant power load to the supercapacitor where smaller current is pulled out of the supercapacitor near its maximum V_{CAP} voltage. However, current drawn from the supercapacitor increases as it discharges to maintain constant power at the load. The amount of energy required in the backup mode is the product of the constant backup power and time defined as backup time, t_{BACKUP}. The amount of energy available in the supercapacitor is calculated using the following formula:

$$E = 1/2 \times C_{SCAP} \times (V_{CAPMAX}^2 - V_{CAPMIN}^2) \text{ (J)}$$

The amount of energy required to complete the backup equals to:

$$E = V_{SYS} \times I_{SYS} \times t_{BACKUP} \text{ (J)}$$

where, I_{SYS} will be the system load during backup.

Since energy required at the system side during the backup event comes from available energy in the supercapacitor, and assuming conversion efficiency η, and given t_{BACKUP}, the required C_{SCAP} is determined by the following equation:

$$C_{SCAP} = (2 \times V_{SYS} \times I_{SYS} \times t_{BACKUP}) / [(V_{CAPMAX}^2 - V_{CAPMIN}^2) \times \eta] \text{ (F)}$$

For example, in *Figure 1* (Application Circuit), the minimum value of the supercapacitor required for 1s backup time, assuming 200mA system load and average efficiency of 93%, is calculated as:

$$C_{SCAP} \geq (2 \times 3.0V \times 0.2A \times 1s) / [((2.7V)^2 - (1.5V)^2) \times 0.93] = 256mF$$

Note: V_{CAPMIN} should be selected such that it supplies the load current to target the SYS voltage. The supercapacitor will continue to discharge till 0.5V (typ).

Inductor Selection

The MAX38886 works with a 1µH inductor in most applications. In applications where lower peak currents are desired, larger inductance may be used in order to reduce the ripple. The recommended inductance range is from 1µH to 4.7µH.

L (µH)	RISET (kΩ)
1 to 1.5	20 to 30
2.2	30 to 45
3.3	45 to 70
4.7	70 to 100

Enabling Device

The MAX38886 has a dedicated enable pin. The pin can either be driven by a digital signal or pulled up or strapped to the SYS rail.

PCB Layout Guidelines

Minimize trace lengths to reduce parasitic capacitance, inductance and resistance, and radiated noise. Keep the main power path from SYS, LX, CAP, and PGND as tight and short as possible. Minimize the surface area used for LX since this is the noisiest node. The trace between the feedback resistor-dividers should be as short as possible and isolated

from the noisy power path. Refer to the EV kit layout for best practices. The PCB layout is important for robust thermal design. The junction to ambient thermal resistance of the package greatly depends on the PCB type, layout, and pad connections. Using thick PCB copper and having the SYS, LX, CAP, and PGND copper pours will enhance the thermal performance. The TDFN package has a large thermal pad under the package, which creates excellent thermal path to PCB. This pad is electrically connected to PGND. Its PCB pad should have multiple thermal vias connecting the pad to the internal PGND plane. Thermal vias should either be capped or have a small diameter to minimize solder wicking and voids.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	FEATURES
MAX38886ATD+	-40°C to +125°C	14 TDFN	Enable input; selectable voltage and currents

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/20	Initial release	—
1	8/20	Release for intro	7