*Click **here** for production status of specific part numbers.*

MAX38913

4μV_{RMS} Ultra-Low-Noise 1A LDO with Two-Level Output-Voltage Selection

General Description

The MAX38913 is a low-noise linear regulator that delivers up to 1A of load current with as low as 4μV_{RMS} of output noise. The MAX38913 can dynamically change its output voltage between two separate levels. The MAX38913 has the pass-through mode which, when enabled, completely bypasses the linear regulator.

This regulator maintains ±1% output accuracy over a wide input voltage range, temperature, and load conditions. The no-load quiescent current in the regulation mode is 1.37mA. During the pass-through mode, unlike the conventional dropout mode of an LDO, the MAX38913 consumes very little quiescent current. The MAX38913 has a 6Ω active discharge feature to quickly discharge output capacitors of up to 300μF.

The MAX38913 has 33 programmable output-voltage settings for both voltage selections.

The MAX38913 is packaged in either a space-saving 12-bump WLP or a full-featured 3mm x 3mm, 14-pin TDFN package. Optional power-OK and power-on-reset pins are available in the 14-pin TDFN version.

Applications

- Image Sensors
- Portable Sensor Applications
- SD Memory Cards

***Ordering Information** appears at end of data sheet.*

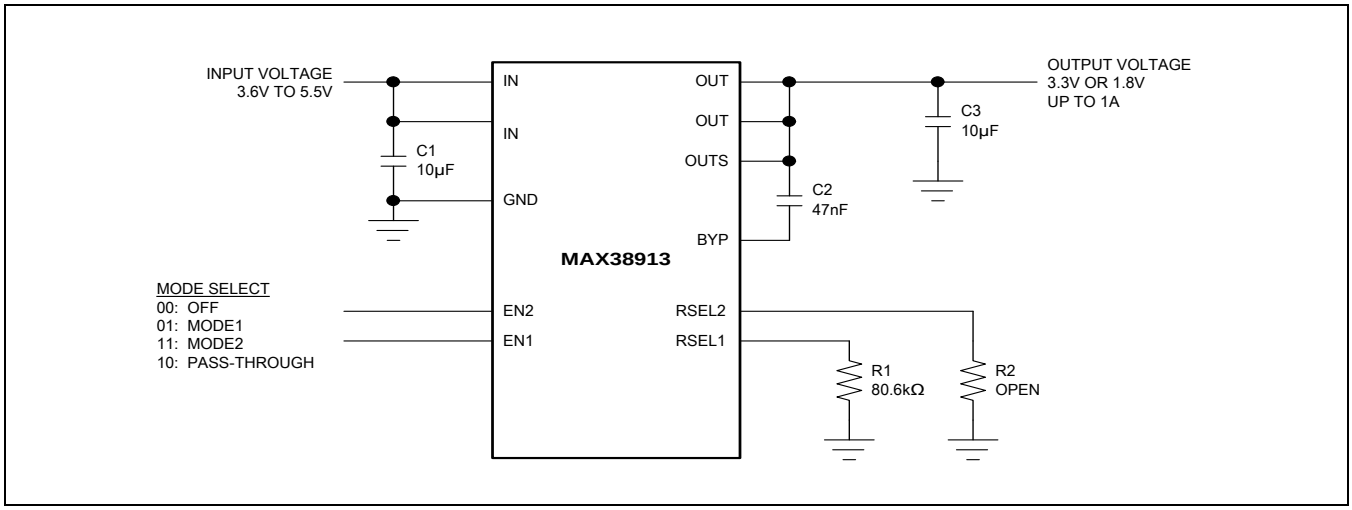
Benefits and Features

- Delivers Flexible Output Range
  - 1.8V to 5.5V Input Voltage Range
  - 0.6V to 5.0V Output Voltage Range
  - 1A Maximum Output Current
  - 28mV Dropout at 1A Load Current and 5.0V Supply
  - 33mV Dropout at 1A Load Current and 3.6V Supply
- Excellent DC and AC Performance
  - 1% Regulation over Line, Load, and Temperature
  - 4μV_{RMS} of Output Noise, 10Hz to 100kHz
  - 75dB PSRR at 10kHz
- High-Level System Integration
  - Integrated Pass-Through Function
  - Fast Active Discharge of 6Ω at OUT
  - Dynamic Two-Level Voltage Scaling with 33 Levels for Each Option for Flexible Configuration
  - Stable with 4μF (Minimum Capacitance)
  - Overcurrent and Overtemperature Protection
  - Power-OK/Power-on-Reset Output
- Operation Temperature Range from -40°C to +125°C
- Package
  - 12-Bump, 0.4mm-Pitch WLP
  - 14-Pin, 3mm x 3mm TDFN

19-101015; Rev 0; 4/21

maxim integrated™

Application Diagram



Absolute Maximum Ratings

IN, OUT, OUTS, BYP to GND ..... -0.3V to +6V

EN1, EN2, POK, PORB to GND ..... -0.3V to +6V

RSEL1, RSEL2 to GND .....-0.3V to V_{IN} + 0.3V

Output Short-Circuit Duration..... Continuous

Continuous Power Dissipation (T_A = +70°C).....

WLP (derate 13.73mW/°C above +70°C) 1096mW

TDFN (derate 24.4mW/°C above +70°C)..... 1951.2mW

Operating Junction Temperature Range ..... -40°C to +125°C

Maximum Junction Temperature .....+150°C

Storage Temperature Range..... -65°C to +150°C

Lead Temperature (soldering, 10 seconds) .....+300°C

Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	**N121E1+1**
Outline Number	*21-100500*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	72.82°C/W
Junction to Case (θ_{JC})	N/A

TDFN

Package Code	**T1433+2C**
Outline Number	*21-0137*
Land Pattern Number	*90-0063*

Thermal Resistance, Single Layer Board:	
Junction to Ambient (θ_{JA})	54°C/W
Junction to Case (θ_{JC})	8°C/W
Thermal Resistance, Four Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8°C/W

*For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.*

*Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.*

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 3.3V, V_{OUTS} = V_{OUT}, T_J = -40°C to +125°C, C_{BYP} = 10nF, C_{IN} = 10μF, C_{OUT} = 10μF, V_{EN1} = V_{EN2} = 3.6V, Typical values are at T_J = +25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Guaranteed by output accuracy		1.8		5.5	V
Input Undervoltage Lockout	V_{IN_UVLO}	V_{IN} rising, 50mV hysteresis		1.7	1.75	1.8	V
Output Voltage Range	V_{OUT}	Guaranteed by output accuracy		0.6		5	V
Output Capacitance	C_{OUT}	Necessary for loop stability		4	10		μF
Shutdown Supply Current	I_{IN_SD}	V_{EN1} = V_{EN2} = 0V	T_J = +25°C		0.2	1	μA
			T_J = +125°C		1.2		
Current Limit	I_{LIM}	V_{OUTS} = 0V, V_{IN} - V_{OUT} = 500mV		1.15	1.4	1.65	A
Current-Limit Response Time	t_{ILIM}				3		μs
BYP Capacitor Range	C_{BYP}	Necessary for regulator to remain stable		10		100	nF
BYP Soft-Start Current	I_{BYP}	From BYP to GND during startup, V_{OUTS} = 0V		40	50	60	μA
EN Input Threshold	V_{IH}	V_{IN} = 1.8V to 5.5V	V_{EN1}, V_{EN2} rising		0.8	1.2	V
	V_{IL}	V_{IN} = 1.8V to 5.5V	V_{EN1}, V_{EN2} falling	0.4	0.7		
EN Input Falling Edge Delay	t_{EN_DELAY}	From V_{EN1} or V_{EN2} falling to mode change		1	2	4	μs
EN Input Leakage Current	I_{EN_LK}	V_{EN1} = V_{EN2} = 5.5V	T_J = +25°C	-1	0.001	1	μA
			T_J = +125°C		0.01		
Input Reverse Current Threshold	I_{IN_RTH}	V_{OUT} = 3.6V, when V_{IN} falls to 0V			400		mA
Thermal Shutdown Threshold	T_{SD}	T_J when output turns off	T_J rising		165		°C
		T_J when output turns on	T_J falling		150		
POK and PORB Threshold		V_{OUT} when POK and PORB switch	V_{OUT} rising		91		%
			V_{OUT} falling		88		
POK and PORB Output Voltage, Low	V_{OL}	I_{POK} = I_{PORB} = 1mA	I_{POK} = I_{PORB} = 1mA		10		mV
POK and PORB Leakage	I_{POK_LK}, I_{PORB_LK}	V_{POK} = V_{PORB} = 5.5V	T_J = +25°C		0.001		μA
			T_J = +125°C		0.01		
RSEL Detection Accuracy		Use the nearest 1% resistor from Table 1		-1		1	%
RSEL Pin Capacitance	C_{IN_RSEL}	When Hi-Z				2	pF
RSEL Acquisition Time	t_{RSEL_ACQ}	From V_{IN} > V_{IN_UVLO} to R_{SEL} capture		240	600	1320	μs
EN1 = HIGH and EN2 = HIGH; EN1 = HIGH, EN2 = LOW (LOW-NOISE LDO MODE 1 and MODE 2)							
Supply Current	I_Q	I_{OUT} = 0mA			1.37	2	mA

(V_{IN} = 3.6V, V_{OUT} = 3.3V, V_{OUTS} = V_{OUT}, T_J = -40°C to +125°C, C_{BYP} = 10nF, C_{IN} = 10μF, C_{OUT} = 10μF, V_{EN1} = V_{EN2} = 3.6V, Typical values are at T_J = +25°C, unless otherwise specified.)

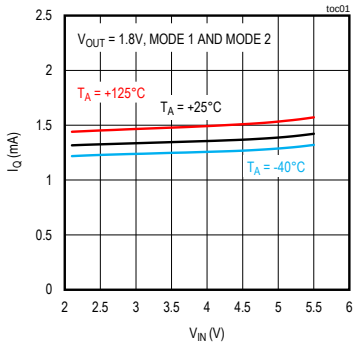
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Accuracy	ACC	I_{OUT} from 0.1mA to 1A, V_{OUT} + 0.3V < V_{IN} < 5.5V, V_{IN} < 1.8V, V_{OUT} from 0.6V to 5.0V		-1		1	%
Load Regulation	ACC_{LOAD_REG}	I_{OUT} from 100μA to 1A			0.09		%
Load Transient		I_{OUT} = 50mA to 1A to 50mA, t_{RISE} = t_{FALL} = 0.1μs, Note 1			50		mV
Line Regulation	ACC_{LINE_REG}	V_{IN} from V_{OUT} + 0.3V to 5.5V, I_{OUT} = 100mA			0.1		%
Line Transient		V_{IN} = V_{OUT} + 0.3V to 5.0V, I_{OUT} = 100mA, t_{RISE} = t_{FALL} = 1μs			3		mV
Power-Supply Rejection Ratio	PSRR	V_{IN} = 2.1V, V_{OUT} = 1.8V, I_{OUT} = 100mA	f = 1kHz		75		dB
			f = 10kHz		75		
			f = 100kHz		60		
			f = 1MHz		50		
Output Noise		I_{OUT} = 100mA, f = 10Hz to 100kHz	C_{BYP} = 47nF		4.05		$μV_{RMS}$
Dropout Voltage	V_{DO}	I_{OUT} = 1A	V_{IN} = 5.0V, WLP		28		mV
			V_{IN} = 3.6V, TDFN		48		
			V_{IN} = 3.6V, WLP		33	100	
			V_{IN} = 2.5V, TDFN		57		
			V_{IN} = 2.5V, WLP		42	160	
			V_{IN} = 1.8V, TDFN		85		
			V_{IN} = 1.8V, WLP		64.2	300	
EN1 = LOW and EN2 = HIGH (PASS-THROUGH MODE)							
Supply Current	I_Q	I_{OUT} = 0mA	T_J = +25°C		115		μA
Short-Circuit Protection Current limit	I_{LIM}	V_{OUT} = 0V			2		A
Pass-Through Switch ON Resistance	R_{PT}	V_{OUT} = 1.8V, I_{OUT} = 100mA			0.06		Ω
EN1 = LOW and EN2 = LOW (SHUTDOWN MODE/ACTIVE DISCHARGE)							
Active Discharge Resistance	R_{DIS}	I_{OUT} = 100mA, V_{EN1} = V_{EN2} = 0V		2	6	14	Ω

Note 1: Load-transient response considers T_A = +25°C. T_J is not assumed to be at +25°C.

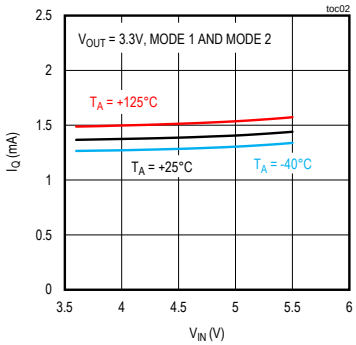
Typical Operating Characteristics

(V_{IN} = 3.6V, V_{OUT} = 3.3V, T_A = +25°C, C_{IN} = 10μF, C_{OUT} = 10μF, C_{BYP} = 47nF, unless otherwise noted.)

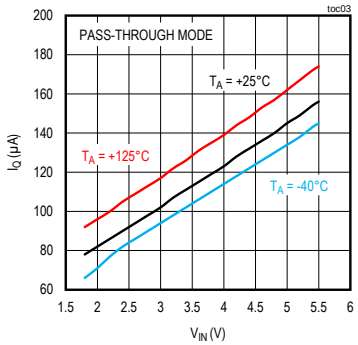
QUIESCENT CURRENT vs. INPUT VOLTAGE



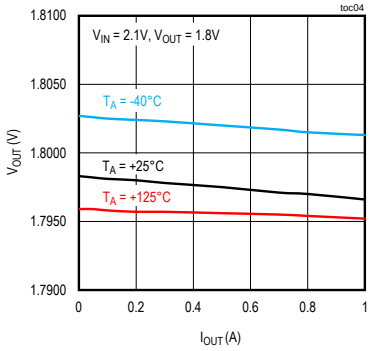
QUIESCENT CURRENT vs. INPUT VOLTAGE



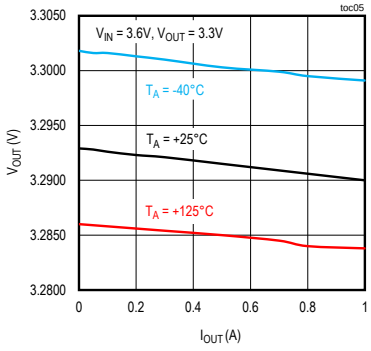
QUIESCENT CURRENT vs. INPUT VOLTAGE



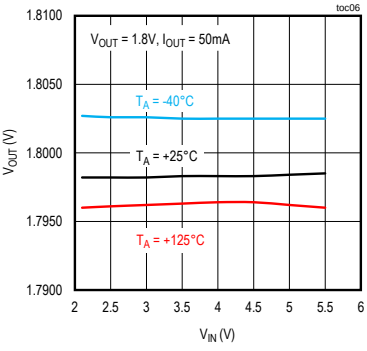
LOAD REGULATION



LOAD REGULATION



LINE REGULATION



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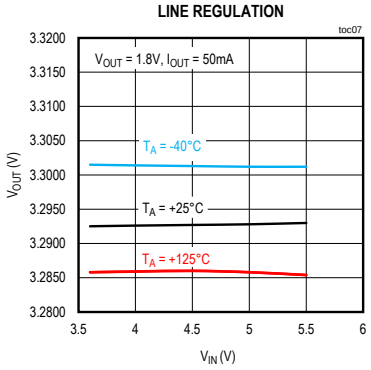
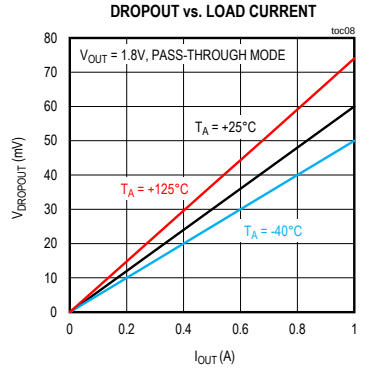
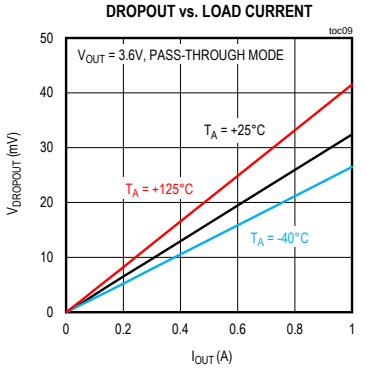


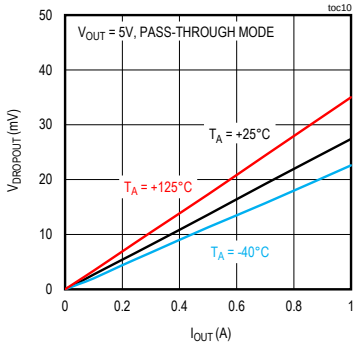
DROPOUT vs. LOAD CURRENT



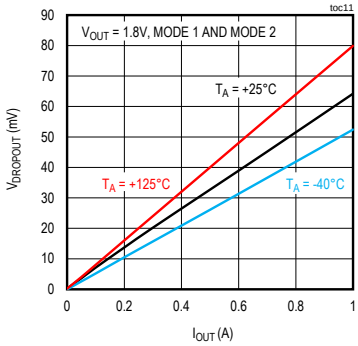
DROPOUT vs. LOAD CURRENT



DROPOUT vs. LOAD CURRENT



DROPOUT vs. LOAD CURRENT



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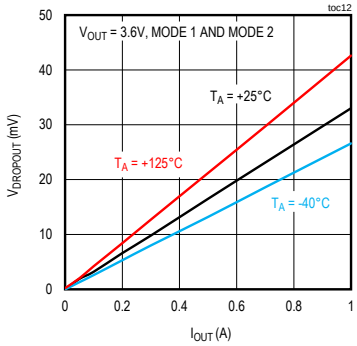
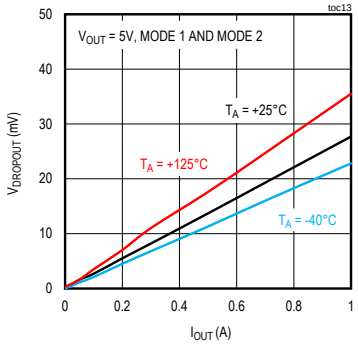
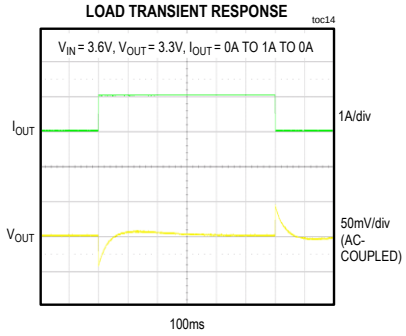


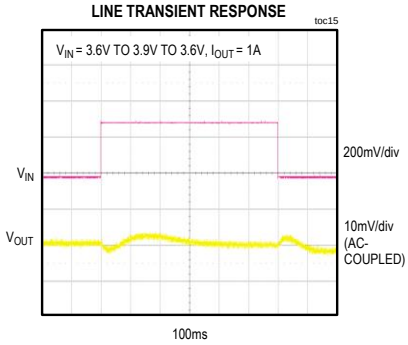
DROPOUT vs. LOAD CURRENT



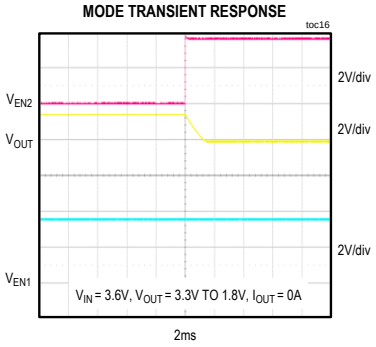
LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



MODE TRANSIENT RESPONSE



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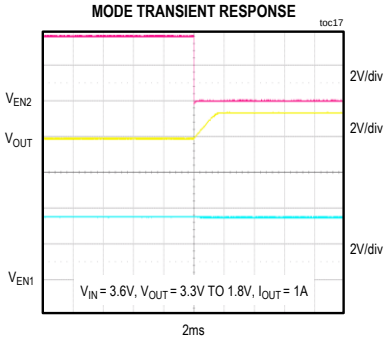
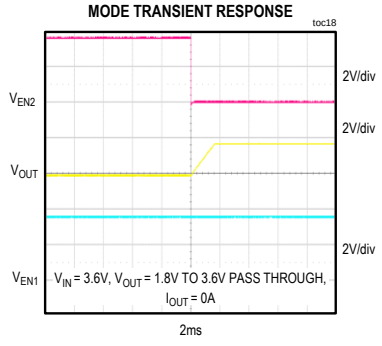
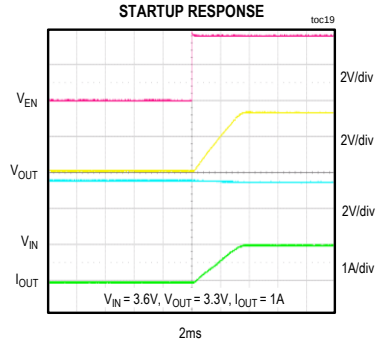


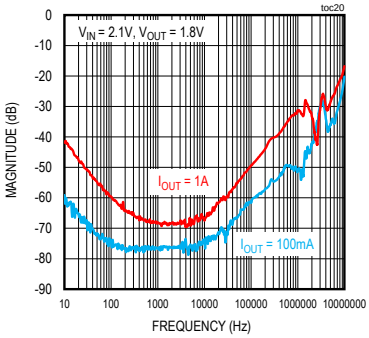
MODE TRANSIENT RESPONSE



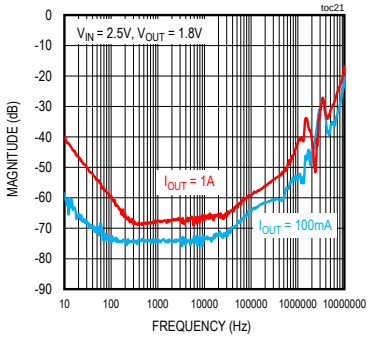
STARTUP RESPONSE



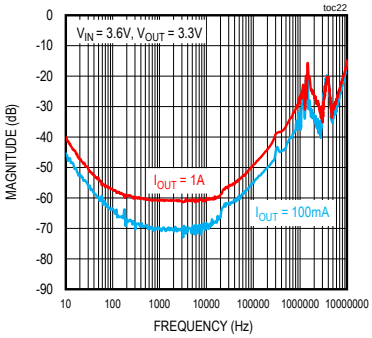
INPUT SUPPLY PSRR vs. FREQUENCY



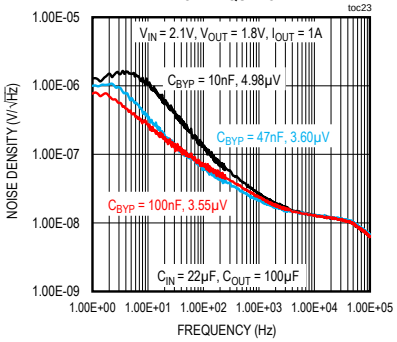
INPUT SUPPLY PSRR vs. FREQUENCY



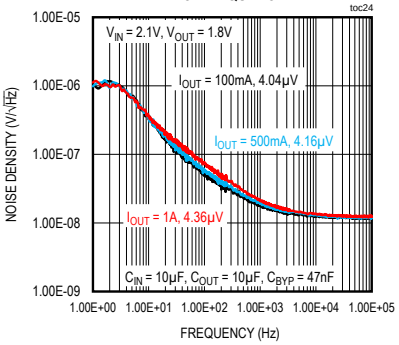
INPUT SUPPLY PSRR vs. FREQUENCY



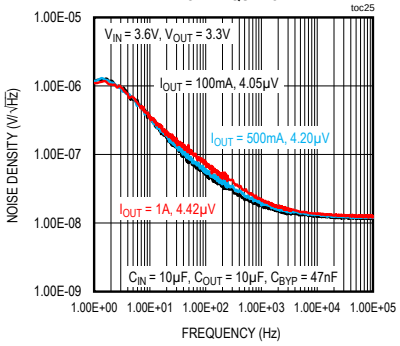
OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY



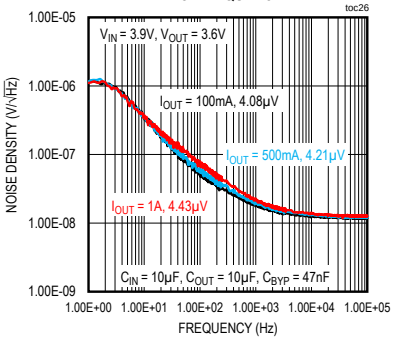
OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY



OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY

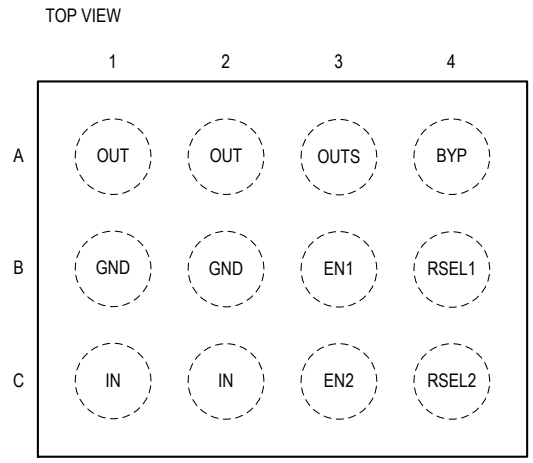


OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY



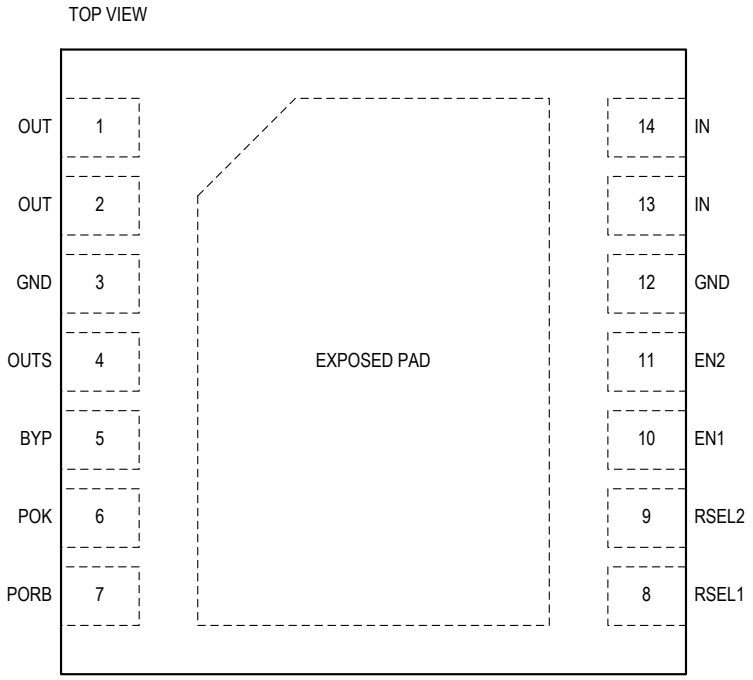
Pin Configurations

WLP



12 WLP

TDFN

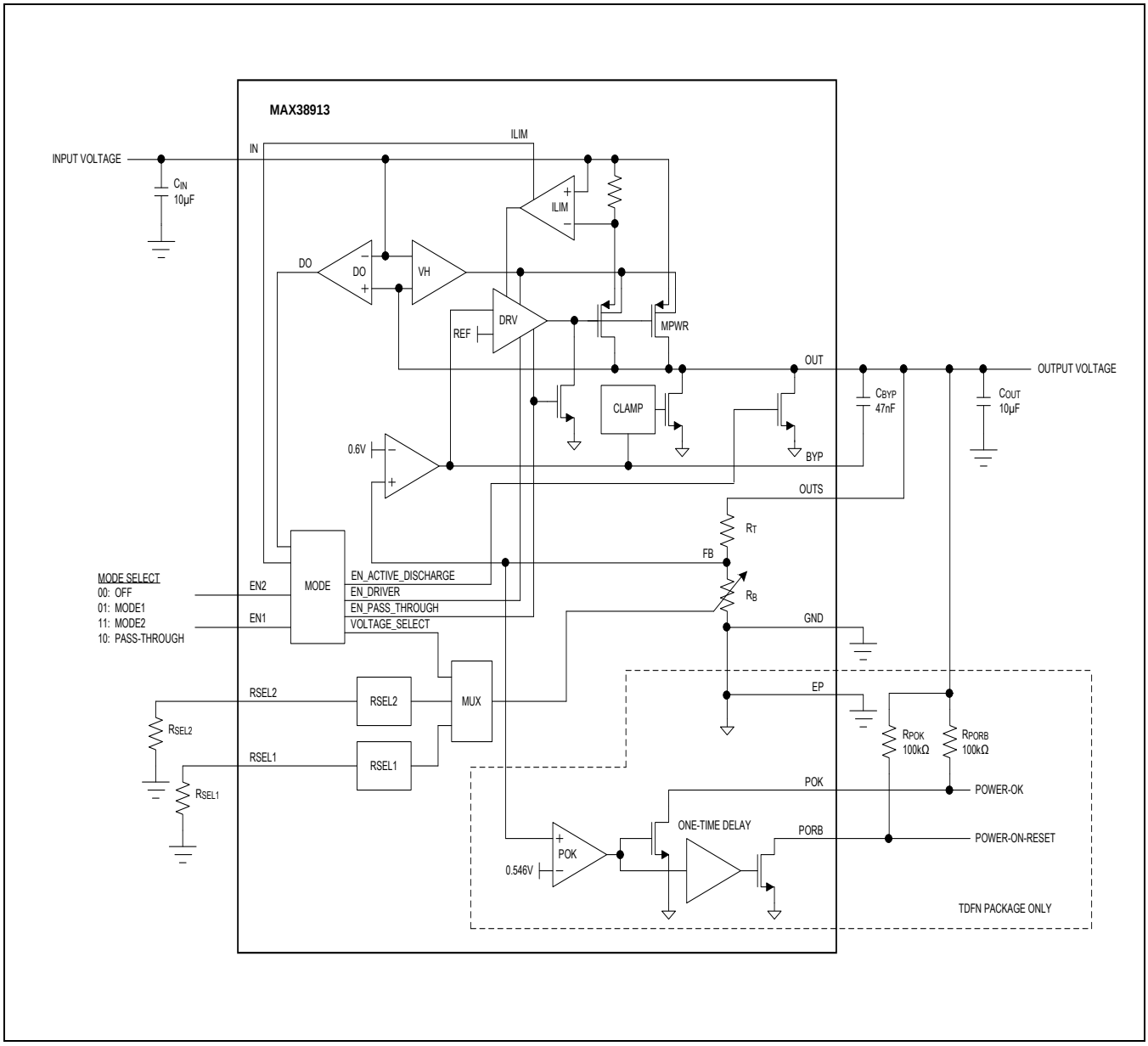


3mm x 3mm, 14 TQFN

Pin Descriptions

PIN		NAME	FUNCTION
WLP	TDFN		
A1, A2	1, 2	OUT	Regulator Output. Deliver up to 1A of load current at the regulated output voltage. Connect a 10μF capacitor (>4μF, effective) with an ESR of <0.03Ω from OUT to GND.
B1, B2	3, 12, EXPOSED PAD	GND	Regulator GND. The output voltage is regulated with respect to the voltage at these pins. Connect to IN and OUT bypass capacitors reference. These pins conduct current when OUT is transitioning to a lower voltage.
A3	4	OUTS	Output-Voltage Sense Input. Connect to the point where accurate output regulation is desired.
A4	5	BYP	Bypass Capacitor Input. Connect a 10nF to 100nF capacitor from OUT to BYP to filter the regulator feedback noise and control the output transition slew rate.
—	6	POK	Power-OK Output. Connect a pullup resistor from POK to OUT or an alternate supply to create an active-high signal that indicates when the output has achieved regulation. This output is low in shutdown.
—	7	PORB	Power-on-Reset. Connect a pullup resistor from PORB to OUT or an alternate supply to create an active-high signal that holds a logic circuit in reset until the output has achieved regulation for 10ms. This output is low in shutdown.
B4	8	RSEL1	Output-Voltage Select. Connect a ±1% resistor from RSEL to GND to set the output regulation voltage in regulation mode 1 (MODE 1). This resistance is read at power-up.
C4	9	RSEL2	Output-Voltage Select. Connect a ±1% resistor from RSEL to GND to set the output regulation voltage in regulation mode 2 (MODE 2). This resistance is read at power-up.
B3	10	EN1	Enable Input 1. The EN1 and EN2 pins are used to set the operating mode. EN2, EN1 = 00: Disabled. The output is shorted to GND through a 6Ω active discharge circuit. EN2, EN1 = 01: Regulation MODE 1. The output is determined by RSEL1. EN2, EN1 = 10: Pass-Through Mode. The output is shorted to the input. EN2, EN1 = 11: Regulation MODE 2. The output is determined by RSEL2.
C3	11	EN2	Enable Input 2. The EN2 and EN1 pins are used to set the operating mode. EN2, EN1 = 00: Disabled. The output is shorted to GND through a 6Ω active discharge circuit. EN2, EN1 = 01: Regulation MODE1. The output is determined by RSEL1. EN2, EN1 = 10: Pass-Through Mode. The output is shorted to the input. EN2, EN1 = 11: Regulation MODE 2. The output is determined by RSEL2.
C1, C2	13, 14	IN	Regulator Input. Connect a 10μF capacitor (>4μF effective) with ESR of <0.03Ω from IN to GND.

Simplified Block Diagram



Detailed Description

Modes of Operation

The MAX38913 features regulation, pass-through, and shutdown modes of operation. The modes are selected based on the state of the EN1 and EN2 pins.

In the regulation modes (MODE 1 and MODE 2), output voltage is regulated to levels selected by the RSEL inputs. When EN2 and EN1 are at logic-low and logic-high states respectively, the device regulates to the level selected by the RSEL1 pin (MODE 1). If both EN2 and EN1 are at a logic-high state, the device regulates to the level selected by the RSEL2 pin

(MODE 2). Both RSEL1 and RSEL 2 pins are read as V_{IN} crosses the UVLO rising threshold. The device holds the RSEL1 and RSEL2 values until V_{IN} drops below the UVLO falling threshold. There are 33 possible output-voltage regulation levels. See the Output-Voltage Selection section for details about different output-voltage level selection. In both regulation modes, the device has excellent transient, power-supply rejection ratio (PSRR), and output noise performance.

The MAX38913 is optimized for applications requiring dynamic transitioning between two regulation levels. The slew rate between the two regulation levels is defined by C_{BYP} in both the up and down transition directions. The slew rate is calculated by:

$$\frac{dV_{OUT}}{dt} = \frac{I_{BYP\_SLEW}}{C_{BYP}} = \frac{50\mu A}{C_{BYP}}$$

Slewing the output voltage from a high to a low level in the regulation mode requires the MAX38913 to shunt high current to ground if the output capacitor is large and the output load current is light. For example, with C_{BYP} = 47nF and C_{OUT} = 100μF, the output voltage is stable while the device is sinking current in the amount of 106.4mA in order to keep the output in regulation during slewing.

$$I = I_{BYP\_SLEW} \times \left(\frac{C_{OUT}}{C_{BYP}} \right) = 50\mu A \times \left(\frac{100\mu F}{47nF} \right) = 106.4mA$$

Slewing the output voltage from a low level to a high level is recommended to be done while the system is placed in the low-current mode of operation. This is to assure that no current limit is tripped during this transition since I_{OUT} is dominated by C_{OUT} charging current. The device output current during this transition is:

$$I_{OUT} = I_{BYP\_SLEW} \times \left(\frac{C_{OUT}}{C_{BYP}} \right) + I_{LOAD}$$

It is recommended to keep the load current constant during the voltage transition from one level to the other.

Once the EN2 and EN1 pins are set to logic-high and logic-low states, respectively, the device transitions to the pass-through mode of operation. Figure 1 illustrates the mode transitions.

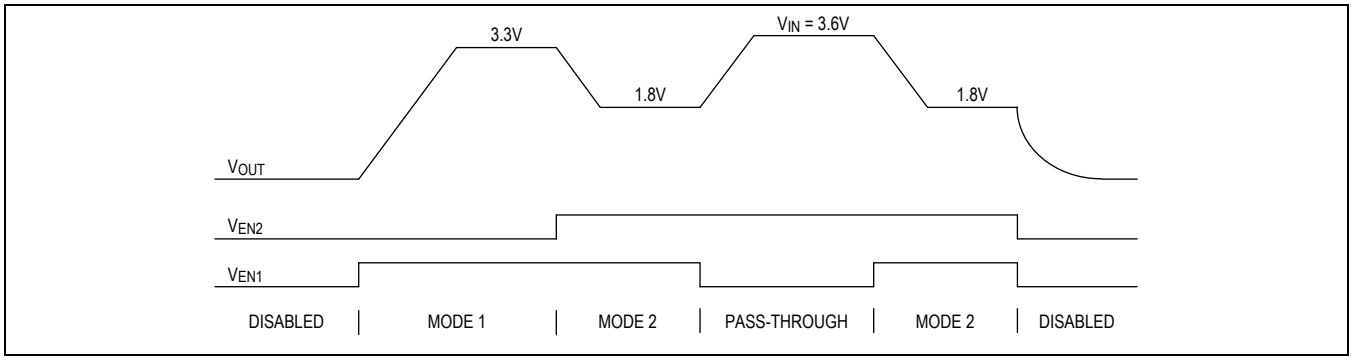


Figure 1. Modes of Operation

Pass-Through Mode

The MAX38913 includes a pass-through mode where the output pass device is turned on hard, shorting the output to the input. In this mode, quiescent current is reduced to 115μA. The controller remains on to support a current-limiting circuit.

The output voltage always slews in the pass-through mode and back to regulation mode at the same rate. The slew rate is defined by the C_{BYP} capacitor used in application, and can be calculated as:

$$\frac{dV_{OUT}}{dt} = \frac{I_{BYP\_SLEW}}{C_{BYP}} = \frac{50\mu A}{C_{BYP}}$$

As the device transitions in and out of the pass-through mode, the regulator is enabled until slewing is completed. After slewing is completed, the controller is disabled to save power while the current-limit detector remains on. The device limits the current in the pass-through mode to about a 2A level.

If the current-limit circuit trips in the pass-through mode, the regulator enables and tries to regulate the output voltage back into dropout with the feedback held low, delivering load current up to the level of the current limit in dropout—about 1.4A. During current limiting, it is common for the device to go into thermal shutdown, and also for the output to turn off and on as the die temperature slews between +150°C and +165°C.

When the overload at the output is removed, the regulator slews the output voltage up at the nominal output-voltage slew rate defined by C_{BYP}. When the output pass device reaches the dropout level, the current-limit circuit resets, and the device returns to the pass-through mode of operation.

Bypass

The capacitor connected from BYP to OUT filters the noise of the reference, feedback resistors, and regulator input stage, thus providing a high-speed feedback path for improved transient response. A 0.01μF capacitor rolls off input noise at around 32Hz.The slew rate of the output voltage during startup and transitions is also determined by the BYP capacitor. A 0.01μF capacitor sets the slew rate to 5V/ms. This startup rate results in a 50mA slew current drawn from the input at start-up to charge the 10μF output capacitance. The BYP capacitor value can be adjusted from 0.01μF to 0.1μF to change the slew rate according to the following formula:

$$\text{Slew Rate} = \frac{50\mu A}{C_{BYP}}$$

$$= (5V/ms) \times \left(\frac{0.01\mu F}{C_{BYP}} \right)$$

where C_{BYP} is in μF.

Selecting the BYP capacitor larger than 10nF is primarily to slow down the soft-start or transition rate and minimize the inrush current since the output noise remains very constant with an improvement of about 1.0μV_{RMS}.

Note that, being a low-frequency filter node, BYP is sensitive to leakage. BYP leakage currents above 10nA cause measurable inaccuracy at the output and should be avoided.

Enable (EN)

The MAX38913 includes two enable inputs (EN1 and EN2). Pulling both enable pins low shuts the device down. In shutdown, the output voltage is pulled to ground through a 6Ω active discharge circuit. In this mode, the device consumes 0.2μA of current from the input supply. Drive the enable pins high to place the device in regulation or pass-through modes. When EN2 and EN1 are driven to logic-low and logic-high states respectively, the device regulates to the level selected by the RSEL1 pin (MODE 1). If both EN2 and EN1 are driven to logic-high state, the device regulates to the level selected by the RSEL2 pin (MODE 2). Once the EN2 and EN1 pins are set to logic-high and logic-low states, respectively, the device transitions to the pass-through mode of operation. The enable signals should be stable for at least 2μs for the MAX38913 to latch in an appropriate state. The enable signal states should not be changed while the output voltage transitions.

Active Discharge

Once the MAX38913 is placed in the shutdown mode, the OUT pin is pulled to ground through a 6Ω active discharge circuit.

Power-OK (POK) and Power-on-Reset (PORB)

The power-OK (POK) function monitors the output voltage to indicate that it is in regulation. The POK pin is open-drain and requires a pullup resistor to an external supply to properly report the device regulation status to other devices so it can be used for sequencing. Check if the external pullup supply voltage results in a valid logic levels for the receiving

device or devices. The range of the pullup resistance is between 10kΩ and 200kΩ. Its lower limit comes from a pulldown strength of the POK transistor while the higher limit is determined by maximum leakage current at the POK pin. The signal is low while the device is in shutdown.

The POK is driven low during startup. It gets released and pulled up once the output voltage reaches the POK rising threshold (91% of the regulation target). If the output voltage sags to below the POK falling threshold during regulation, the POK signal is driven low to indicate that the output voltage dropped out of regulation. During shutdown, the POK signal is driven low once the output voltage crosses the POK falling threshold (88% of the regulation target). The POK signal is active during output voltage transition.

PORB is an open-drain signal that indicates the output voltage has achieved stable regulation. The signal is used to keep the system in reset until the regulation has been achieved for 10ms. This signal is low in shutdown. PORB requires a pullup resistor in the range between 10kΩ and 200kΩ.

Protection

The MAX38913 is fully protected from an over-circuit condition by current-limiting and thermal-overload protection circuits. If the output is shorted to GND, the output current is limited to 1.4A (typ) after the output capacitor discharges through the shorting path. Under these conditions, the device quickly heats up. When the junction temperature reaches +165°C, the thermal-protection circuit shuts the output device off. Once the device cools to +150°C, the regulator enables regulation to be established. If the fault persists, the output cycles on and off as the junction temperature slews between +150°C and +165°C. Continuously operating in the fault conditions or above a +125°C junction temperature is not recommended since long-term reliability may be reduced. The MAX38913 provides reverse-current protection when the output voltage is higher than the input. The MAX38913 includes a reverse voltage detector that trips when IN drops below OUT, shutting off the regulator and opening the body diode connection to prevent any reverse current. Reverse current flows through the body diode of the pass element and is undesired due to its impact on power dissipation and long-term reliability, especially at higher current levels. Thermal protection can also be triggered when the device is exposed to excessive heat in the system causing the die temperature to reach undesired levels.

Undervoltage Lockout (UVLO)

The MAX38913 undervoltage lockout (UVLO) circuit responds quickly to glitches at the input voltage and disables the output of the device if the rail dips below the UVLO falling threshold. The local input capacitance prevents transient brownout conditions in most applications. The device is ready once the input voltage exceeds the UVLO rising threshold during power-up. The RSEL1 and RSEL2 values get acquired once V_{IN} crosses its rising UVLO threshold.

During V_{IN} power-up, the MAX38913 begins output-voltage soft-start after the input voltage crosses its UVLO rising threshold. This assures proper V_{OUT} ramp-up and transition to regulation. The V_{OUT} soft-start rate should be kept at or slower than the V_{IN} slew rate to avoid entering dropout. In some situations, V_{IN} transients can place the regulator into dropout. As V_{IN} starts climbing again and the device comes out of dropout, the output can overshoot. This condition is avoided by using an enable signal or by increasing the soft-start time with larger C_{BYP}.

Output-Voltage Selection

The output-voltage level selection is done by selecting resistor values to be loaded from the RSEL1 and RSEL2 pins to ground according to Table 1.

The output voltage in low-noise LDO mode 1 (MODE 1) is determined by the resistance connected from the RSEL1 pin to GND. Likewise, the resistance at the RSEL2 pin determines the output voltage in low-noise LDO mode 2 (MODE 2).

Table 1. RSEL Values vs. Output Voltages

R_{RSEL1} OR R_{RSEL2} (kΩ)	V_{OUT} IN MODE 1 OR MODE 2 (V)
OPEN	1.8
909	0.6
768	0.7
634	0.8
536	0.95

453	1
383	1.2
324	1.35
267	1.5
226	1.75
191	1.85
162	2
133	2.5
113	2.7
95.3	3
80.6	3.3
66.5	3.45
56.2	3.55
47.5	3.6
40.2	3.75
34	3.85
28	3.9
23.7	3.95
20	4.0
16.9	4.2
14	4.4
11.8	4.5
10	4.55
8.45	4.6
7.15	4.65
5.9	4.8
4.99	5
Short	3.5

The MAX38913 features preprogramming capability for both voltage levels (in MODE 1 and MODE 2) in 50mV steps within the output voltage range. This preprogrammed device has the RSEL1 and RSEL2 circuits disabled. Contact a Maxim Integrated representative for more information and availability.

Application Information

Input and Output Capacitors

The MAX38913 is designed to have stable operation using low equivalent series resistance (ESR) ceramic capacitors at the input and output pins. Multilayer ceramic capacitors (MLCC) with X7R dielectric are commonly used for these types of applications and are recommended due to their relatively stable capacitance across temperature. Nevertheless, the amount of effective capacitance depends on operating DC voltage, AC voltage ripple, temperature, etc. Therefore, the capacitor data sheet must be properly examined. The MAX38913 is designed and characterized for operation with X7R ceramic capacitors of 10μF (4μF of effective capacitance) both at the input and output. These capacitors should be placed as close as possible to the respective input and output pins to minimize trace parasitics. There is no maximum output capacitance limitation due to stability.

Thermal Consideration

To optimize the MAX38913 performance, special consideration is given to device power dissipation and PCB thermal design. Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. It can be calculated by following equation:

$$\text{Loss (W)} = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

The optimal power dissipation can be achieved by carefully choosing input voltage for a given output target voltage. The main thermal conduction path for the device is through the exposed pad of the package. As a result, the thermal pad must be soldered to a copper pad area under the device. Thermal-plated vias must be placed inside the thermal PCB pad to transfer heat to different GND layers in the system. The vias should be capped to minimize solder voids. The maximum power dissipation is determined by using thermal resistance from the device junction to ambient, keeping the maximum junction temperature below +125°C. Thermal properties of the package are given in the Package Information section.

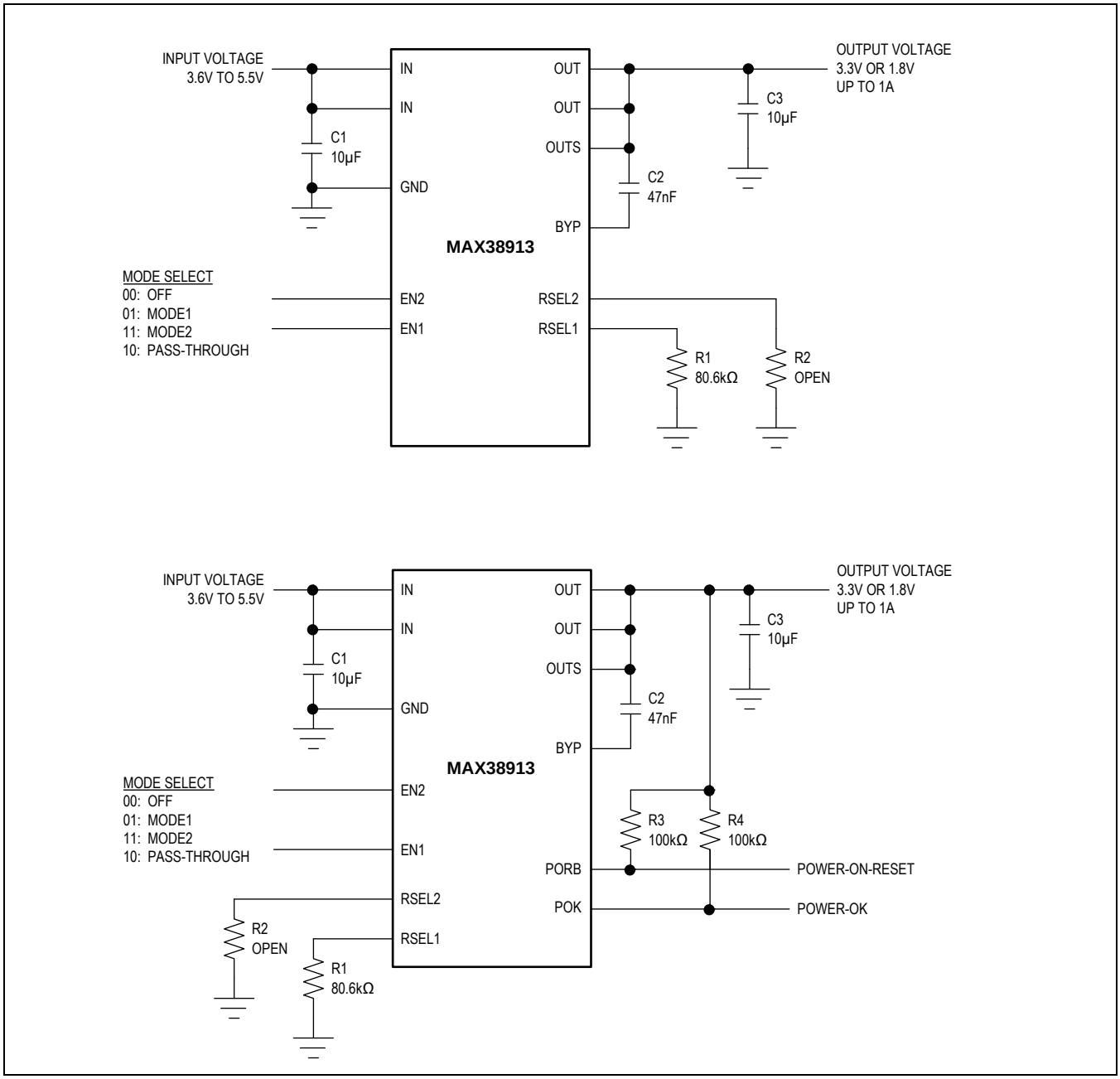
The first-order power dissipation for the 3.3V V_{IN} and 2.5V V_{OUT} with a load current of 700mA condition is:

$$P_{DIS}\ (W) = (V_{IN} - V_{OUT}) \times I_{LOAD}$$
$$= (3.3V - 2.5V) \times 0.7A$$
$$= 0.56W$$

Assuming the MAX38913ATA+, this power dissipation raises the junction temperature (T_J) to an estimated:

$$T_J = (P_{DIS} \times \theta_{JA}) + 25°C$$
$$= (0.56W \times 41°C/W) + 25°C$$
$$= 47.96°C$$

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PACKAGE	FEATURE
MAX38913AANC+	-40°C to +125°C	12 WLP	Four modes of operation, output voltage in MODE 1 and MODE 2 selected by RSEL1 and RSEL2
MAX38913AATD+*	-40°C to +125°C	3mm x 3mm, 14 TDFN	Four modes of operation, output voltage in MODE 1 and MODE 2 selected by RSEL1 and RSEL2

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/21	Initial release	—