19-2434; Rev 1; 1/03

MAXIM

10.7Gbps Linear Transimpedance Amplifier with Output Offset Adjust

General Description

The MAX3910 is a 10.7Gbps transimpedance amplifier designed for SONET OC-192/SDH STM-64, DWDM, and 10Gbps systems employing optical amplifiers. Operating from a single +5V or -5.2V supply, it converts a photodiode current into a measurable differential voltage. This product has a linear gain for an input current up to 950µA$_{P-P}$ and a soft-limiting feature that provides an increasing output swing for an input current up to the 3.5mA$_{P-P}$ overload. An offset adjust circuit and output-level monitors allow system threshold adjustments. Additional features include back-terminated 50Ω outputs and an integrated 200Ω filter resistor to bias the photodiode.

The MAX3910 has a small-signal bandwidth of 9.1GHz and a small-signal transimpedance of 1.65kΩ. The part achieves an input sensitivity of 15.5µA$_{P-P}$ for a BER of 10^{-12}, translating to an optical sensitivity of -19.3dBm for a PIN (r = 0.9, r_e = 6.6) photo detector and -28.8dBm for an APD (M = 8, ρ = 0.9, r_e = 10) photo detector.

The MAX3910 is fabricated in Maxim's in-house SiGe process and is available in die form.

Applications

DWDM Systems

OC-192/STM-64 Transmission Systems

10Gbps Systems Using Optical Amplifiers

10Gbps Optical Receivers

Features

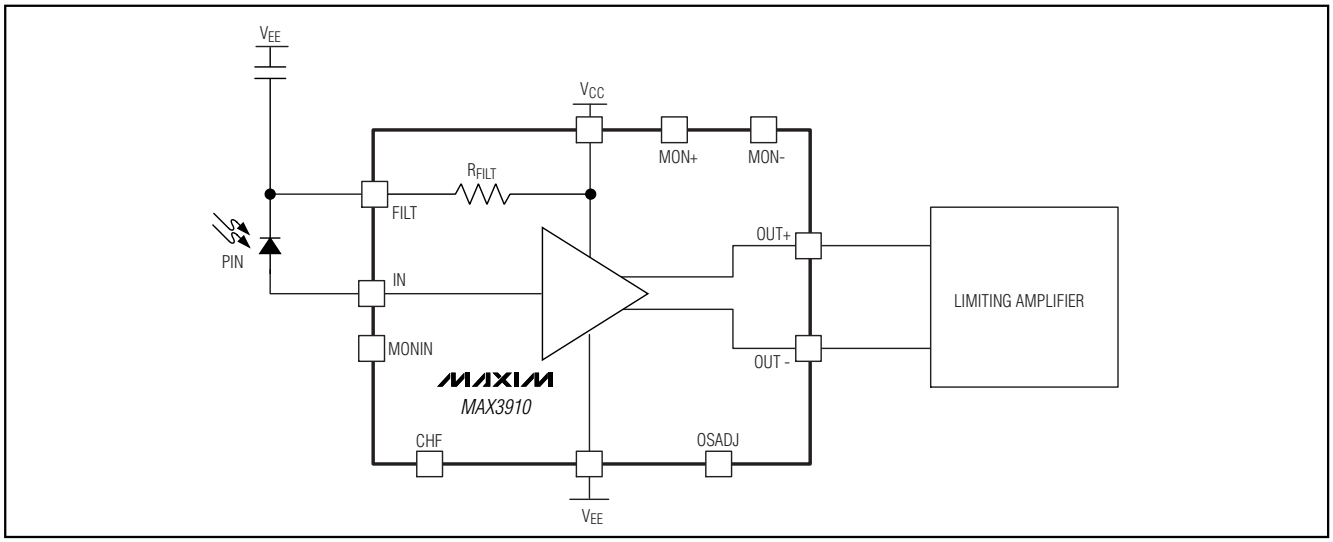
- **950µA$_{P-P}$ Linear Range**
- **15.5µA$_{P-P}$ Sensitivity**
- **3.5mA$_{P-P}$ Overload**
- **1.65kΩ Transimpedance**
- **9.1GHz Bandwidth**
- **110mA Supply Current**
- **Output Offset Adjustment**
- **Soft-Limiting Beyond Linear Input Range**
- **Single +5V or -5.2V Power Supply**
- **ESD Protection**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3910U/D	0°C to +85°C	Dice*

**Dice are designed to operate over a 0°C to +100°C junction temperature (T_J) range, but are tested and guaranteed at T_A = +25°C.*

Typical Operating Circuit



10.7Gbps Linear Transimpedance Amplifier with Output Offset Adjust

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC} - V_{EE}).....-0.5V to +6.0V
Continuous Input Current (IN).....4.2mA
Continuous Input Current (FILT) 9.8mA
Continuous Output Current (OUT+, OUT-) 35mA
Voltage at CHF, FILT, MON+, MON-,
MONIN, OSADJ .....(V_{EE} - 0.5V) to the lesser of +6.0V and (V_{CC} + 0.5V)
Storage Ambient Temperature Range (T_{STG}) ...-55°C to +150°C
Die Attach Temperature .....+400°C
Operating Temperature Range
(Junction Temperature Range).....-20°C to +120°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 4.75V to 5.5V, T_J = 0°C to +100°C. Typical values are at V_{EE} = -5.2V, V_{CC} = GND, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{EE}	V_{EE}2 open, Figure 1 (Note 3)		95	138	mA
Supply Current	I_{EE}	V_{EE}2 connected to negative supply, Figure 1 (Note 3)		110	158	mA
Power-Supply Noise Rejection	PSNR	$I_{IN} \le 450\mu A_{P-P}$, f ≤ 1MHz		23		dB
		$I_{IN} \le 450\mu A_{P-P}$, f ≤ 10MHz (Note 4)		22		
Input Bias Voltage				V_{EE} + 0.95	V_{EE} + 1.1	V
Transimpedance (Note 5)	Z_F	$I_{IN} \le 450\mu A_{P-P}$	1.40	1.65	1.87	kΩ
		I_{IN} = 1.0mA_{P-P}		1.37		
		I_{IN} = 2.0mA_{P-P}		0.84		
Linear Input Current Range	I_{LIN}	(Note 5)	450	950		μA_{P-P}
Low-Frequency Cutoff		CHF open, $I_{IN} \le 450\mu A_{P-P}$		6	25	kHz
		CHF = 0.1µF, $I_{IN} \le 450\mu A_{P-P}$		0.5		
Photodiode Filter Resistor	R_{FILT}		165	200	240	Ω
Output Monitor Resistance		To OUT+ or OUT-		10		kΩ
Single-Ended Output Resistance		To V_{CC}	42	50	59	Ω
Maximum Differential Output Swing	V_{OD}	(Note 6)	1.45	1.75	1.90	V_{P-P}
Single-Ended Output Range	V_{OS}	Outputs DC-coupled to 50Ω to V_{CC} (Note 6)	-1.3		0	V
Output DC Offset		I_{IN} = 7.5µA DC	-7		+7	mV
		I_{IN} = 1.4mA DC	-10		+10	
OSADJ Input Resistance			15	20		kΩ
OSADJ Input Range	V_{OSADJ}		-2.1		-0.4	V
OSADJ Voltage for Zero Offset			-1.375	-1.25	-1.125	V
Minimum Differential Output Offset		V_{OSADJ} = -0.4V, R_L = 50Ω to V_{CC}		-320	-250	mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = 4.75V to 5.5V, T_J = 0°C to +100°C. Typical values are at V_{EE} = -5.2V, V_{CC} = GND, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Offset		V_{OSADJ} = -2.1V, R_L = 50Ω to V_{CC}	250	320		mV
OSADJ Voltage Control Factor: OUT+		$(\Delta V_{OSADJ})/\Delta V_{OUT+}$	-3	-2		V/V
OSADJ Voltage Control Factor: OUT-		$(\Delta V_{OSADJ})/\Delta V_{OUT-}$		2	3	V/V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 4.75V to 5.5V, T_J = 0°C to +100°C. Typical values are at V_{EE} = -5.2V, V_{CC} = GND, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bandwidth	BW_{3dB}	$I_{IN} \le 450\mu A_{P-P}$ (Notes 2, 11)	8.2	9.1		GHz
Input-Referred Noise	I_N	(Notes 2, 7)		1.1	1.62	μA_{RMS}
Input Sensitivity		(Notes 2, 8)		15.5		μA_{P-P}
Input Overload	I_{OL}	AC component (Note 9)	2.5	3.5		mA_{P-P}
		DC component (Note 9)	1.4	1.8		mA
Gain Flatness		100MHz - 4GHz, $I_{IN} \le 450\mu A_{P-P}$ (Note 2)		±0.75		dB
Gain Ripple		4GHz - BW_{3dB}, $I_{IN} \le 450\mu A_{P-P}$ (Note 2)		1.5		dB
Deterministic Jitter (Notes 2, 10)		$I_{IN} \le 450\mu A_{P-P}$		6.2	10.7	ps_{P-P}
		$450\mu A_{P-P} \le I_{IN} \le 2.5mA_{P-P}$		7.5	14.6	
Single-Ended Output Return Loss (Note 2)		≤7.5GHz		10		dB

Note 1: Default test conditions: $V_{EE}2$ and CHF = open (Figure 1), R_L = 50Ω to V_{CC}, DC-coupled at each output, unless otherwise noted. AC characteristics are guaranteed by design and characterization.

Note 2: Source capacitance = 0.25pF, source series resistance = 20Ω, and source series inductance = 0.6nH. Output series inductance = 0.5nH at each of the differential outputs.

Note 3: Supply current increases as average signal level increases. Maximum supply current is specified for I_{IN} = 1.4mA average current. Typical supply current is specified for $I_{IN} \le 225\mu A$ average current.

Note 4: PSNR is measured by detecting the differential output voltage ΔV_{OUT} while applying $\Delta V_{EE} = 55mV_{P-P}$ signal on $V_{EE}1$. PSNR = $20\log(\Delta V_{EE}/\Delta V_{OUT})$. Output offset adjust feature disabled.

Note 5: Transimpedance is defined as $V_{OUT(P-P)} / I_{IN(P-P)}$ at 10MHz. Linear range is defined as the input signal level where the transimpedance deviates from the small-signal transimpedance value by no more than 10% (Figure 2).

Note 6: Input current ≤ $2.5mA_{P-P}$ and ≤ 1.4mA DC.

Note 7: Measured with a 4th-order Bessel-Thompson filter with a cutoff frequency of 8GHz.

Note 8: Input sensitivity calculated from S/N ≥ 14.1 (BER ≤ 10^{-12}).

Note 9: For input signal less than or equal to the input overload, deterministic jitter is guaranteed to be within specifications.

Note 10: Deterministic jitter is characterized with 2^7 - 1 PRBS + 80 zeros + 80 ones at 10.7Gbps.

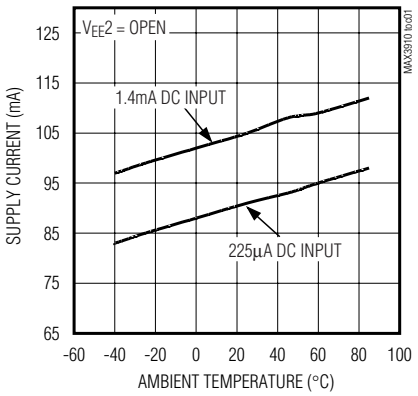
Note 11: Bandwidth is measured in an electrical environment and corrected to match the conditions of Note 2.

10.7Gbps Linear Transimpedance Amplifier with Output Offset Adjust

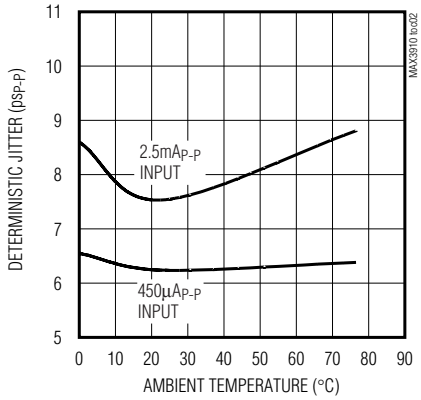
Typical Operating Characteristics

(V_{EE} = -5.2V, V_{CC} = GND, T_A = +25°C, unless otherwise noted.)

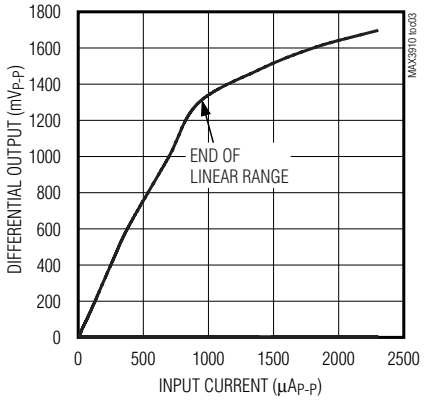
SUPPLY CURRENT



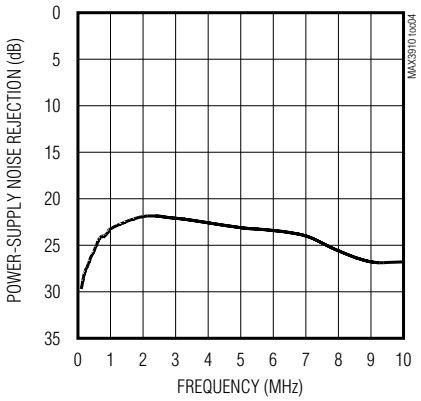
DETERMINISTIC JITTER



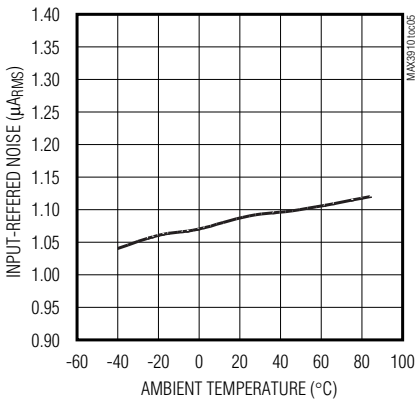
LINEAR RANGE



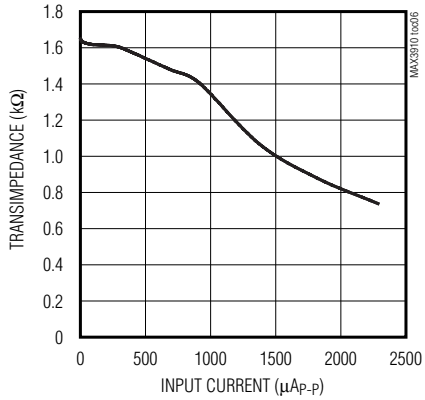
POWER-SUPPLY NOISE REJECTION



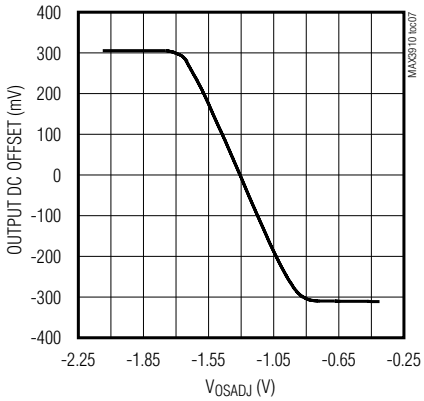
INPUT-REFERRED NOISE



TRANSIMPEDANCE



OFFSET ADJUST CIRCUIT

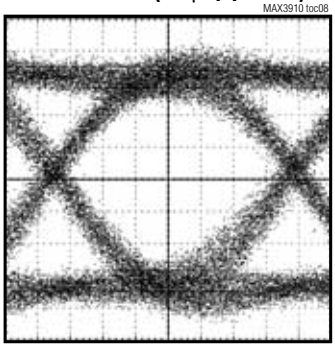


10.7Gbps Linear Transimpedance Amplifier with Output Offset Adjust

Typical Operating Characteristics (continued)

(V_{EE} = -5.2V, V_{CC} = GND, T_A = +25°C, unless otherwise noted.)

ELECTRICAL EYE DIAGRAM (150µAP-P INPUT)



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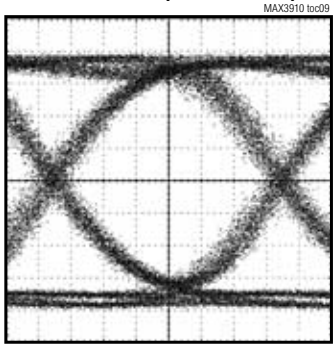
ELECTRICAL EYE DIAGRAM (1mAP-P INPUT)



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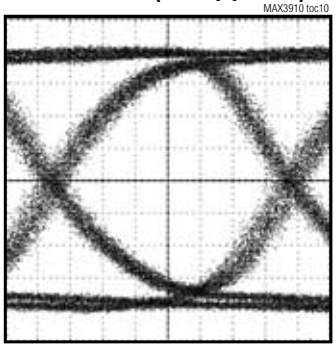
ELECTRICAL EYE DIAGRAM (2.5mAP-P INPUT)



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Pad Description

PAD	NAME	FUNCTION
1, 8–16, 31, 32, 33	$V_{EE}1$	Main Negative Power-Supply Voltage*
2	MONIN	Monitor Output Providing Replica Current from DC Offset Loop. Internally connected to V_{CC} through 1kΩ resistor.
3, 4, 7	N.C.	No Connection. Do not connect.
5	IN	Signal Input. Connected to photodiode anode.
6	FILT	On-Chip Resistor for Photodiode Biasing. Internally connected to V_{CC} through a 200Ω resistor.
17	$V_{EE}2$	Separate Power Supply for Output Offset Adjustment. Leave open to disable this feature. Offset adjust feature must be disabled for AC-coupled load.*
18, 19, 21, 23, 24, 26, 30	V_{CC}	Positive Power-Supply Voltage*
20	OUT-	Inverted Data Output with 50Ω Back Termination
22	OUT+	Noninverted Data Output with 50Ω Back Termination
25	CHF	Connect a capacitor to ground to increase the on-chip DC-cancellation loop time constant.
27	MON-	Monitors DC Voltage at OUT-. Internally connected to OUT- through a 10kΩ resistor.
28	MON+	Monitors DC Voltage at OUT+. Internally connected to OUT+ through a 10kΩ resistor.
29	OSADJ	DC Offset Control. Voltage at this pad sets the output DC offset when the offset adjust feature is enabled. (See Figure 3.)

**The MAX3910 can operate with a positive supply (V_{EE} = GND) or a negative supply (V_{CC} = GND). 4.75V ≤ (V_{CC} - V_{EE}) ≤ 5.5V.*

10.7Gbps Linear Transimpedance Amplifier with Output Offset Adjust

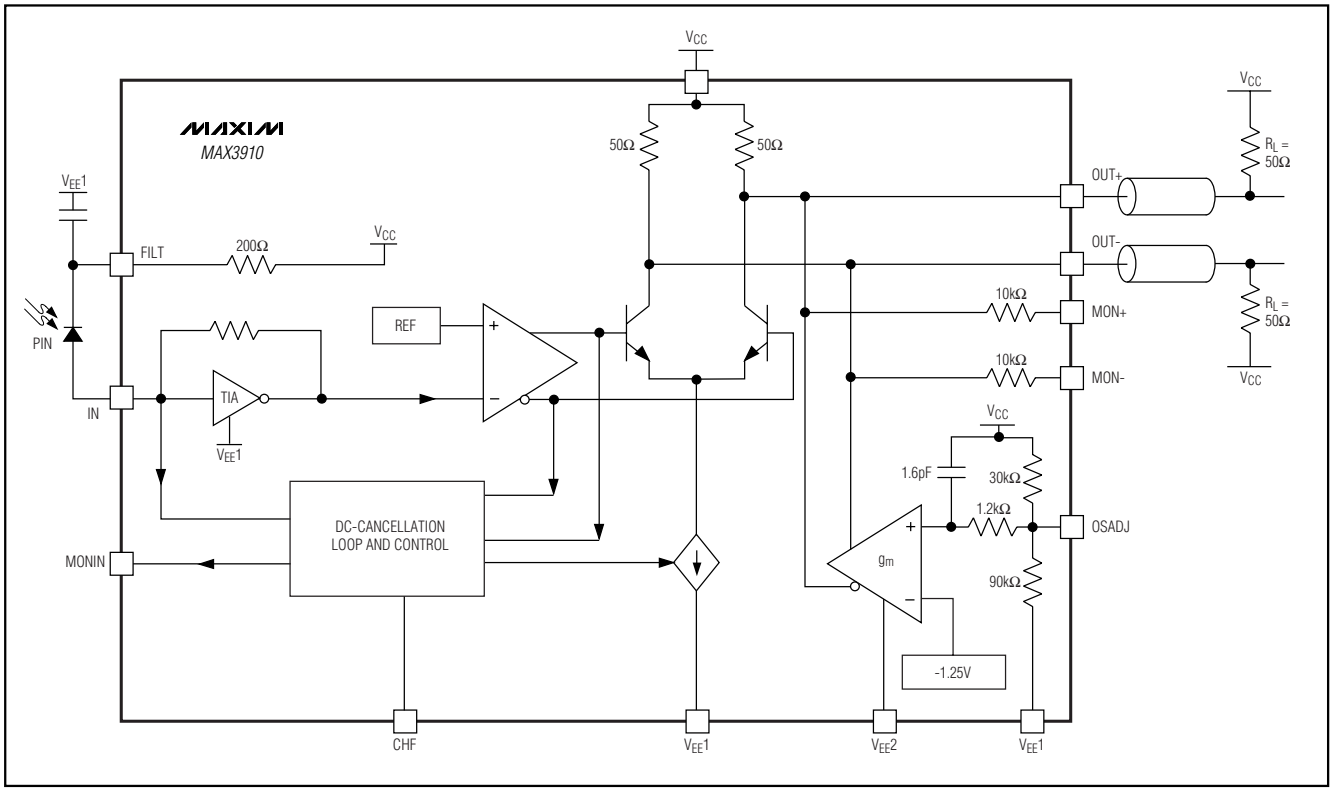

Figure 1. Functional Diagram

Detailed Description

Figure 1 is a functional diagram of the MAX3910 linear transimpedance amplifier. It comprises a transimpedance amplifier stage, a gain stage, an output buffer, and a DC-cancellation circuit. An output offset adjust circuit is implemented to perform threshold adjust for systems using optical amplifiers.

Transimpedance Amplifier

The photodiode current flows into the summing node of a high-gain amplifier and a shunt feedback resistor. A DC-cancellation circuit removes the average current, and the AC component is linearly converted into a voltage over a wide input range.

DC-Cancellation Loop

The DC-cancellation circuit uses low-frequency feedback to remove the DC component of the input signal. This feature centers the input signal within the transimpedance amplifier's linear range, thereby reducing pulse-width distortion (PWD) on large input signals. The DC-cancellation circuit has a built-in capacitor to achieve a low-frequency cutoff of 25kHz, and an external capacitor bonded between CHF and V_{CC} can be used to further reduce the cutoff frequency. This circuit minimizes PWD for data sequences that exhibit a 50% duty cycle and mark density. A duty cycle or mark density significantly different from 50% causes the MAX3910 to generate PWD.

Voltage Amplifier

The single-ended signal from the transimpedance amplifier stage is converted to a differential signal and further amplified.

Output Buffer

In addition to having a wide linear range, the MAX3910 has a soft-limiting feature. For inputs less than 950μA_{P-P}, the MAX3910 operates linearly. Beyond this range, a soft-limiting feature is implemented so that the differential output swing is proportional to the input current, as shown in Figure 2. The output buffer is back-terminated with 50Ω on-chip resistors and can drive either a DC-coupled 50Ω load to V_{CC} or a 50Ω AC-coupled load.

10.7Gbps Linear Transimpedance Amplifier with Output Offset Adjust

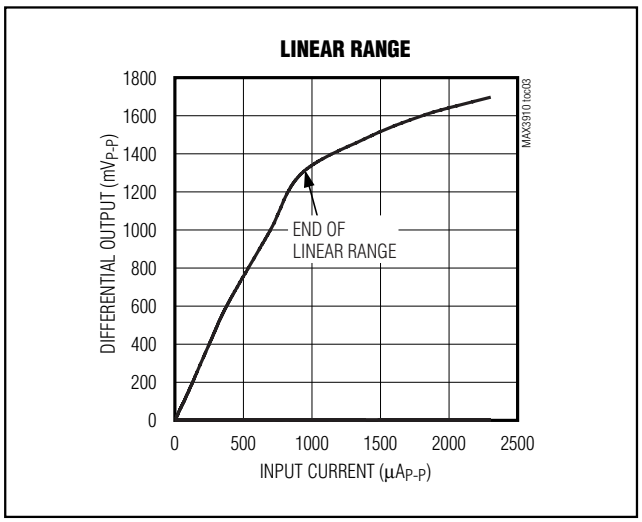

Figure 2. Linear Range of the MAX3910

Offset Adjust Circuit

Connecting $V_{EE}2$ to the negative supply enables the offset adjust circuit. The circuit compares the external voltage applied to the OSADJ pad to an internal (V_{CC} - 1.25V) reference to introduce a DC offset at the differential outputs (Figure 3). This function is useful in systems that need threshold adjust. For AC-coupled loads, the circuit must be disabled.

The input network of the offset adjust circuit creates a lowpass filter with a cutoff frequency of approximately 85MHz. If the pad is left unconnected, an internal voltage-divider sets the voltage at the pad to (V_{CC} - 1.25V). The input impedance is approximately 20kΩ.

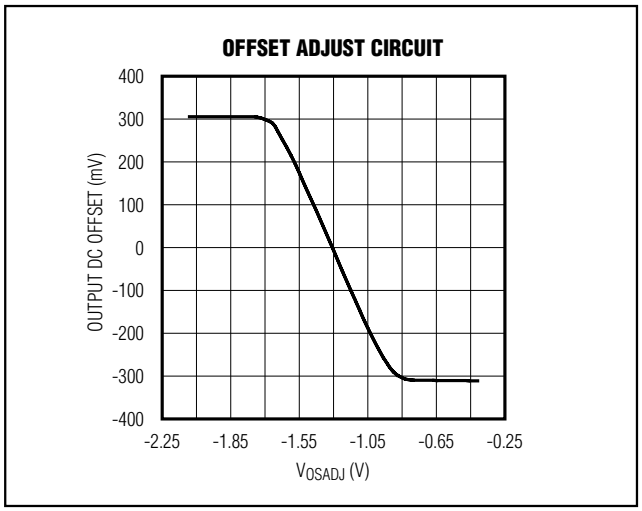

Figure 3. Offset Adjust Circuit Behavior

MONIN Pad

The voltage at MONIN (V_{MONIN}) serves as a received signal strength indicator (RSSI). The transimpedance gain of the average input current (I_{INAVE}) to V_{MONIN} is typically:

$$\frac{\Delta V_{MONIN}}{\Delta I_{INAVE}} = 1000(V/A)$$

Design Procedure

Power Supply

The MAX3910 requires wideband power-supply decoupling. Power-supply bypassing should provide low impedance between $V_{EE}1$ and V_{CC} for frequencies up to 10GHz. If the offset-adjust circuit is enabled, it is recommended that the same filtering be applied to $V_{EE}2$.

Photodiode Filter

Supply-voltage noise at the cathode of the photodiode produces a noise current $I = C_{PD}\ \Delta V/\Delta t$, which reduces the receiver sensitivity (C_{PD} is the photodiode capacitance). The MAX3910 contains an internal 200Ω resistor between the FILT pad and V_{CC}. Combining this resistor with an external capacitor connected between the FILT pad and $V_{EE}1$ creates a lowpass filter, which reduces photodiode noise current and improves receiver sensitivity. Current generated by supply-noise voltage is divided between the external capacitance and the photodiode capacitance. Assuming the filter capacitance is much larger than the photodiode capacitance, the input noise current because of supply noise is:

$$I_{NOISE} = \frac{V_{NOISE} \times C_{PD}}{R_{FILT} \times C_{FILT}}$$

where C_{FILT} is the external capacitance. If the amount of tolerable noise is known, the filter capacitance can be selected easily.

Wire Bonding

For high-current density and reliable operation, the MAX3910 uses gold metalization. Make connections to the die with gold wire only. Aluminum bonding is not recommended. Die thickness is typically 8 mils. Bondwire inductance between the photodiode and the IN pad can be optimized to obtain best performance. Higher inductance improves bandwidth, and lower bondwire inductance reduces time domain ringing. Keep bondwires on all other pads as short as possible to optimize performance. The backside of the MAX3910 die is fully insulated and can be connected to V_{CC} or V_{EE}.

10.7Gbps Linear Transimpedance Amplifier with Output Offset Adjust

Input Capacitance

Noise and bandwidth are adversely affected by capacitance on the MAX3910's input node. Use any techniques available to minimize input capacitance.

Output-Coupling Capacitors

The outputs of the MAX3910 can be AC- or DC-coupled. For more information on selecting AC-coupling capacitors, visit Maxim's website and follow the links to HFAN-01.1: *Choosing AC-Coupling Capacitors*.

Applications Information

Optical Power Relations

Many MAX3910 specifications relate to the input signal amplitude. When working with fiber optic receivers, the input sometimes is expressed in terms of average optical power and extinction ratio.

Optical power relations are shown in Table 1 for an average mark density of 50% and an average duty cycle of 50%.

Optical Sensitivity Calculation

The MAX3910 input-referred RMS noise current (I_N) generally determines receiver sensitivity. To obtain a system bit-error rate of 10^{-12}, the signal-to-noise ratio must be 14.1 or better. The input sensitivity, expressed in average power, can be estimated as:

$$\text{Sensitivity} = 10\log\left(\frac{14.1\times I_N\times(r_e+1)}{2\times\rho\times(r_e-1)}\times 1000\right)\text{dBm}$$

where ρ is the photodiode responsivity in A/W, and I_N is measured in amperes.

Input Optical Overload

The overload is the largest input that the MAX3910 accepts while meeting specifications. Optical overload can be estimated in terms of average power with the following equation:

$$\text{Overload} = 10\log\left(\frac{I_{OL}\times(r_e+1)}{2\times\rho\,(r_e-1)}\right)\text{dBm}$$

where $I_{OL}(mA_{P-P})$ is the DC overload for the MAX3910.

Optical Linear Range

The MAX3910 has high gain and operates in a linear range for inputs not exceeding:

$$\text{Linear range} = 10\log\left(\frac{I_{LIN}\times(r_e+1)}{2\times\rho\,(r_e-1)}\right)\text{dBm}$$

where $I_{LIN}(mA_{P-P})$ is the peak-to-peak linear range.

Table 1. Optical Power Relations*

PARAMETER	SYMBOL	PIN-PACKAGE
Average	P_{AVG}	$P_{AVG} = (P0 + P1) / 2$
Extinction	r_e	$r_e = P1 / P0$
Optical Power of a 1	P1	$P1 = 2P_{AVG}\frac{r_e}{r_e+1}$
Optical Power of a 0	P0	$P0 = 2P_{AVG} / (r_e + 1)$
Optical Modulation Amplitude	P_{IN}	$P_{IN} = P1 - P0 = 2P_{AVG}\frac{r_e-1}{r_e+1}$

**Assuming a 50% average mark density.*

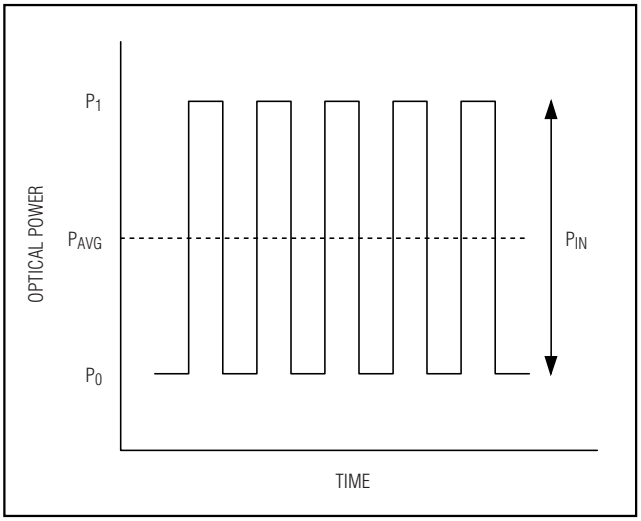

Figure 4. Optical Power Relations

10.7Gbps Linear Transimpedance Amplifier with Output Offset Adjust

Pad Coordinates

PAD	NAME	COORDINATES (µm)	
		X	Y
1	$V_{EE}1$	38	1259
2	MONIN	43	1034
3	N.C.	43	908
4	N.C.	43	782
5	IN	43	656
6	FILT	43	530
7	N.C.	50	282
8	$V_{EE}1$	47	47
9	$V_{EE}1$	173	47
10	$V_{EE}1$	299	47
11	$V_{EE}1$	425	47
12	$V_{EE}1$	551	47
13	$V_{EE}1$	677	47
14	$V_{EE}1$	803	47
15	$V_{EE}1$	929	47
16	$V_{EE}1$	1055	47
17	$V_{EE}1$	1181	47
18	V_{CC}	1255	267
19	V_{CC}	1255	393
20	OUT-	1255	519
21	V_{CC}	1255	645
22	OUT+	1255	771
23	V_{CC}	1255	897
24	V_{CC}	1255	1055
25	CHF	1172	1259
26	V_{CC}	1046	1259
27	MON-	920	1259
28	MON+	794	1259
29	OSADJ	668	1259
30	V_{CC}	542	1259
31	$V_{EE}1$	416	1259
32	$V_{EE}1$	290	1259
33	$V_{EE}1$	164	1259

Coordinates are in µm from the lower left corner of the circuit die to the center of the pad. For more information, refer to HFAN-08.0.1: Understanding Bonding Coordinates and Physical Die Size.

Chip Information

TRANSISTOR COUNT: 1291

PROCESS: BiPOLAR SiGe, SOI

Die Size: 1.6mm × 1.6mm