19-2605; Rev 0; 10/02

MAXIM

10.7Gbps Compact Laser Diode Driver

General Description

The MAX3934 is a compact +5V or -5.2V laser driver designed to directly modulate a laser diode at data rates up to 10.7Gbps. The driver provides externally programmable laser biasing and modulation currents. DC-coupling with an integrated compensation network, consisting of a series-damping resistor and a shunt RC, makes the MAX3934 ideal for compact subassemblies.

The MAX3934 accepts a differential CML or PECL data signal and includes 50Ω on-chip termination resistors. It delivers a 1mA to 60mA laser bias current and a 20mA to 80mA laser modulation current with a typical edge speed of 25ps (20% to 80%). A high-bandwidth, fully differential signal path is internally implemented to minimize jitter accumulation. Additional features include a data polarity control, bias current, and modulation current monitors.

Applications

Compact Optical Transmitters

Add/Drop Multiplexer

XFP Modules

XENPAK/XPAK Modules

Features

- **1.30mm × 1.35mm Die Size**
- **Integrated Compensation Network**
- **Single +5V or -5.2V Power Supply**
- **73mA Supply Current**
- **Up to 10.7Gbps (NRZ) Operation**
- **Programmable Laser Bias Current Up to 60mA**
- **Programmable Modulation Current Up to 80mA**
- **Polarity Control**
- **25ps Output Edge Speed**
- **CML-/PECL-Compatible Signal Inputs**
- **Integrated Input Termination Resistors**

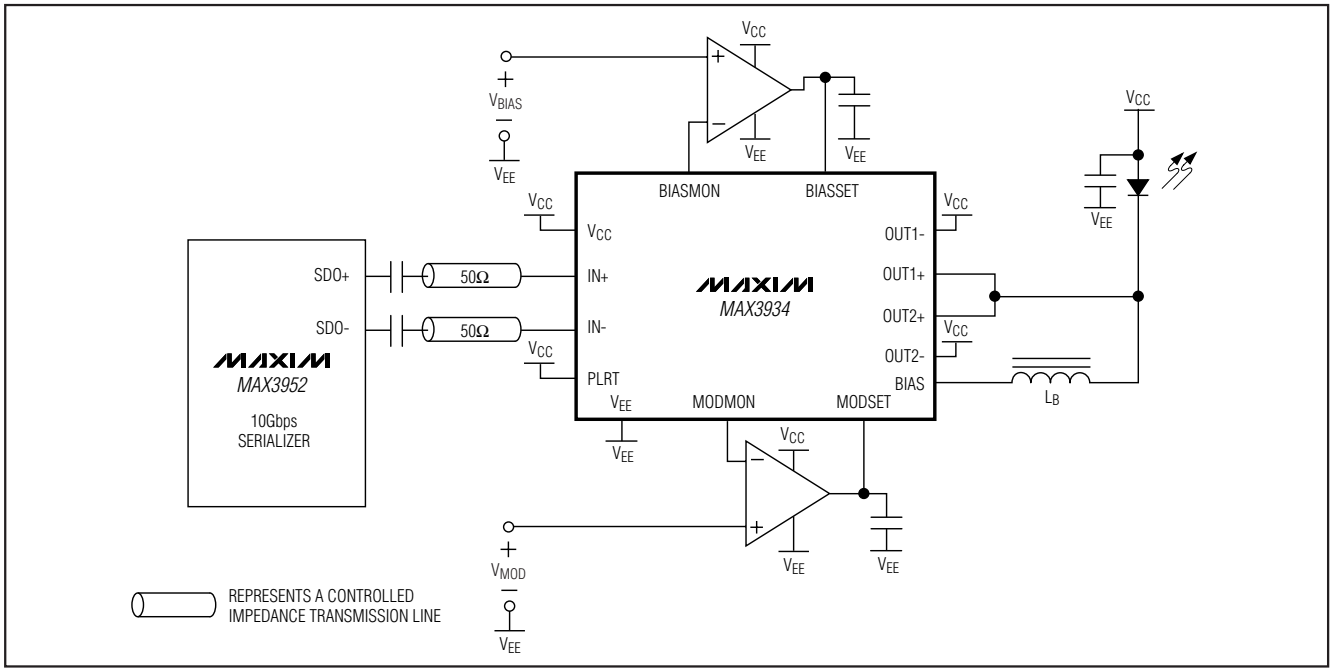
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	R_D/C_{COMP}**
MAX3934AE/D	-40°C to +85°C	Dice*	12Ω/580fF
MAX3934BE/D	-40°C to +85°C	Dice*	15Ω/464fF

**Dice are designed to operate over a -40°C to +120°C junction temperature (T_J) range, but are tested and guaranteed only at T_A = +25°C.*

***See Figure 3.*

Typical Application Circuit



10.7Gbps Compact Laser Diode Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} - V_{EE}) .....-0.5V to +6.0V
Voltage at IN+, IN- .....(V_{CC} - 1.2V) to (V_{CC} + 0.5V)
PLRT, BIASMON, MODMON .....(V_{EE} - 0.5V) to (V_{CC} + 0.5V)
BIASSET .....(V_{EE} - 0.5V) to (V_{EE} + 2.6V)
MODSET .....(V_{EE} - 0.5V) to (V_{EE} + 1.4V)
Current into IN+, IN-.....-24mA to +30.5mA
Current into OUT1+, OUT2+,OUT1-, OUT2-....-20mA to +200mA
Current into BIAS .....-20mA to +100mA
Storage Temperature Range .....-55°C to +150°C
Operating Junction Temperature Range.....-55°C to +150°C
Processing Temperature (die) .....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 4.75V to 5.5V, T_A = -40°C to +85°C. Typical values are at V_{CC} - V_{EE} = 5V, I_{BIAS} = 35mA, I_{MOD} = 65mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{CC} - V_{EE}		4.75	5	5.50	V
Power-Supply Current	I_{CC}	Excluding I_{MOD} and I_{BIAS}, data inputs AC-coupled		73	110	mA
Power-Supply Noise Rejection	PSNR	(Notes 1, 2)		20		dB
SIGNAL INPUT						
Input Data Rates		NRZ		10.7		Gbps
Single-Ended Input Resistance		To V_{CC}	42.5	50	58.5	Ω
Single-Ended Input Return Loss (Note 1)		f < 10GHz		14		dB
		10GHz ≤ f ≤ 15GHz		8		
Single-Ended Input Voltage (DC-Coupled)	V_{IS}	Figure 2a	V_{CC} - 1		V_{CC}	V
Single-Ended Input Voltage (AC-Coupled)	V_{IS}	Figure 2b	V_{CC} - 0.4		V_{CC} + 0.4	V
Differential Input Voltage (DC-Coupled)	V_{ID}	Figure 4	0.2		2.0	V_{P-P}
Differential Input Voltage (AC-Coupled)	V_{ID}	Figure 4	0.2		1.6	V_{P-P}
LASER BIAS						
Bias Current-Setting Range	I_{BIAS}	(Note 3)	1		60	mA
Bias Sensing Resistor	R_{BIAS}		5.4	6	6.6	Ω
Bias Current Temperature Stability		(Note 1)	-480		+480	ppm/°C
Bias Current-Setting Error (Note 3)		I_{BIAS} ≥ 10mA, V_{BIAS} < V_{CC} - 1.2V	-10		+10	%
		I_{BIAS} = 1mA, V_{BIAS} < V_{CC} - 1.2V	-20		+20	
Bias Off-Current		BIASSET ≤ V_{EE} + 0.4V			0.1	mA
LASER MODULATION						
Modulation Current-Setting Range	I_{MOD}	(Note 5)	20		80	mA
Modulation Sensing Resistor	R_{MOD}		2.7	3	3.3	Ω
Modulation Current Temperature Stability		(Note 1)	-480		+480	ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = 4.75V to 5.5V, T_A = -40°C to +85°C. Typical values are at V_{CC} - V_{EE} = 5V, I_{BIAS} = 35mA, I_{MOD} = 65mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Modulation Current-Setting Error		V_{OUT_+} < V_{CC} - 1.2V (Note 5)	-10		+10	%
Modulation Off-Current		MODSET ≤ V_{EE} + 0.4V			0.2	mA
Output Edge Speed	t_R, t_F	20% to 80% (Notes 1, 4, 6)		25	35	ps
Output Overshoot/Undershoot	δ	(Notes 1, 4, 6)	-15		+15	%
Driver Random Jitter	RJ	R_{EXT} + R_D = 20Ω (Note 1)		0.3		ps_{RMS}
Driver Deterministic Jitter	DJ	(Notes 1, 7)		9.7		ps_{P-P}
TTL INPUT						
Input High Voltage			V_{EE} + 2.0			V
Input Low Voltage					V_{EE} + 0.8	V
Input Current			-70		+70	µA

Note 1: Guaranteed by design and characterization using the circuit shown in Figure 1.

Note 2: PSNR = 20 × log[ΔV_{CC} / (ΔI_{MOD} × 20)]. Measured with ΔV_{CC} = 100mV_{P-P} and f ≤ 10MHz. Excludes the effect of the external op amp.

Note 3: The minimum voltage at the BIAS pad is V_{EE} + 1.85V + (I_{BIAS} × 8Ω).

Note 4: The combined driver AC load (on-chip load and off-chip laser load) is 20Ω. Measured using a 10.7Gbps repeating 0000 0000 1111 1111 pattern.

Note 5: The minimum voltage at the OUT_+ pad is V_{EE} + 1.65V + (I_{MOD} × R_D) (Figure 3).

Note 6: The maximum allowed inductance per bond wire is 0.4nH for OUT1±, OUT2±, V_{CC}, V_{EE}, and 0.5nH for IN±.

Note 7: Deterministic jitter is defined as the arithmetic sum of PWD (pulse-width distortion) and PDJ (pattern-dependent jitter). Measured using a 10.7Gbps 2^7 - 1 PRBS with eighty 0s and eighty 1s inserted in the data pattern.

10.7Gbps Compact Laser Diode Driver

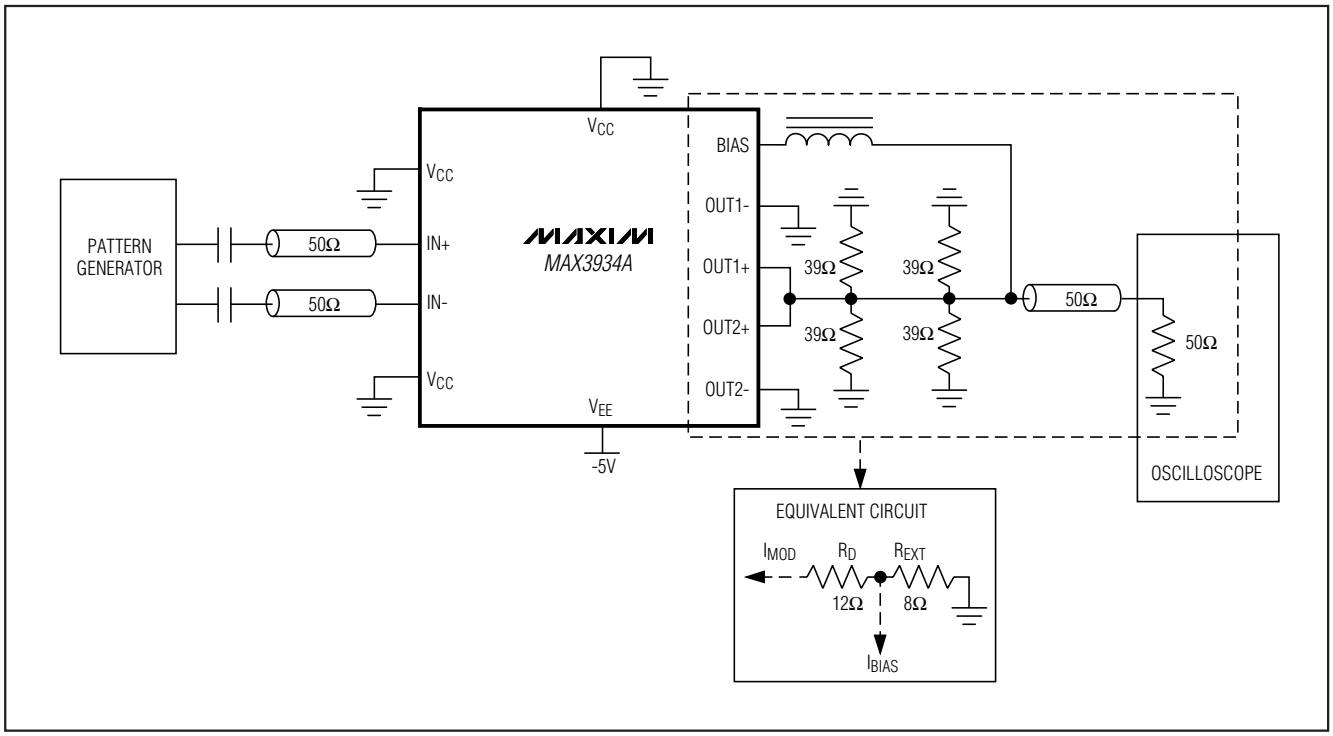


Figure 1. AC Characterization Circuit

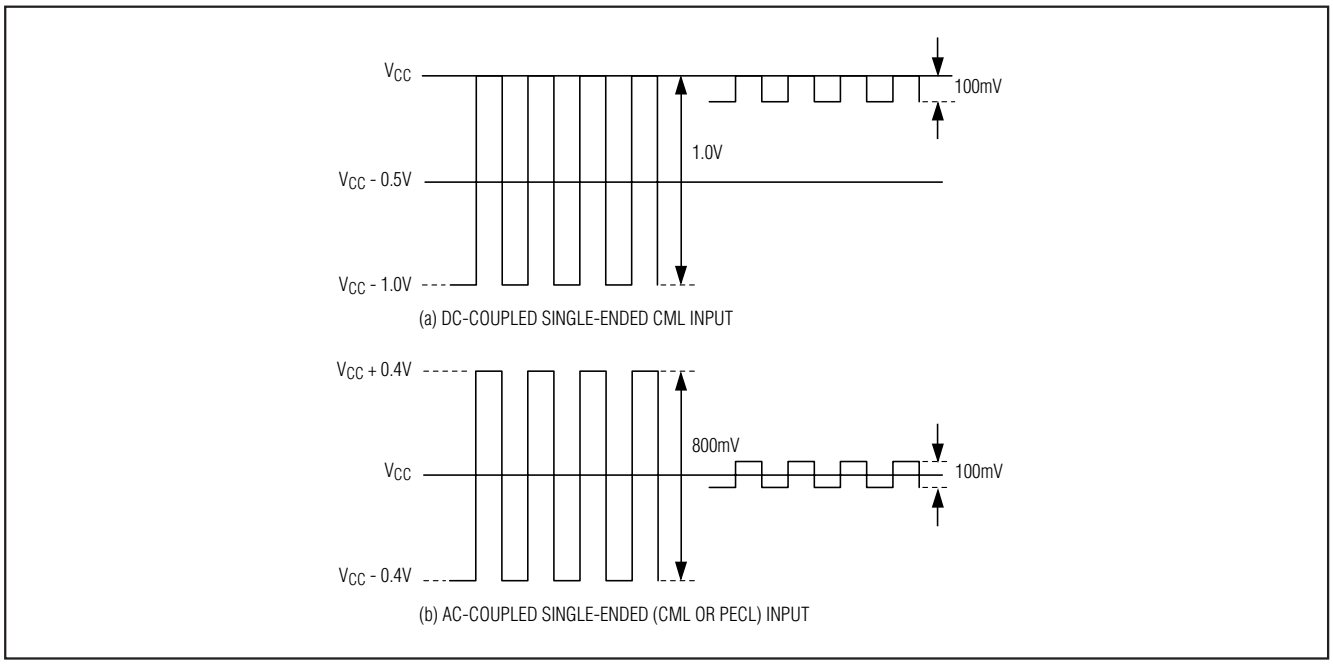
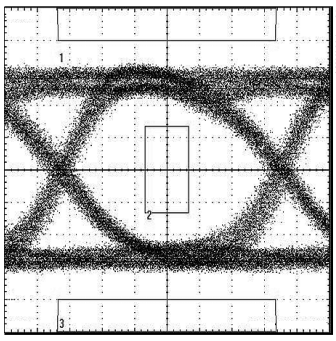


Figure 2. Definition of Input Voltage Swing

Typical Operating Characteristics

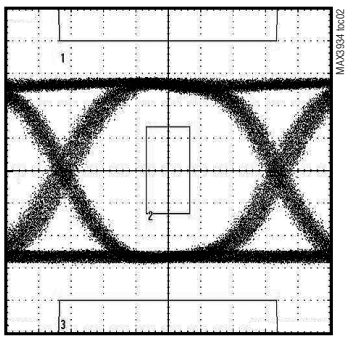
(Typical values at V_{CC} - V_{EE} = 5V, I_{BIAS} = 35mA, I_{MOD} = 65mA, T_A= +25°C, unless otherwise noted.)

OC-192 OPTICAL EYE DIAGRAM (I_{MOD} = 55mA, I_{BIAS} = 30mA, 2^{23} - 1 PRBS)



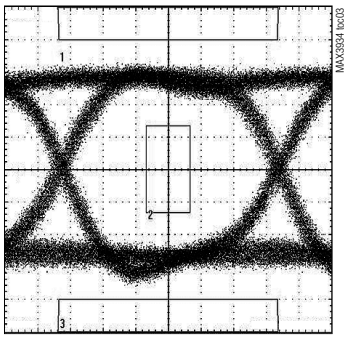
15ps/div

OC-192 ELECTRICAL EYE DIAGRAM (I_{MOD} = 80mA, 2^{23} - 1 PRBS)



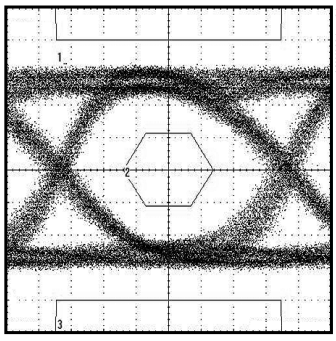
15ps/div

OC-192 ELECTRICAL EYE DIAGRAM (I_{MOD} = 20mA, 2^{23} - 1 PRBS)



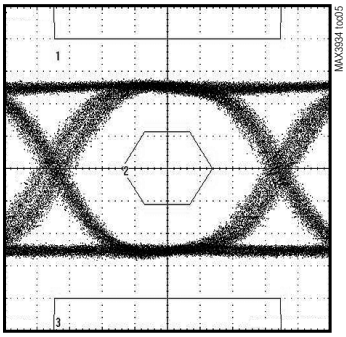
15ps/div

10.31Gbps OPTICAL EYE DIAGRAM (I_{MOD} = 55mA, I_{BIAS} = 30mA, 2^{23} - 1 PRBS)



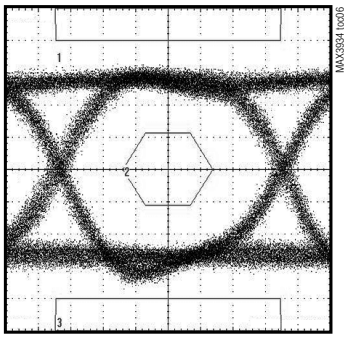
14ps/div

10.31Gbps ELECTRICAL EYE DIAGRAM (I_{MOD} = 80mA, 2^{23} - 1 PRBS)



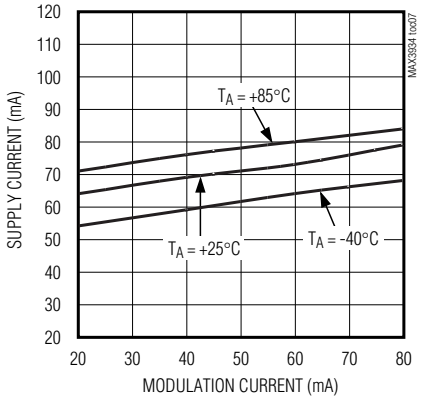
14ps/div

10.31Gbps ELECTRICAL EYE DIAGRAM (I_{MOD} = 20mA, 2^{23} - 1 PRBS)

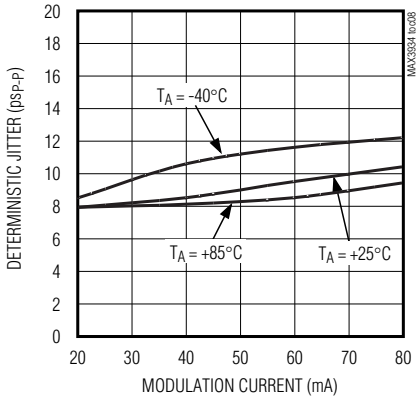


14ps/div

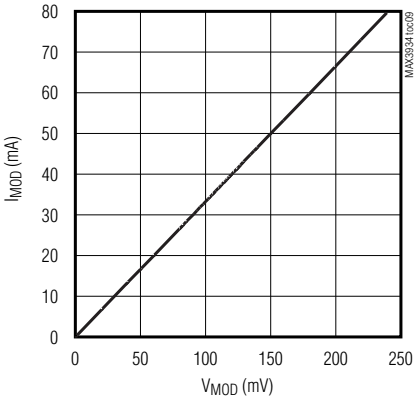
SUPPLY CURRENT vs. MODULATION CURRENT (EXCLUDES BIAS AND MODULATION CURRENTS)



DETERMINISTIC JITTER vs. MODULATION CURRENT (10.7Gbps, 2^7 - 1 PRBS + 80CIDS)



I_{MOD} vs. V_{MOD}

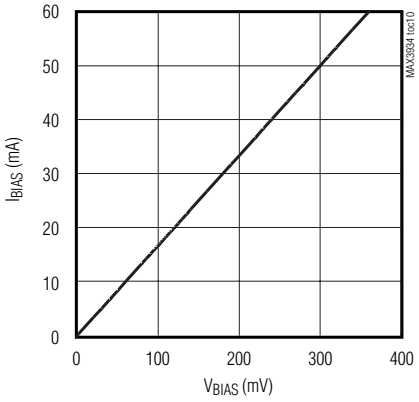


10.7Gbps Compact Laser Diode Driver

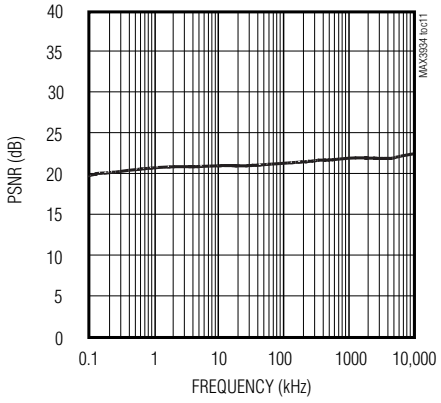
Typical Operating Characteristics (continued)

(Typical values at V_{CC} - V_{EE} = 5V, I_{BIAS} = 35mA, I_{MOD} = 65mA, T_A= +25°C, unless otherwise noted.)

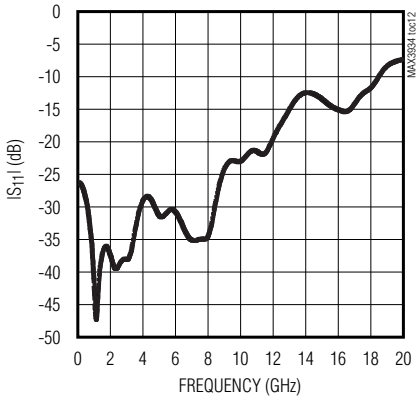
I_{BIAS} vs. V_{BIAS}



POWER-SUPPLY NOISE REJECTION vs. FREQUENCY



DIFFERENTIAL S_{11} vs. FREQUENCY



Pad Description

PAD	NAME	FUNCTION
1–5, 17–20	V_{EE}	Negative Supply Voltage. All pads must be connected to V_{EE}.
6	BIASSET	Bias Current Set. Connected to the output of an external op amp (see the *Design Procedure* section).
7	BIASMON	Bias Current Monitor ($V_{BIASMON}$ - V_{EE}) / R_{BIAS} = I_{BIAS}
8, 9, 11, 13, 21, 22, 27	V_{CC}	Positive Supply Voltage. All pads must be connected to V_{CC}.
10	IN+	Positive Data Input. CML/PECL with 50Ω integrated termination resistor.
12	IN-	Negative Data Input. CML/PECL with 50Ω integrated termination resistor.
14	PLRT	Differential Data Polarity Swap Input. TTL. Set high or floating for normal operation. Set low to invert the differential signal polarity.
15	MODMON	Modulation Current Monitor (V_{MODMON} - V_{EE}) / R_{MOD} = I_{MOD}
16	MODSET	Modulation Current Set. Connected to the output of an external op amp (see the *Design Procedure* section).
23, 26	OUT2-, OUT1-	Complementary Laser Modulation Current Outputs. Include 20Ω equivalent on-chip output resistor. Connect both to V_{CC}.
24, 25	OUT2+, OUT1+	Laser Modulation Current Outputs. Include integrated damping resistor and provide laser modulation current (sinking). Connect both to laser diode cathode.
28	BIAS	Laser Bias Current Output (Sinking)

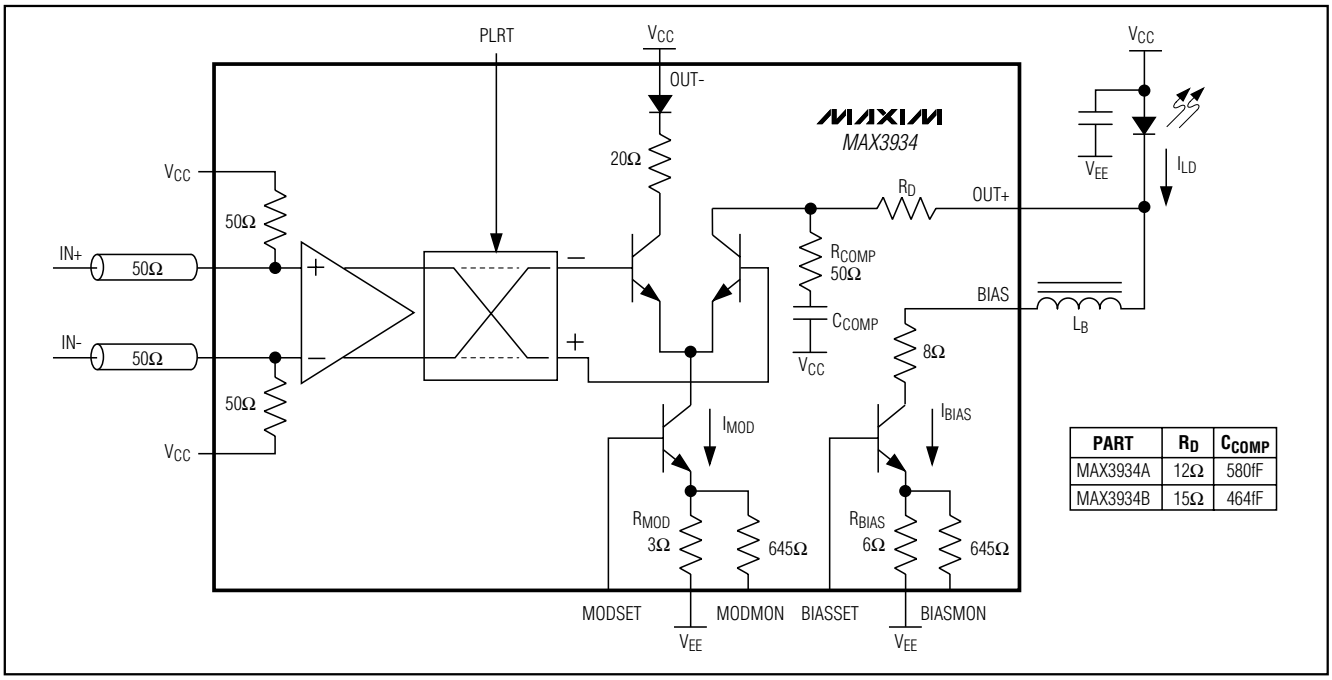


Figure 3. Functional Diagram

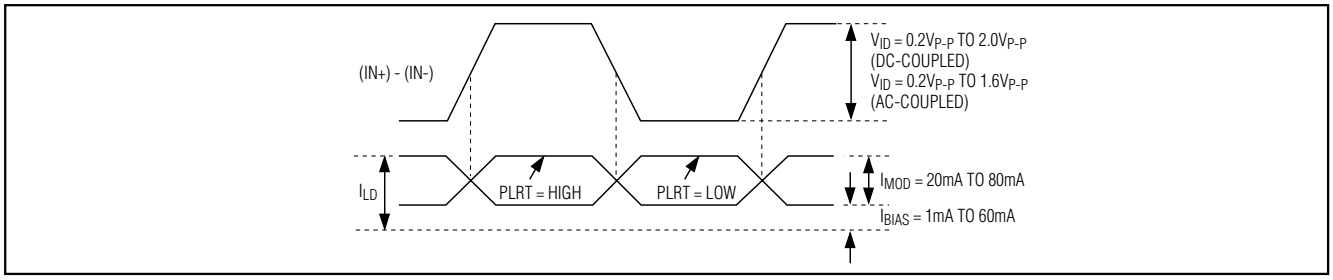


Figure 4. Required Input Signal and Output Polarity

Detailed Description

The MAX3934 laser driver consists of two main parts, a high-speed modulation driver and a laser-biasing block (see Figure 3). The circuit operates from a single +5V or -5.2V supply. When operating from a +5V supply, connect all V_{CC} pads to +5V and all V_{EE} pads to ground. If operating from a -5.2V supply, connect all V_{EE} pads to -5.2V and all V_{CC} pads to ground.

The modulation output stage is composed of a high-speed differential pair and a programmable modulation current source with a maximum modulation current of 80mA. The rise and fall times are typically 25ps.

The MAX3934 contains an integrated damping resistor (R_D) with the value of 12Ω or 15Ω depending on part version. The modulation output is optimized for driving a 20Ω load; therefore, the total series load of R_D and R_{LD} (where R_{LD} represents the laser diode resistance) should equal 20Ω.

At the data rate of 10.7Gbps, capacitive loads at the cathode of a laser diode degrade the optical output performance. Because the BIAS output is directly connected to the laser cathode, use a ferrite bead (L_B) with low shunt capacitance to isolate the BIAS pad from the laser cathode.

Polarity Switch

The MAX3934 includes a TTL controlled polarity switch. When the PLRT pad is high or floating, the output maintains the polarity of the input data. When the PLRT pad is low, the output is inverted relative to the input data (see Figure 4).

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVG}	$P_{AVG} = (P_0 + P_1) / 2$
Extinction Ratio	r_e	$r_e = P_1 / P_0$
Optical Power of a "1"	P_1	$P_1 = 2P_{AVG} r_e / (r_e + 1)$
Optical Power of a "0"	P_0	$P_0 = 2P_{AVG} / (r_e + 1)$
Optical Amplitude	P_{P-P}	$P_{P-P} = P_1 - P_0 = 2P_{AVG}(r_e - 1) / (r_e + 1)$
Laser Slope Efficiency	η	$\eta = P_{P-P} / I_{MOD}$
Modulation Current	I_{MOD}	$I_{MOD} = P_{P-P} / \eta$

Note: *Assuming a 50% average duty cycle and mark density.*

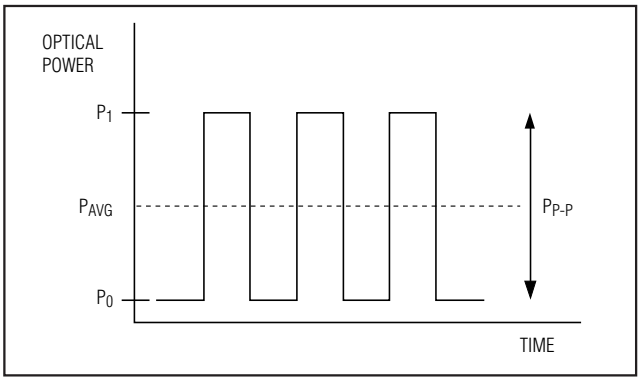


Figure 5. Optical Power Definitions

Current Monitors

The MAX3934 features a bias current monitor output (BIASMON) and a modulation current monitor output (MODMON). The voltage at BIASMON is equal to ($I_{BIAS} \times R_{BIAS}$) + V_{EE}, and the voltage at MODMON is equal to ($I_{MOD} \times R_{MOD}$) + V_{EE}, where I_{BIAS} represents the laser bias current, I_{MOD} represents the modulation current, and R_{BIAS} and R_{MOD} are internal 6Ω and 3Ω (±10%) resistors, respectively. BIASMON and MODMON should be connected to the inverting input of an operational amplifier to program the bias and modulation current (see the *Design Procedure* section).

Design Procedure

When designing a laser transmitter, the optical output usually is expressed in terms of average power and extinction ratio. Table 1 gives relationships helpful in converting between the optical average power and the modulation current. These relationships are valid if the mark density and duty cycle of the optical waveform are 50%.

Programming the Modulation Current

For a desired laser average optical power (P_{AVG}) and optical extinction ratio (r_e) the required modulation current can be calculated based on the laser slope efficiency (η) using the equations in Table 1.

To program the desired modulation current, connect the inverting input of an op amp (such as the MAX4281) to MODMON and connect the output to MODSET. Connect the positive op-amp voltage supply to V_{CC} and the negative supply to V_{EE} (for +5V operation, V_{CC} = +5V and V_{EE} = ground; for -5.2V operation V_{CC} = ground and V_{EE} = -5.2V). Connect a reference voltage (V_{MOD}) to the noninverting input of the op amp to set the modulation current. See the I_{MOD} vs. V_{MOD} graph in the *Typical Operating Characteristics* to select the value of V_{MOD} that corresponds to the required modulation current.

Programming the Bias Current

To program the desired laser bias current, connect the inverting input of an op amp (such as the MAX4281) to BIASMON and connect the output to BIASSET. Connect the positive op-amp voltage supply to V_{CC} and the negative supply to V_{EE} (for +5V operation, V_{CC} = +5V and V_{EE} = ground; for -5.2V operation, V_{CC} = ground and V_{EE} = -5.2V). Connect a reference voltage (V_{BIAS}) to the noninverting input of the op amp to set the laser bias current. Refer to the I_{BIAS} vs. V_{BIAS} graph in the *Typical Operating Characteristics* to select the value of V_{BIAS} that corresponds to the required laser bias current.

External Op-Amp Selection

External op amps are required for regulating the bias and modulation currents. The ability to operate from a single supply with input common-mode range extending to the negative supply rail is critical in op-amp selection. Low bias current and high PSNR are also important. The op-amp gain bandwidth must be high enough to regulate at the power-supply ripple frequency to maintain the PSNR of the laser driver. Filtering the op-amp output is recommended (see the *Typical Application Circuit*). To maintain stability, the filter capacitor should be smaller than the op-amp capacitive load specification.

Interfacing with Laser Diodes

Refer to Maxim application note HFAN-2.0: *Interfacing Maxim Laser Drivers with Laser Diodes* for detailed information.

The MAX3934 contains an integrated damping resistor (R_D) with values of 12Ω or 15Ω, depending on part version. The modulation output is optimized for driving a 20Ω load; therefore, the total series load of R_D and R_{LD}

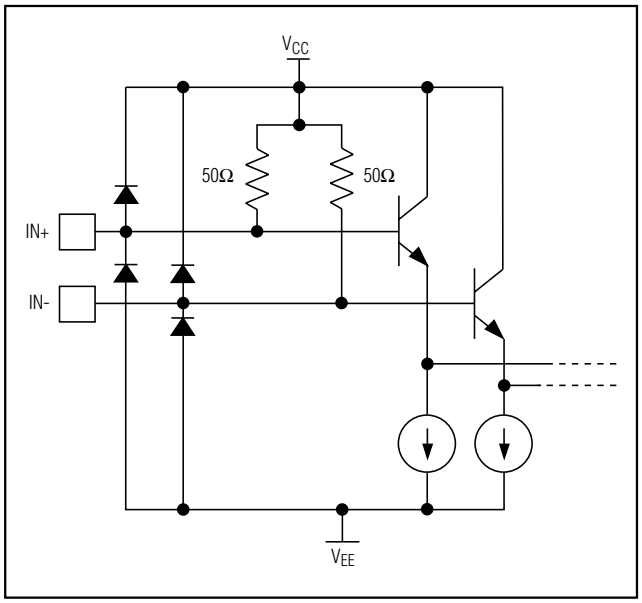


Figure 6. Equivalent Input Circuit

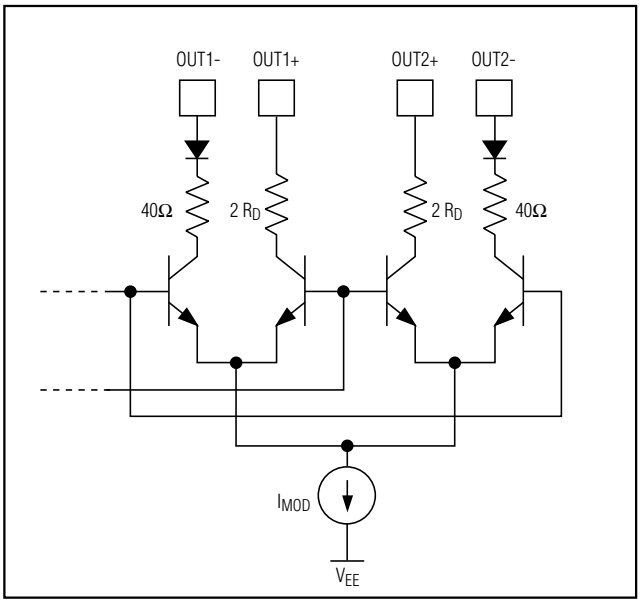


Figure 7. Equivalent Output Circuit

(where R_{LD} represents the laser diode resistance) should equal 20Ω.

In some applications (depending on the laser diode parasitic inductance), an RF matching network at the laser cathode improves the optical output.

For best performance, place a bypass capacitor as close as possible to the anode of the laser diode.

Applications Information

Interfacing to CML and PECL Outputs

The MAX3934 data input accepts CML or PECL signals, but care must be taken to maintain proper biasing and common-mode voltages. Refer to Figure 6 and the Maxim application note HFAN-01.0: *Introduction to LVDS, PECL, and CML* for additional information.

Wire-Bonding Die

For high-current density and reliable operation, the MAX3934 uses gold metalization. Make connections to the die with gold wire only, using ball-bonding techniques.

Minimize bond-wire lengths and ensure that the span between the ends of the bond wire does not come closer to the edge of the die than two times the bond-wire diameter. The minimum length of the bond wires might be constrained by the type of wire bonder used, as well as the dimensions of the die.

To minimize inductance, keep the connections from OUT1±, OUT2±, V_{CC}, and V_{EE} as short as possible. This is crucial for optimal performance. Both modulation outputs (OUT1+, OUT2+) must be bonded to the laser diode cathode for proper operation.

Layout Considerations

Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk. Use controlled impedance lines for the data inputs. Power-supply decoupling should be placed as close to the die as possible. Wafer capacitors are required to filter the V_{EE} supplies on both sides of the die. Connect the backside of the die to V_{CC}.

Laser Safety and IEC 825

Using the MAX3934 laser driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Each customer must determine the level of fault tolerance required by their application, recognizing that Maxim products are not designed or authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application where the failure of a Maxim product could create a situation where personal injury or death may occur.

10.7Gbps Compact Laser Diode Driver

Table 2. Bondpad Locations

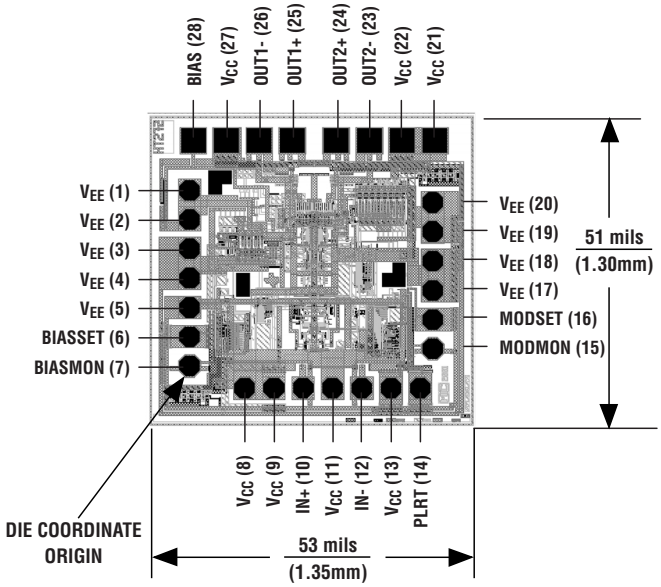
PAD	NAME	COORDINATES (μm)	
		X	Y
1	V_{EE}	16	711
2	V_{EE}	16	599
3	V_{EE}	16	487
4	V_{EE}	16	375
5	V_{EE}	16	263
6	BIASSET	16	151
7	BIASMON	16	39
8	V_{CC}	226	-46
9	V_{CC}	338	-46
10	IN+	450	-46
11	V_{CC}	562	-46
12	IN-	674	-46
13	V_{CC}	786	-46
14	PLRT	898	-46
15	MODMON	946	105
16	MODSET	946	217
17	V_{EE}	946	329
18	V_{EE}	946	441
19	V_{EE}	946	553
20	V_{EE}	946	665
21	V_{CC}	954	901
22	V_{CC}	828	901
23	OUT2-	704	901
24	OUT2+	576	901
25	OUT1+	408	901
26	OUT1-	282	901
27	V_{CC}	156	901
28	BIAS	30	901

Chip Topology/ Pad Configuration

The origin for pad coordinates is defined as the bottom left corner of the bottom left pad. All pad locations are referenced from the origin and indicate the center of the pad where the bond wire should be connected. Refer to Maxim application note HFAN-08.0.1: *Understanding Bonding Coordinates and Physical Die Size* for detailed information.

The die size is 51mil × 53mil (1.30mm × 1.35mm) with 3mil (76μm) octagonal pads and 4mil (102μm) square pads. The die thickness is 8 mils (203μm).

Chip Topology



Chip Information

TRANSISTOR COUNT: 884

SUBSTRATE: SOI

PROCESS: SiGe BIPOLAR

DIE THICKNESS: 8 mils