MAX40660/MAX40661

High-Bandwidth Automotive Transimpedance Amplifier with Fast Output Recovery and Input Current Clamp for LiDAR

General Description

The MAX40660/MAX40661 are transimpedance amplifiers for optical distance measurement receivers in LiDAR applications. Low noise, high gain, low group delay, and fast recovery from overload make these TIAs ideal for distance-measurement applications. Important features include 2.1pA input-referred noise density (MAX40660), an internal input clamp, pin-selectable 25kΩ and 50kΩ transimpedance, and wide bandwidth (490MHz (typ) for the MAX40660 with 0.5pF input capacitance and 25kΩ transimpedance; 160MHz (typ) for the MAX40661 with 10pF input capacitance). An offset current input allows optional adjustment of input offset current. A low-power/standby control input reduces the supply current by better than 80% to help reduce average power supply current between pulses. The MAX40660/MAX40661 transimpedance amplifiers feature AEC-Q100 qualification over the -40°C to +125°C automotive operating temperature range and are available in a 3mm x 3mm, 10-lead TDFN package with side-wettable flanks, making them excellent choices for automotive LiDAR applications.

In addition to the TDFN package, the MAX40660 is available as bare die.

Applications

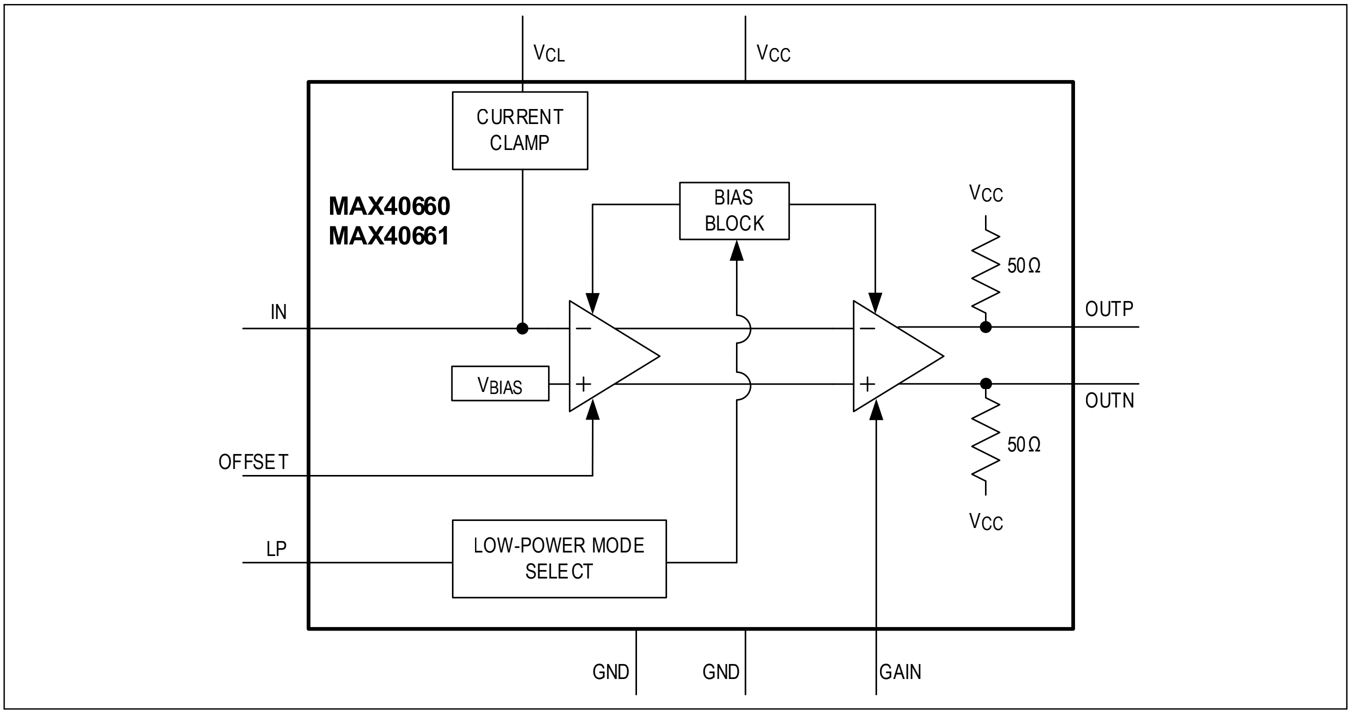
- Optical Distance Measurement
- LiDAR Receivers
- Industrial Safety Systems
- Autonomous Driving Systems
- Automotive Applications

Benefits and Features

- AEC-Q100
- Enables ASIL Compliance (FMEDA Available upon Request)
- MAX40660
  - Optimized for C_{IN} = 0.25pF to 5pF
  - Bandwidth = 490MHz (typ)
- MAX40661
  - Optimized for C_{IN} = 5pF to 12pF
  - Bandwidth (C_{IN} = 10pF) = 160MHz (typ), 100MHz (min)
- Low Noise
- Two Pin-Selectable Transimpedance Values
  - 25kΩ
  - 50kΩ
- Internal Clamp for Input Current up to 2A (Transient)
- Fast Overload Recovery: 2ns at 100mA
- Offset Input Provides Offset Adjust Feature
- LP Input Reduces Power Dissipation Between Pulses
- 3.3V Operation
- 10-Pin TDFN (Side-Wettable) or Bare Die

Ordering Information **appears at end of data sheet.**

Simplified Block Diagram



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Absolute Maximum Ratings

Supply Voltage .... -0.3V to +3.6V
Current Into IN (10ns pulse width, 0.5% duty cycle) ....-2A
Current Into IN, OFFSET (continuous)................ -0.4mA to 0mA
Current into LP, Gain (continuous)................... -10mA to +10mA
Current into OUTP and OUTN (continuous)...... -20mA to +20mA
Voltage at OUTN, OUTP .... V_{CC} + 0.3V
Voltage at GAIN, LP .... -0.3V to V_{CC} + 0.3V
Operating Temperature Range ....-40°C to +125°C
Operating Junction Temperature Range (die) ....-40°C to +150°C
Storage Temperature Range ....-55°C to +150°C
Soldering Temperature (reflow) ....+260°C
Die Attach Temperature...+400°C
Continuous Power Dissipation (T_A = +125°C, derate 24.4mW/°C above +70°C (multilayer board))................................1951.20mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

10 TDFN

Package Code	T1033Y+4C
Outline Number	21-100317
Land Pattern Number	90-0003
Thermal Resistance, Single-Layer Board	
Junction to Ambient (θ_{JA})	54°C/W
Junction to Case (θ_{JC})	9°C/W
Thermal Resistance, Four-Layer Board	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	9°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC} = +2.9V to +3.5V, V_{CL} = V_{CC}, 100Ω AC-coupled load between OUTN and OUTP, T_A = -40°C to +125°C, C_{IN} (MAX40660) = 0.5pF (Note 1), C_{IN} (MAX40661) = 8pF (Note 1), Input current is defined as flowing out of IN. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CC}	LP > 2.0V (logic-high) (Note 4)		41	70	mA
		LP < 0.8V (logic-low) (Note 4)		8	13	
V_{CL} Quiescent Supply Current		LP > 2.0V (logic-high) (Note 4)		0.1	20	µA
		LP < 0.8V (logic-low) (Note 4)		0.1	20	
Input Bias Voltage	V_{BIAS}	IN and OFFSET		0.85	1.0	V
Transimpedance Linearity		GAIN = GND (Note 2)	-10	±2	+10	%
		GAIN = V_{CC} (Note 2)	-10	±2	+10	

Electrical Characteristics (continued)

(V_{CC} = +2.9V to +3.5V, V_{CL} = V_{CC}, 100Ω AC-coupled load between OUTN and OUTP, T_A = -40°C to +125°C, C_{IN} (MAX40660) = 0.5pF (Note 1), C_{IN} (MAX40661) = 8pF (Note 1), Input current is defined as flowing out of IN. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Transimpedance	Z_{21}	GAIN logic-low, I_{IN} < 2µA$_{P-P}$	18	25	32	kΩ
		GAIN logic-high, I_{IN} < 1µA$_{P-P}$	36	50	64	
		In low-power standby mode: LP < V_{IL}, I_{IN} = 1µA$_{RMS}$, f_{IN} = 100MHz.		300		mΩ
OFFSET Input Transimpedance		GAIN logic-low, I_{OFFSET} < 2µA$_{P-P}$	18	25	32	kΩ
		GAIN logic-high, I_{OFFSET} < 1µA$_{P-P}$	36	50	64	
Overload Recovery Time		0 to -100mA input current		2		ns
Input Logic 0	V_{IL}	GAIN, LP (Note 4)	0		+0.8	V
Input Logic 1	V_{IH}	GAIN, LP (Note 4)	2.0		V_{CC}	
Logic Input Current Low	I_{IL}	GAIN, LP (Note 4)		±0.001	±1.0	µA
Logic Input Current High	I_{IH}	GAIN, LP (Note 4)		±0.001	±1	µA
Standby De-Assert Delay		Time from LP > V_{IL} to output common-mode voltage 90% of nominal value. Measured at OUTP and OUTN.		200		ns
Output Common-Mode Voltage			V_{CC} - 1.15	V_{CC} - 0.73	V_{CC} - 0.40	V
Differential Output Offset	ΔV_{OUT}	I_{IN} = 0mA, GAIN = GND		-200		mV
		I_{IN} = 0mA, GAIN = V_{CC}		-400		
Output Impedance	Z_{OUT}	Single-ended	40	50	60	Ω
Maximum Differential Output Voltage Swing	$V_{OUT(MAX)}$	I_{IN} = 0mA to -200µA pulse, GAIN logic-low	475	825	1290	mV
		I_{IN} = 0mA to -200µA pulse, GAIN logic-high	500	920	1490	
Input Resistance	R_{IN}			65		Ω
Bandwidth	BW	MAX40660, C_{IN} = 0.5pF	300	490	660	MHz
		MAX40660, C_{IN} = 10pF	70	165	280	
		MAX40661, C_{IN} = 10pF (Note 3)	100	160	210	
		MAX40661, C_{IN} = 5pF (Note 3)	130	200	280	
Input Noise Density		MAX40660, f = 10MHz, C_{IN} = 0.8pF		2.1		pA/√Hz
		MAX40660, f = 10MHz, C_{IN} = 10pF		2.8		
		MAX40661, f = 10MHz, C_{IN} = 5pF		2.5		
		MAX40661, f = 10MHz, C_{IN} = 8pF		2.7		
		MAX40661, f = 10MHz, C_{IN} = 10pF		3.0		pA/√Hz

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. For die-form sale, EC table parameters are not tested, excepting parameters with Note 4. Specs are guaranteed by design.

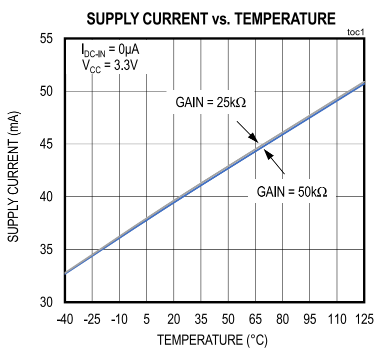
Note 2: Linearity is calculated as follows:
For 25kΩ transimpedance, Linearity = (Large signal gain at 20µA – Large signal gain at 2µA)/Large signal gain at 2µA, where large signal gain at X is (V_{OUT} at I_IN = X - V_{OUT} at I_IN = 0)/I_IN
For 50kΩ transimpedance, Linearity = (Large signal gain at 10µA – Large signal gain at 1µA)/Large signal gain at 1µA, where large signal gain at X is (V_{OUT} at I_IN = X - V_{OUT} at I_IN = 0)/I_IN

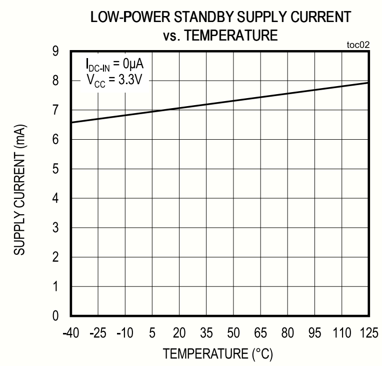
Note 3: -3dB bandwidth is measured relative to the gain at 10MHz.

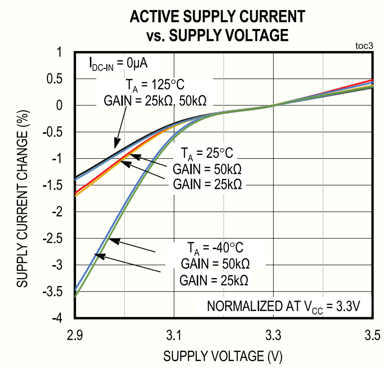
Note 4: For die only. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

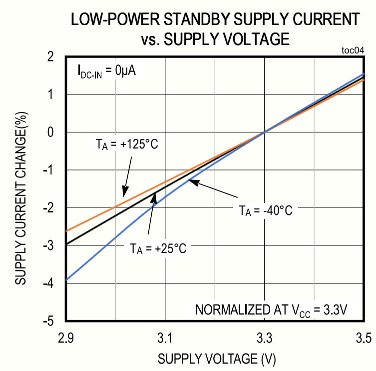
Typical Operating Characteristics

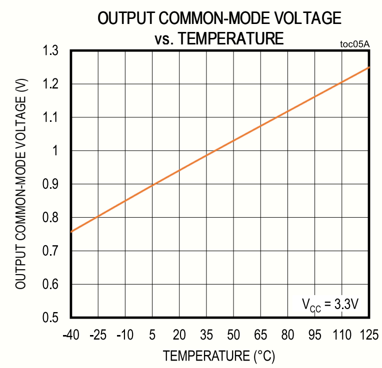
(V_{CC} = +3.3V, C_{IN} = 0.5pF (MAX40660), C_{IN} = 8pF (MAX40661), T_A= +25°C; unless otherwise noted.)

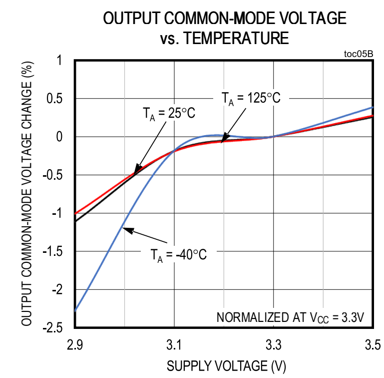


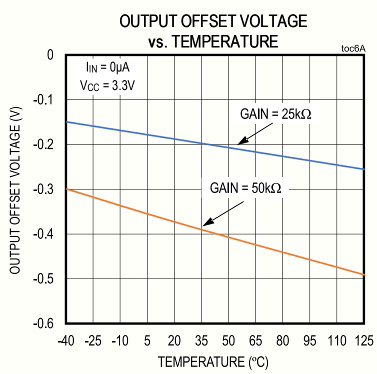


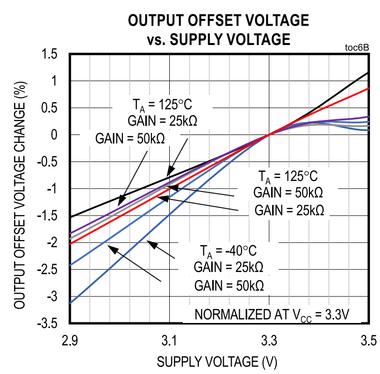


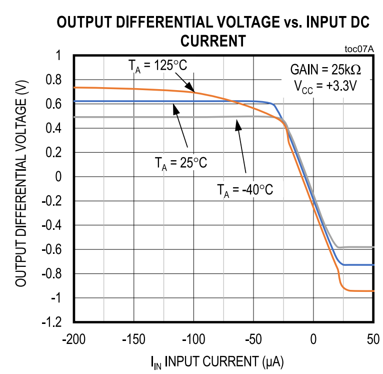












Typical Operating Characteristics (continued)

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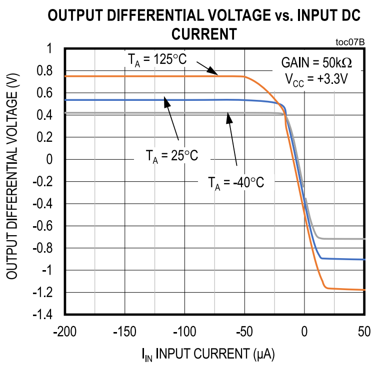

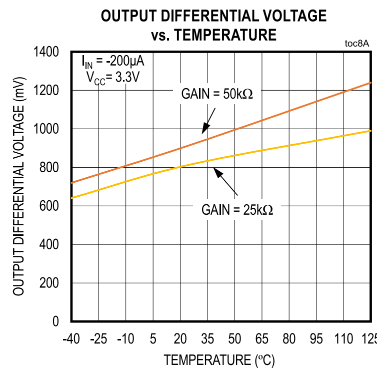

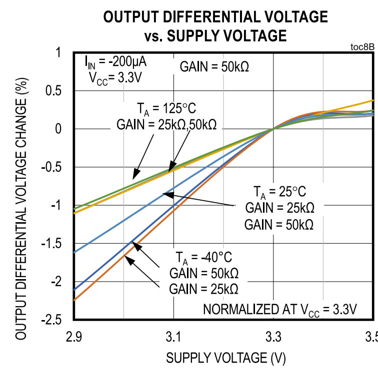

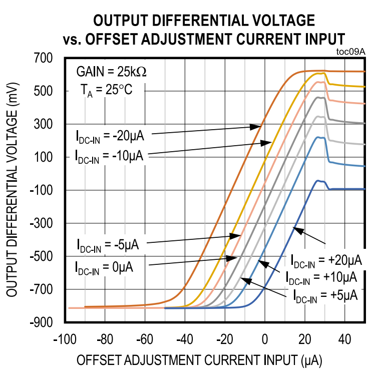

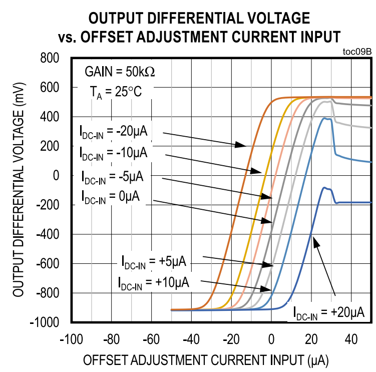

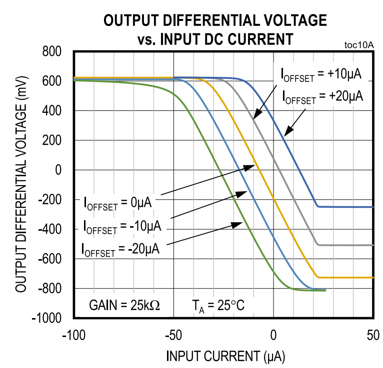

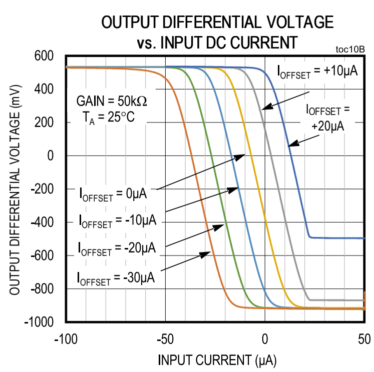

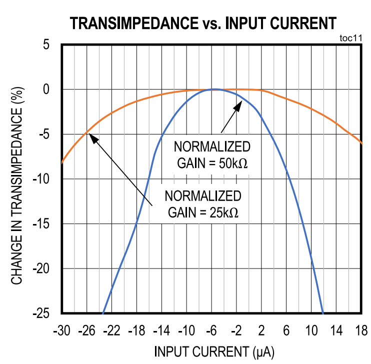

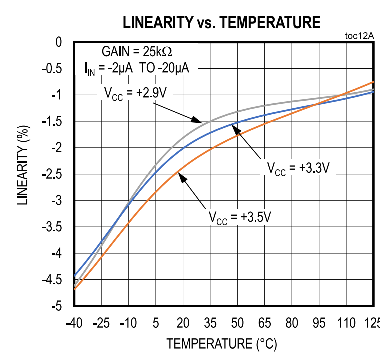

Typical Operating Characteristics (continued)

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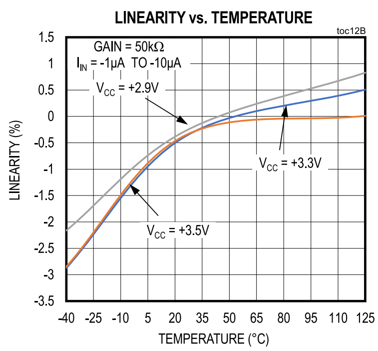

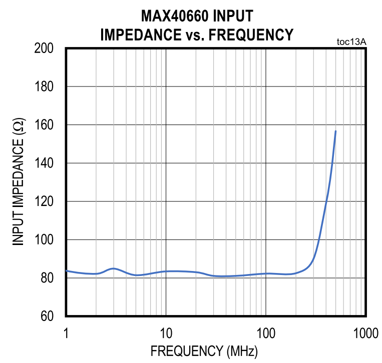

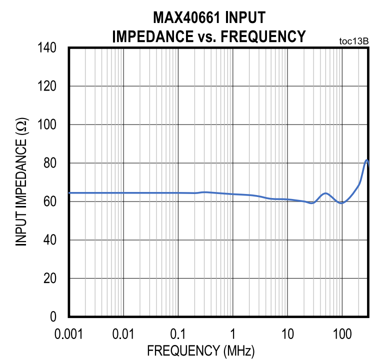

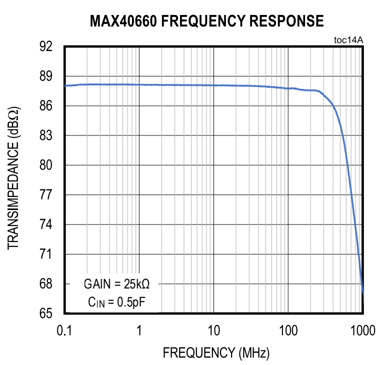

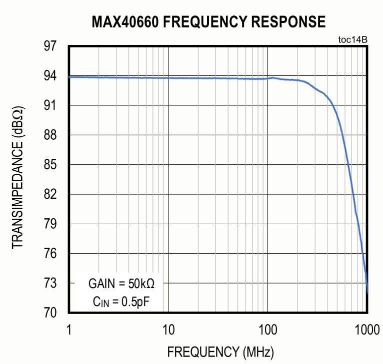

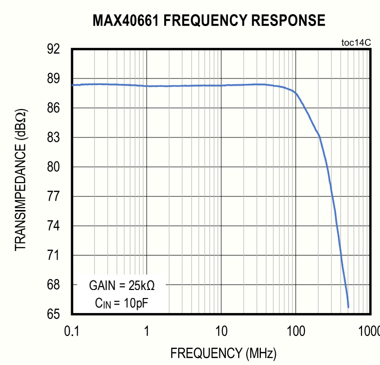

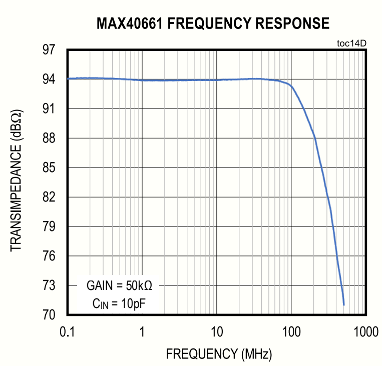

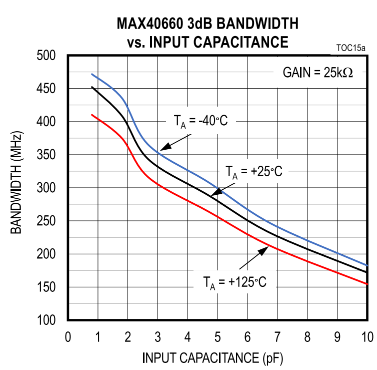

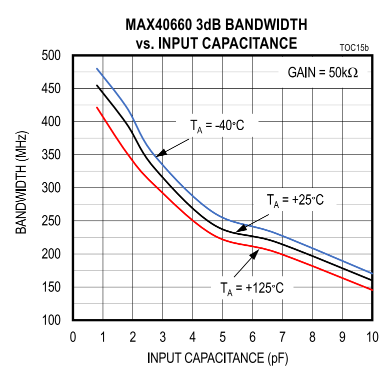

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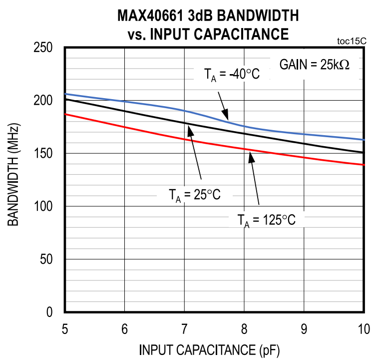

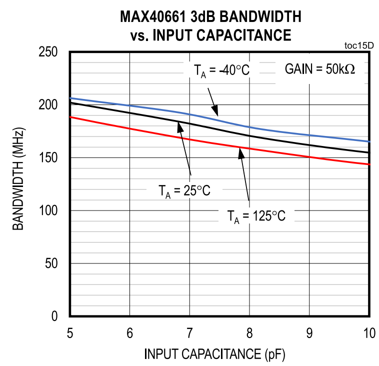

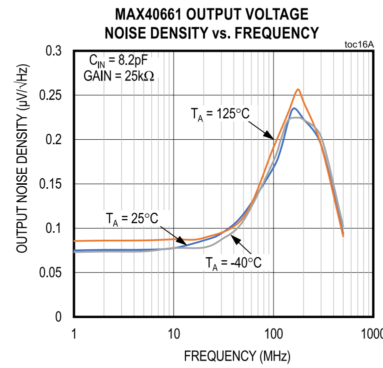

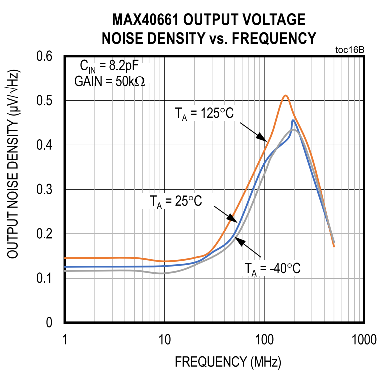

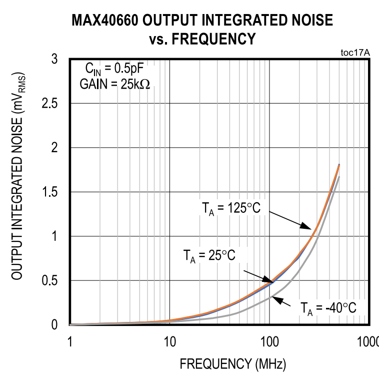

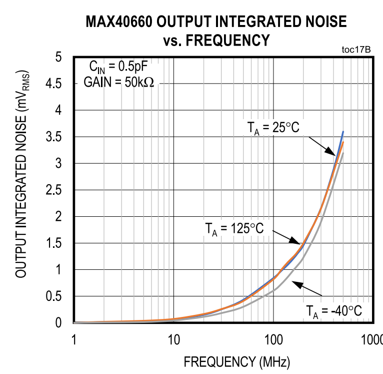

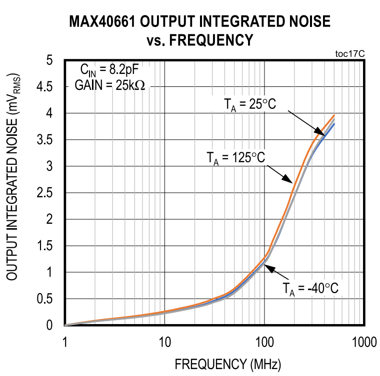

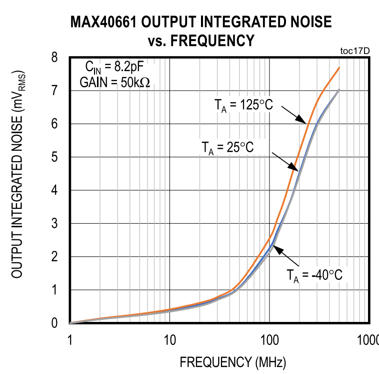

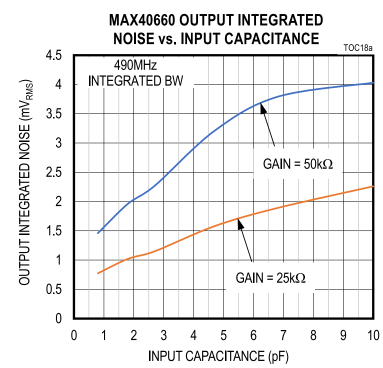

Typical Operating Characteristics (continued)

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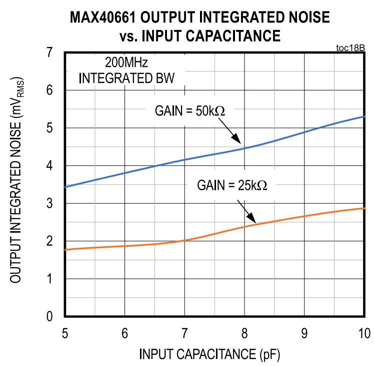
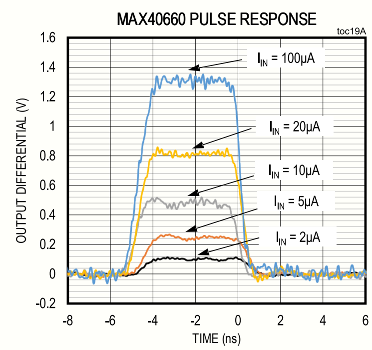
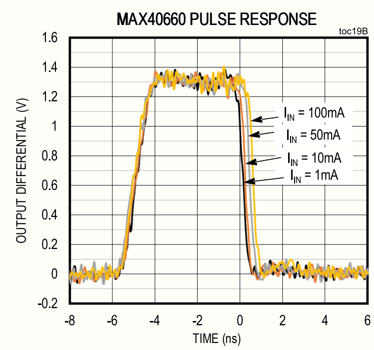
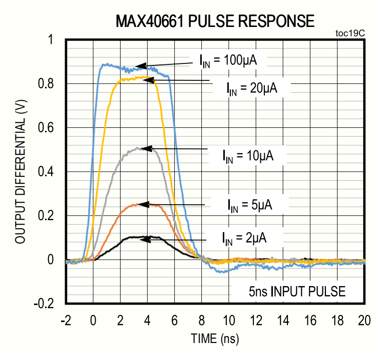
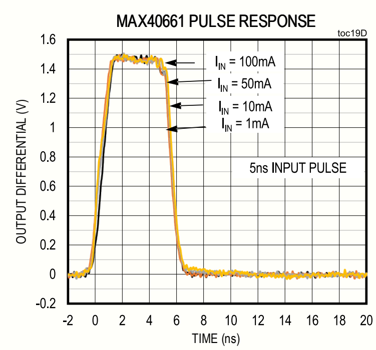
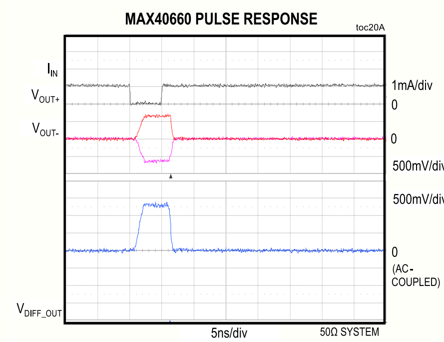


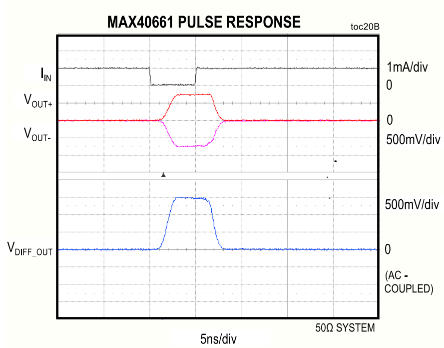


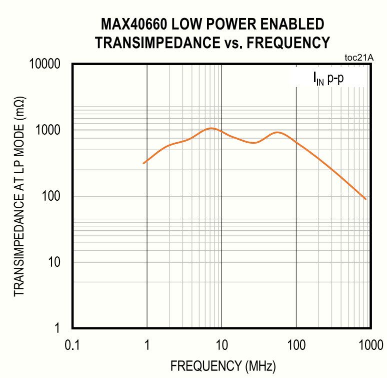


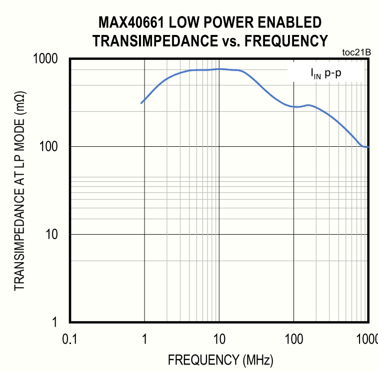




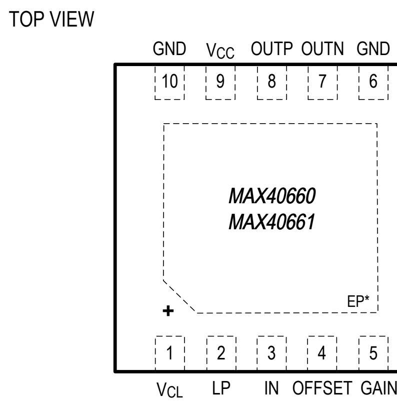








Pin Configuration



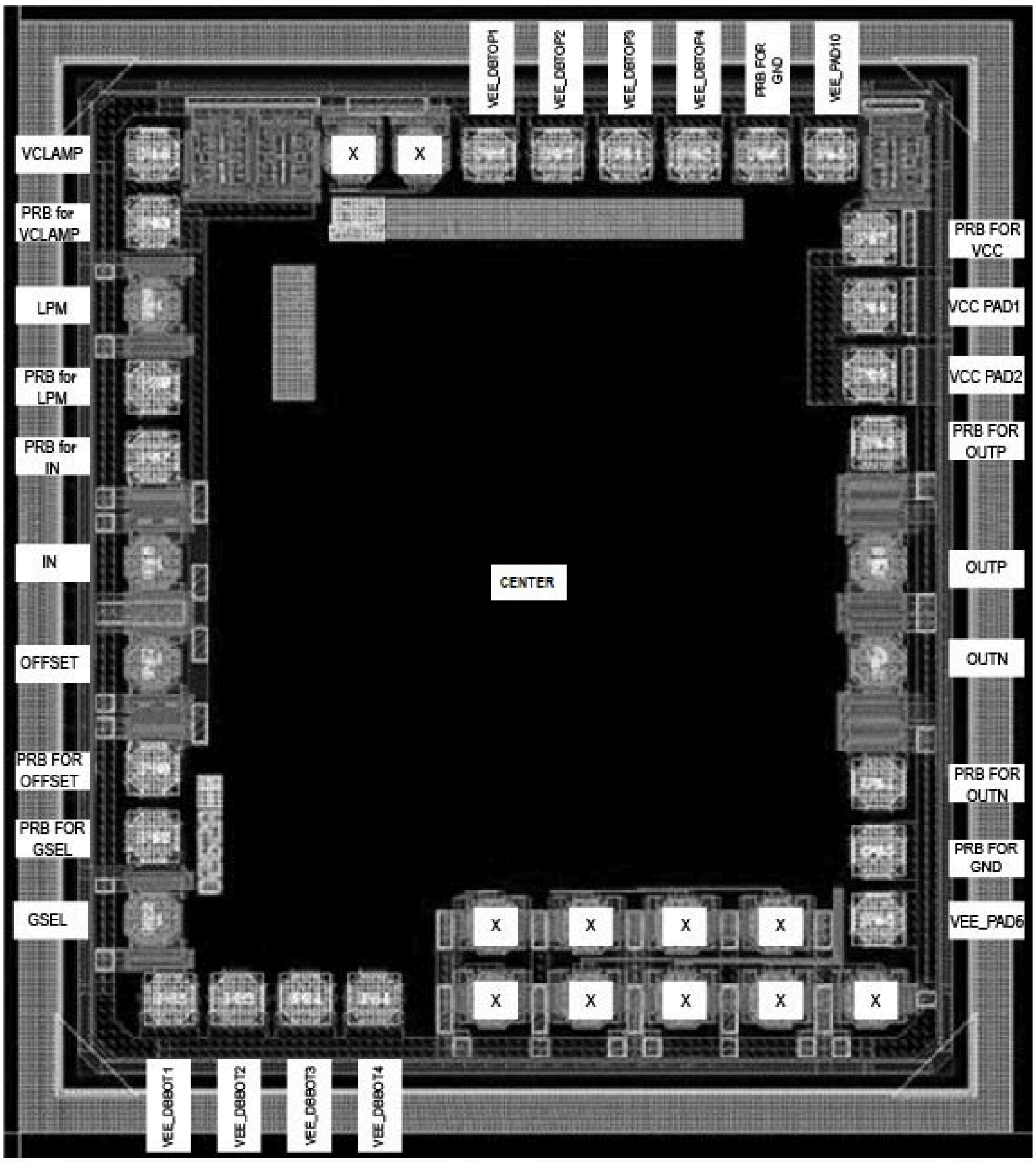
TDFN-EP
3mm x 3mm

* THE EXPOSED PAD MUST BE CONNECTED TO CIRCUIT BOARD GROUND FOR PROPER THERMAL AND ELECTRICAL PERFORMANCE.

Pin Description

PIN	NAME	FUNCTION
1	V_{CL}	Power Supply Connection for Input Current Clamp. Connect to V_{CC}.
2	LP	Enable/Low-Power Input. Logic-high = normal operation. Logic-low = low-power standby.
3	IN	Signal Input. Connect to photodiode cathode through a coupling capacitor when using positive bias voltage at cathode. Connect to photodiode cathode when using negative bias voltage at anode.
4	OFFSET	Offset Adjustment Input. Sink current from this input to adjust the effective input offset current. If offset adjustment is not needed, this pin should be left unconnected.
5	GAIN	Gain Select Input. Connect to GND for gain = 25kΩ. Connect to V_{CC} for gain = 50kΩ.
6, 10	GND	Circuit Ground
7	OUTN	Negative 50Ω Output. Increasing input current causes OUT- to decrease.
8	OUTP	Positive 50Ω Output. Increasing input current causes OUT+ to increase.
9	V_{CC}	+3.3V Supply Voltage
EP	EP	Exposed Pad (GND). This pad must be connected to ground.

Die Information



X DENOTES PADS THAT ARE FOR MAXIM'S INTERNAL USE ONLY

BOND PAD NAME	X COORDINATE (µm)	Y COORDINATE (µm)
CENTER	0	0
VCLAMP	-548	638
PRB For VCLAMP	-548	535
LPM	-548	411

Die Information (continued)

BOND PAD NAME	X COORDINATE (µm)	Y COORDINATE (µm)
PRB For LPM	-548	286
IN	-548	21
PRB for IN	-548	181
OFFSET	-548	-130
PRB For OFFSET	-548	-290
GSEL	-548	-517
PRB For GSEL	-548	-393
VEE_PAD6	548	-518
PRB For GND	548	-415
OUTN	548	-130
PRB For OUTN	548	-311
OUTP	548	20
PRB For OUTP	548	202
VCC_PAD2	535	305
VCC_PAD1	535	408
PRB For VCC	535	511
VEE_PAD10	476	638
PRB For GND	373	638
VEE_DBTOP4	270	638
VEE_DBTOP3	166	638
VEE_DBTOP2	63	638
VEE_DBTOP1	-39	638
VEE_DBBOT1	-523	-638
VEE_DBBOT2	-420	-638
VEE_DBBOT3	-317	-638
VEE_DBBOT4	-214	-638

The back side of the die must be connected to GND.

Detailed Description

The MAX40660/MAX40661 transimpedance amplifiers are designed for optical distance measurement applications and are comprised of a transimpedance amplifier input stage and a voltage amplifier/output buffer. The input stage accepts negative input current pulses; the input current will flow out of the TIA's input pin.

Gain Stage 1

When a photodiode with negative bias voltage is connected to the TIA input, the signal current flows out of the amplifier's summing node and into the photodiode. The input current flows through an internal load resistor to develop a voltage that is then applied to the input of the second stage. An internal clamp circuit protects against input currents as high as 2A for a 10ns pulse at 0.5% duty cycle. (Longer pulses or higher duty cycles will reduce this value.) The clamp circuit also maintains very fast overload recovery times (about 2ns) for input currents up to 100mA (see *Typical Operating Characteristics*).

Gain Stage 2

The second gain stage provides additional gain and converts the transimpedance amplifier's single-ended output into a differential signal.

This stage is designed to drive a 100Ω differential load between OUT+ and OUT-. For optimum supply noise rejection, the outputs should be terminated with a differential load. The outputs are not intended to drive a DC-coupled grounded load. The outputs should be AC-coupled or terminated to V_{CC}. If a single-ended output is required, both the used and unused outputs should be terminated in a similar manner.

OFFSET Input

OFFSET is a current input. The offset input current, I_{OFFSET}, is the current flowing from the OFFSET pin. This current affects the TIA's output voltage with a polarity opposite that of the current flowing from IN, so it may be used to effectively apply an offset correction to the output voltage. The OFFSET pin is biased to the same voltage as the IN pin. TOC 9A, 9B, 10A, and 10B show different load line transfer functions at the output with varying I_{IN} and I_{OFFSET} input currents (see Typical Operating Characteristics). I_{OFFSET} inputs shown in these TOCs may be used for applications where the linear region of the output is desired for a range of input current from the sensor.

Use of OFFSET is optional. If the OFFSET function is not required, simply leave this input unconnected.

LP Input

The LP (Low Power) Input accepts a logic signal that can be used to put the TIA into a low-power standby mode, thereby reducing the supply current significantly. Driving this input with a logic-high enables the TIA, while a logic-low disables the circuit and places it into a low-power mode.

The MAX40660/MAX40661 transimpedance amplifiers return to active mode from low-power mode in 200ns (typ).

Applications Information

Photodiode

Noise performance and bandwidth are adversely affected by capacitance on a TIA's input node. Although the MAX40660/MAX40661 are less sensitive than most TIAs to input capacitance, it is good practice to minimize any unnecessary capacitance. The MAX40660 is optimized for 0.25pF to 5pF of capacitance on the input. Selecting a low-capacitance photodiode for use with the MAX40660 helps to minimize the total input capacitance on the input pin. Assembling the TIA in die form using chip and wire technology provides the lowest capacitance input and the best possible performance. The MAX40661 is optimized for use with higher-capacitance photodiodes in the range of 5pF to 12pF.

Supply Filter

Sensitive optical receivers require wide-band power supply decoupling. Power supply bypassing should provide low impedance between V_{CC} and ground for frequencies between 10kHz and 700MHz. Isolate the amplifier from noise sources with LC supply filters and shielding. Place a supply filter as close to the amplifier as possible.

Layout Considerations

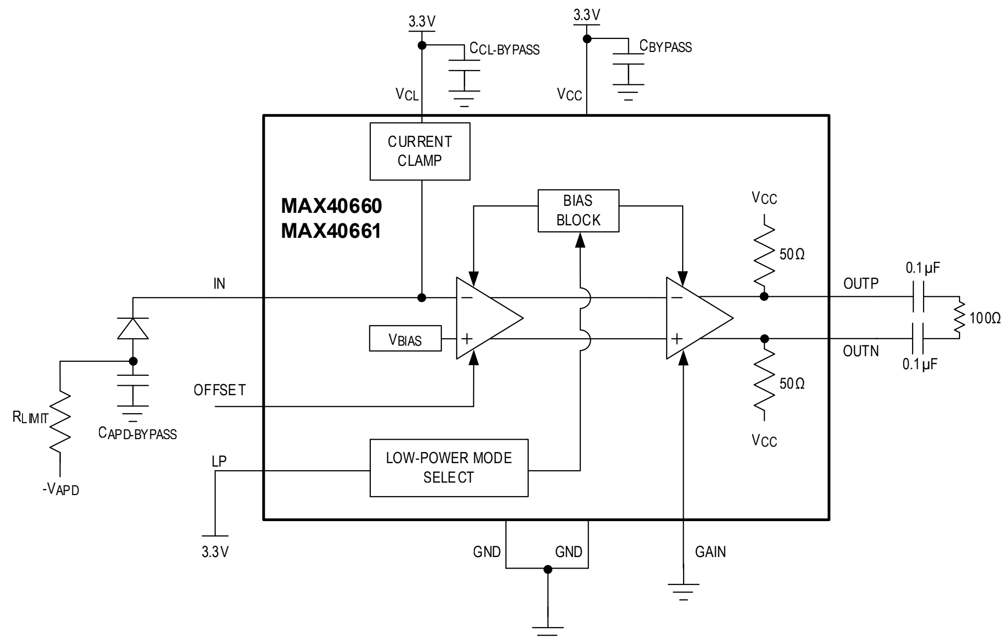
Some critical layout guidelines are listed below.

- A differential microstrip is the recommended layout for MAX40660/MAX40661 outputs with terminations done close to the outputs. Care must be taken to avoid unwanted stubs by removing ground below the traces that are not part of the 50Ω termination line leading into input pins. The parasitic capacitance created between traces and ground slow down and even distort the signals by creating reflections on the path.
- The input trace connecting the photodiode to IN of the MAX40660/MAX40661 should be as short as possible and have ground etched/removed underneath. This will reduce/avoid unwanted parasitic capacitance created in the PCB. Having longer trace lengths will increase the parasitic inductance in signal trace paths.
- Use a PC board with a low-impedance ground plane.
- Mount one or more 10nF ceramic capacitors between GND and V_{CC} as close to the pins as possible. Multiple bypass capacitors help to reduce the effect of trace impedance and capacitor ESR.
- Choose bypass capacitors for minimum inductance and ESR.
- Use a 100Ω termination resistor for the output, connected directly between OUTP and OUTN after the AC-coupling capacitors, if practical. If the destination inputs can't be located adjacent to the outputs, use a 100Ω microstrip between the output pins and the termination resistor, which should be close to the inputs of the destination component. This will avoid the creation of stub beyond the termination resistor, which will cause reflections. The added length of the differential trace has less degrading affects than added stub length.
- Minimize any parasitic layout inductance.
- It is recommended to use higher-performance substrate materials (e.g., Rogers).

Slew Rate on the Supply Ramp

Ramp rate of the supply needs to be 50μs or more to make sure the core clamp is not triggered during the power-up. If the supply ramp is faster than 50μs, then the core clamp triggers and there will be excess current consumption for about 6μs.

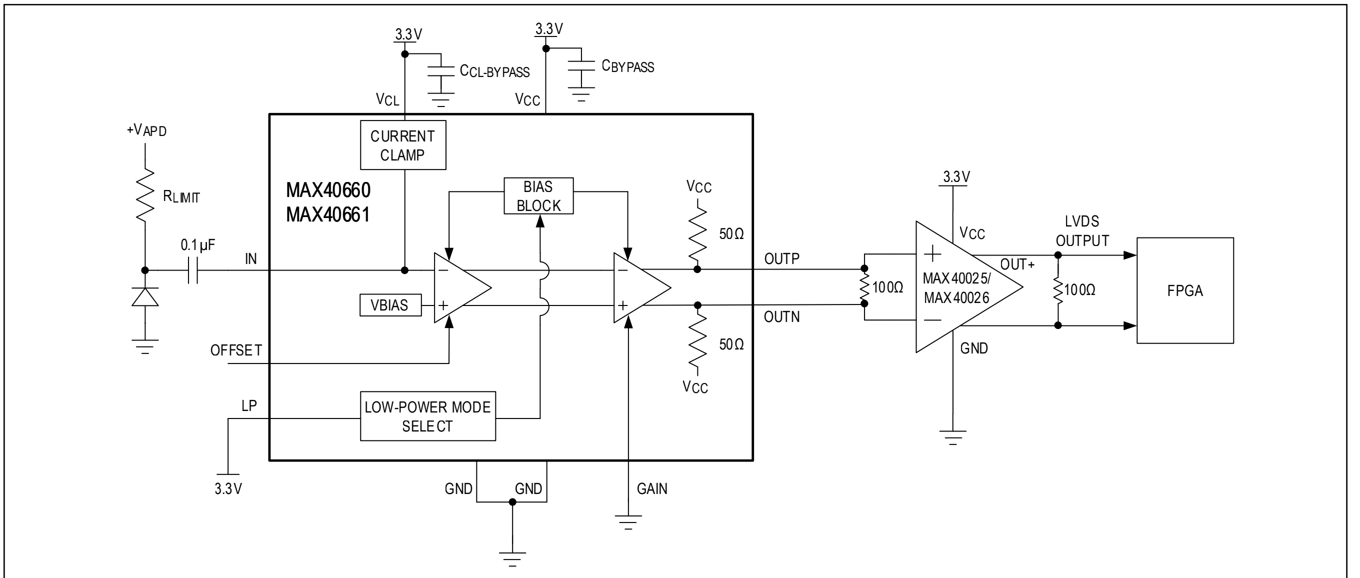
Typical Application Circuits



DC-COUPLED APD RECEIVER TIA

The APD's cathode is connected to to the TIA's input, and the anode is connected to the negative bias voltage through a resistor. Incident light pulses cause current to flow from the IN pin and into the APD. This input current also flows through an internal resistor to create a voltage, which is then amplified by the second stage to create a differential output signal that can drive a high-speed ADC or comparator.

Typical Application Circuits (continued)



AC-COUPLED APD RECEIVER TIA

The APD's cathode is connected through a coupling capacitor to to the TIA's input, with the anode connected to ground. The bias voltage in this case is positive, and is connected to the cathode through a resistor. Incident light pulses cause current to flow from the IN pin and into the APD. This input current also flows through an internal resistor to create a voltage, which is then amplified by the second stage to create a differential output signal that can drive a high-speed ADC or comparator.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARK	C_{IN} (pF)	BANDWIDTH (MHz)
MAX40660ATB+**	-40°C to +125°C	10 TDFN	—	0.25 to 5	490
MAX40660ATB/VY+	-40°C to +125°C	10 TDFN (side-wettable)	+BCYBAC	0.25 to 5	490
MAX40660A/D+*	-40°C to +125°C	Dice*	—	0.25 to 5	490
MAX40661ATB+**	-40°C to +125°C	10 TDFN	—	5 to 12	160
MAX40661ATB/VY+	-40°C to +125°C	10 TDFN (side-wettable)	+BCXNAA	5 to 12	160
MAX40661A/D+**	-40°C to +125°C	Dice*	—	5 to 12	160

**Dice are designed to operate over a -40°C to +125°C junction temperature (Tj) range, but are tested and guaranteed at T_A = +25°C.*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

/V denotes an automotive qualified part.

***Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/19	Initial release	—
1	6/19	Updated *Ordering Information*	14
2	7/19	Updated *General Description*, *Benefits and Features*, *Electrical Characteristics*, and *Ordering Information*	1, 4, 14
3	6/20	Updated *Electrical Characteristics*, *Typical Operating Characteristics*, *Die Information*, *Typical Application Circuits*, and *Ordering Information*	4, 5, 6, 8, 9, 10, 11, 13, 14, 19
4	1/21	Updated *Electrical Characteristics*, *Typical Operating Characteristics*	5, 9, 10