MAX5862 High-Density Downstream Cable QAM Modulator

General Description

The MAX5862 is an integrated, high-density, downstream cable QAM modulator, digital upconverter (DUC) and RF digital-to-analog converter (RF-DAC). The device performs QAM mapping, pulse shaping and digital RF upconversion of forward-error-correction (FEC) encoded data with full agility and drives a single RF-port using a 14-bit 4.6Gsps DAC. The device digitally synthesizes RF signals with up to 32 DOCSIS-compliant 6MHz QAM or 8MHz QAM channels. The device has fixed QAM capacity and provides high-density QAM modulation with very low power dissipation (4.2W at 32 QAMs) in a compact 12mm x 17mm footprint.

The device accepts FEC-encoded CMOS data (symbols) on a single 10-bit input port that accepts up to 32 time-interleaved digital data streams. Each channel features an individually configurable QAM mapper, RRC filter, and arbitrary rate resampler (ARR). The device performs pulse shaping, resampling, interpolation and quadrature modulation of input data, supporting all data rates defined in DOCSIS 3.0 and DVB-C. A cascade of interpolation filters, complex modulators, and channel combiners allow modulation of the signal to any frequency from 47MHz to 1006MHz. Integrated direct digital frequency synthesizers allow positioning of the QAM channels with a resolution of 125Hz. The interpolation filters and resamplers provide linear phase and excellent gain flatness. Output data from the last modulator is fed to a digital-predistortion (DPD) block that can be used to correct distortion in the device's integrated RF-DAC and output amplifiers external to the device.

Benefits and Features

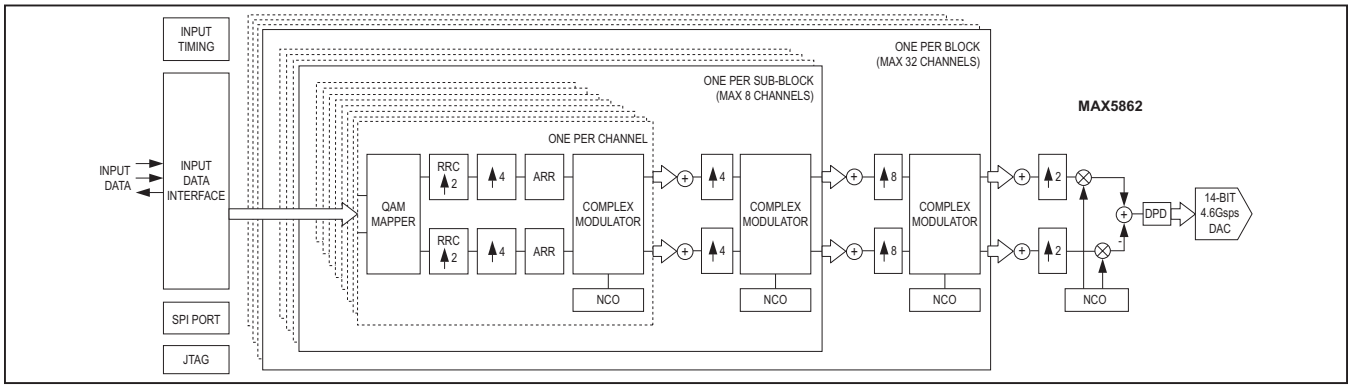
- Integrated Downstream Cable QAM Modulator
  - High-Density: 8, 16, 24, or 32 QAM Channels
  - 14-Bit 4.6Gsps RF-DAC
  - DOCSIS 3.0 DRFI Compliant
- Highly Flexible and Configurable
  - RRC Filters Support ITU-T J.83 Annex A, B, and C
  - 1MHz to 8MHz Channel Bandwidth
  - Full Carrier Agility within Each of Four 192MHz Blocks
    Block Agility within 950MHz Output Bandwidth
  - Reconfigurable Without Service Interruption
  - Input Symbol Rate: 1Msym/s to 7.14Msym/s
    Independently Set for Each Channel
  - Integrated QAM Mapper (16/32/64/128/256-QAM)
    Supports All ITU-T J.83-Defined Constellations
  - CMOS Input Port Supports Up to 1024-QAM
- Additional Features Ease RF Design
  - Programmable Digital Predistortion
  - High DAC Output Power 9dBm (CW) Eliminates Pre-amp
- Low Power, Compact Solution
  - 4.2W at 32 (6MHz) QAMs, f_S = 4.6Gsps
  - 12mm x 17mm, 280-Ball FCBGA

Applications

- Edge QAM, CMTS, CCAP, IP-QAM
- Remote PHY, Coax Media Converters
- Multi-Dweller Unit Mini-Headends

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX5862.related.

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Absolute Maximum Ratings

AVDD33 to GND, DACREF .....-0.3V to +3.6V
AVDD18, AVCLK to GND, DACREF .....-0.3V to +2.05V
V_{DD10} to GND .....-0.3V to +1.2V
AVCLK, V_{DD18}, V_{DD18L}, V_{DDDLL} to GND .....-0.3V to +2.05V
CMOS Outputs/Inputs to GND .....-0.3V to (V_{DD18} + 0.3V)
REFIO, FSADJ, to GND, DACREF ...-0.3V to (V_{AVDD33} + 0.3V)
OUTP, OUTN to GND, DACREF .....-0.3V to (V_{AVDD33} + 1.0V)
SE, DLLOFF, DELAY,
REFRES to GND, DACREF .....-0.3V to (V_{AVDD33} + 0.3V)
CLKP, CLKN to GND, DACREF .....-0.3V to (V_{AVCLK} + 0.3V)
LOCK, PERR to GND, DACREF .....-0.3V to (V_{AVDD18} + 0.3V)
CMOS (except LOCK, PERR) Output Short-Circuit Current.... 16mA
TDA, TDC Short-Circuit Current.....8mA
LOCK, PERR Continuous Current 8mA
Continuous Power Dissipation (T_A = +70°C)*
FCBGA (derate 91.2mW/°C above +70°C) 5018mW
Operating Ambient Temperature Range.....0°C to +85°C
Operating Junction Temperature Range (Note 1) 0°C to +110°C
Junction Temperature.....+150°C
Storage Temperature..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

*Use a heatsink for higher power dissipation.

Note 1: Temperature measured using the thermal diode. See the *Thermal Management* section.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

FCBGA
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....10.96°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....0.71°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL} = 1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ (between FSADJ and DACREF), V_{REFIO} = external 1.25V, V_{DLLOFF} = 0V, V_{DELAY} = 0V, f_{CLK} = 2304MHz, DPD off, R_{REFRES} = 500Ω, tested at T_A = +25°C and T_J = +110°C to an accuracy of ±15°C, unless otherwise noted. Typical values are at T_J = 65°C ±15°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS LOGIC INPUTS (Except SE)						
High-Level Input Voltage	V_{IH}		1.17			V
Low-Level Input Voltage	V_{IL}				0.63	V
Input Leakage Current	I_{IN}	All CMOS pins except JTDI, $\overline{JTRST}$ and JTMS, V_{IN} = 0V to V_{DD18}	-10	±1	+10	µA
		CMOS pins JTDI, $\overline{JTRST}$ and JTMS (Note 6); V_{IN} = 0V to V_{DD18}			100	
Input Capacitance	C_{IN}			5		pF
CMOS LOGIC OUTPUTS (Except LOCK, PERR)						
High-Level Output Voltage	V_{OH}	I_{OH} = -100µA	1.35			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 100µA			0.45	V
High-Impedance Output Current	I_{OZ}	0V < V_{OUT} < V_{DD18}	-10		+10	µA
Output Short-Circuit Current	I_{OS}			16		mA
Output Capacitance	C_{OUT}			5		pF

DC Electrical Characteristics (continued)

(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL} = 1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ (between FSADJ and DACREF), V_{REFIO} = external 1.25V, V_{DLLOFF} = 0V, V_{DELAY} = 0V, f_{CLK} = 2304MHz, DPD off, R_{REFRES} = 500Ω, tested at T_A = +25°C and T_J = +110°C to an accuracy of ±15°C, unless otherwise noted. Typical values are at T_J = 65°C ±15°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS LOGIC OUTPUTS (LOCK, PERR)						
High-Level Output Voltage	V_{OH}	I_{OH} = -200µA	V_{AVDD18} - 0.2			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 200µA			0.2	V
Output Capacitance	C_{OUT}			5		pF
CMOS LOGIC INPUTS (SE)						
High-Level Input Voltage	V_{IH}		0.7 x V_{AVDD18}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{AVDD18}	V
Input Leakage Current	I_{IN}		-10		10	µA
Input Capacitance	C_{IN}			5		pF
1.8V 4-LEVEL LOGIC INPUTS (DLLOFF, DELAY)						
Input 4-Level Logic Open	V_{OC4}		23/32 x V_{AVDD18} + 60mV		29/32 x V_{AVDD18} - 60mV	V
Input 4-Level Logic Res	V_{RC4}		7/32 x V_{AVDD18} + 60mV		23/32 x V_{AVDD18} - 60mV	V
Input 4-Level Logic High	V_{IH4}		29/32 x V_{AVDD18} + 60mV		V_{AVDD18}	V
Input 4-Level Logic Low	V_{IL4}		0		7/32 x V_{AVDD18} - 60mV	V
Input Pullup Current	I_{PU4}		8	11.3	15	µA
Input Pulldown Current	I_{PD4}		32		64	µA
POWER SUPPLY						
Analog Supply Voltage Range	V_{AVDD33}		3.1	3.3	3.5	V
Clock Supply Voltage Range	V_{AVCLK}		1.7	1.8	1.9	V
Analog 1.8V Supply Voltage Range	V_{AVDD18}		1.7	1.8	1.9	V
CMOS I/O Supply Voltage Range	V_{DD18}		1.7	1.8	1.9	V
LVDS I/O Supply Voltage Range	V_{DD18L}		1.7	1.8	1.9	V
Bias Supply Voltage Range	V_{DDDLL}		1.7	1.8	1.9	V
Core Supply Voltage Range	V_{DD10}		0.95	1.0	1.1	V

DC Electrical Characteristics (continued)

(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL} = 1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ (between FSADJ and DACREF), V_{REFIO} = external 1.25V, V_{DLLOFF} = 0V, V_{DELAY} = 0V, f_{CLK} = 2304MHz, DPD off, R_{REFRES} = 500Ω, tested at T_A = +25°C and T_J = +110°C to an accuracy of ±15°C, unless otherwise noted. Typical values are at T_J = 65°C ±15°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Current	I_{AVDD33}	Current is measured using internal PRBS generators as the source; configured for 32 channels, 256-QAM Annex B		330	360	mA
Clock Supply Current	I_{AVCLK}	Current is measured using internal PRBS generators as the source; configured for 32 channels, 256-QAM Annex B		450	500	mA
Analog 1.8V Supply Current	I_{AVDD18}	Current is measured using internal PRBS generators as the source; configured for 32 channels, 256-QAM Annex B		245	290	mA
1.8V Supply Current, V_{DD18}	I_{VDD18}			25		mA
1.8V Supply Current, V_{DD18L}	I_{VDD18L}	Current is measured using internal PRBS generators as the source; configured for 32 channels, 256-QAM Annex B		321	350	mA
Bias Supply Current, V_{DDDLL}	I_{VDDDLL}	Current is measured using internal PRBS generators as the source; configured for 32 channels, 256-QAM Annex B		32	37	mA
1.0V Supply Current (Active)	I_{VDD10}	Current is measured using internal PRBS generators as the source; configured for 32 channels, 256-QAM Annex B		1190	2900	mA
1.0V Supply Current (Standby)	$I_{VDD10SB}$	$\overline{RST}$= 0, SCLK = 0, PCLK = 0			2350	mA
1.0V Supply Current (Static)	$I_{VDD10ST}$	$\overline{RST}$ = 0, CLKN/P = 0, SCLK = 0, PCLK = 0			2350	mA
Power Dissipation	P_{DISS}	Power is measured using internal PRBS generators as the source; configured for 32 channels. 256-QAM (Note 7)		4.2	6.25	W
REFERENCE						
Internal Reference Voltage Range	V_{REFIO}		1.1	1.2	1.3	V
Reference Input Voltage Compliance Range	V_{REFIOR}		0.5		1.8	V
Reference Input Resistance	R_{REFIO}			10		kΩ
Reference Voltage Drift	TCO_{REF}			50		ppm/°C

AC Electrical Characteristics

(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL} = 1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ (between FSADJ and DACREF), V_{REFIO} = external 1.25V, V_{DLLOFF} = 0V, V_{DELAY} = 0V, f_{CLK} = 2304MHz, DPD off, R_{REFRES} = 500Ω, tested at T_A = +25°C and T_J = +110°C to an accuracy of ±15°C, unless otherwise noted. Typical values are at T_J = 65°C ±15°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC CLOCK INPUTS (CLKP, CLKN)						
Minimum Clock Input Power	$P_{CLK,MIN}$	(Note 8)		6		dBm
Maximum Clock Input Power	$P_{CLK,MAX}$	Power measured into DAC clock input with 100Ω external differential termination resistor		12		dBm
Common-Mode Voltage	V_{COMCLK}	Input is self biased		V_{AVCLK}/3		V
Input Resistance	R_{CLK}	Differential		100		Ω
Input Capacitance	C_{CLK}			2		pF
CMOS PORT CLOCK INPUT (PCLK)						
Clock Frequency	f_{PCLK}	$1/t_{TP}$ (Note 9)			128	MHz
Input Capacitance				3		pF
Minimum Clock Duty Cycle				45		%
Maximum Clock Duty Cycle				55		%
CMOS DATA INPUTS (Note 10)						
Data to Port Clock Setup Time			1			ns
Data to Port Clock Hold Time			1			ns
Input Capacitance				3		pF
CMOS DATA OUTPUTS (Note 10)						
Output Rise Time		10% to 90% of V_{DD18}, 10pF load		2		ns
Output Fall Time		10% to 90% of V_{DD18}, 10pF load		2		ns
RDYCLK to RDYA Data Valid Time			0		1.5	ns
Output Capacitance				3		pF
SERIAL PORT INTERFACE TIMING (SCLK,SDI,SDO,$\overline{SS}$)						
SCLK Write Frequency	f_{SCLW}				66	MHz
SCLK Read Frequency	f_{SCLR}				66	MHz
$\overline{SS}$ Setup time	t_{SS}	(Note 10)	1.5			ns
Input Hold Time	t_{SDH}	(Note 10)	1.1			ns
Input Setup Time	t_{SDS}	(Note 10)	2.2			ns
Data Valid Duration	t_{SDV}	(Note 10)			7.8	ns
JTAG INTERFACE TIMING (JTDI, JTDO, JTCLK, JTMS, $\overline{JTRST}$) (Notes 6 and 11)						
JTCLK Clock Frequency		Bypass mode			50	MHz
		Boundary scan mode			25	

AC Electrical Characteristics (continued)

(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL} = 1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ (between FSADJ and DACREF), V_{REFIO} = external 1.25V, V_{DLLOFF} = 0V, V_{DELAY} = 0V, f_{CLK} = 2304MHz, DPD off, R_{REFRES} = 500Ω, tested at T_A = +25°C and T_J = +110°C to an accuracy of ±15°C, unless otherwise noted. Typical values are at T_J = 65°C ±15°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
JTCLK Clock High/Low Time		(Notes 10 and 12)		5			ns
JTCLK to JTDI Setup Time		(Note 10)		0			ns
JTCLK to JTDI Hold Time		(Note 10)		2.5			ns
JTCLK to JTDO Delay		(Note 10)		4.1			ns
JTCK to JTDO High-Z Delay		(Note 10)		10			ns
$\overline{JTRST}$ Width Low Time					100		ns
DAC STATIC PERFORMANCE							
Resolution					14		Bits
Full-Scale Output Current Range	I_{OUT}	(Note 13)		10		80	mA
Output-Power Gain Error	GE	Differential, into 50Ω load, f_{OUT} = 103.5MHz		-0.7		0.7	dB
Output Power Drift		Internal reference			-0.003		dB/°C
		External reference			-0.0025		
Full-Scale Output Power	P_{OUT}	Differential, into 50Ω load, f_{OUT} = 103.5MHz			8.6		dBm
Output Resistance	R_{OUT}	Differential			50		Ω
DAC DYNAMIC PERFORMANCE (Note 17)							
Clock Rate	f_{CLK}					2304	MHz
Output Update Rate	f_{DAC}					4608	Msps
Out-of-Band Noise and Spurious, Eight 6MHz QAM Carriers, Average Total Power = -18.7dBFS		f_{OUT} = 400MHz f_{DAC} = 4608Msps	Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)		-71	-64	dBc
			Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)		-73	-66	
			Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)		-73	-66	
			Noise in any other channel (Note 16)		-73		

AC Electrical Characteristics (continued)

(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL} = 1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ (between FSADJ and DACREF), V_{REFIO} = external 1.25V, V_{DLLOFF} = 0V, V_{DELAY} = 0V, f_{CLK} = 2304MHz, DPD off, R_{REFRES} = 500Ω, tested at T_A = +25°C and T_J = +110°C to an accuracy of ±15°C, unless otherwise noted. Typical values are at T_J = 65°C ±15°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Out-of-Band Noise and Spurious, Eight 6MHz QAM Carriers, Average Total Power = -18.7dBFS		f_{OUT} = 860MHz f_{DAC} = 4608Msps	Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)		-67		dBc
			Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)		-66		
			Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)		-66		
			Noise in any other channel (Note 16)		-65		
		f_{OUT} = 1000MHz f_{DAC} = 4608Msps	Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)		-67		dBc
			Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)		-67		
			Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)		-67		
			Noise in any other channel (Note 16)		-66		

AC Electrical Characteristics (continued)

(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL} = 1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ (between FSADJ and DACREF), V_{REFIO} = external 1.25V, V_{DLLOFF} = 0V, V_{DELAY} = 0V, f_{CLK} = 2304MHz, DPD off, R_{REFRES} = 500Ω, tested at T_A = +25°C and T_J = +110°C to an accuracy of ±15°C, unless otherwise noted. Typical values are at T_J = 65°C ±15°C.) (Note 5)

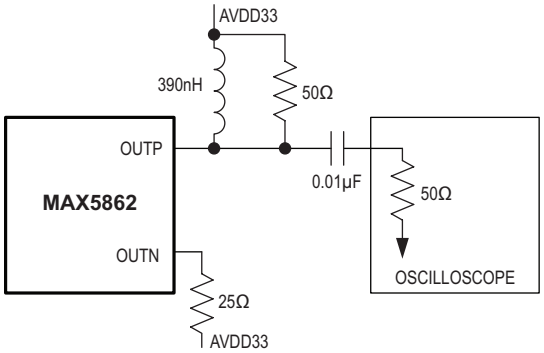
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Harmonic Distortion, Block of Four 6MHz QAM Carriers, Average Total Power = -15.7dBFS		f_{OUT} = 300MHz f_{DAC} = 4608Msps	In each of eight 6MHz channels coinciding with 2nd harmonic components		-72	-64	dBc
			In each of twelve 6MHz channels coinciding with 3rd harmonic components		-72	-65	
Gain Flatness	GF	Over any single 6MHz channel			0.05		dB
		Within 45MHz to 1003MHz band			1.6		
Clock Spurs		f_{DAC}/4 spur, f_{DAC} = 4608Msps, 8 QAM carriers			-80		dBm
		f_{DAC}/8 spur, f_{DAC} = 4608Msps, 8 QAM carriers			-100		
f_{DAC}/2 - f_{OUT} Image		f_{DAC} = 4608Msps, 8 QAM carriers covering the band from 952MHz to 1000MHz			-40		dBc
f_{DAC}/2 - 2f_{OUT} Spurious		f_{DAC} = 4608Msps, 8 QAM carriers covering the band from 952MHz to 1000MHz			-64		dBc
TIMING CHARACTERISTICS							
DAC DLL Frequency Range	f_{DLL}	f_{DLL} = f_{CLK}/2 DLLOFF = Low	DELAY = High	1075		1152	MHz
			DELAY = Open	950		1075	
Parity Error Pulse Width	t_{ERR}	Pulse width of PERR when a parity error is detected			48		Data Clock Cycles
ANALOG OUTPUT							
Output Bandwidth	BW	(Note 15)			2.0		GHz

Note 5: All specifications are 100% tested at T_A = +25°C and T_J = +110°C with an accuracy of ±15°C. Specifications at T_A < +25°C are guaranteed by design and characterization.
Note 6: JTAG control signals JTDI, $\overline{JTRST}$, and JTMS each have a ~50kΩ pullup resistor.
Note 7: Power does not include the V_{DD18} supply.
Note 8: Transformer-coupled clock input.
Note 9: PCLK is a continuous clock and must not be gapped.
Note 10: Guaranteed by design and characterization.
Note 11: All CMOS signals are bidirectional in JTAG mode except for LOCK, SE, PERR, MODE, MODE2, $\overline{TEST}$, and JTAG control pins (JTCLK, JTMS, $\overline{JTRST}$, JTDI, JTDO).
Note 12: Clock can be stopped high or low.
Note 13: Nominal full-scale current I_{OUT} = 128 x I_{REF}.

AC Electrical Characteristics (continued)

(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL} = 1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ (between FSADJ and DACREF), V_{REFIO} = external 1.25V, V_{DLLOFF} = 0V, V_{DELAY} = 0V, f_{CLK} = 2304MHz, DPD off, R_{REFRES} = 500Ω, tested at T_A = +25°C and T_J = +110°C to an accuracy of ±15°C, unless otherwise noted. Typical values are at T_J = 65°C ±15°C.) (Note 5)

Note 14: Measured single-ended into a double terminated 50Ω load.

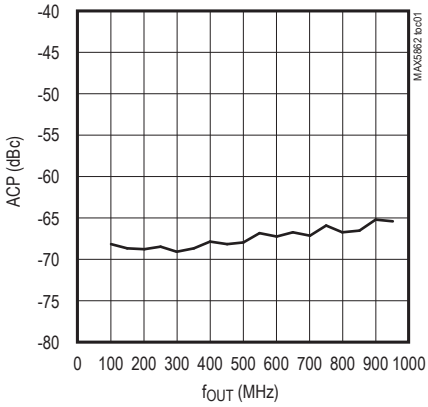


Note 15: Excludes impulse-response dependent rolloff inherent in the DAC.
Note 16: Excludes clock, clock images, $f_{DAC}/2 - f_{OUT}$, and $f_{DAC}/2 - 2f_{OUT}$ spurs, which are specified separately.
Note 17: CLK input = +9dBm, AC-coupled sine wave.

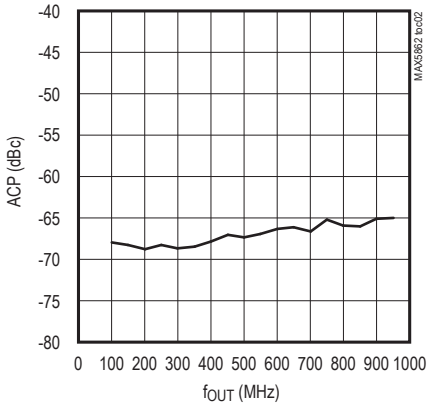
Typical Operating Characteristics

(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL}=1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = V_{CLKDIV} = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, DPD off, tests at T_J = +60°C, unless otherwise noted.)

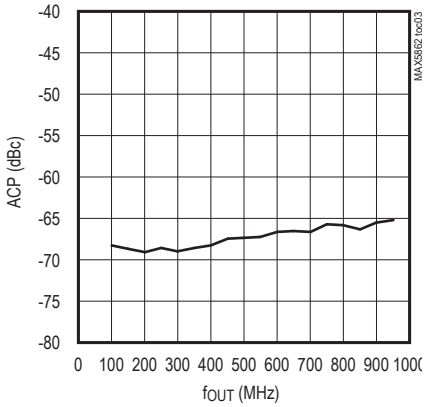
8-CHANNEL 256-QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.608Gsps, 750kHz TO 6MHz FROM CHANNEL BLOCK EDGE)



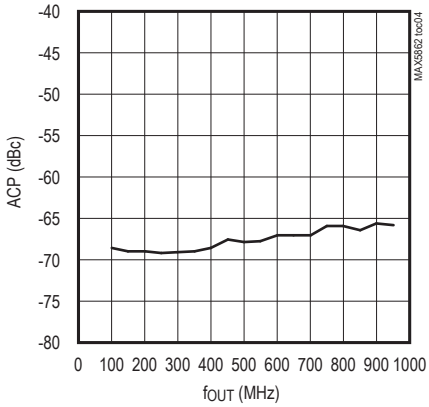
8-CHANNEL 256-QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.608Gsps, 6MHz TO 12MHz FROM CHANNEL BLOCK EDGE)



8-CHANNEL 256-QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.608Gsps, 12MHz TO 18MHz FROM CHANNEL BLOCK EDGE)



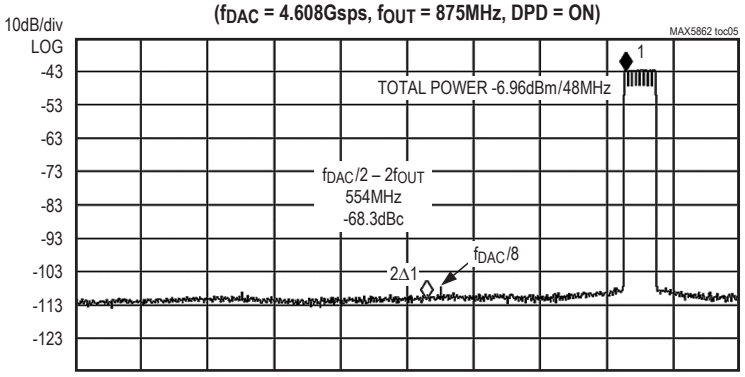
8-CHANNEL 256-QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.608Gsps, 18MHz TO 24MHz FROM CHANNEL BLOCK EDGE)



Typical Operating Characteristics (continued)

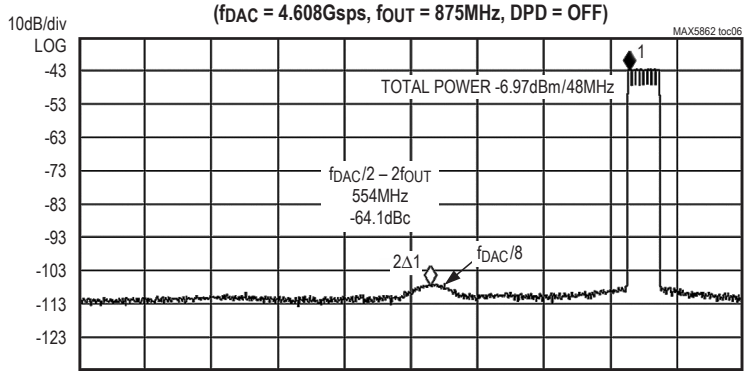
(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL}=1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = V_{CLKDIV} = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, DPD off, tests at T_J = +60°C, unless otherwise noted.)

8-CHANNEL 256-QAM (DOCSIS)
(f_{DAC} = 4.608Gsps, f_{OUT} = 875MHz, DPD = ON)



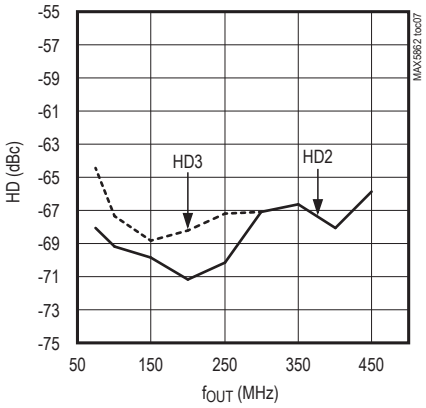
CENTER = 525MHz, SPAN = 1GHz, RBW = 10kHz,
VBW = 1kHz, SWEEP = 101s

8-CHANNEL 256-QAM (DOCSIS)
(f_{DAC} = 4.608Gsps, f_{OUT} = 875MHz, DPD = OFF)



CENTER = 525MHz, SPAN = 1GHz, RBW = 10kHz,
VBW = 1Hz, SWEEP = 101s

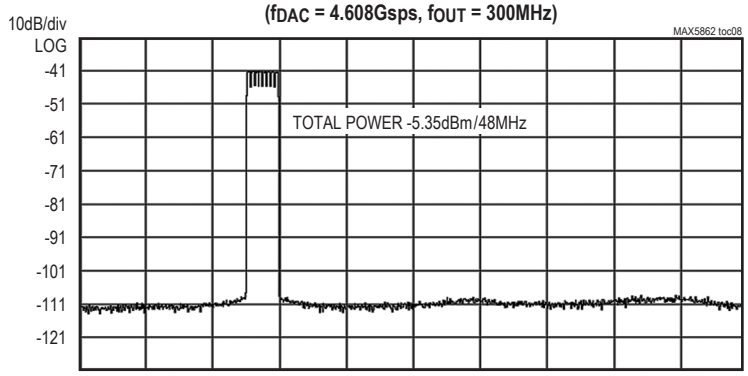
8-CHANNEL 256-QAM HARMONIC DISTORTION vs. OUTPUT FREQUENCY
(f_{DAC} = 4.608Gsps)



Typical Operating Characteristics (continued)

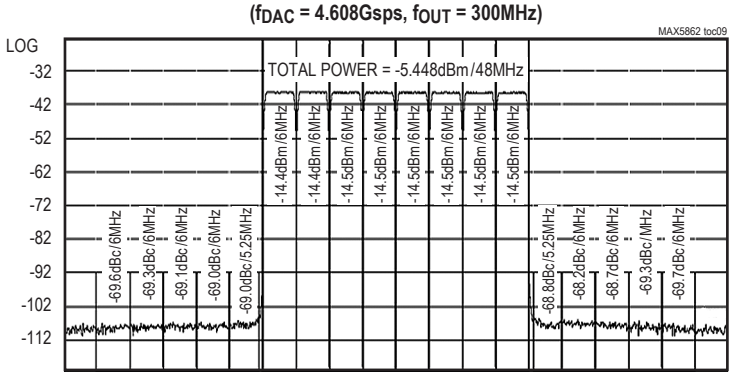
(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL}=1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = V_{CLKDIV} = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, DPD off, tests at T_J = +60°C, unless otherwise noted.)

8-CHANNEL 256-QAM (DOCSIS)
(f_{DAC} = 4.608Gsps, f_{OUT} = 300MHz)



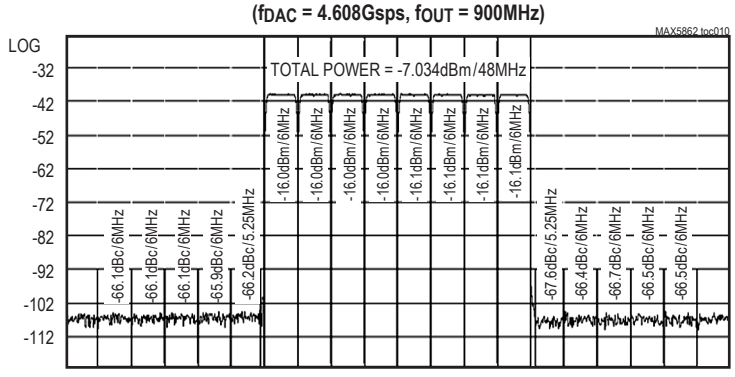
CENTER = 525MHz, SPAN = 1GHz, RBW = 10kHz,
VBW = 1kHz, SWEEP = 101s

8-CHANNEL 256-QAM (DOCSIS) ACP
(f_{DAC} = 4.608Gsps, f_{OUT} = 300MHz)



CENTER = 300MHz, SPAN = 120MHz, RBW = 20kHz,
VBW = 2kHz, SWEEP = 7.449s

8-CHANNEL 256-QAM (DOCSIS) ACP
(f_{DAC} = 4.608Gsps, f_{OUT} = 900MHz)

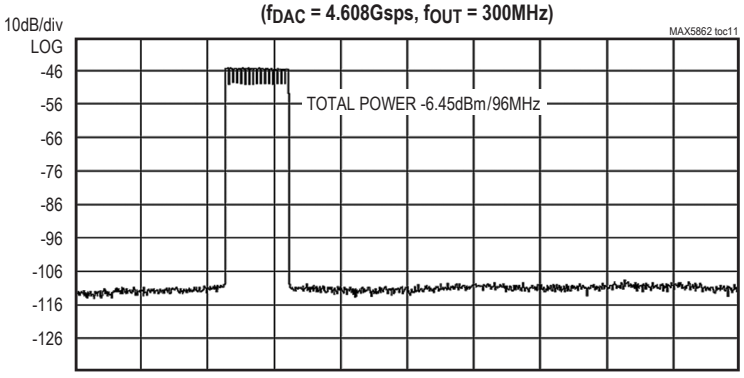


CENTER = 900MHz, SPAN = 120MHz, RBW = 20kHz,
VBW = 2kHz, SWEEP = 7.449s

Typical Operating Characteristics (continued)

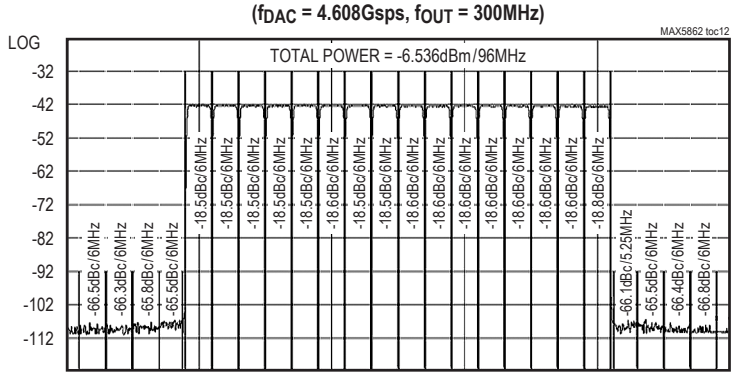
(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL}=1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = V_{CLKDIV} = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, DPD off, tests at T_J = +60°C, unless otherwise noted.)

16-CHANNEL 256-QAM (DOCSIS)
(f_{DAC} = 4.608Gsps, f_{OUT} = 300MHz)



CENTER = 525MHz, SPAN = 1GHz, RBW = 10kHz,
VBW = 1kHz, SWEEP = 101s

16-CHANNEL 256-QAM (DOCSIS) ACP
(f_{DAC} = 4.608Gsps, f_{OUT} = 300MHz)

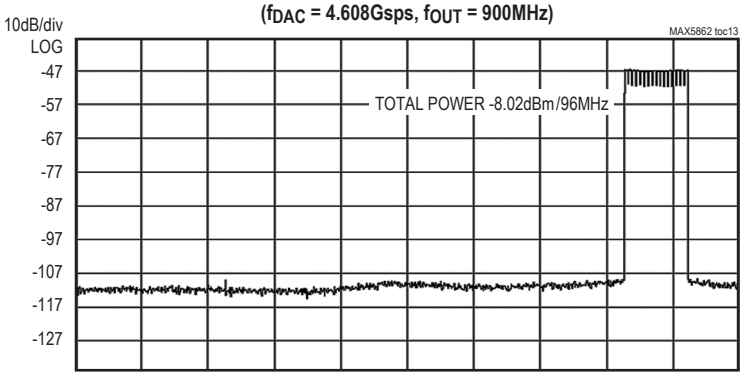


CENTER = 300MHz, SPAN = 150MHz, RBW = 20kHz,
VBW = 2kHz, SWEEP = 9.311s

Typical Operating Characteristics (continued)

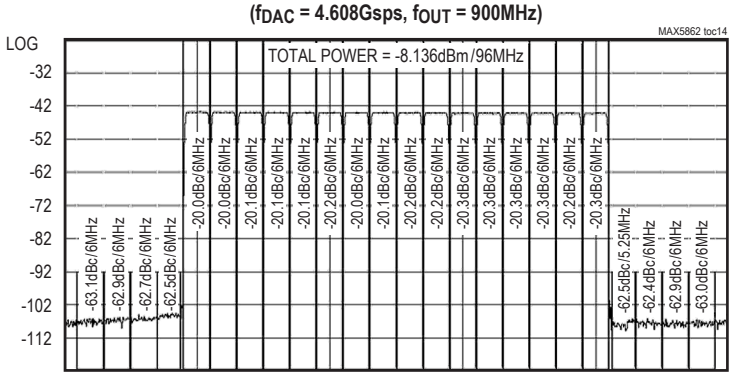
(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL}=1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = V_{CLKDIV} = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, DPD off, tests at T_J = +60°C, unless otherwise noted.)

16-CHANNEL 256-QAM (DOCSIS)
(f_{DAC} = 4.608Gsps, f_{OUT} = 900MHz)



CENTER = 525MHz, SPAN = 1GHz, RBW = 10kHz,
VBW = 1kHz, SWEEP = 101s

16-CHANNEL 256-QAM (DOCSIS) ACP
(f_{DAC} = 4.608Gsps, f_{OUT} = 900MHz)

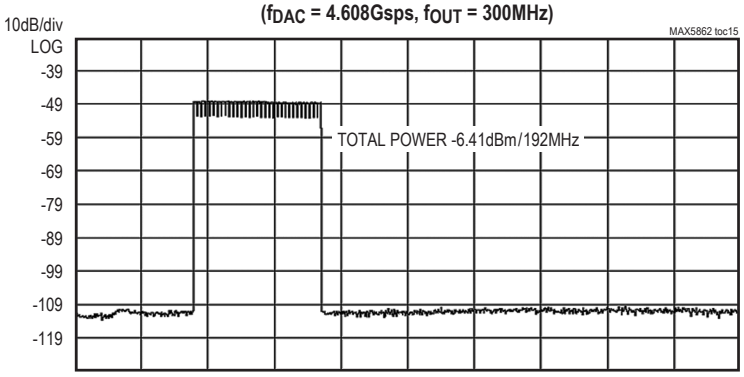


CENTER = 900MHz, SPAN = 160MHz, RBW = 20kHz,
VBW = 2kHz, SWEEP = 9.931s

Typical Operating Characteristics (continued)

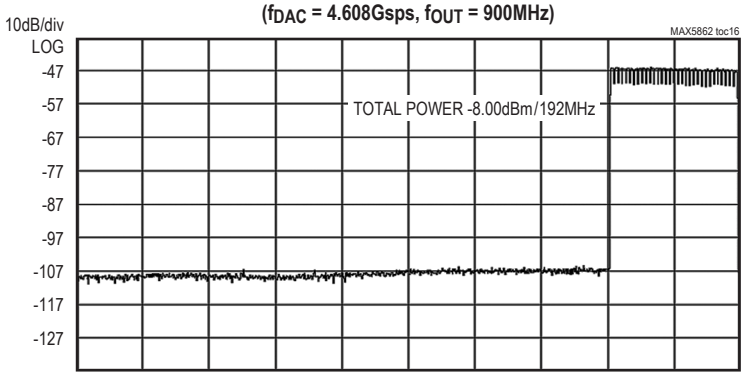
(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL}=1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = V_{CLKDIV} = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, DPD off, tests at T_J = +60°C, unless otherwise noted.)

32-CHANNEL 256-QAM (DOCSIS)
(f_{DAC} = 4.608Gsps, f_{OUT} = 300MHz)



CENTER = 525MHz, SPAN = 1GHz, RBW = 10kHz,
VBW = 1kHz, SWEEP = 101s

32-CHANNEL 256-QAM (DOCSIS)
(f_{DAC} = 4.608Gsps, f_{OUT} = 900MHz)

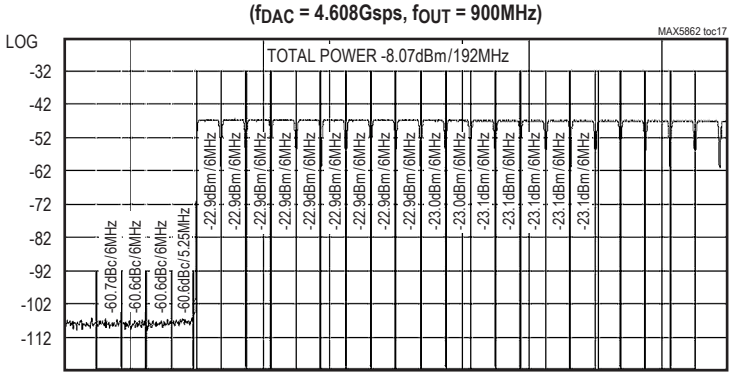


CENTER = 500MHz, SPAN = 1GHz, RBW = 20kHz,
VBW = 2kHz, SWEEP = 25.3s

Typical Operating Characteristics (continued)

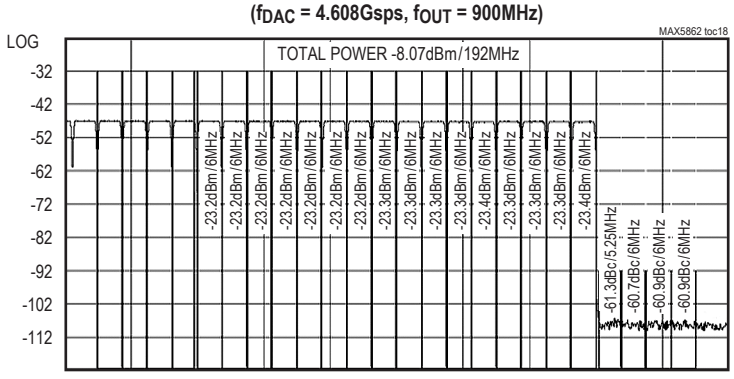
(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL}=1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = V_{CLKDIV} = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, DPD off, tests at T_J = +60°C, unless otherwise noted.)

32-CHANNEL 256-QAM (DOCSIS) ACP-UPPER CHANNELS
(f_{DAC} = 4.608Gsps, f_{OUT} = 900MHz)



CENTER = 948MHz, SPAN = 160MHz, RBW = 20kHz,
VBW = 2kHz, SWEEP = 9.931s

32-CHANNEL 256-QAM (DOCSIS) ACP-UPPER CHANNELS
(f_{DAC} = 4.608Gsps, f_{OUT} = 900MHz)

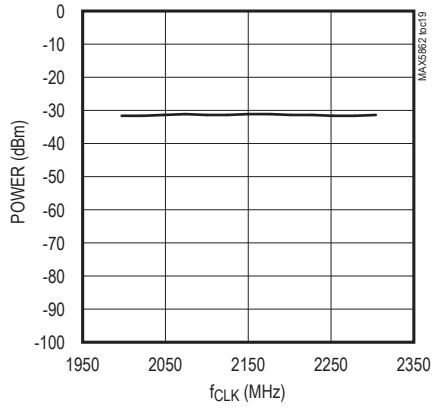


CENTER = 948MHz, SPAN = 160MHz, RBW = 20kHz,
VBW = 2kHz, SWEEP = 9.931s

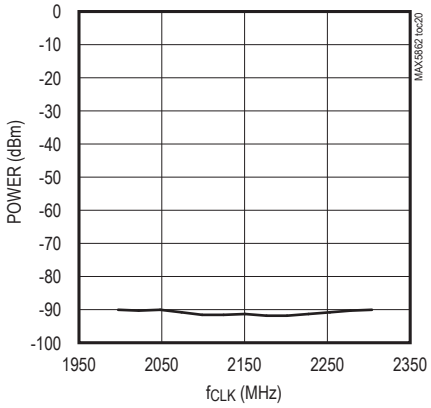
Typical Operating Characteristics (continued)

(V_{AVDD33} = 3.3V, V_{AVDD18} = V_{AVCLK} = V_{DD18} = V_{DD18L} = V_{DDDLL}=1.8V, V_{DD10} = 1.0V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = V_{CLKDIV} = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, DPD off, tests at T_J = +60°C, unless otherwise noted.)

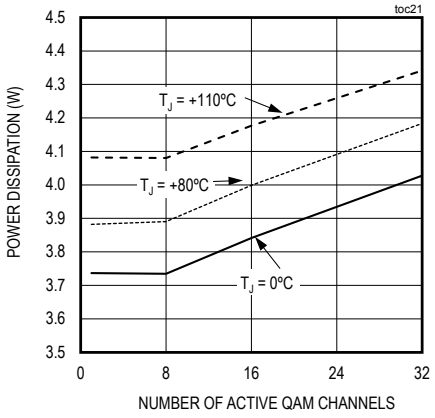
CLOCK FEEDTHROUGH vs. CLOCK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = -0.1dBFS)



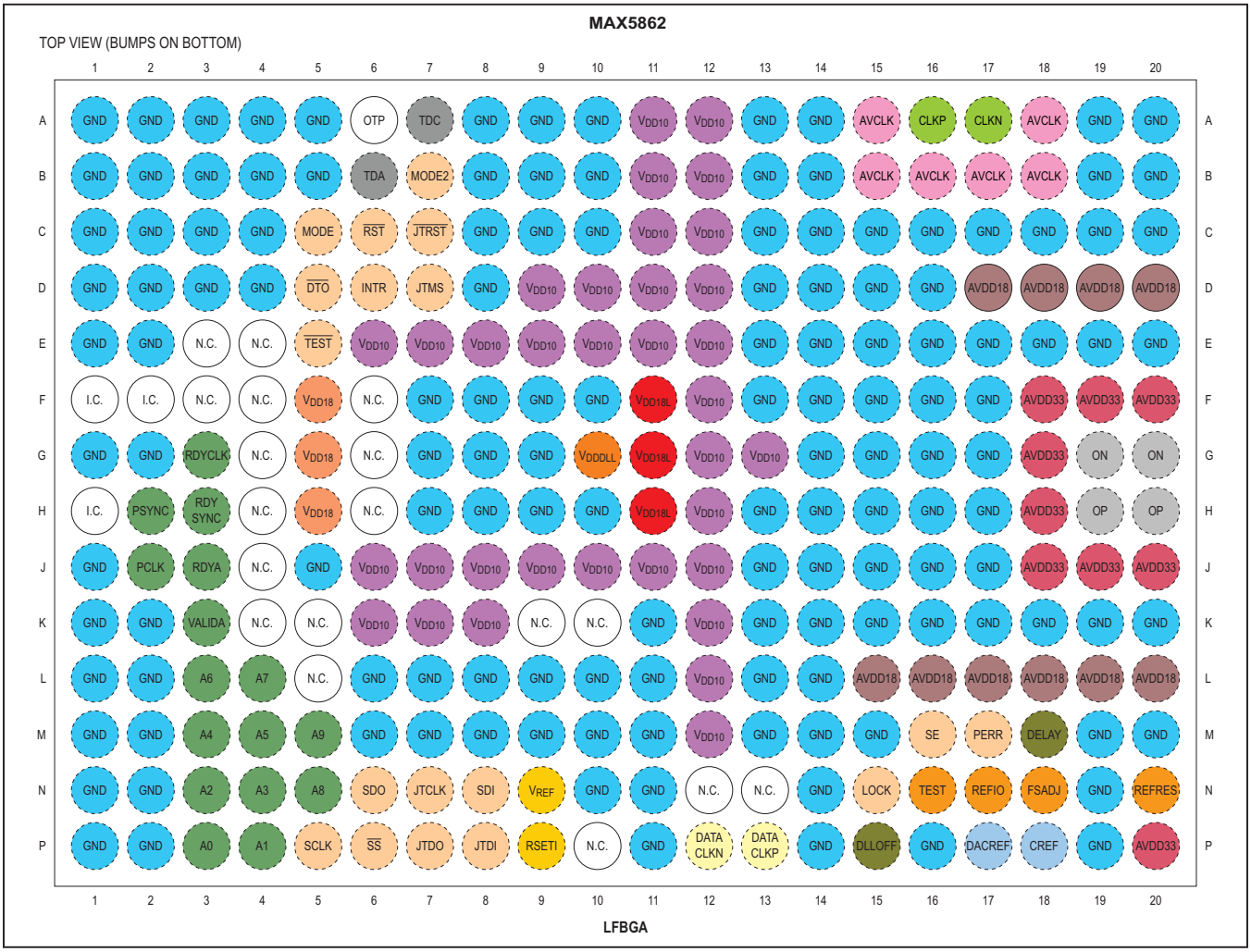
CLOCK/2 FEEDTHROUGH vs. CLOCK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = -0.1dBFS)



POWER DISSIPATION vs. NUMBER OF ACTIVE QAM CHANNELS



Ball Configuration



Ball Description

BALL	NAME	FUNCTION
A1–A5, A8–A10, A13, A14, A19, A20, B1–B5, B8–B10, B13, B14, B19, B20, C1–C4, C8–C10, C13–C20, D1–D4, D8, D13–D16, E1, E2, E13–E20, F7–F10, F13–F17, G1, G2, G7–G9, G14 –G17, H7–H10, H13–H17, J1, J5, J13–J17, K1, K2, K11, K13–K20, L1, L2, L6–L11, L13, L14, M1, M2, M6–M11, M13–M15, M19, M20, N1, N2, N10, N11, N14, N19, P1, P2, P11, P14, P16, P19	GND	Ground. Connect to ground plane with minimum inductance. P11 can be used as GND sense.
A6	OTP	Manufacturer Test Pin. Connect to GND.
A7	TDC	Temperature Diode Cathode Connection (MAX6642). Connect to GND.

Ball Description (continued)

BALL	NAME	FUNCTION
A11, A12, B11, B12, C11, C12, D9–D12, E6–E12, F12, G12, G13, H12, J6–J12, K6–K8, K12, L12, M12	V_{DD10}	Core V_{DD} (1.0V). A11 can be used as V_{DD10} sense
A15, A18, B15–B18	AVCLK	Clock 1.8V Supply Voltage. Connect 47nF bypass capacitors between each AVCLK pin and GND
A16	CLKP	Positive Converter Clock Input. There is an internal 100Ω termination resistor between CLKP and CLKN.
A17	CLKN	Negative Converter Clock Input. There is an internal 100Ω termination resistor between CLKP and CLKN.
B6	TDA	Temperature Diode Anode Connection (MAX6642)
B7	MODE2	Test Mode Control Pin 2.
C5	MODE	Manufacturing Test Pin. Connect to V_{DD18} (logic 1).
C6	$\overline{RST}$	Active-Low Global Reset (except JTAG)
C7	$\overline{JTRST}$	Active-Low JTAG Reset (Internal 50kΩ Pullup Resistor). This pin should be pulsed low at startup or connected in parallel with $\overline{RST}$.
D5	DTO	Digital Test Output. External pullup resistor may be required if DTO output state is high-impedance.
D6	$\overline{INTR}$	Active-Low Interrupt Flag
D7	JTMS	JTAG Mode Select (Internal 50kΩ Pullup Resistor)
D17–D20, L15–L20	AVDD18	Analog 1.8V Supply Voltage. Connect 47nF bypass capacitors between each AVDD18 pin and GND.
E3, E4, F3, F4, F6, G4, G6, H4, H6, J4, K4, K5, K9, K10, L5, N12, N13, P10	N.C.	No connection. Not internally connected.
E5	$\overline{TEST}$	Active-Low Manufacturing Test Pin. Connect to V_{DD18} (logic 1).
F1, F2, H1	I.C.	Internally connected. Do not connect.
F5, G5, H5	V_{DD18}	CMOS I/O V_{DD} (1.8V)
F11, G11, H11	V_{DD18L}	LVDS I/O V_{DD} (1.8V)
F18–F20, G18, H18, J18–J20, P20	AVDD33	Analog 3.3V Supply Voltage. Connect 47nF bypass capacitors between each AVDD33 pin and GND.
G3	RDYCLK	Port Delayed Ready Clock Output
G10	V_{DDDLL}	Dedicated V_{DD} for DLL and LVDS Bias Generator (1.8V). Connect to 1.8V even if DLL is not used.
G19, G20	ON	Negative Terminal of Differential DAC Output. OUTN has an internal 25Ω resistor to AVDD33.
H2	PSYNC	Common Port Sync Input
H3	RDYSYNC	Port Delayed Ready Sync Output
H19, H20	OP	Positive Terminal of Differential DAC Output. OUTN has an internal 25Ω resistor to AVDD33.
J2	PCLK	Common Port Clock Input
J3	RDYA	Port A Ready Output

Ball Description (continued)

BALL	NAME	FUNCTION
K3	VALIDA	Valid A Data Input
L3	A6	Port A Input Symbol Data, Bit 6
L4	A7	Port A Input Symbol Data, Bit 7
M3	A4	Port A Input Symbol Data, Bit 4
M4	A5	Port A Input Symbol Data, Bit 5
M5	A9	Port A Input Symbol Data, Bit 9
M16	SE	Scan Enable Input. Connect to GND for normal operation. See the *Thermal Management* section for more detail.
M17	PERR	1.8V CMOS Logic-Level Parity Error Output. When a parity error is detected in the DAC input data, this pin is set high for a minimum of 48 f_{CLK} data periods. This can be used to provide failure monitoring for the system. Note that this pin can pulse high when power is initially applied and before the DLL is locked.
M18	DELAY	Data Clock Mode Control. DELAY is a 1.8V, 3.3V tolerant, 4-level logic input (see Table 1 for details).
N3	A2	Port A Input Symbol Data, Bit 2
N4	A3	Port A Input Symbol Data, Bit 3
N5	A8	Port A Input Symbol Data, Bit 8
N6	SDO	SPI Serial-Data Out
N7	JTCLK	JTAG Clock
N8	SDI	SPI Serial-Data In
N9	V_{REF}	Voltage Reference Output. Connect a 100pF capacitor between V_{REF} and ground.
N15	LOCK	DLL Locking Indicator Output. Logic-high indicates DLL is locked.
N16	TEST	Manufacturer Test pin. Connect TEST to ground.
N17	REFIO	Reference Input/Output. Output pin for the internal 1.2V bandgap reference. REFIO has a 10kΩ series resistance and can be driven using an external reference. Connect a 1µF capacitor between REFIO and DACREF.
N18	FSADJ	Full-Scale Adjust Input. Sets the full-scale output current of the DAC. For 80mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF.
N20	RFRES	Connect a 500Ω resistor between REFRES and AVDD33.
P3	A0	Port A Input Symbol Data, Bit 0
P4	A1	Port A Input Symbol Data, Bit 1
P5	SCLK	SPI Clock
P6	$\overline{SS}$	Active-Low SPI Select
P7	JTDO	JTAG Serial Data Out
P8	JTDI	JTAG Serial Data In (Internal 50kΩ Pullup Resistor)
P9	RSETI	Manufacturing Test Pin. Connect RSETI to ground.
P12	DATACLKN	Data Clock Complementary Output. Output data clock from DAC. Connect to an external resonator circuit for optimized duty cycle operation.

Ball Description (continued)

BALL	NAME	FUNCTION
P13	DATACLKP	Data Clock Primary Output. Output data clock from DAC. Connect to an external resonator circuit for optimized duty cycle operation.
P15	DLLOFF	Data Clock Mode Control. DLLOFF is a 1.8V, 3.3V tolerant, 4-level logic input (see Table 1 for details). DLLOFF needs to be pulsed high for 1ms before using the data clock.
P17	DACREF	Current-Set Resistor Return Path. For 80mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. DACREF is internally connected to GND. **Do not connect DACREF to external ground.**
P18	CREF	Noise Bypass Pin. A 1µF capacitor between CREF and DACREF band limits the phase noise of the device.

Signal Description

NAME	I/O TYPE	BALLS	DESCRIPTION
A[9:0]	CMOS Input	10	Port A Input Symbol Data
AVCLK	Power	6	Clock 1.8V Supply Voltage. Connect 47nF bypass capacitors between each AVCLK and GND.
AVDD33	Power	9	Analog 3.3V Supply Voltage. Connect 47nF bypass capacitors between each AVDD33 pin and GND.
AVDD18	Power	10	1.8V Supply Voltage. Connect 47nF bypass capacitors between each V_{DD18} pin and GND.
CLKN	Analog	1	Negative Converter Clock Input. There is an internal 100Ω termination resistor between CLKP and CLKN.
CLKP	Analog	1	Positive Converter Clock Input. There is an internal 100Ω termination resistor between CLKP and CLKN.
CREF	Analog	1	Noise Bypass Pin. A 1µF capacitor between the CREF and DACREF band limits the phase noise of the DAC.
DACREF	Analog	1	Current-Set Resistor Return Path. For an 80mA full-scale output current, connect a 2kΩ (R_{SET}) resistor between FSADJ and DACREF. DACREF is internally connected to GND. DO NOT EXTERNALLY CONNECT TO GROUND.
DATACLKN	LVDS Output	1	DAC Negative Clock Output. Connect to an external resonator circuit for optimized duty-cycle operation.
DATACLKP	LVDS Output	1	DAC Positive Clock Output. Connect to an external resonator circuit for optimized duty-cycle operation.
DELAY	1.8V 4-Level Logic Input	1	Data Clock Mode Control. DELAY is used along with DLLOFF to set the DLL operating range (Table 1).
DLLOFF	1.8V 4-Level Logic Input	1	Data Clock Mode Control. Must be pulsed high at power-up. DLLOFF is used along with DELAY to set the DLL operating range (Table 1).
DTO	Hi-Z CMOS Output	1	Digital Test Output. External pullup resistor may be required when DTO is high impedance.
FSADJ	Analog	1	Full-Scale Adjust Input. Sets the full-scale output current of the DAC. For an 80mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF.

Signal Description (continued)

NAME	I/O TYPE	BALLS	DESCRIPTION
GND	Power	138	Digital Ground. Connect to ground plane with minimum inductance.
I.C.	—	3	Internally Connected. Do not connect.
$\overline{INTR}$	CMOS Output	1	Interrupt Flag (Active Low)
JTCLK	CMOS Input	1	JTAG Clock
JTDI	CMOS Input	1	JTAG Serial Data In (Internal 50kΩ Pullup Resistor)
JTDO	Hi-Z CMOS Output	1	JTAG Serial Data Out
JTMS	CMOS Input	1	JTAG Mode Select (Internal 50kΩ Pullup Resistor)
$\overline{JTRST}$	CMOS Input	1	JTAG Reset (Active-Low) (Internal 50kΩ Pullup Resistor). This pin should be pulsed low at startup or tied in parallel with $\overline{RST}$.
LOCK	CMOS Output	1	1.8V CMOS Logic Output. LOCK is DLL locking indicator output, and logic high indicates DLL is locked.
MODE	CMOS Input	1	Manufacturing Test Pin. Connect to 1.8V (logic 1).
MODE2	CMOS Input	1	Test Mode Control Pin 2
N.C.	—	18	No Connection. Unconnected Balls.
OP	Analog	2	Positive Terminal of Differential DAC Output. OP has an internal 25Ω resistor to AVDD33.
ON	Analog	2	Negative Terminal of Differential DAC Output. ON has an internal 25Ω resistor to AVDD33.
PCLK	CMOS Input	1	Port Clock Input
PERR	CMOS Output	1	1.8V CMOS Logic-Level Parity Error Output. When a parity error is detected in the DAC input data, this pin is set high for a minimum of 48 f_{CLK} data periods. This may be used to provide failure monitoring for the system. Note that this pin may pulse high when power is initially applied and before the DLL is locked.
PSYNC	CMOS Input	1	Port Sync Input
RDYA	CMOS Output	1	Port A Ready Output
RDYCLK	CMOS Output	1	Port Delayed Ready Clock Output
RDYSYNC	CMOS Output	1	Port Delayed Ready Sync Output
REFIO	Analog	1	Reference Input/Output. Output pin for the internal 1.2V-bandgap reference. REFIO has a 10kΩ series resistance and can be driven using an external reference. Connect a 1µF capacitor between REFIO and DACREF.
REFRES	Analog	1	Connect a 500Ω resistor between REFRES and AVDD33
RSETI	Analog	1	Manufacturing Test Pin. Connect RSETI to ground.
$\overline{RST}$	CMOS Input	1	Global Reset (Except JTAG Logic) (Active Low)
SCLK	CMOS Input	1	SPI Clock
SDI	CMOS Input	1	SPI Serial Data In
SDO	CMOS Output	1	SPI Serial Data Out
SE	CMOS Input	1	Scan Enable. 1.8V CMOS logic input. Connect SE to GND.
$\overline{SS}$	CMOS Input	1	SPI Select (Active-Low)
TDA	Analog	1	Temperature Diode Anode Connection (MAX6642)
TDC	Analog	1	Temperature Diode Cathode Connection (MAX6642). Connect TDC to ground.
TEST	Analog	1	Manufacturing Test Pin. Connect TEST to ground.
$\overline{TEST}$	CMOS Input	1	Manufacturing Test Pin. Connect to 1.8V (logic 1).
VALIDA	CMOS Input	1	Valid A Data Input

Signal Description (continued)

NAME	I/O TYPE	BALLS	DESCRIPTION
V_{DD10}	Power	34	Core V_{DD} (1.0V)
V_{DD18}	Power	3	CMOS I/O V_{DD} (1.8V)
V_{DD18L}	Power	3	LVDS I/O V_{DD} (1.8V)
V_{DDDLL}	Power	1	Dedicated V_{DD} for DLL and LVDS bias generator (1.8V). This must always be connected to 1.8V even if DLL is not used.
V_{REF}	Analog	1	Manufacturing Test Pin. Connect a 100pF capacitor between V_{REF} and ground.

Table 1. Pin Function (DLLOFF, DELAY)

DLLOFF	DELAY	f_{CLK} (MHz)	OPERATION
Low	High	2150 to 2304	$f_{DLL} = f_{CLK}/2$
Low	Low	1900 to 2105	$f_{DLL} = f_{CLK}/2$

Detailed Description

The MAX5862 integrates a high-performance, scalable, 32-channel digital upconverter (DUC) and 14-bit, 4.6Gsps RF-DAC for direct RF synthesis of multicarrier quadrature amplitude modulation (QAM) signals in cable modem termination systems (CMTS) and edge QAM (EQAM) devices. The device combines Maxim Integrated's industry-proven DUC and RF-DAC technology in a single package to provide a compact, 12mm x 17mm, QAM modulation solution with logical system partitioning. The MAX5862 features excellent spurious, noise, and adjacent channel power (ACP) performance and can directly synthesize up to 32 carriers in the 47MHz to 1006MHz cable downstream band as defined by the Data-Over-Cable Service Interface Specification (DOCSIS). The MAX5862 is capable of operating with a clock rate (f_{CLK}) up to 2.3GHz. Since the output is latched on both rising and falling clock edges, a 2.3GHz clock results in a DAC update rate (f_{DAC}) of 4.6Gsps.

The device accepts FEC-encoded CMOS data (symbols) on a single 10-bit input port that accepts up to 32 time-interleaved digital data streams. The 10-bit input port uses 5-bits for I and Q, and with the use of an offset bias bit, allows QAM mapped signals up to 1024-QAM.

The MAX5862 QAM mapper supports all QAM constellations defined in ITU-T J.83. It performs pulse shaping, resampling, interpolation and quadrature modulation of input data, supporting all data rates defined in DOCSIS. A cascade of interpolation filters, complex modulators, and channel combiners allow modulation of the signal to any frequency in the frequency band from 47MHz to 1006MHz. Integrated Direct Digital Frequency Synthesizers (DDFS) allow positioning of the carrier blocks with a resolution of 125Hz. The interpolation filters and resampler have linear phase, and excellent gain flatness. Output data from the last modulator is fed to a Digital Predistortion (DPD) block to eliminate distortion performance limitations in the DAC and output amplifiers.

The MAX5862 contains a current-steering DAC with an integrated 50Ω differential output termination to ensure optimum dynamic performance. Operating from 3.3V, 1.8V, and 1.0V power supplies, the MAX5862 dissipates 4.2W at 4.6Gsps. The device is specified over the upper commercial temperature range (0°C to +85°C) and is offered in a 280-ball FCBGA package.

An interrupt pin signals when a system error condition has occurred. The SPI port allows full configuration and debug capability.

Operational Overview

The MAX5862 (Figure 1) integrates a QAM modulator and digital upconverter (DUC) and the 4.6Gsps 14-bit RF-DAC into a single package. The MAX5862 provides the digital signal-processing capability to QAM modulate and up-convert 32 digital data streams to 32 DOCSIS-compliant frequency-agile channels. The MAX5862 can accept data on a 10-bit CMOS parallel port at double data rate (DDR) or single data rate (SDR). A cascade of interpolation filters, complex modulators, and channel combiners allow modulation of the signal to any frequency in the frequency band from 47MHz to 1006MHz. Integrated Direct Digital Frequency Synthesizers (DDFS) allow positioning of the carrier block with a resolution of 125Hz. Output data from the last modulator is fed to a Digital Predistortion (DPD) block to enhance IM3 and HD3 performance of the MAX5862 RF-DAC and output amplifiers.

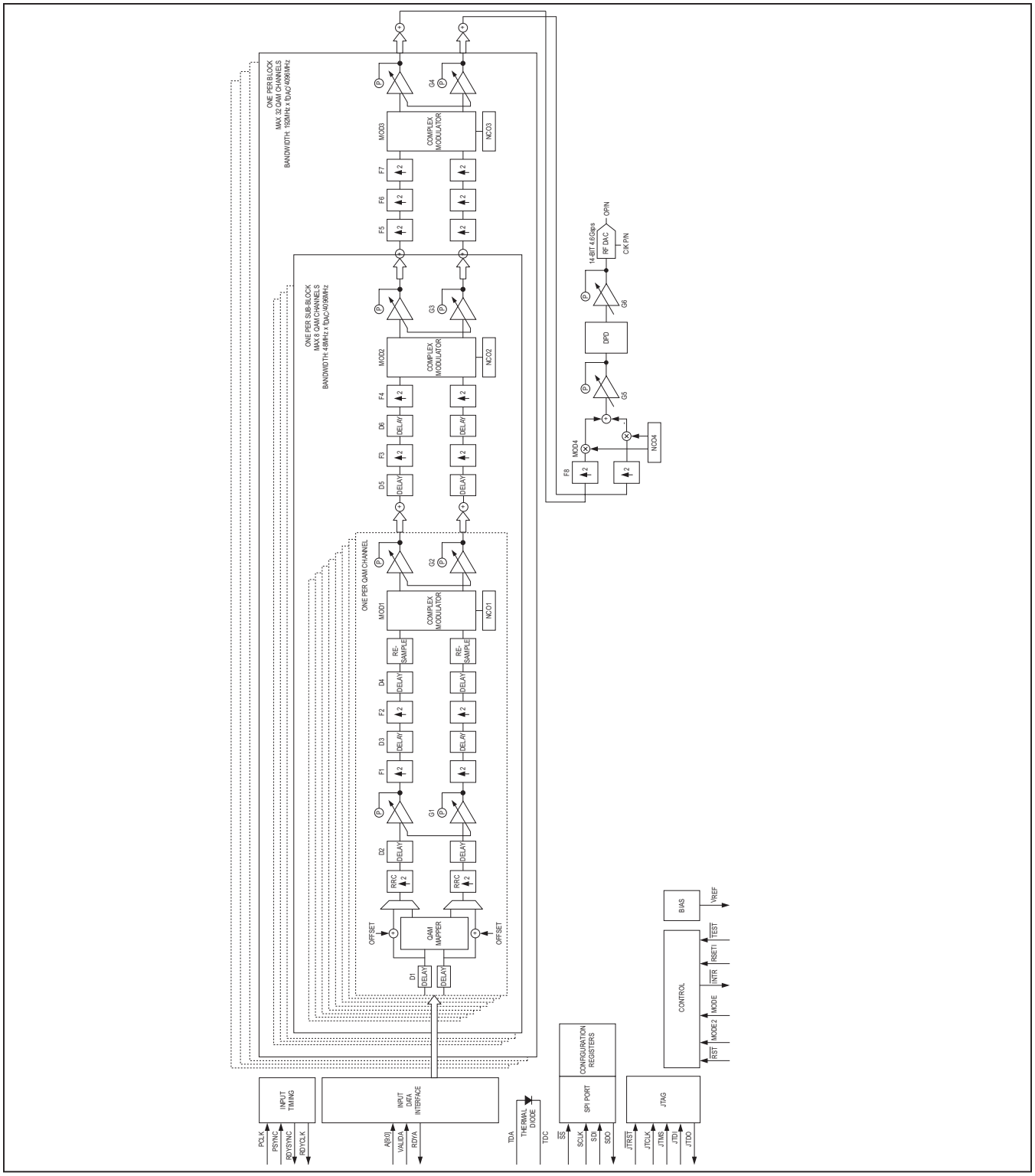


Figure 1. Block Diagram

Reference System

The MAX5862 supports operation with the on-chip 1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source and as the output if the DAC is operating with the internal reference. For stable operation with the internal reference, decouple REFIO to DACREF with a 1µF capacitor. Since REFIO has a 10kΩ series resistance, buffer REFIO with an external amplifier to drive external loads.

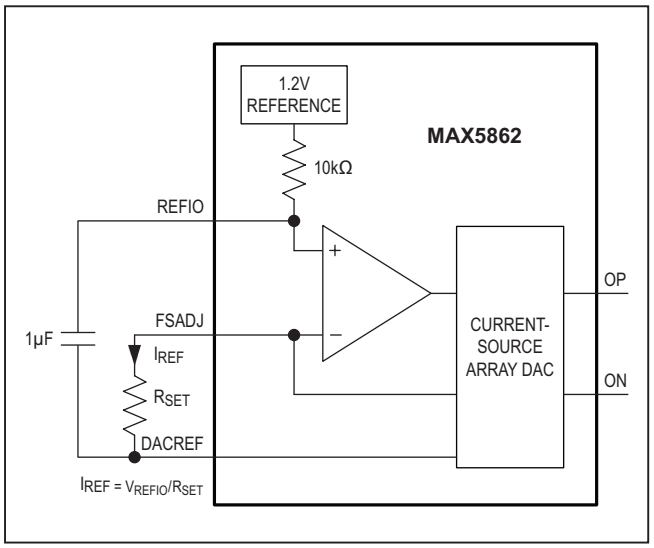


Figure 2. Reference System Architecture

The MAX5862's reference circuit (Figure 2) employs a control amplifier, designed to regulate the full-scale current I_{OUT} for the differential current outputs of the DAC. The bandwidth of the control amplifier is typically less than 100kHz. The DAC full-scale output current can be calculated as follows:

$$I_{OUT} = 128 \times I_{REF} \times 16383/16384$$

where I_{REF} is the reference output current ($I_{REF} = V_{REFIO}/R_{SET}$) and I_{OUT} is the full-scale output current of the DAC. With an external reference voltage of 1.25V, R_{SET} is typically set to 2kΩ, resulting in a full-scale current of 80mA and maximum 9.46dBm output power for a continuous wave (CW) signal. Generally, the dynamic performance of the DAC improves with increasing full-scale current.

Analog Output

The MAX5862 contains a differential current-steering DAC with built-in output termination resistors. The outputs are terminated to AVDD33 providing a 50Ω differential output resistance. In addition to the signal current, a constant 40mA current sink is connected to each DAC output. Figure 3 shows an equivalent circuit of the internal output structure of the MAX5862. The circuit has some resistive, capacitive, and inductive elements. These elements limit the output bandwidth to 2GHz with an external resistive differential 50Ω load.

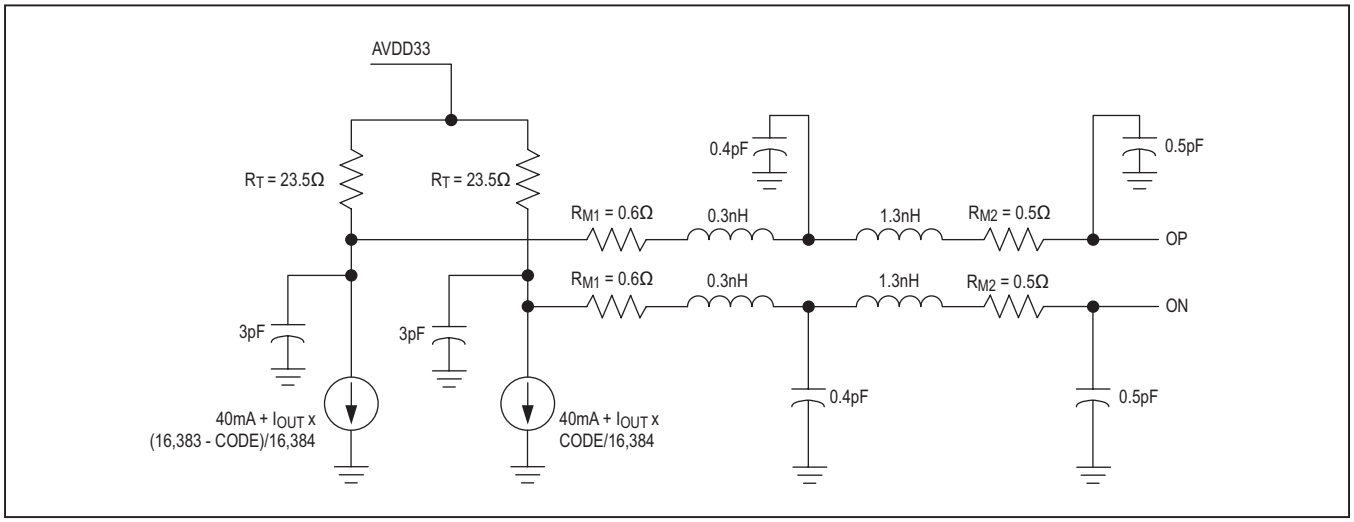


Figure 3. Equivalent Output Circuit

The outputs need to be pulled up externally to AVDD33. It is recommended that inductors be used for this purpose as shown in Figure 4. The use of discrete inductors and capacitors allows for near perfect symmetry in the output circuit layout. An external 50Ω differential load is also required to avoid excessive voltage swings at the DAC output pins.

Clock Inputs

The MAX5862 has a universal, differential clock input (CLKP, CLKN) operating from a separate power supply (AVCLK) to achieve the best possible jitter performance. The two clock inputs should be driven from a differential clock source. A sine wave or a square wave signal can be used.

For the highest speeds and highest performance, a sinusoidal clock should be used. At rates where it is feasible, a LVDS or PECL clock may also be utilized. The LVDS or PECL clock must be AC coupled to the MAX5862.

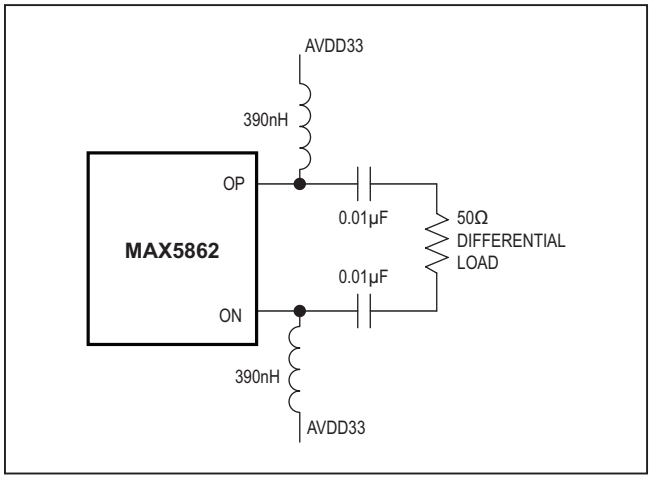


Figure 4. Typical Output Circuit

Each pin is internally DC-biased to 1/3 the supply voltage AVCLK. The clock input has an internal 100Ω differential termination resistor. For 50Ω (differential) termination at high clock frequencies, an additional external termination resistor is required between CLKP and CLKN. The balanced input should be AC-coupled unless the common-mode of the clock source is within the specifications for the MAX5862's RF-DAC clock input (CLKP/CLKN). An example of a well balanced single-ended to differential application circuit using three baluns is shown in Figure 5.

Clock Duty Cycle

The MAX5862 input clock is supplied at a frequency (f_{CLK}) that is one half the DAC update rate (f_{DAC}). The DAC output updates on both edges of the clock. Deviation from a balanced duty cycle will contribute to images in the output spectrum. The magnitude of the images is dependent on the absolute value of the deviation from an ideal 50% duty cycle. These artifacts will occur at the following frequencies:

$$f_{IMAGE} = \frac{f_{DAC}}{2} \pm f_{OUT}$$

To minimize the image at $f_{DAC}/2 - f_{OUT}$, the clock duty-cycle should be close to 50%. A filtered sine wave will have this characteristic. An offset voltage at the input of the clock input buffer will cause a duty-cycle change. The duty-cycle change in percent is approximately (100/π) x V_{OFS}/Ampl where V_{OFS} is the offset voltage and Ampl is the peak clock input amplitude. With clock amplitude of 1V peak (differential), an offset of 3.14mV would shift the duty cycle from 50.0% to 50.1/49.9%.

LOCK Signal

The LOCK pin is an output signal. When SE is logic-low (0V), the LOCK signal indicates the lock condition of the DLL circuit; LOCK is logic-high (1.8V) when the DLL is locked.

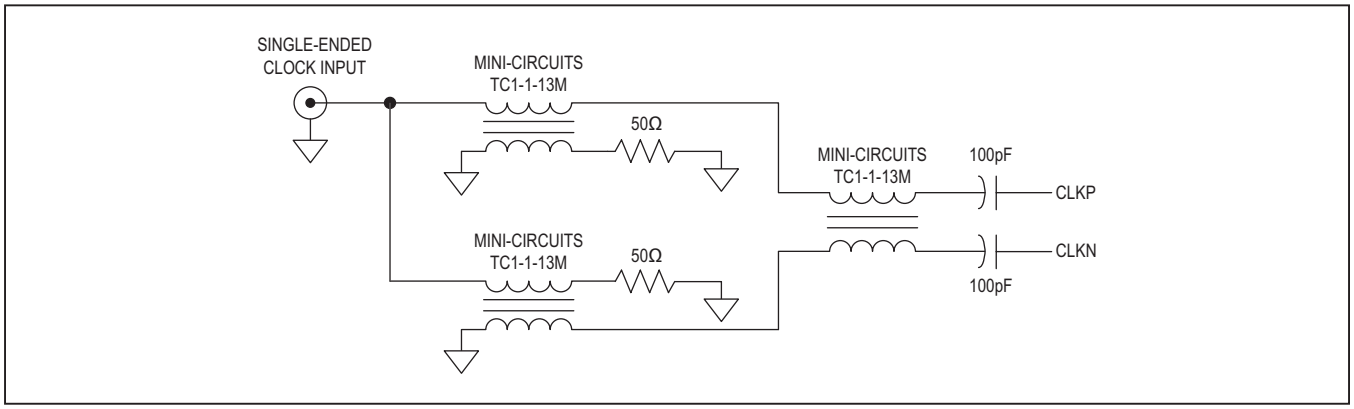


Figure 5. Balanced RF-DAC Clock Interface Circuit

Input Symbol Interface

Symbol Interface Description

Interface the digital data streams to the device through the port/channel multiplexer and provide a clock and sync signal. Each active clock edge marks a time slot. The device loads parallel input data (up to 10 bits in width) on each active edge of the clock signal. Assert the periodic PSYNC signal high for one clock period every N clocks to indicate which clock period (time slot) is slot 1. The value N can range from 2 to 32. Each channel utilizes a configuration register that contains the assigned port and time slot from which the channel receives data. This configuration information is referred to as the port/time slot. The port/time slot state machine accepts the clock and sync signals and generates the slot-tagging information. The *Port Input Timing* section describes the timing of a port/time slot.

The input port consists of a 10-bit data input bus, a VALIDA input signal, and a RDYA output signal. Use 6-bit wide data for 64-QAM mapping, 8-bit-wide data for 256-QAM mapping, or bypass the QAM mapper and use an I/Q word width of up to 10 bits wide (12 bits wide with internal offset register). For 12-bit I/Q data, the internal offset register, which is shared by I and Q, can be set through the SPI channel configuration register. The input word in QAM mapper bypass mode is presented with the Q bits as the MSBs and the I bits as the LSBs. An active-high VALIDA signal indicates that valid data is being presented to the input that is loaded into the FIFO. The RDYA output indicates that the channel FIFO is ready to accept data.

Each channel features a 16-word deep input FIFO to buffer the data stream from the user clock domain to the channel's symbol clock domain. The RDYA signal for a port/time slot originates from a channel's FIFO and is routed to the appropriate port/time slot. RDYA asserts high when the FIFO is ready to accept data, and asserts low when the channel FIFO is near full (8 words or greater). The FIFO continues to load data as long as the VALIDA signal is high. Drive the valid signal low to block a FIFO load. Continuous writes could eventually result in a FIFO overflow and loss of data. The channel-overflow flag bit is saved in the corresponding FIFO overflow error register and is cleared after a register read. A FIFO underflow error is generated when the resampler initiates a read on an empty FIFO. An underflow error indicates that the channel has missed a symbol, and this condition is signaled by the assertion (active-low) of the interrupt flag if it is programmed. The channel-underflow flag bit is saved in the corresponding FIFO underflow error register and is cleared after a register read. After an underflow occurs, the FIFO must fill halfway (eight words) before the FIFO read pointer starts incrementing again. A FIFO underflow cannot be generated until after the FIFO has started operation (filled to half-full and symbol transfer has started). A channel can be unmuted and sit idle (when its FIFO is not being loaded with data or before the FIFO has 8 symbols loaded) without generating an underflow flag.

The device's flexible configuration permits configuring the port to accept an arbitrary amount of data by specifying the number of time slots, by adjusting the PCLK and PSYNC signals. The device is configurable to input from 2 up to 32 data streams. A single data stream requires the slot count be set to 2 with only one slot containing user data. The data in a port/time slot is only significant if a digital stream is configured for that particular time slot.

To maintain proper symbol flow to the channels and proper FIFO operation, the minimum port clock speed must be greater than or equal to the number of time slots multiplied by the maximum symbol rate. To accommodate a large number of channels, configure the device input interface for DDR mode where the data is clocked on both the rising and falling edge of the clock. When using the DDR mode, ensure a 50% (±5%) clock duty cycle. When a lower number of channels are required, configure the MAX5862 to operate in SDR mode. SDR mode captures data only on the rising edge of the port clock.

Port Input Timing

The input port provides a flexible time-multiplexed method of accepting multiple digital data streams, as shown in Figure 6. The PCLK and PSYNC signals control the time-division-multiplexing feature of the device. RDYA and VALIDA signals provide FIFO handshaking for each channel and the interrupt-flag signals channel FIFO error conditions.

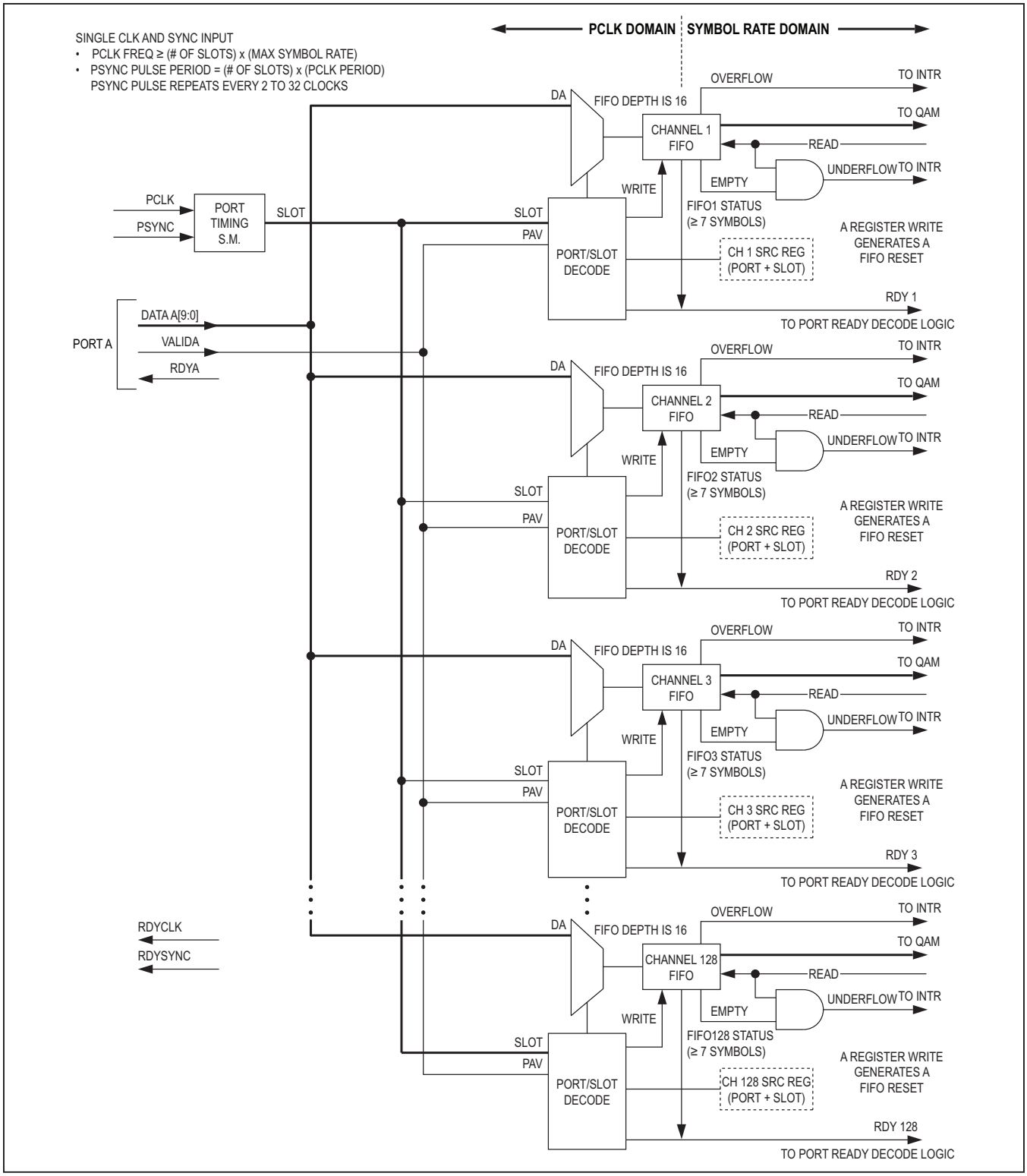


Figure 6. Symbol Interface Port Block Diagram

Handshaking

The two FIFO handshaking signals for each time slot are VALIDA (input signal) and RDYA (output signal). VALIDA is asserted high along with the incoming data word to indicate that the data is loaded into the FIFO. If VALIDA is asserted low, then a FIFO write cannot occur and the data word cannot be loaded into the FIFO. RDYA is an output from the FIFO circuitry to indicate the FIFO fill status. RDYA is asserted high if the FIFO is less than eight words from being full, thus allowing for an 8-word write buffer. If RDYA is asserted low and VALIDA is asserted high, a FIFO data write still occurs. Should FIFO writes continue (VALIDA asserted high) when the FIFO RDYA signal is asserted low, a FIFO overflow condition would eventually occur once the 8-word buffer space was consumed with resulting data loss. When a FIFO underflow occurs, data loss has occurred for the channel and the FIFO must fill at least halfway before normal FIFO operation begins. For the highest safety margin, RDYA should be detected on the current cycle and VALIDA asserted appropriately on the following cycle. The FIFO RDYA signal is expected to toggle during normal operation. To avoid a persistent underflow-interrupt condition after a global reset, FIFO reset, or FIFO underflow condition, the FIFO read pointer logic resets and the FIFO fills to half capacity (eight words) before data begins to be read and transferred to the DSP circuits. Time slots for data transfer are numbered from 1 to 32. Time slot 0 is not for data transfer since it represents a mute condition for an enabled channel (no data, no handshaking).

Port Clock

The frequency of the port clock can be synchronous or asynchronous to the output symbol rate. The port clock signal must be continuous with maximum frequency of 128MHz. Calculate the frequency of the port clock and input mode using the following formula:

In SDR mode:

PCLK_freq ≥ (fastest symbol rate of any channel) x (no. of time slots)

In DDR mode:

PCLK_freq ≥ (fastest symbol rate of any channel) x (no. of time slots) /2

To determine if SDR mode can be used or DDR mode must be used, considerations of the fastest symbol rate programmed, the number of time slots defined and the specified maximum PCLK frequency of 128MHz must be calculated. In the MAX5862, SDR mode can be used for a maximum of 16 channels. For 24 and 32 channel operation, DDR mode must be used. For example, if the fastest symbol rate is 7Msps and 16 time slots are desired, then the port clock is required to operate at a frequency higher than or equal to 56MHz using DDR mode. Clocking this interface slightly faster ensures that the DUC FIFOs do not empty (monitoring the VALIDA and RDYA handshake signals ensures that the DUC FIFOs do not overflow).

Single Data Rate (SDR)

Figure 7 shows the port timing for an SDR clocking scheme. Data is clocked in using only the rising edge of the common PCLK clock. SDR is suitable when the number of channels is low. Select between SDR and DDR using a configuration bit. The periodic port sync signal (PSYNC) is active-high for one clock period each N clocks, where N is the number of time slots.

For SDR operation, this equates to N number of slots. PSYNC is required to mark slot 1. The RSYNC bit in the CFG register allows for automatic generation of the RDYSYNC signal without a periodic PSYNC signal. When the RSYNC generator is enabled, PSYNC is only required once to mark slot 1, otherwise PSYNC must be applied on each data transfer cycle. If RSYNC is enabled and a periodic PSYNC are both used, be sure that PSYNC is properly applied. Otherwise, it could affect the RSYNC generator by short-cycling the slot count. Data is multiplexed onto the port data bus in discrete time segments called time slots. The rising edge when port sync is clocked into the DUC marks the first time slot. Port sync is only sampled on the rising edge of port clock.

To help account for the single-ended (early) clock on the port input when sampling FIFO output handshaking signals, a buffered (delayed) version of the port clock is available from the device called RDYCLK. The RDYCLK signal is delayed by 4ns to 9ns over temperature/voltage. It may be helpful to time-shift RDYCLK by 1/4 clock phase by an FPGA DLL or PLL to aid in capturing the channel FIFO RDYOUT signals. To synchronize the order of the RDYA signals, a RDYSYNC output is also provided. The RDYSYNC output is delayed by two port clock cycle periods from PSYNC.

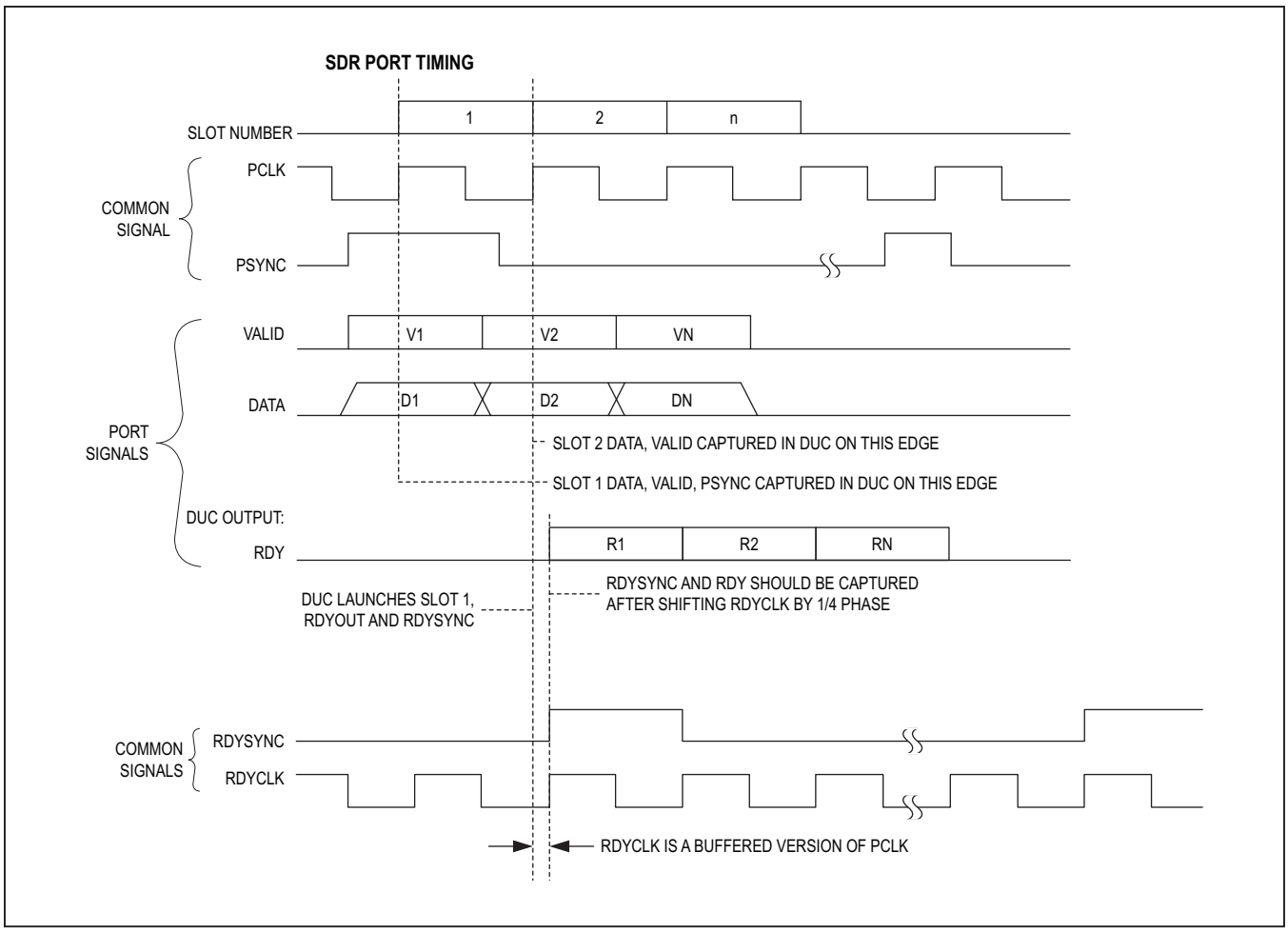


Figure 7. Example of Port Timing Diagram (SDR)

Double Data Rate (DDR)

The periodic port sync signal (PSYNC) is active-high for one clock period each N clocks, where N is the number of time slots. For DDR mode, this equates to 2N number of slots. The rising edge of PSYNC marks slot 1 on each transfer. Port sync is sampled on the rising edge of port clock. A repetitive (continuous) PSYNC signal is not required. Thus, in DDR mode there is always an even number of time slots.

The port timing diagram for DDR clocking is shown in Figure 8. The port clock is a continuous signal that must not be stopped. PSYNC is active for one clock period and is captured on the rising edge of port clock inside the DUC. DATA and VALIDA signals captured on this same edge are defined as slot 1 DATA and VALIDA. For DDR operation, slot 2 DATA and VALIDA are captured on the following falling edge. For SDR operation, slot 2 DATA and VALIDA are captured on the following rising edge (Figure 7). The slot count continues to increment until the internal sync counter rolls over, or another sync signal occurs. A PSYNC signal must occur at least once at the beginning of data transfers to the port. The PSYNC input pulse is not required to be periodic after the initial input pulse has been applied. The RDYSYNC pulse repeats, based on the programmed PSYNC counter value. PSYNC counter values for DDR mode can range from 2 to 32 in even-value increments only (i.e., 2, 4, 8, 10, etc.). PSYNC counter values for SDR mode can range from 2 to 16 and be even or odd values (i.e., 2, 3, 4, 5, etc.). SYNC counter values of 0 and 1 are not valid.

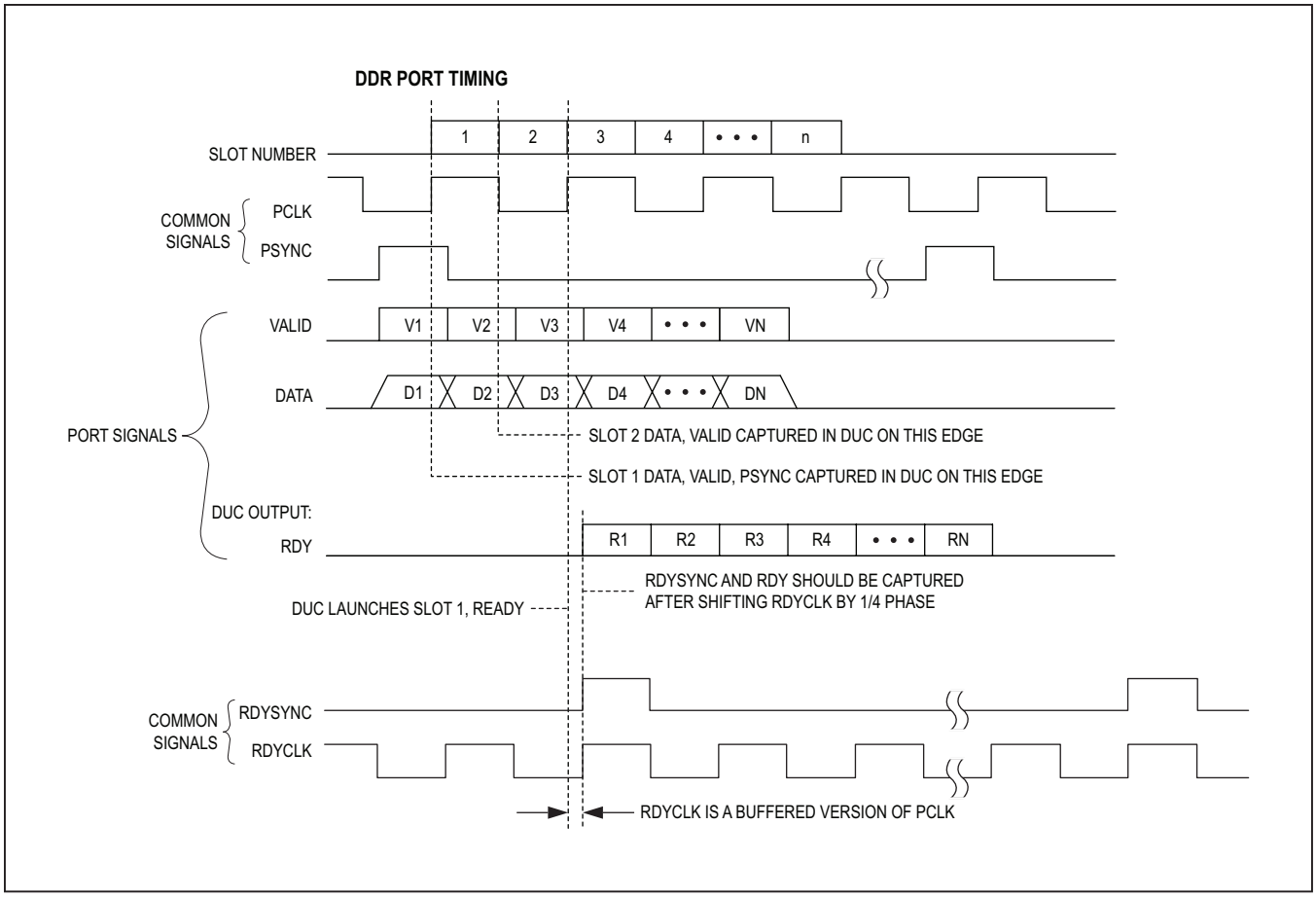


Figure 8. Example of Port Timing Diagram (DDR)

Channel FIFO Operation

Each channel features a 16-word deep FIFO for buffering the incoming demultiplexed symbol data. The input FIFO (one per channel) is the only elastic memory in the data path. After global (hardware) reset, the FIFO contents are set to all zeros.

After global reset or an underflow condition, the FIFO read pointer is reset and held at location 0. The FIFO must fill to 7 symbols before the FIFO read counter increments. While a channel is unmuted and before the FIFO pointer is allowed to increment, symbol data continues to be sampled from FIFO location 0. After global reset or underflow, the first input symbol word to be loaded into the FIFO is loaded at location 0.

The FIFO is clocked by the asynchronous port clock signal, which is not required to have any particular relationship to symbol rate or the DATACLK frequency. If the port clock frequency is higher than the required symbol “feed” rate for a channel, the FIFO absorbs the differences. The FIFO handshaking signals are used to avoid overflow or underflow. Should a channel FIFO underflow, the FIFO contents are set to zero and the associated QAM mapper output is zero (no symbol) until normal FIFO operation resumes again. An interrupt is not generated for the initial underflow condition (after reset) and only one interrupt is generated for each FIFO underflow thereafter. Soft-FIFO reset is accomplished by toggling the FIFO reset bit for the channel of interest through an SPI command. While the FIFO reset bit is logic 1, the FIFO pointer is reset to location 0, overflow/underflow indicators are cleared, FIFO ready is inactive (logic 0), and FIFO writes are stopped (the previous contents of the FIFO are not zeroed).

When the FIFO reset bit is released (set to logic 0), the FIFO ready signal goes to logic 1, which indicates that the FIFO is ready to accept data. The FIFO disallows data reads from the channel (ARR) until the pointer is at eight words.

A FIFO reset for a particular channel can be performed using one of three ways:

1) Set the self-clearing register bit in the channel configuration register space.
2) Enable the “use global reset” bit in the channel configuration register, then set a self-clearing global-FIFO reset register bit in the global configuration (*GBL_ CFG0*) register section.
3) Enable the “use global reset” bit in the channel configuration register and set the “use external input for FIFO reset” bit in the global external sync register, then apply a pulse at the MODE2 input to reset the FIFO.

Modulator and Upconverter Core

DSP Path Block Diagram

The DSP path performs QAM mapping, pulse shaping, resampling, interpolation, and modulation of the incoming data. Up to 32 channels with a symbol rate up to 7.14MSym/s are synthesized into one digital RF signal, driving a 4:1 multiplexed DAC as fast as 5Gsps. Incoming data can be bytes or QAM-mapped data. Bytes should be QAM mapped using the QAM mapper at the input of the DSP path. The QAM mapper supports 16-QAM, 32-QAM, 64-QAM, 128-QAM, and 256-QAM constellations, as defined in ITU-T J.83 [1] and DVB-C [3]. If QAM-mapped QAM mapper. QAM-mapped data are first pulse shaped using a root-raised cosine (RRC) filter. Each RRC filter has a configurable excess bandwidth factor of 0.12, 0.13, 0.15, or 0.18, meeting the requirements in J.83 Annex A, B, and C. [1]

As shown in Figure 6, at the first stage of multiplexing, all 128 channels are routed into up to 16 blocks of up to 8 channels each. In each octal-channel combiner, up to 8 individual channels are frequency translated and combined, forming a baseband block with a bandwidth up to 48MHz. In the next stage, four of these blocks are frequency translated and combined into a larger baseband block with a maximum bandwidth of 192MHz. Next, up to four of these blocks are frequency translated and combined into a block with a maximum bandwidth of 950MHz. This block is passed through a final 2x interpolation filter and the block is frequency translated to the desired output frequency using a quadrature modulator.

Spurious emissions and noise below 1GHz comply with DOCSIS 3.0 DRFI requirements (Tables 6-5 in CM-SP-DRFI-I06-080215 [2]). Stopband attenuation above 1GHz is higher than 60dB. Since the MAX5862’s RF-DAC has an attenuated image at $f_{DAC}/2 - f_{OUT}$, image attenuation above 1GHz is limited by the DAC to approximately 40dB. Further image attenuation can be achieved using an analog lowpass filter.

Octal Channel Combiner (48MHz Block)

A block diagram of the octal-channel combiner is shown in Figure 9. For simplicity, only one channel is shown. Seven more identical channels are added together in the adder (S1), forming a sub-block. Five-bit baseband I and Q data is received. The programmable delay block (D1) allows modifying the delay of each channel individually from 0 to 12 symbol periods in steps of 1 symbol period. The data can be passed through or bypass a QAM mapper. If the bypass function is used, an offset of 1/2 LSB can be set to allow representation of mapped 1024-QAM symbols. QAM-mapped data is pulse shaped using an RRC filter. The RRC filter interpolates the symbol rate by a factor of 2. Each RRC filter can be individually set to any of the J.83 standard excess bandwidth factors equal to 0.12, 0.13, 0.15, or 0.18. The programmable delay block following the RRC filter allows delaying the RRC filter output by 0 or 1/2 symbol periods. A programmable gain block (G1) allows setting the gain with 11-bit resolution for leveling and equalization purposes. The sample rate is increased by a factor of 8 from the symbol rate using the RRC filter, the F1 and F2 half-band filters. Interpolated data is resampled with an arbitrary sample rate using an ARR. Each channel is frequency translated within the ±24MHz channel before being combined using an adder network. All channels can be delayed the same in up to 3/8 symbol periods with 1/8 symbol period resolution using delays D3 and D4. Configure the QAM mapper for 16/32/64/128/256-QAM modulation. QAM constellations are defined in ITU-T J.83 [1] and EN 300 429 V1.2.1 [3]. The QAM mapper can be bypassed. If the QAM mapper is bypassed, an adjustable offset is provided to allow representation of a 1024-QAM-mapped signal using only 10 bits. The SPI interface programs the offset that moves the constellation off zero.

The arbitrary-rate resampler (ARR) is a Farrow filter that allows transitioning the sample rate from the symbol rate synchronous domain to the DAC clock synchronous domain. Sample rates must always be selected such that the resampler has a higher output data rate than the input data rate. Both the symbol clock and the DAC clock are derived from the same 10.24MHz DTI clock (DTI-I04-061222 [4]). Their frequencies are derived as f_{DAC} = M1/N1 x 10.24MHz and f_{SYM} = M2/N2 x 10.24MHz, where M1, M2, N1, and N2 are positive 16-bit integers. M2 and N2 can be different for different modulation schemes and standards. Because their frequencies are derived from the same 10.24MHz clock, the phase relationship between the two clocks is exactly known and can be calculated using 2-phase accumulators. While the DAC clock must run continuously, with very low jitter, symbol information can be transmitted with several samples of jitter, to be absorbed in FIFOs before the octal-channel combiner and at the input of the re-sampler. The resampler requests a new sample when needed to maintain the programmed, constant output rate. The output of the resampler and thereafter operates from a clock that is divided down from the DAC update rate by a factor of 64. A more detailed description of the ARR is given in the *Arbitrary Rate Resampler* (ARR) section. The complex modulator with its associated NCO is used to frequency translate the channels within the block. The frequency tuning word for the NCO is defined with 19-bit resolution. All programmable parameters are programmed through the SPI interface.

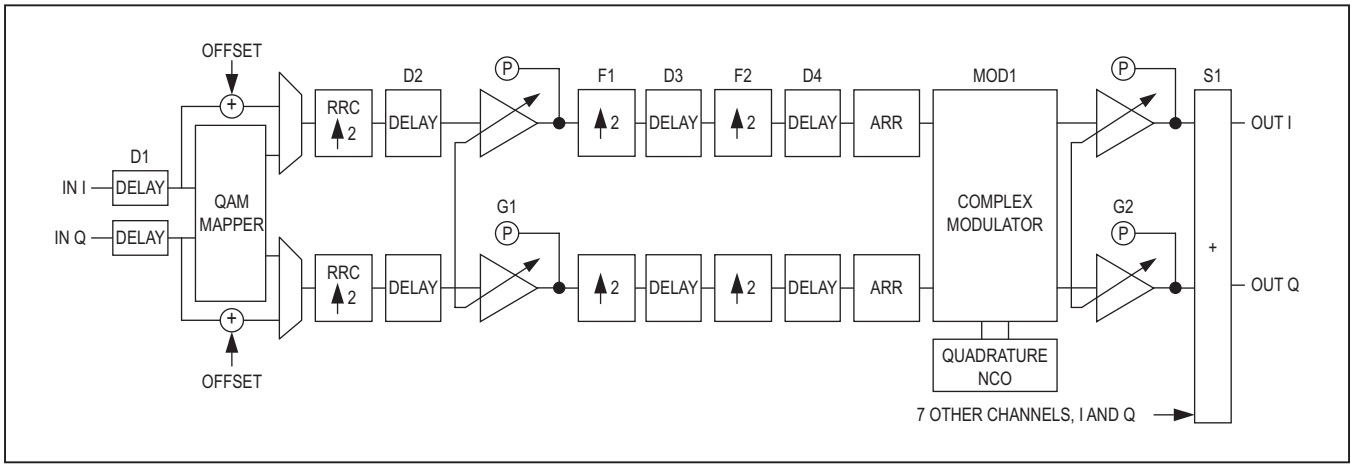


Figure 9. Octal Channel Combiner

Block Combiners and Digital Upconversion

The octal-channel combiners are followed by two stages of block combiners and a quadrature modulator, as shown in Figure 10. The sample rate of each sub-block of 8 channels is interpolated up by a factor of 4 before four sub-blocks are combined into one block of a maximum 32 channels.

The sample rate of each one of these blocks is again interpolated up by a factor of 8 and combined into a final output of up to 32 active channels with a maximum bandwidth of 950MHz. Finally, the sample rate is interpolated up by another factor of 2 and the output is frequency translated using a digital quadrature modulator. The gain of each sub-block, block, and output can be set with 8-bit resolution using gain controls G3 and G4 and with 9-bit resolution using G5 and G6. The latency of the entire data path can be changed in steps of 32 DAC update periods, using programmable delay registers D5 and D6. All D5 registers have a common control bit and all D6 registers have a common control bit.

QAM Mapper

The QAM mapper performs QAM mapping of input data. There is a separate QAM mapper for each channel and all QAM mappers are configured independently. The QAM mapper supports the following constellations:

- ITU-T J.83 Annex A: 16-QAM, 32-QAM, 64-QAM, 128-QAM, and 256-QAM
- ITU-T J.83 Annex B: 64-QAM and 256-QAM
- ITU-T J.83 Annex C: 64-QAM and 256-QAM

See Notes 18 and 20 below Table 2 for QAM constellations.

Table 2 explains the QAM options for the internal mapper. The input port to the device is 10 bits in width.

The bypass mode option allows the input of a constellation choice. The bypass mode option also allows the addition of an internal LSB static bit value (same for I and Q buses) to expand the effective bus width to 12 bits for 1024-QAM operation. This offset bit is set through an SPI register for each channel. The complex symbol data input in bypass mode is assumed to be (I + j Q) and the data input format is two's complement.

Table 3 shows the calculated RMS values for each modulation at the RRC filter input, calculated as the average vector length for all symbols. When using the bypass mode, all inputs expect two's complement formatted data.

In case of mapped data being applied in bypass mode, the user would place 5 bits of I data in bits [9:5] and 5 bits of Q data in bits [4:0] on the bus. Since there is a 10-bit data bus, the I/Q data can be represented by a minimum of 5 bits. The I/Q symbols are all odd numbers. Internally the 5 bits of I/Q are multiplied by 2 and an optional 1/2 LSB can be added.

RRC Filter

The RRC filter performs pulse shaping of the input symbols. The RRC filter excess bandwidth, passband flatness, stopband attenuation, and impulse response shape conform to ITU-T J.83 [1]. The RRC filter interpolates the symbol rate by a factor of 2. Use the SPI port to configure the excess bandwidth of each individual RRC filter.

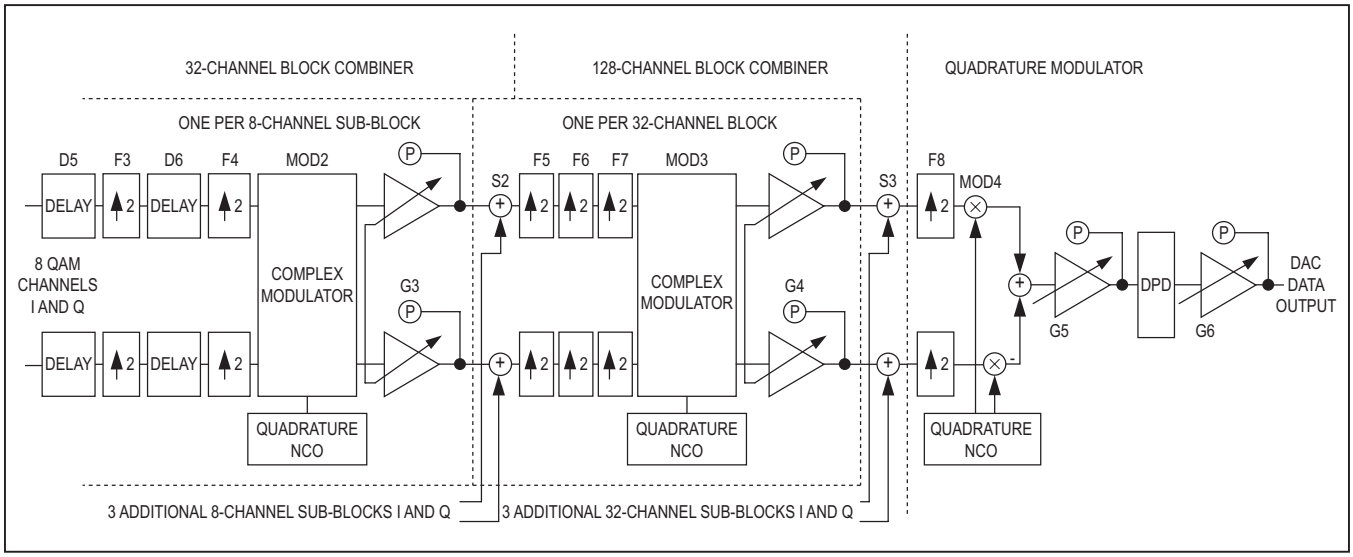


Figure 10. Channel Combiners and Interpolation/Modulation

Table 2. Internal QAM Mapper Options

SELECTION	TYPE	BUS BIT WIDTH	INPUT PORT BUS PARTITIONING	MSB
000	TCM 256-QAM (Note 18)	8	Bits [7:4] are I Bits [3:0] are Q	Bit 7 is MSB - I Bit 3 is MSB - Q
001	TCM 64-QAM	6	Bits [5:3] are I Bits [2:0] are Q	Bit 5 is MSB - I Bit 2 is MSB - Q
010	Diff Grey 16-QAM	4	Bits [3:0] are used	Bit 3 is MSB
011	Diff Grey 32-QAM	5	Bits [4:0] are used	Bit 4 is MSB
100	Diff Grey 64-QAM (Note 19)	6	Bits [5:0] are used	Bit 5 is MSB
101	Diff Grey 128-QAM	7	Bits [6:0] are used	Bit 6 is MSB
110	Diff Grey 256-QAM	8	Bits [7:0] are used	Bit 7 is MSB
111	10-bit bypass mode with Offset register (Notes 20, 21)	10	Bits [9:5] are I Bits [4:0] are Q	Bit 9 is MSB - I Bit 4 is MSB - Q

Note 18: The constellation mapping is as described in the Figure B.19 of the ITU J.83 standard document. Input bits are C7 to C0.
Note 19: The constellation mapping is as described in the Figure A.7 of the ITU J.83 standard document.
Note 20: Constellation mapping is outside the MAX5862. The complex symbol data input in bypass mode is (I + j Q) and the data input format is two's complement. Operation is y = 2x+b, where x is the 5-bit I or Q at the input and b is the LSB set by the register. For 64-QAM or 256-QAM, b = 0, for 1024-QAM, b = 1.
Note 21: An internal LSB offset register (same bit value for I and Q) is provided to expand the bus to effectively be 12 bits with the LSB offset bit enabled.

Table 3. QAM Mapper Symbol Levels

QAM TYPE	VALUES ASSIGNED TO SYMBOLS	VALUES SEEN AT THE INPUT OF THE RRC FILTER	LEVELS SCALED TO ±1
256-QAM	±1, 3, 5, 7, 9, 11, 13, 15	±2, 6, 10, 14, 18, 22, 26, 30	±0.0625 to 0.9375
128-QAM	±1, 3, 5, 7, 9, 11	±2, 6, 10, 14, 18, 22	±0.0625 to 0.6875
64-QAM	±1, 3, 5, 7	±4, 12, 20, 28	±0.125 to 0.875
32-QAM	±1, 3, 5	±4,12, 20	±0.125 to 0.625
16-QAM	±1, 3	±8, 24	±0.25 to 0.75
Bypass Mode with Offset	-32, -30, -28 to -2, 0, 2 to 30	±1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	±0.03125 to 0.96875
Bypass Mode without Offset	-32, -30, -28 to -2, 0, 2 to 30	-32, -30 to -2, 0, 2 to 30	-1.0 to 0.9375

Rate Resampler

The ARR converts the sample rate of the input symbols to a clock rate that is an integer division of the DAC clock rate. Both the symbol rate and the DAC update rate maintain a rational relationship to the 10.24MHz DTI clock. The symbol clock is related to the DTI clock as M/N x 10.24MHz, where M and N are integers. According to DOCSIS 3.0, these should be 16-bit integers. No M and N are published for Annex C. Table 4 shows the calculated M/N that meets the required symbol rate within 1ppm. To meet this accuracy, 16-bit numbers are needed.

The output rate of the ARR equals $f_{DAC}/64$. The RF-DAC update rate is higher than 4096Msps when all streams have a symbol rate lower than 8MSym/s.

The ARR is configured by two parameters. These parameters are KF and LF.

The DAC update rate can be calculated as:

$$f_{DAC} = 8 \times 64 \times LF/KF \times (f_{SYM})$$

where f_{DAC} is the DAC update rate and f_{SYM} is the symbol rate; LF and KF are represented using 27-bit integers. Avoid an LF value equal to 2^N, where N is any integer. If LF = 2^N, a calculation error causes artifacts in the output spectrum.

Modulators

Complex modulators are used for frequency translation of the carriers within the channel combiners (Figure 11). The complex modulators allow both positive- and negative-frequency translation of the input signal. A quadrature modulator (MOD4) is used for frequency translation of the final block.

Power Adjustment and Power Probes

The gain-adjustment blocks in the block diagram can be programmed using the SPI interface. A clipping monitor is also associated with the gain adjustment. A clipping measurement is initiated as follows: A threshold, the number of samples to be measured over, and the count reset are set in registers. The number of times the signal exceeds the set threshold during the measurement is written to a register. By performing a number of these measurements, the amplitude distribution of the signal can be derived, and power, PAPR, and clipping probability can be estimated using an external microprocessor.

In addition to adjusting the gain, the power-adjustment blocks can also be used to mute channels. A channel can be configured without affecting the channels that are already online. For this reason, the gain adjustment at the output of the device is adjustable in fine steps (< 0.1dB) to allow for slowly ramping down the gain when adding additional channels.

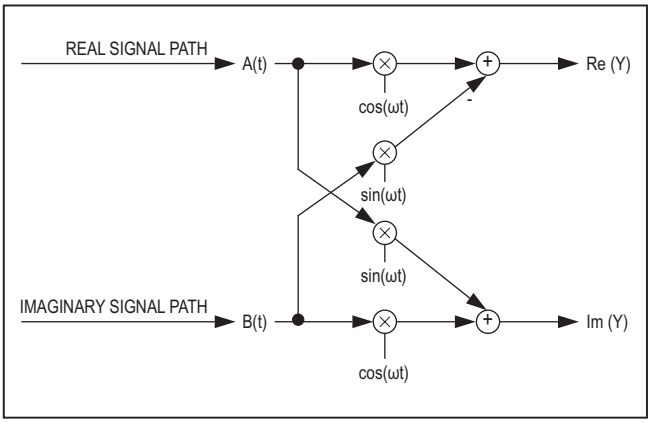


Figure 11. Complex Modulator Block Diagram

Table 4. Resampling Ratio Recommendations

SUPPORTED SYMBOL RATE (Msym/s)	ITU-T J.83 ANNEX	CHANNEL SPACING (f_C, MHz)	MODULATION (QAM)	M	N	M ÷ N
5.056941	B	6	64	401	812	0.4938423645
5.360537	B	6	256	78	149	0.5234899329
6.952	A	8	64	869	1280	0.6789062500
6.952	A	8	256	869	1280	0.6789062500
5.309734	C	6	64	1889	3643	0.5185286851
5.309734	C	6	256	1889	3643	0.5185286851

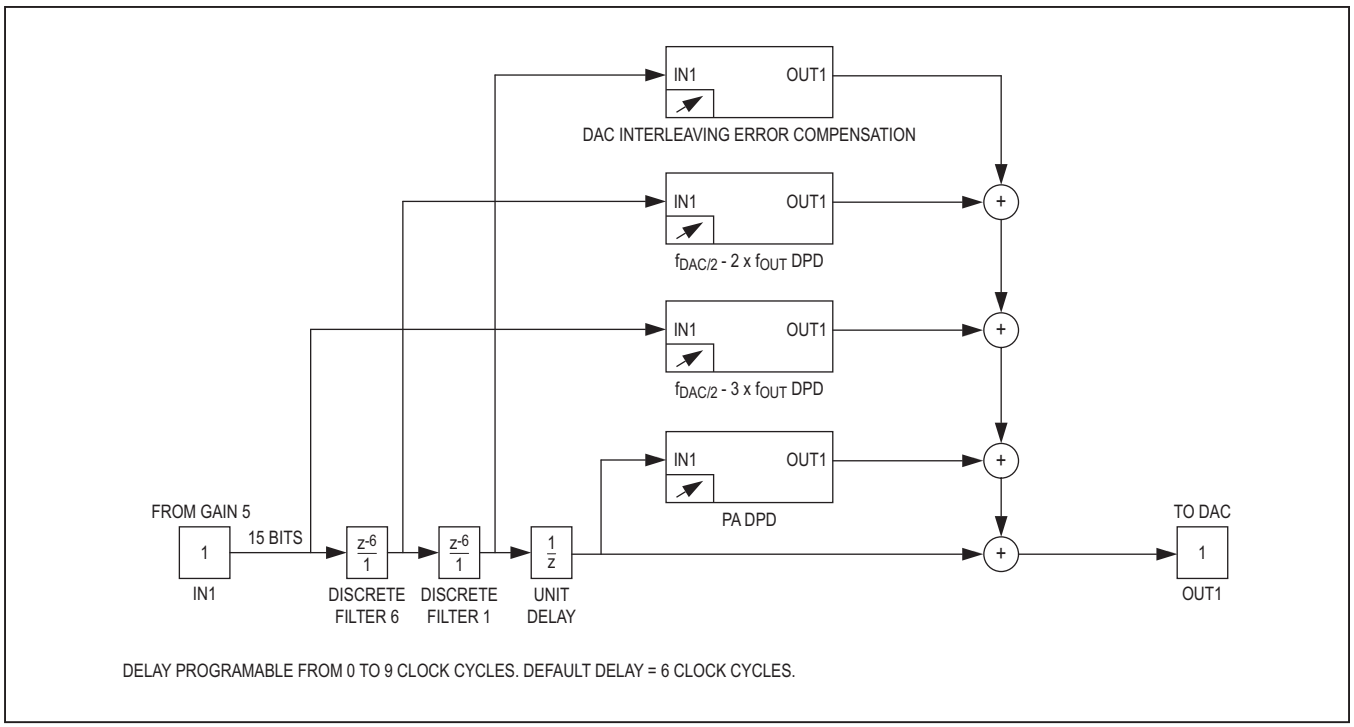


Figure 12. DPD - Top Level Block Diagram

Digital Predistortion (DPD)

DPD Function

The DPD block allows optimization of RF performance by correcting for distortion in the RF-DAC and the following RF amplifier chain. DPD is capable of correcting third-harmonic distortion (HD3), second-harmonic distortion (HD2), second- and third-order intermodulation products of the DAC and power amplifier, ($f_{DAC}/2$) - 2 x f_{OUT} spur in the RF-DAC as well as the DAC interleaving errors. Figure 12 shows the top-level block diagram of the DPD consisting of four blocks, which are generating correction signals that are added to the device output signal. These are:

- DAC Interleaving-Error Compensation: Since the DAC is updating on both clock edges, every other sample has an error resulting from the clock duty cycle being different by 50%. The DAC can also have a gain error in every other sample. The DAC interleaving compensation can correct for these two errors. By optimizing for these errors, the $f_{DAC}/2$ - f_{OUT} image is minimized. The block diagram of the DAC interleaving-error compensation block is shown in Figure 13.

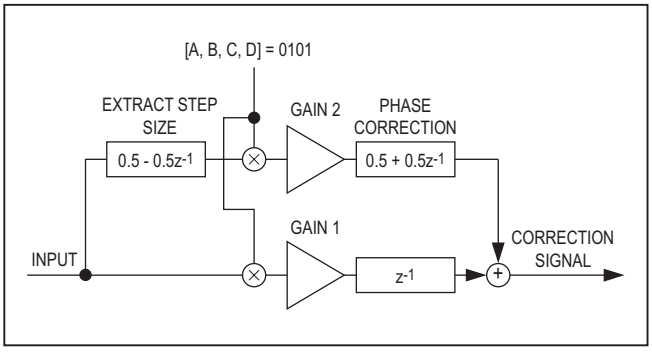


Figure 13. DAC Interleaving Error Compensation Block Diagram

- PA DPD: This block allows correction for HD2, IM2, HD3, and IM3 that can be represented with the diagonal kernel of a third-order Volterra series. This is intended for correction of “classical” second- and third-order nonlinearities in the DAC and the following amplifiers. The block diagram of this block is shown in Figure 14.

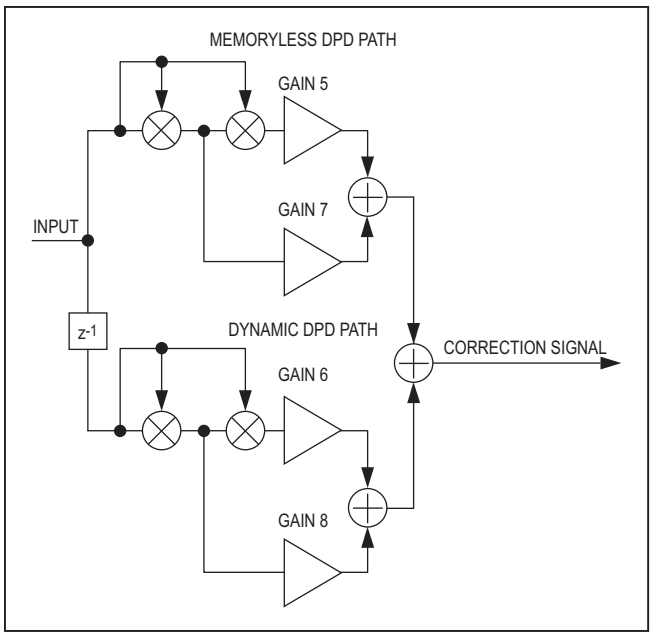


Figure 14. PA DPD Block Diagram (Correction for HD2/IM2, HD3/IM3 with Memory Effect)

- $f_{DAC}/2$ - 2 x f_{OUT} DPD: This block allows for the correction of $f_{DAC}/2$ - 2 x f_{OUT} spur. The block diagram of this section is shown in Figure 15.

Using the SPI interface, program the gain for all DPD paths and delays for the paths as indicated in the previous block diagrams. Table 5 provides a summary of the programmable parameters, ranges, and resolution. Review the *Register Descriptions* section for programming information.

The DAC interleaving compensation shown in Figure 13 contains two paths. Interleaving compensation adjusts for gain errors of every other sample, caused by either actual DC gain error or by clock duty-cycle error. The uppermost data path in this figure corrects for clock duty-cycle error. A duty-cycle error causes an error in the boundary between two samples that is proportional to the step size. In the uppermost data path, the step size is extracted and then every other step is extracted and scaled. The phase-correction filter aligns the phase of the correction signal with the transition between two adjacent samples. The lowermost data path in Figure 13 extracts every other sample of the input signal and scales the input signal using the Gain 1 parameter. When added into the signal path, a gain adjustment for every other sample results.

The PA DPD block (Figure 14) corrects for second- and third-order distortion products in the DAC and following amplifiers that result from squaring or cubing of the input signal and also terms that are dependent on the slew rate of the signal. Using this block, distortion products represented by the diagonal kernel of a Volterra series can be corrected.

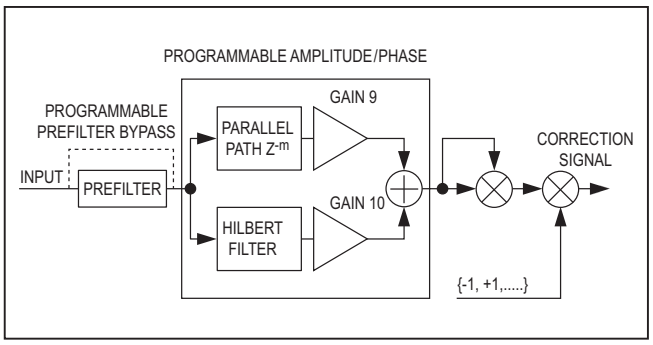


Figure 15. $f_{DAC}/2$ - 2 x f_{OUT} DAC DPD

Table 5. DPD Parameters Range and Resolution

PARAMETER	RANGE	RESOLUTION
Delay 1	0–15	1 DAC sample
Delay 2	0–15	1 DAC sample
Delay 3	0–9	1 DAC sample
Gain 1	±1/8	12 bits
Gain 2	±1/8	12 bits
Gain 3	±1/512	12 bits
Gain 4	±1/512	12 bits
Gain 5	±1/32	12 bits
Gain 6	±1/32	12 bits
Gain 7	±1/32	12 bits
Gain 8	±1/32	12 bits
Gain 9	±1/32	8 bits
Gain 10	±1/32	8 bits

The $f_{DAC}/2$ - 2 x f_{OUT} DPD block (Figure 15) includes a bypassable prefilter with a nonlinear phase response that approximates the characteristics of the MAX5862's RF-DAC spur. The prefilter output feeds a Hilbert filter and a parallel path, which produce -90° and 0° phase shifts, respectively. A weighted sum of these two is squared and modulated with ±1 to calculate the block's DPD output. The modulation pattern is programmable and can start with either +1 or -1 for the first output sample, and alternates for the rest of the seven output samples from the DPD. The Hilbert filter is scaled by the gain coefficient Gain 10, and the parallel path with 0° phase shift is scaled by the gain coefficient Gain 9.

When the DPD block is in normal functional mode, the latency is Delay 3 clock cycles longer than when the block is in functional bypass mode.

By default after global reset, all gains (Gain 1–Gain 10) default to zero. The DPD block takes 15-bit input signals and removes the LSB to form a 14-bit-wide signal. Gains (Gain 1–Gain 10) need to be configured for the DPD to begin calculations. After reset, Delay 1 = 1, Delay 2 = 12, and Delay 3 = 6. Program these delay registers to the appropriate values if needed. The Delay 3 value is used as it is for $f_{DAC}/2$ - 2 x f_{OUT} DPD block. (Delay 3 + 6) value is used for interleaving compensation DAC DPD. (Delay 3 + 6 + 1) is used for both PA DPD and undistorted signal passing to the output. The maximum value of Delay 3 that can be programmed is 9; any higher number defaults to 9.

DPDCFG Register Bit Explanation (Address 0x081)

- SIGN_f_{DAC}_by 2_2f_{OUT}: This bit sets the sign of the $f_{DAC}/2$ - 2 x f_{OUT} compensation.
- PREFILT_BYPASS: Controls the prefilter bypassing in $f_{DAC}/2$ - 2 x f_{OUT} branch. When set to '1', the prefilter is bypassed.
- DAC_EVEN_SAMP: Used to indicate even sampling programmability to the DPD for nullifying 3rd order IMD and $f_{DAC}/2$ - 3 x f_{OUT}. A '0' on this bit indicates odd sample programmability. i.e. odd samples are taken and repeated in the place of even samples in DAC dpd. Output from the zero order hold in the DAC DPD looks like: sample1, sample1, sample3, sample3, sample5, sample5, sample7, sample7, etc. A '1' on this bit indicates even sample programmability. Output from the zero order hold in the DAC DPD looks like: sample0, sample0, sample2, sample2, sample4, sample4, sample6, sample6, sample8, sample8, etc. Default is odd sample programmability.
- BYPASS: Setting this bit is the same as setting all DPD gains to 0.

Synthesizable Bandwidth vs. Clock Rate

The DSP receives a clock from the DAC with frequency f_{CLK} equal to 1/2 the DAC clock rate. The bandwidths stated elsewhere in this data sheet can be synthesized with a clock frequency of 1024MHz or higher. The bandwidth of all the filters behind the resampler is proportional to the clock rate. A clock rate higher than 1024MHz results in a higher synthesizable bandwidth. The synthesizable bandwidths, taking the clock rate into account, are:

- Octal-channel combiner: 48MHz x f_{CLK}/1024MHz
- 32-channel combiner: 192MHz x f_{CLK}/1024MHz
- Continuous bandwidth that channels can be placed in: 192MHz x f_{CLK}/1024MHz
- Maximum bandwidth that channels can be placed in: 950MHz x f_{CLK}/1024MHz

SPI Interface

The MAX5862 contains a slave SPI interface. Data transfers are initiated by the master, which generates the SCLK and $\overline{SS}$ signals. The MAX5862 receives serial data on SDI and transmits serial data on SDO. SDO remains in high impedance except when the MAX5862 is transmitting data to the bus master. The addressing of the SPI port is accomplished using the $\overline{SS}$ select signal. Drive $\overline{SS}$ high between SPI commands.

SCLK frequency must be no higher than that of DATACLK/6 (up to the SPI maximum frequency of ~60MHz). DATACLK must be active during SPI read/write operations. SCLK can be discontinuous. Timing for the SPI interface is shown in Figure 16.

SPI Command Format

The SPI command consists of a read/write bit, a 12-bit address field, an idle bit, and a 16-bit data field. Set the read/write bit to logic 1 for reads and logic 0 for writes. The idle bit is not decoded so it can be set to either 0 or 1. Drive $\overline{SS}$ to logic 0 (selected) at the beginning of a frame, and set to logic 1 (deselected) at the end of the frame. Read/write data is always 16 bits wide.

Write Command

Set the read/write bit to logic 0 for an SPI write. Figure 17 shows the write command waveform. SDO maintains a high-impedance state during write operations.

Read Command

Set the read/write bit to logic 1 for an SPI read. Figure 18 shows the read command waveform. After receiving the idle bit, SDO switches from a high-impedance state to outputting the requested 16-bit data. SDI and SDO can be connected together if a 3-wire interface is desired.

Global Reset

The external global reset input $\overline{RST}$ clears all registers and flip-flops in the design (except JTAG). Global reset may be applied and removed asynchronously.

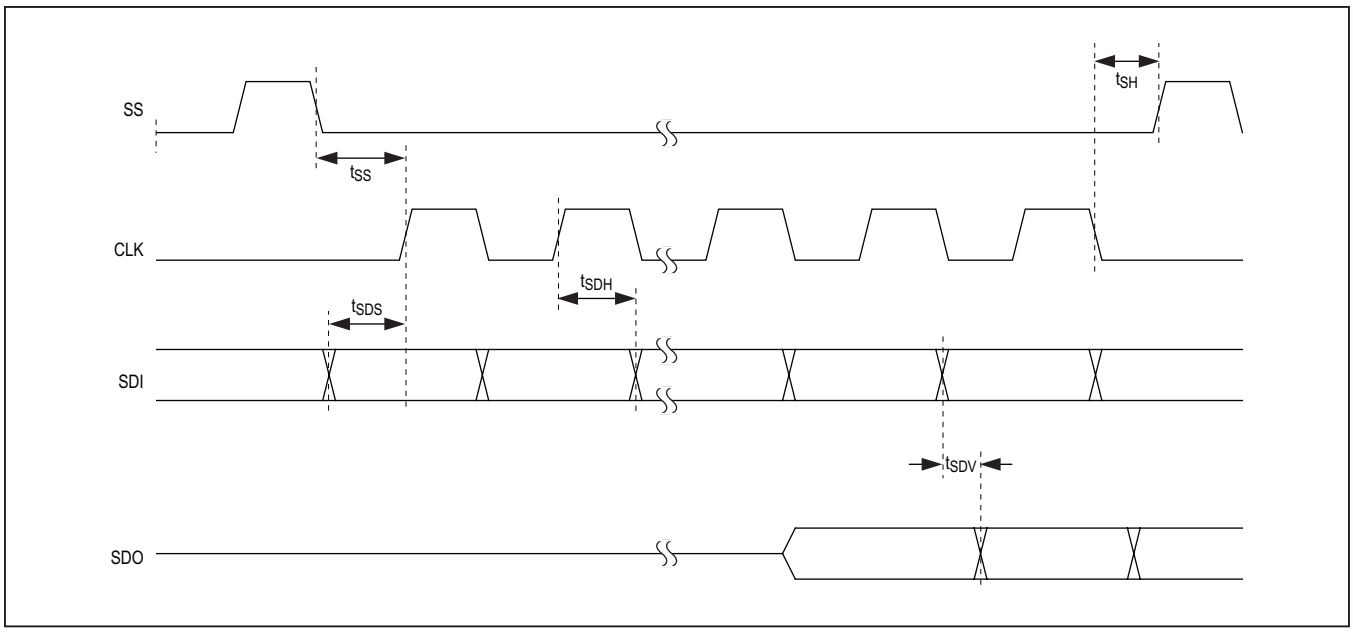


Figure 16. SPI Timing Diagram

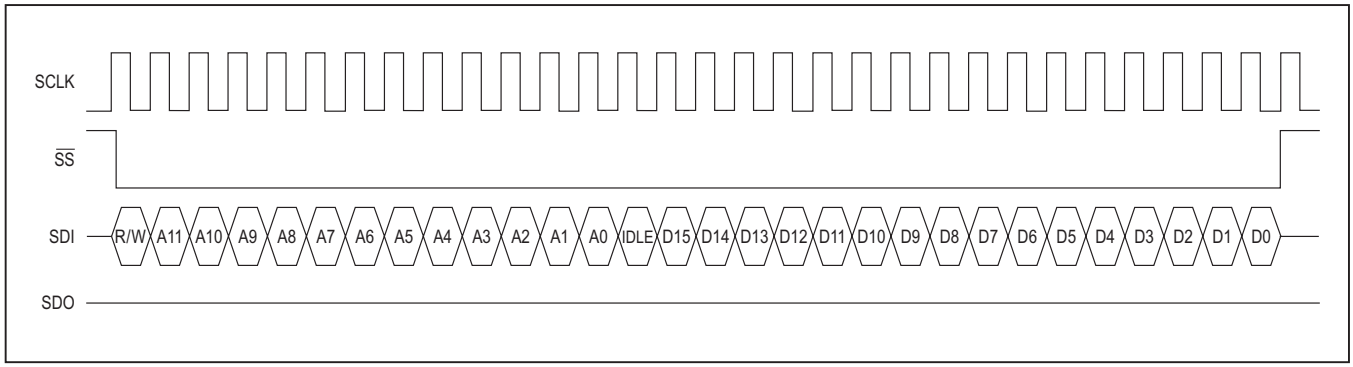


Figure 17. SPI Write Waveform

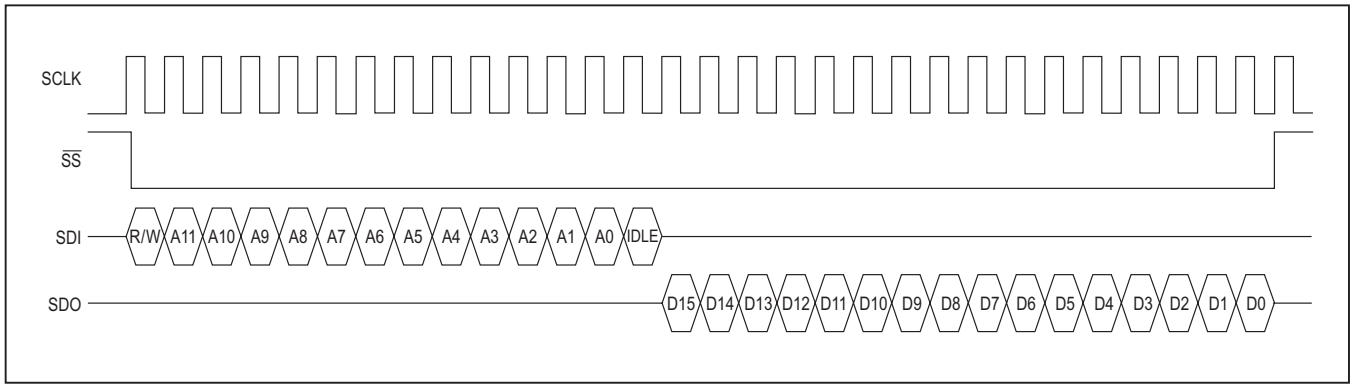


Figure 18. SPI Read Waveform

Interrupts

All interrupt functions are enabled after reset by default; however, disabling the interrupt bit disables all interrupts. The interrupt flag is active-low. The interrupt flag is for information purposes only and does not otherwise affect the operation of the device. Interrupts cannot be disabled for individual active channels. In normal operation, the interrupt flag remains at logic 1 (inactive).

The interrupt output signals a condition of degraded performance of the system. Following the detection of a logic 0 on the interrupt output, read the interrupt source register to determine the source. There are channel status registers to track an overflow or underflow to a specific channel.

FIFO Overflow

Each of the 32 active channels features a 16-word-deep FIFO. The channel RDYA signal asserts high when the FIFO is accepting data, and asserts low to signify when the port stops writing data. The RDYA signal asserts high when the FIFO count indicates that fewer than seven register locations are available. As a system-timing buffer, data writes are accepted by the FIFO when the RDYA signal is low. When the FIFO is full and a write occurs, the interrupt bit of this channel is set and the interrupt flag is asserted logic 0 to signify the loss of data.

Each channel has an individual bit to signify an overflow condition. The bit is edge-detected and resets when the overflow channel status register is read. Muted channels cannot set a channel FIFO overflow flag bit.

FIFO Underflow

Each of the 32 active channels features a 16-word-deep FIFO. The channel accepts data from the FIFO as needed at a rate commensurate with the symbol rate for that specific channel. When a channel is ready for the next symbol, it issues a read to the FIFO. When the FIFO stored word count is 0 and a read occurs, the interrupt bit for this channel is set and the interrupt flag is asserted low to signify a symbol is unavailable when requested by the channel. Each channel has an individual bit to signify an underflow condition. The bit is edge-detected and resets when the underflow channel status register is read. Muted channels cannot set a channel FIFO underflow flag bit.

Channel Capacity

The device is available with factory-set channel capacities of 32 channels or less. For QAM capacity greater than 32 channels, refer to the MAX5860 data sheet.

Power Monitor Timer

The power-monitor block contains a counter that times the interval over which data collection occurs. An interrupt is generated once the counter counts down to zero. At that time the power-monitor registers can be read through the SPI interface.

Interrupt Tree

Figure 19 shows the device interrupt tree. The interrupt-flag enable bit is located as part of the global configuration register. System interrupts are FIFO overflow, FIFO underflow, output test mode enabled, and power-monitor timer.

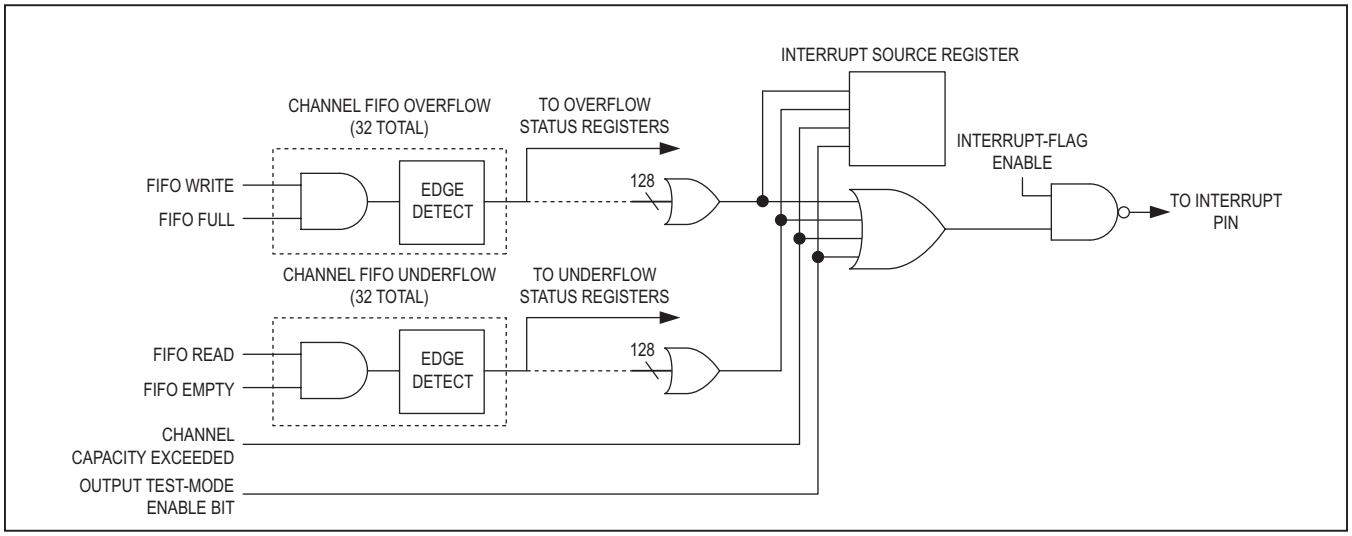


Figure 19. Interrupt Tree Diagram

Applications Information

Grounding, Bypassing, Power Supply, and Board-Layout Considerations

Grounding and power-supply decoupling can strongly influence the performance of the MAX5862. Unwanted digital crosstalk may couple through the input, reference, power supply, and ground connections, affecting dynamic performance. Proper grounding and power supply decoupling guidelines for high-speed, high-frequency applications should be closely followed. This reduces EMI and internal crosstalk that can significantly affect the dynamic performance of the MAX5862.

Use of a multilayer PCB with separate ground and power-supply planes is required. It is recommended that the analog output and the clock input are run as controlled-impedance microstrip lines on the top layer of the board, directly above a ground plane, and that no vias are used for the clock input (CLKP, CLKN) and the analog output (OUTP, OUTN) signals. Depending on the length of the traces, and the operating condition, a low-loss dielectric material (such as ROGERS RO4003) as the top-layer dielectric may be advisable.

The MAX5862 high-speed DAC section supports three separate power-supply inputs for analog 3.3V (AVDD33), switching (AVDD18), and clock (AVCLK) circuits. Each AVDD33, AVDD18, and AVCLK input should at least be decoupled with a separate 47nF capacitor as close as possible to the input and their opposite ends with the shortest possible connection to the corresponding ground plane, to minimize loop inductance. All three power-supply voltages should also be decoupled at the point they enter the PCB with tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi-network could also improve performance.

The MAX5862 digital section supports four separate power-supply inputs for the core 1.0V (V_{DD10}), CMOS (V_{DD18}), LVDS (V_{DD18L}), and DLL (V_{DDDLL}) circuits. Each V_{DD10}, V_{DD18}, V_{DD18L}, and V_{DDDLL} input should at least be decoupled with a separate 47nF capacitor as close as possible to the input and their opposite ends with the shortest possible connection to the corresponding ground plane, to minimize loop inductance. All three power-supply voltages should also be decoupled at the point they enter the PCB with tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi-network could also improve performance. Recommended decoupling on the V_{DD10} includes 0.22µF, 0201 package capacitors. Pins from the MAX5862 V_{DD10} and GND can be used as sense lines into the supply. See the *Ball Description* section for appropriate pin selection.

LC Resonator for DATACLK

Additional timing margin can be gained for the DUC to DAC interface by adding a parallel LC resonator across the DATACLKP/N pins. This circuit brings the duty cycle of the clock close to 50%. For the DATACLK frequency of 1.152GHz, this circuit uses a 6.8pF capacitor (Johanson EIA0402 500R07N6R8CV4T) and a 1.3nH inductor (Murata EIA0402 LQW15AN1N3C10) in parallel. The addition of this circuit as close as possible to the DATACLKP/N pins is recommended.

Output Coupling

The differential voltage between OP and ON can be converted to a single-ended voltage using a transformer or a differential amplifier configuration. The DAC outputs should be pulled up to AVDD33. It is recommended to use bias tees built from discrete inductors and capacitors for the pullups. Two recommended output circuit configurations are shown in Figure 20. To achieve the maximum bandwidth, minimize the inductance in the ground lead on the secondary side of the transformer. Use a very short trace and multiple vias for the connection to the ground plane.

Configuration

The configuration of the device can be simplified by using the configuration Perl scripts included in the MAX5862 Evaluation Kit software package. The Perl scripts located under the MAX5862ConfigurationScripts directory can assist in generating register configurations to load into the MAX5862. These files provide both a very high level definition and a lower level definition file. The highest level is the gen_inp_cfg Perl file. This file has basic inputs to generate a simple configuration of defined channel count, QAM mapping, center frequency and data rate. An examples call to this Perl script could look like the following:

“perl gen_inp_cfg.pl -NOC 1 -ANNEX B -QAM 256 -DDR -PRBS -MAX_TS 2 -Z 450 -BCF 600e6 -OPF 001DB256_5862_PRBS_4608M_600M_cfgen.txt” or “perl gen_inp_cfg.pl -NOC 1 -ANNEX A -M 869 -N 1280 -QAM 256 -SDR -PRBS -MAX_TS 2 -Z 450 -BCF 600e6 -OPF 001SA256_5862_PRBS_4608M_600M_cfgen.txt”

where -NOC is number of channels, -ANNEX and -QAM is modulation and mapping settings, -SDR or -DDR is the input single or double data rate, -PRBS will use the internal PRBS generator for data, -MAX_TS defines the input interface maximum time slot setting, -Z defines the data rate (10.24MHz x 450 = 4608MHz), -M and –N define the

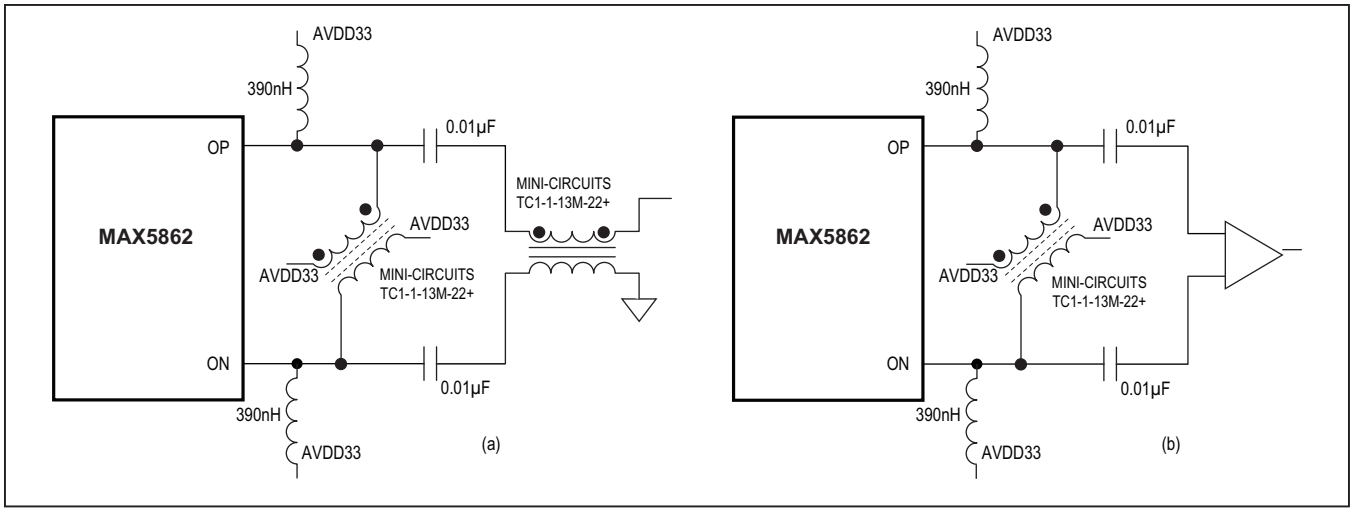


Figure 20. Balun Transformer Output (a) and Amplified Output Configuration (b)

symbol rate, -BCF is the center frequency and the -OPF generates the output file with the name specified.

The gen_inp_cfg perl script will generate a file that is then the input to the gen_spi_cmd Perl script, which determines the register bit settings. The call to this Perl script file might look like the following:

"perl gen_spi_cmd.pl 001DB256_5862_PRBS_4608M_600M_cfgen.txt> 001DB256_5862_PRBS_4608M_600M.txt" or "perl gen_spi_cmd.pl 001SA256_5862_PRBS_4608M_600M_cfgen.txt> 001SA256_5862_PRBS_4608M_600M.txt"

where 001DB256_5862_PRBS_4608M_600M.txt and 001SA256_5862_PRBS_4608M_100M.txt would be the output files to load into the MAX5862 device through the SPI interface.

If desired, the configuration can begin at the lower level of detail. But initially it is easiest to generate the basic files with the gen_inp_cfg script, followed by the gen_spi_cmd script. The gen_spi_cmd file will generate a list of SPI addresses and data in hexadecimal format to be written to the MAX5862 using the MAX5862 software controller. There are more details in the Readme.txt file in the MAX5862ConfigurationScripts directory.

Application Note 5673: *MAX5860/MAX5862 Usage and Configuration Guide* is available to assist in configuring the MAX5862.

Channel Center Frequency

The center frequency of each channel is configured by setting the four NCOs involved in the channel combining process. Each channel goes through the 4 stages of channel combining process so four NCOs will need to be configured to get the correct center frequency for each channel. Although only 32 channels can be active, there is an NCO associated with each channel (128 total), 16 NCOs for octave channel combining, four NCOs for block level combining process and a single NCO for the entire 128 channels block's modulation. Table 6 lists the resolution and control word width used to calculate the output frequency of each NCO.

All of the control words should be written in a 'signed magnitude' format. There can be many combinations to generate the same center frequency. The Application Note 5673: *MAX5860/MAX5862 Usage and Configuration Guide* is available to assist in configuring the MAX5862.

Optimizing Channel Power

To get the best performance from the MAX5862, each channel's power must be balanced. The power contribution through each channel depends on the channel symbol sequence and carrier signal's value. If gains are set too high, saturation in the filters and other blocks may occur. If it is set too low, then the signal-to-noise ratio will be degraded. Table 7 lists the suggested gains to set this balance. The balancing of gains with respect to channel count can be seen in the G2 gain values. The G2 values will change according to the number of active channels within the MAX5862 device but are independent of modulation and QAM mapping selections. Table 8 shows the full gain table for Annex B, 256-QAM mapping mode, optimizing the internal data path width in the device. Multichannel configurations may be subject to adjustments for optimum performance.

Table 6. NCO Output Frequency Table

TYPE	FREQ RESOLUTION	CONTROL WORD SIZE	OUTPUT FREQ RANGE.
NCO1	$f_{DAC}/(2^{\wedge}25)$	19 bits	$\pm f_{DAC}/128$
NCO2	$f_{DAC}/(2^{\wedge}25)$	21 bits	$\pm f_{DAC}/32$
NCO3	$f_{DAC}/(2^{\wedge}22)$	20 bits	$\pm f_{DAC}/8$
NCO4	$f_{DAC}/(2^{\wedge}22)$	21 bits	$\pm f_{DAC}/4$

Table 7. Gain Registers

NO. OF CHANNELS	GAIN1 11 BITS	GAIN2 8 BITS	GAIN3 8 BITS	GAIN4 8 BITS	GAIN5 8 BITS
1	0x28A	0xFE	0xFE	0xFE	0xFE
2	0x28A	0xA1	0xFE	0xFE	0xFE
4	0x28A	0x66	0xFE	0xFE	0xFE
8	0x28A	0x48	0xFE	0xFE	0xFE
16	0x28A	0x2D	0xFE	0xFE	0xFE
32	0x28A	0x20	0xFE	0xFE	0xFE

Note: *All the gain values must be positive numbers and only the 'magnitude bits' are written to the respective registers. This table shows the gain settings for Annex B, 256-QAM.*

Table 8. Gain Settings for Modulation and QAM Mapping Selection

ANNEX B 64-QAM	ANNEX B 256-QAM	ANNEX C 64-QAM	ANNEX C 256-QAM	
G1 = 0x2B9 G3 = 0xFE G4 = 0xFE G5 = 0xFE	G1 = 0x28A G3 = 0xFE G4 = 0xFE G5 = 0xFE	G1 = 0x2B9 G3 = 0xFE G4 = 0xFE G5 = 0xFE	G1 = 0x28A G3 = 0xFE G4 = 0xFE G5 = 0xFE	
ANNEX A 16-QAM	**ANNEX A 32-QAM**	**ANNEX A 64-QAM**	**ANNEX A 128-QAM**	**ANNEX A 256-QAM**
G1 = 0x32E G3 = 0xFE G4 = 0xFE G5 = 0xFE	G1 = 0x49F G3 = 0xFE G4 = 0xFE G5 = 0xFE	G1 = 0x2B9 G3 = 0xFE G4 = 0xFE G5 = 0xFE	G1 = 0x422 G3 = 0xFE G4 = 0xFE G5 = 0xFE	G1 = 0x28A G3 = 0xFE G4 = 0xFE G5 = 0xFE

Table 8 shows the appropriate settings for the G1, G3, G4, and G5 configuration bits. These settings are not affected by the channel count, but the G1 setting can be optimized based on the desired modulation and QAM mapping selection.

Channel Modifications

A clean technique for adding a channel or changing a channel's settings without disturbing the spectrum is by using the gain settings. Setting the G1 and G2 of a channel to zero will eliminate the signal from the spectrum. The channel's other settings, such as the LF and KF, can then be set or modified without interruption to the spectrum. After the other configuration parameters are set and loaded, then the G1 and G2 can be set appropriately and the channel will appear in the spectrum as configured.

Spectral Considerations

DOCSIS 3.0 Spurious Emissions Requirements

The DOCSIS 3.0 DRFI (Downstream Radio Frequency Interface) specification [2] places stringent requirements on a DAC to be used for direct synthesis. It limits spurious emissions in the entire band from 47MHz to 1006MHz.

DAC Sample Rate Selection

The 4.6Gsps maximum sample rate of the MAX5862 allows flexibility in system design. Several trade-offs exist in terms of sample rate versus performance or circuit complexity, and these should be considered when selecting the DAC sample rate.

An attenuated image of the desired DAC output is present at $f_{DAC}/2 - f_{OUT}$ due to the DAC output updated on both edges of the clock. The DAC update rate must be at least four times higher than the highest frequency generated to keep this image outside of the cable band. Since DOCSIS defines the upper frequency as 1006MHz, the minimum DAC sample rate, to keep this spur out of band, is 4024Msps. In many cases, a lowpass filter will be required to further attenuate this image. As the DAC sample rate is reduced towards the lower requirement, the design of the filter becomes increasingly difficult. However, there are several potential advantages to using lower sample rates. First, the overall spurious performance of the MAX5862 improves as the sample rate is reduced from the 4.6Gsps maximum towards 4.0Gsps. Second, the power requirement for the system solution should be lower; the MAX5862 dissipates approximately 15% less power at 4.0Gsps versus 4.6Gsps. Another consideration is that timing margins are reduced at higher sample rates and may be more difficult to meet.

Harmonic Distortion

The MAX5862 features low harmonic distortion. Second harmonic distortion (HD2) and third harmonic distortion (HD3) are usually the dominant harmonics, and they increase with increasing output frequency. The frequency of HD2 is below 1GHz for frequencies below 500MHz and the frequency of HD3 is below 1GHz for output frequencies lower than 333MHz.

Harmonics of Images Around the Clock Frequency

The MAX5862 has a spur at $f_{DAC}/2 - 2 \times f_{OUT}$. This spur is lower than the DOCSIS limit for channel counts greater than 8 but may violate DOCSIS for lower channel counts and high output frequencies. This spur is coincident with f_{OUT} for $f_{OUT} = f_{DAC}/6$. This spur can be corrected with the use of the internal DPD.

Latency

The device symbol latency is variable since the CLK frequency is not required to be frequency-locked to the symbol rate. Achieving the proper symbol rate in the device causes the ratio of KF/LF to be a noninteger value, which in turn forces the device to make periodic adjustments to average the KF/LF rate. This adjustment appears every certain number of symbol clocks as one CLK_D16 clock difference in the symbol rate (relatively either +1 or -1 CLK_D16). One CLK_D16 is 32 CLK periods.

For example, in the case of KF/LF = 869/1000, four symbols have one latency value and the next five symbols have a one CLK_D16 latency value difference. This relative sequence is cyclic and would continue to repeat.

The total latency through the device depends on the many parameters (i.e., the maximum time-slot value programmed for the input interface, time-slot selection for each channel, the port clock, KF and LF values, and individual programmable delay stage parameters). The input interface uses an asynchronous clock for capturing the input data and for FIFO loading. It is impossible to define an equation to calculate the latency through the input block. Latency is therefore defined from the point a symbol is read by the ARR to the output of the device. Since symbols are upsampled as many as 512 times by the device during processing, the center sample at the output is taken as the reference point for this calculation. The following equation defines the latency through the device in terms of CLK clock periods:

Latency = [(lat_sym x 512) + lat_cc ± 512] + lat_DAC

Where:

lat_sym = (12480 + (256 x D1) + (128 x D2) + (64 x D3) + D4)/(KF/LF)

lat_cc = 19968 + (512 x D5) + (256 x D6) + DPD_D3

lat_DAC = 11

D1 through D6 are the user-selectable delay values for the channel-combiner path.

DPD_D3 is the programmable delay for DPD (default value of 6 DATACLKs which is 192 CLKs).

The parameter lat_unc is the uncertainty due to the division by LF in the ARR and is equal to one CLK_D16 (16 DATACLK cycles or 32 CLK periods). When a symbol's sampling rate is changed from the symbol rate to the internal MAX5862 output sampling rate, an adjustment to the data read rate from the FIFO to the ARR occurs dynamically to maintain the target symbol rate (LF and KF values). This uncertainty would be reduced to zero if the 1/(LF/KF) ratio became an integer value.

Parameter lat_DAC is the latency through the high-speed DAC.

User Configurable Delays

User-configurable delays are present in the design. Each individual channel block (of which there are 128) has three configurable delays:

– D1: 0 to 12 symbol periods (selectable)

– D2: 0 or ½ symbol period

– D3: 0 or ¼ symbol period

Each 8 channel combiner (of which there are 16) has two user-configurable delays:

– D5: 0 or 1 DATACLK/16 clock period

– D6: 0 or 1 DATACLK/8 clock period

The DPD has three user-configurable delays:

– D1: 0 to 15 DATACLK/2 periods (default 1)

– D2: 0 to 15 DATACLK/2 periods (default 12)

– D3: 0 to 15 DATACLK/2 periods (default 12)

One DATACLK = 2 CLK periods.

Symbol Timing Alignment (Synchronization)

Aligning Multiple Channels Within a Single MAX5862

The MAX5862 allows symbols in groups of multiple (same symbol rate) channels to be exactly time-aligned. Within an individual MAX5862, timing alignment of channels requires no external FPGA and will have zero skew. No internal mechanism is provided to allow byte order alignment of data; however, it is possible for the user to byte-align data by careful manipulation of input port timing and the transfer of data. If channels are muted after synchronizing, synchronization is lost; therefore, it is recommended that the channel gain be set to 0 after synchronization rather than muting a channel.

A group of FIFOs can be configured via SPI commands and by using the MODE2 pin to release read pointers and synchronize reads at exactly the same time. Without using this configuration method, a group of unsynchronized FIFOs could spread their symbols across two symbol time slots.

It may be desirable to synchronize all of the channels in one operation at startup. The unused channels would have their G1/G2 (and possibly G3) gains set to zero. G1 and G2 are channel gains for the specific channel, and G3 is the gain for the associated 8 channel combiner. When removing channels, these gains would also be set to zero. This allows all of the channels to maintain exact synchronization. Figure 21 indicates the use of the MODE2 pin for synchronization.

Aligning Channels Across Multiple MAX5862 Devices

Multiple symbol rate groups can also be time-aligned within a tolerance across separate MAX5862 devices. Timing alignment over multiple devices is achieved by use of external logic. The MAX5862 does not source time-alignment signals, but rather it responds to input control signals. This configuration avoids the complexity of a master-slave system and avoids reliability issues.

Figure 21 is an example of a symbol time-alignment implementation for multiple MAX5862 devices. The FPGA sources the timing-alignment control signals for the channel symbol groups and multiple devices. There are no feedback signals from the MAX5862 to the FPGA. DUC1 would be an operational MAX5862 and DUC2 would be the MAX5862 being brought on-line and into synchronization.

The FPGA contains mirrors of the MAX5862 KF/LF symbol rate generators which are driven by the d16m signal. The accuracy of the synchronization depends on how closely the d16m signal mirrors the MAX5862 internal clk_d16 clock. The phase and frequency of the d16m clock is dependent upon the quality of the input HSCLK, the best choice being the DAC clock or the DAC DATACLK. Timing alignment is possible with less skew than two clk_d16 clock periods (~30ns or less) when using a quality clock.

There would be a symbol rate (KF/LF) generator in the FPGA for each symbol rate being aligned in the MAX5862 devices. The zero-count signals from the generators would be muxed via logic to the desired MAX5862 at the appropriate times.

The reset signals from the FPGA ($\overline{RST1}$ and $\overline{RST2}$) attaches to the global reset ($\overline{RST}$). The global reset aligns the skew and phase of the internal clocks of the MAX5862 device being brought on-line. An already-operational MAX5862 would not have its global reset toggled, as all configuration registers would be cleared.

The MODE2 input receives the zero-count signal. MODE2 is synchronized and rising-edge detected using the internal clk_d16 clock. Alignment of symbol rate generators to the MODE2 input is selectively configured via SPI commands.

A general setup procedure for a MAX5862 being brought into alignment would be:

1) Power up the MAX5862 being brought online. Start clocks (PCLK, DATACLK).

2) FPGA provides new MAX5862 with hardware reset.

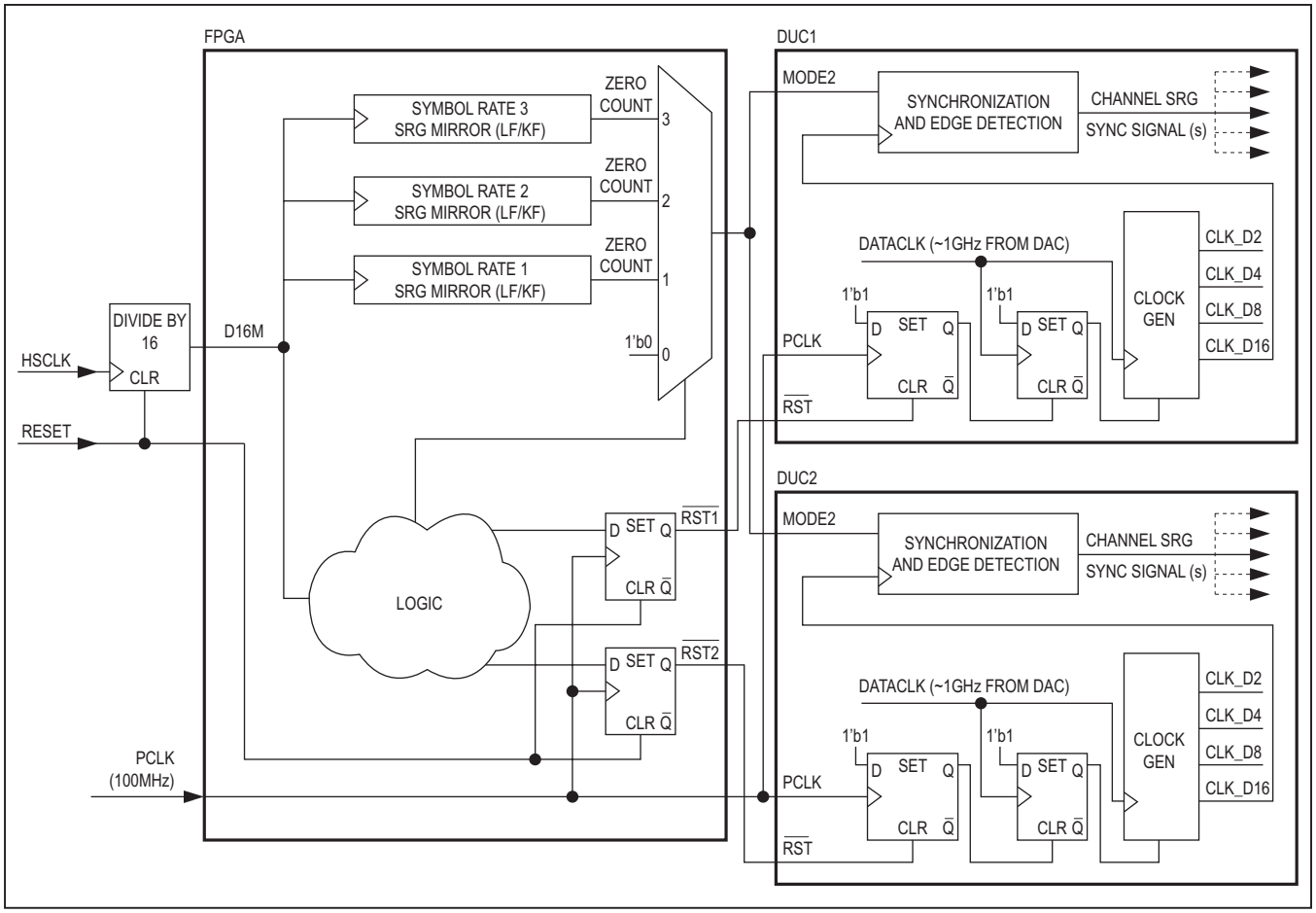


Figure 21. Symbol Time-Alignment Functional Block Diagram

3) Configure the MAX5862:
   - Turn on gated clocks at 32-channel block level.
   - Unmute channels
   - Configure each channel (port, slot, mute, LF, KF....)
   - Configure frequency map.
   - Enable selected channels for synchronization.
4) Configure FPGA:
   - Configure internal symbol rate generator (LF/KF).
   - Turn off data to the MAX5862 (force port VALIDA low).
   - Generate sync pulse to align FPGA SRGs and MAX5862 SRGs.
   - Pulse MODE2 aligned to the d16m clock domain (The NCOs, global LF/KF network and FIFO reset network will be aligned by reset).
   - Wait a few clocks for the reset pulse to propagate.
   - Enable PSYNC, data, and port valid signals to DUC. Send at least 8 words consecutively to all channels during the next 8 symbol periods to ready the FIFOs.
   - Send symbol data as required based on MAX5862 handshaking signals.
5) Configure DUC:
   - Disable global FIFO reset enables.
   - Remove ext_dds_load enable.
6) Let the MODE2 sync pulse free run.
7) Configure some other symbol rate (LF/KF):
   - Repeat step 4 and 5 for those channels.

Power Reduction

Significant power reduction can be achieved if a smaller number of channels are used and frequency agility is limited.

Lowest Standby Power

The lowest standby power for the MAX5862 may be achieved by holding the external global reset input $\overline{RST}$ at logic 0 (active). Holding the hardware reset pin at logic 0 will stop the internal clock dividers from operating, and therefore it will remove most dynamic power from the device. The major power component will be static power with a minor contribution from the logic driven by the master clock and standby power from the DLL block.

Since the MAX5862 configuration registers are cleared by $\overline{RST}$, the device must be reconfigured after global reset is removed.

Channel Muting

Power may be reduced by muting unused channels. When a channel is muted, the clock is turned off to symbol interface block. This includes the circuitry from the D1_delay block to the MOD1 block.

Another way to minimize channel power is to set individual channel gain controls 1 and 2 to zero. This reduces data toggling power to zero but the associated clocks will remain active.

Block Shutdown of 32-Channel Combiners

The MAX5862 has four 32-channel block combiners, each of which may be configured to be turned off for significant power savings. The block includes 32 input channels and the associated four 8-channel combiners. Shutting down a 32-channel combiner will remove the output frequency block of 192MHz.

Individual DPD Branch Shutdown

Each branch of the DPD is active (clocking) after reset. Unused branches of the DPD can be deactivated (remove clocking) to minimize power (register 0x081 bits [10:7]). De-activating all four branches of the DPD can save about 250mW.

Thermal Management

The user should conduct a thorough thermal analysis when designing with the MAX5862 (use of a heatsink may be required). Maintain the proper die temperature (< 110°C) to avoid thermal damage. The MAX5862 has a built-in thermal diode junction that interfaces to an external dual current temperature sensor, such as the MAX6642, for measuring the T_{JDUC}. This sensor allows the user to monitor the die temperature of the MAX5862 and it can also output an over temperature warning signal. The interface circuit is shown in Figure 22. For board layout recommendations, please refer to the MAX6642 data sheet. Refer to the Application Note 5674: *MAX5860/MAX5862 Thermal Model Considerations*.

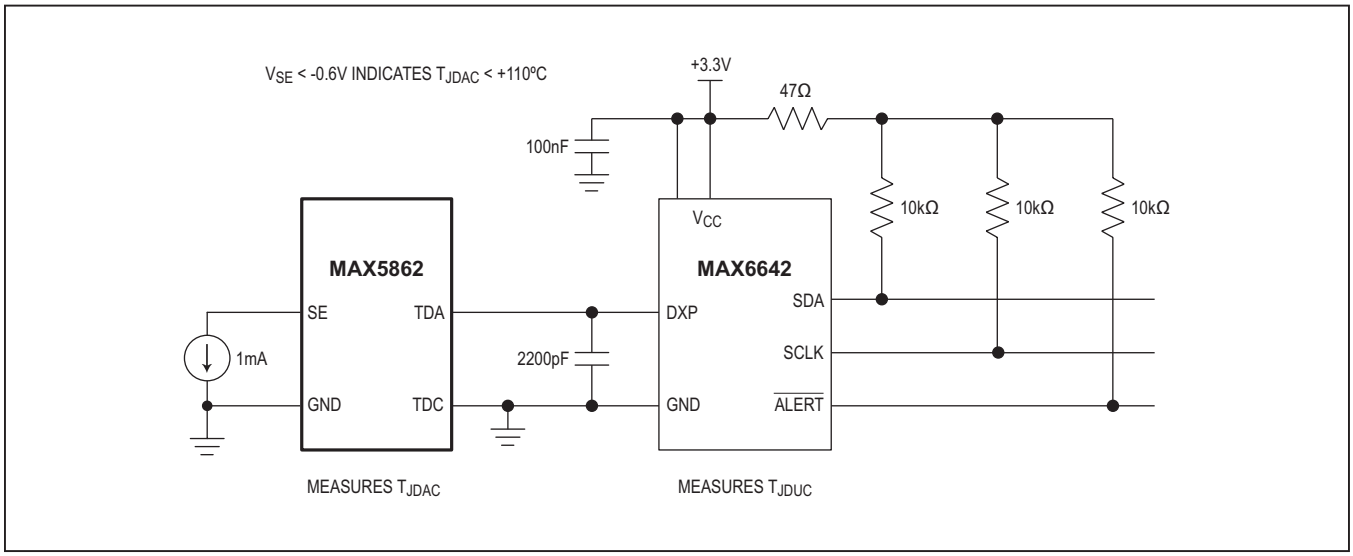


Figure 22. Die Temperature Monitoring Circuits

PRBS Operation

LFSR Operation

The block diagram of the PRBS generator is shown in Figure 23. The generator consists of two LFSRs. The top LFSR is 10 bits long and it is used to generate a uniformly distributed sequence of 10-bit values. The bottom LFSR is 20 bits long and it is used to decorrelate the sequence generated by the first LFSR. The output of the 20-bit LFSR drives the inputs of the XOR gates controlling the polarity of the sequence generated by the first LFSR. The feedback taps in both LFSRs are selected such that they generate maximum length sequences, and there is no need to make the taps programmable.

However, the seed values have to be programmable in both LFSRs. The seed word is 10 bits long for the top LFSR and 12 bits long for the bottom LFSR. The 12-bit seed value should be aligned with the MSBs of the LFSR. This is shown in Figure 24.

The output sequence of the PRBS generator should have a uniform amplitude distribution and a spectral characteristic of white noise.

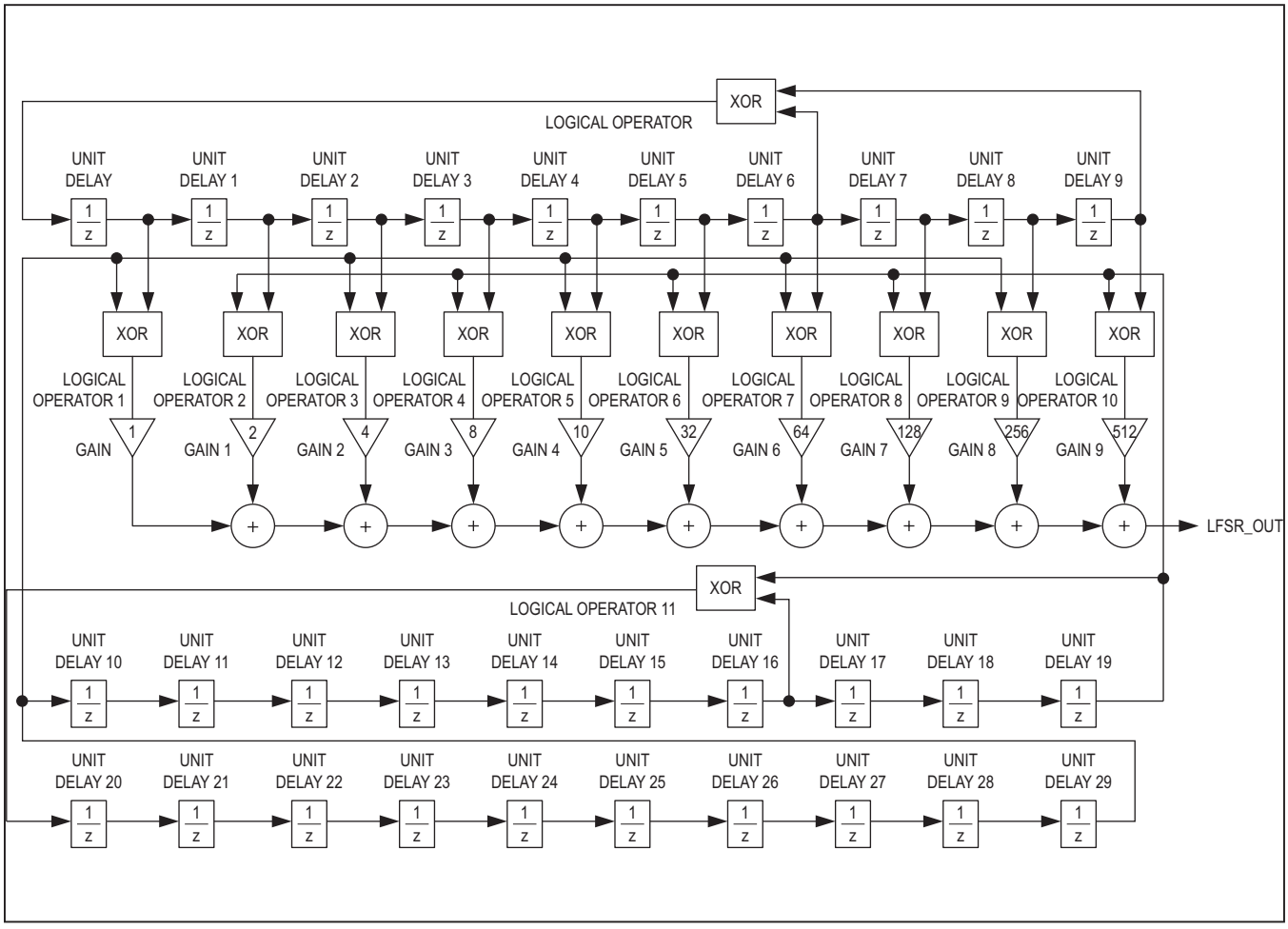


Figure 23. LFSR Block Diagram

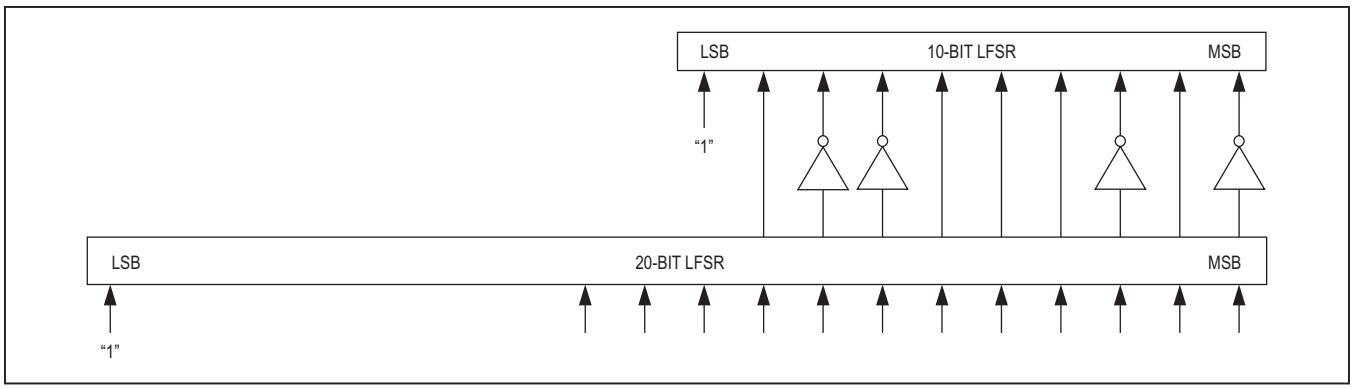


Figure 24. LFSR Seeds

Creating the LFSR Seeds

Figure 24 diagrams the LFSR seeding operation. In picking a seed, the user need only set the 4 d1 select bits (register SYMIF, one per channel) and the 8 bits of the appropriate SEEDA or SEEDB value (PRBS register) so they combine to a unique value for each channel. During PRBS operation, the d1_delay function is not operational.

Detailed operation of the LFSR is now described. To create the seeds internally, the d1 delay register bits (1 set of 4 per channel) are utilized along with the appropriate 8-bit PRBS seeds for each channel.

The seed for the upper 10-bit LFSR is formed according to the following equation:

seed10 = {!d1_select[3], d1_select[2], !d1_select[1], d1_select[0], seed[7], seed[6], !seed[5], !seed[4], seed[3], 1'b1 } where seed[] refers to the appropriate SEEDA or SEEDB register.

The seed for the lower 20-bit LFSR is formed according to the following equation:

seed20 = { d1_select[3:0], SEEDA[7:0] or SEEDB[7:0], 8'b1 };

Manufacturing Test Pins

For end-user applications, the following signal connection rules apply:

- $\overline{TEST}$ and MODE must always be tied logic-high (1.8V)
- TEST and RSETI are connected directly to ground.
- V_{REF} must have a 100pF capacitor to ground (size in 0402 or 0603 is good). Otherwise, instability may be observed in the LVDS outputs and/or in the operation of the DLL.

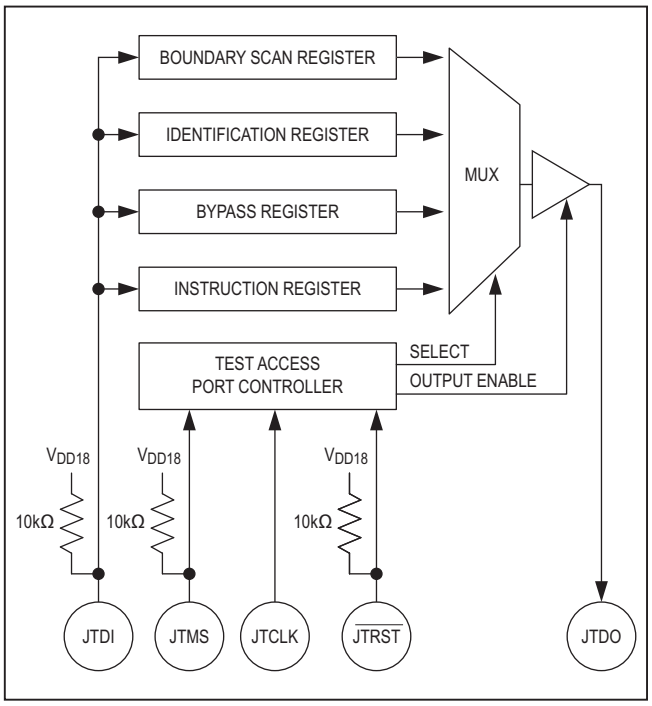


Figure 25. JTAG Block Diagram

JTAG

JTAG Description

The periphery JTAG on the CMOS I/O supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. See Figure 25 for a block diagram. The MAX5862 contains the following items which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register
- Bypass Register
- Boundary Scan Register
- Device Identification Register

The Test Access Port has the necessary interface pins, namely JTCLK, JTRST, JTDI, JTDO, and JTMS. Details on these pins can be found in Section 3 Pin Descriptions. Details on the Boundary Scan Architecture and the Test Access Port can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

JTAG TAP Controller State Machine Description

This section covers the details on the operation of the Test Access Port (TAP) Controller State Machine. See Figure 26 for details on each of the states described below. The TAP controller is a finite state machine which responds to the logic level at JTMS on the rising edge of JTCLK.

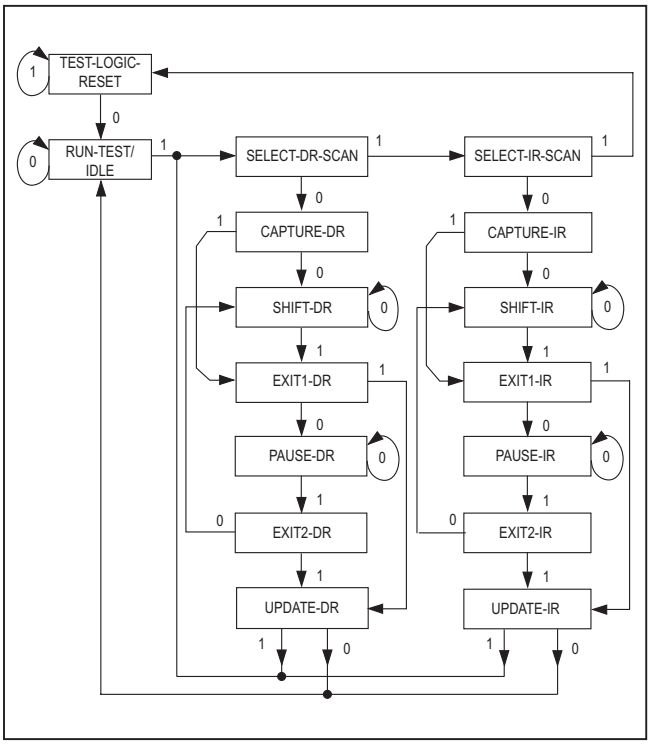


Figure 26. JTAG TAP Controller State Machine

Test-Logic-Reset. Upon power-up of the device, the TAP controller starts in the Test-Logic-Reset state. The Instruction Register contains the IDCODE instruction. All system logic on the device operates normally.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The Instruction Register and Test Register remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR. Data may be parallel loaded into the Test Data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the Test Register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or it to the Exit1-DR state if JTMS is high.

Shift-DR. The Test Data Register selected by the current instruction is connected between JTDI and JTDO and shifts data one stage towards its serial output on each rising edge of JTCLK. If a Test Register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the Test registers is halted while in this state. All Test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the Test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All Test registers retain their previous state. The Instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the Instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the Instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the shift register in the Instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register, as well as all Test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state while moving data one stage through the Instruction shift register.

Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

Pause-IR. Shifting of the Instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high put the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the Instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low, puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

JTAG Instruction Register And Instructions

The Instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage towards the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Instructions supported are shown in Table 9.

SAMPLE/PRELOAD. A mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the Boundary Scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE/PRELOAD also allows the device to shift data into the Boundary Scan register via JTDI using the Shift-DR state.

EXTEST. The EXTEST instruction allows testing of all interconnections to the device. When EXTEST is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins are driven. The Boundary Scan register is connected between JTDI and JTDO. The Capture-DR samples all digital inputs into the Boundary Scan register.

Table 9. JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

BYPASS. When the BYPASS instruction is latched into the parallel Instruction register, JTDI connects to JTDO through the one-bit Bypass Test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation.

IDCODE. When the IDCODE instruction is latched into the parallel Instruction register, the Identification Test register is selected. The device identification code is loaded into the Identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The device ID code always has a one in the LSB position. The device ID code is listed in Table 10.

HIGHZ. All digital outputs are placed into a high-impedance state. The Bypass Register is connected between JTDI and JTDO.

CLAMP. All digital outputs pins output data from the boundary scan parallel output while connecting the Bypass Register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

JTAG Test Registers

IEEE 1149.1 requires a minimum of two Test registers; the Bypass register and the Boundary Scan register. An optional Test register has been included in the device design. This Test register is the Identification register and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Bypass Register. This is a single one-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions, which provides a short path between JTDI and JTDO.

Identification Register. The Identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

Boundary Scan Register. This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is 32 bits in length.

References

[1] ITU-T J.83, Digital multiprogrammed systems for television, sound, and data services for cable distribution (12/2007), download from www.itu.int.

[2] Data-Over-Cable Service Interface Specifications, Downstream RF Interface Specification CM-SP-DRFI-I06-080215, download from www.cablelabs.com.

[3] DVB-C standard: EN 300 429 V1.2.1 (1998-04) Digital Video Broadcasting (DVB); Framing Structure, channel coding and modulation for cable systems, download from www.etsi.org.

[4] Data-Over-Cable Service Interface Specifications, Modular CMTS, DOCSIS Timing Interface Specification, CM-SP-DTI-I04-061222, download from www.cablelabs.com.

Table 10. JTAG ID Code

PART NUMBER	4-BIT VERSION [31:28]	16-BIT PART NUMBER [27:12]	11-BIT MANUFACTURER ID [11:1]	1-BIT MANDATORY [0]
MAX5862	0011	0000000000000011	00011001011	1

Register Descriptions

This list of 93 register tables represents 1818 addresses, 3980 unique bit functions, and a total of 26483 bit assignments. Each 12-bit address references up to 16 bits in each register data field. The address line of each register block may contain a formula for calculating a specific address from a possible range of addresses. The numbering scheme for the channels and combiner blocks is shown in Figure 27.

Configuration of the registers is complex due to the exceptional flexibility of the device and the many system variables which must be considered. A set of Perl scripts are provided with the MAX5862 Evaluation Kit software package or will be provided to the user on request to assist in setting register values for their specific operating conditions. A text file can also be provided with the registers listed individually by address.

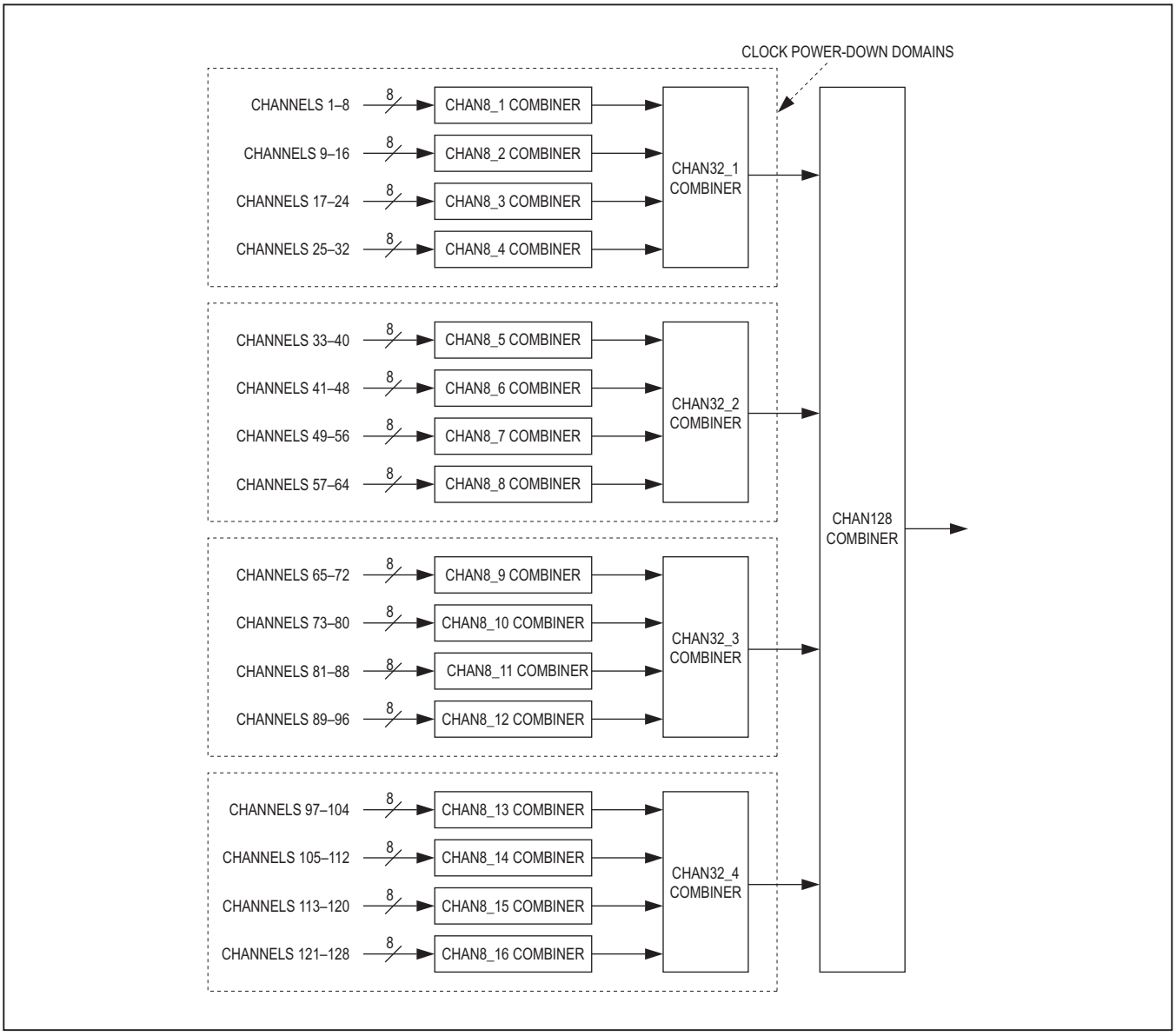


Figure 27. Channel and Block Combiner Numbering Reference

GLOBAL REGISTERS

Table 11. JTAG Register (0x000)

ADDRESS	0x000							
REGISTER NAME	JTAG							
DESCRIPTION	JTAG ID							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	PN[15]	PN[14]	PN[13]	PN[12]	PN[11]	PN[10]	PN[9]	PN[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	PN[7]	PN[6]	PN[5]	PN[4]	PN[3]	PN[2]	PN[1]	PN[0]
DEFAULT VALUE	0	0	0	0	0	0	1	1

PN[15:0] : 16-bit JTAG part number [15:0], read-only

Table 12. GBL_CFG0 Register (0x001)

ADDRESS	0x001							
REGISTER NAME	GBL_CFG0							
DESCRIPTION	General Configuration							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	RSVD	--	SPARE2	SPARE1	REV[3]	REV[2]	REV[1]	REV[0]
DEFAULT VALUE	1	0	0	0	0	0	1	1
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	GBL_PRBS	D6	D5	D4	D3	GBL_FIFO	GBL_KFLF	GBL_FCW
DEFAULT VALUE	0	0	0	0	0	0	0	0

RSVD: Reserved bit.
SPARE2: Spare bit.
SPARE1: Spare bit.
REV[3:0]: Device revision number [3:0].
The revision code for pre-production devices is 0000.
GBL_PRBS: global PRBS enable pulse, self-clearing.
D6: Enable d6 delay enable.
D5: Enable d5 delay enable.
D4: Enable d4 delay enable.
D3: Enable d3 delay enable.
GBL_FIFO: global FIFO reset pulse, self-clearing.
GBL_KFLF: global LF/KF load pulse, self-clearing.
GBL_FCW: global nco load pulse, self-clearing.

DEMULTIPLEXED REGISTERS

Table 13. EXT_SYNC Register (0x002)

ADDRESS	0X002							
REGISTER NAME	EXT_SYNC							
DESCRIPTION	External Sync enable register (MODE2 Pin Timing Sync Functionality)							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	—	—	DSEL[4]	DSEL[3]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	DSEL[2]	DSEL[1]	DSEL[0]	EN_CKDS	EN_PRBS	EN_NCO	EN_LF	EN_FF
DEFAULT VALUE	0	0	0	0	1	1	1	1

DSEL[4:0]: Select for digital test out pin.

0x00	hi-z	High-impedance state (default).
0x01	clk_d16	DATACLK/16.
0x02	syncd_rd_release	FIFO sync'ed release signal.
0x03	mode2_reg	Internally sync'ed MODE2 pulse.
0x04	misr_sample	MISR Sample Clock (Manufacturing Test).
0x05	dll_lock	DLL lock signal.
0x10	rd_1	Channel 1 FIFO read signal.
0x11	rd_9	Channel 9 FIFO read signal.
0x12	rd_17	Channel 17 FIFO read signal
0x13	rd_25	Channel 25 FIFO read signal
0x14	rd_33	Channel 33 FIFO read signal
0x15	rd_41	Channel 41 FIFO read signal
0x16	rd_49	Channel 49 FIFO read signal
0x17	rd_57	Channel 57 FIFO read signal
0x18	rd_65	Channel 65 FIFO read signal
0x19	rd_73	Channel 73 FIFO read signal
0x1A	rd_81	Channel 81 FIFO read signal
0x0B	rd_89	Channel 89 FIFO read signal
0x1C	rd_97	Channel 97 FIFO read signal
0x1D	rd_105	Channel 105 FIFO read signal
0x1E	rd_113	Channel 113 FIFO read signal
0x1F	rd_121	Channel 121 FIFO read signal

EN_CKDS: Enable syncing dataclk clock generator to MODE2 pin.
EN_PRBS: Enable syncing PRBS's using pulse on MODE2 pin.
EN_NCO: Enable syncing NCO's using pulse on MODE2 pin.
EN_LF: Enable loading LF/KF counter using pulse on MODE2 pin.
EN_FF: Enable FIFO reset using pulse on MODE2 pin.

Table 14. CFG Register (0x500)

ADDRESS	0x500							
REGISTER NAME	CFG							
BIT	15	14	13	12	11	10	9	8
NAME	TSTI	SPARE3	SLOTS[5]	SLOTS[4]	SLOTS[3]	SLOTS[2]	SLOTS[1]	SLOTS[0]
DEFAULT VALUE	0	0	0	1	1	1	0	0
BIT	7	6	5	4	3	2	1	0
NAME	SPARE2	RSYNC	SPARE1	SDR	MUTE32_D	MUTE32_C	MUTE32_B	MUTE32_A
DEFAULT VALUE	0	1	0	0	1	1	1	1

TSTI: Test bit to set interrupts.
SPARE3: Spare register bit.
SLOTS[5:0]: Rollover value for slot counter [5:0].
SPARE2: Spare register bit.
RSYNC: Enables internal ready sync generation.
SPARE1: Spare register bit.
SDR: Input mode, 1:single data rate, 0:double data rate.
MUTE32_D: Disables fourth 32-block channel combiner, clocks are gated off.
MUTE32_C: Disables third 32-block channel combiner, clocks are gated off.
MUTE32_B: Disables second 32-block channel combiner, clocks are gated off.
MUTE32_A: Disables first 32-block channel combiner, clocks are gated off.

Table 15. INTERRUPT_CTRL Register (0x581)

ADDRESS	0x581							
REGISTER NAME	INTERRUPT_CTRL							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	INTRP	PMON	OTEST	OFIFO	UFIFO	CAP
DEFAULT VALUE	0	0	1	1	1	1	1	1
BIT	7	6	5	4	3	2	1	0
NAME	PWR_MON	OUT_TEST	MAX_CH	PWR_MON_IN	LAT_OTEST	LAT_OFIFO	LAT_UFIFO	LAT_MAX_CH
DEFAULT VALUE	1	0	0	1	0	0	0	0

INTRP: Global interrupt enable.
PMON: Enable power monitor interrupt.
OTEST: Enable output test mode interrupt.
OFIFO: Enable input FIFO overflow interrupt.
UFIFO: Enable input FIFO underflow interrupt.
CAP: Enable channel count exceeded interrupt.
PWR_MON: Power monitor period complete status.
OUT_TEST: Output test mode status.
MAX_CH: Channel count exceeded status.
PWR_MON_IN: Power monitor period complete latched status, clear-on-read.
LAT_OTEST: Output test mode latched status, clear-on-read.
LAT_OFIFO: Input FIFO overflow status.
LAT_UFIFO: Input FIFO underflow status.
LAT_MAX_CH: Channel count exceeded latched status, clear-on-read.

Table 16. INT_FIFO_SUM Register (0x582)

ADDRESS	0x582							
REGISTER NAME	INT_FIFO_SUM							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	UFSUM_15	UFSUM_14	UFSUM_13	UFSUM_12	UFSUM_11	UFSUM_10	UFSUM_9	UFSUM_8
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	OFSUM_7	OFSUM_6	OFSUM_5	OFSUM_4	OFSUM_3	OFSUM_2	OFSUM_1	OFSUM_0
DEFAULT VALUE	0	0	0	0	0	0	0	0

UFSUM_15: Underflow summary for channels 128–113
UFSUM_14: Underflow summary for channels 112–97
UFSUM_13: Underflow summary for channels 96–81
UFSUM_12: Underflow summary for channels 80–65
UFSUM_11: Underflow summary for channels 64–49
UFSUM_10: Underflow summary for channels 48–33
UFSUM_9: Underflow summary for channels 32–17
UFSUM_8: Underflow summary for channels 16–1
OFSUM_7: Overflow summary for channels 128–113
OFSUM_6: Overflow summary for channels 112–97
OFSUM_5: Overflow summary for channels 96–81
OFSUM_4: Overflow summary for channels 80–65
OFSUM_3: Overflow summary for channels 64–49
OFSUM_2: Overflow summary for channels 48–33
OFSUM_1: Overflow summary for channels 32–17
OFSUM_0: Overflow summary for channels 16–1

Table 17. OFLOW_AL Register (0x583)

ADDRESS	0x583							
REGISTER NAME	OFLOW_AL							
BIT	15	14	13	12	11	10	9	8
NAME	OF_16	OF_15	OF_14	OF_13	OF_12	OF_11	OF_10	OF_9
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	OF_8	OF_7	OF_6	OF_5	OF_4	OF_3	OF_2	OF_1
DEFAULT VALUE	0	0	0	0	0	0	0	0

OF_16: Input FIFO 16 overflow latched status, clear-on-read
OF_15: Input FIFO 15 overflow latched status, clear-on-read
OF_14: Input FIFO 14 overflow latched status, clear-on-read
OF_13: Input FIFO 13 overflow latched status, clear-on-read
OF_12: Input FIFO 12 overflow latched status, clear-on-read
OF_11: Input FIFO 11 overflow latched status, clear-on-read
OF_10: Input FIFO 10 overflow latched status, clear-on-read
OF_9: Input FIFO 9 overflow latched status, clear-on-read
OF_8: Input FIFO 8 overflow latched status, clear-on-read
OF_7: Input FIFO 7 overflow latched status, clear-on-read
OF_6: Input FIFO 6 overflow latched status, clear-on-read
OF_5: Input FIFO 5 overflow latched status, clear-on-read
OF_4: Input FIFO 4 overflow latched status, clear-on-read
OF_3: Input FIFO 3 overflow latched status, clear-on-read
OF_2: Input FIFO 2 overflow latched status, clear-on-read
OF_1: Input FIFO 1 overflow latched status, clear-on-read

Table 18. OFLOW_AH Register (0x584)

ADDRESS	0x584							
REGISTER NAME	OFLOW_AH							
BIT	15	14	13	12	11	10	9	8
NAME	OF_32	OF_31	OF_30	OF_29	OF_28	OF_27	OF_26	OF_25
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	OF_24	OF_23	OF_22	OF_21	OF_20	OF_19	OF_18	OF_17
DEFAULT VALUE	0	0	0	0	0	0	0	0

OF_32 : Input FIFO 32 overflow latched status, clear-on-read
OF_31 : Input FIFO 31 overflow latched status, clear-on-read
OF_30 : Input FIFO 30 overflow latched status, clear-on-read
OF_29 : Input FIFO 29 overflow latched status, clear-on-read
OF_28 : Input FIFO 28 overflow latched status, clear-on-read
OF_27 : Input FIFO 27 overflow latched status, clear-on-read
OF_26 : Input FIFO 26 overflow latched status, clear-on-read
OF_25 : Input FIFO 25 overflow latched status, clear-on-read
OF_24 : Input FIFO 24 overflow latched status, clear-on-read
OF_23 : Input FIFO 23 overflow latched status, clear-on-read
OF_22 : Input FIFO 22 overflow latched status, clear-on-read
OF_21 : Input FIFO 21 overflow latched status, clear-on-read
OF_20 : Input FIFO 20 overflow latched status, clear-on-read
OF_19 : Input FIFO 19 overflow latched status, clear-on-read
OF_18 : Input FIFO 18 overflow latched status, clear-on-read
OF_17 : Input FIFO 17 overflow latched status, clear-on-read

Table 19. OFLOW_BL Register (0x585)

ADDRESS	0x585							
REGISTER NAME	OFLOW_BL							
BIT	15	14	13	12	11	10	9	8
NAME	OF_48	OF_47	OF_46	OF_45	OF_44	OF_43	OF_42	OF_41
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	OF_40	OF_39	OF_38	OF_37	OF_36	OF_35	OF_34	OF_33
DEFAULT VALUE	0	0	0	0	0	0	0	0

OF_48 : Input FIFO 48 overflow latched status, clear-on-read
OF_47 : Input FIFO 47 overflow latched status, clear-on-read
OF_46 : Input FIFO 46 overflow latched status, clear-on-read
OF_45 : Input FIFO 45 overflow latched status, clear-on-read
OF_44 : Input FIFO 44 overflow latched status, clear-on-read
OF_43 : Input FIFO 43 overflow latched status, clear-on-read
OF_42 : Input FIFO 42 overflow latched status, clear-on-read
OF_41 : Input FIFO 41 overflow latched status, clear-on-read
OF_40 : Input FIFO 40 overflow latched status, clear-on-read
OF_39 : Input FIFO 39 overflow latched status, clear-on-read
OF_38 : Input FIFO 38 overflow latched status, clear-on-read
OF_37 : Input FIFO 37 overflow latched status, clear-on-read
OF_36 : Input FIFO 36 overflow latched status, clear-on-read
OF_35 : Input FIFO 35 overflow latched status, clear-on-read
OF_34 : Input FIFO 34 overflow latched status, clear-on-read
OF_33 : Input FIFO 33 overflow latched status, clear-on-read

Table 20. OFLOW_BH Register (0x586)

ADDRESS	0x586							
REGISTER NAME	OFLOW_BH							
BIT	15	14	13	12	11	10	9	8
NAME	OF_64	OF_63	OF_62	OF_61	OF_60	OF_59	OF_58	OF_57
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	OF_56	OF_55	OF_54	OF_53	OF_52	OF_51	OF_50	OF_49
DEFAULT VALUE	0	0	0	0	0	0	0	0

OF_64 : Input FIFO 64 overflow latched status, clear-on-read
OF_63 : Input FIFO 63 overflow latched status, clear-on-read
OF_62 : Input FIFO 62 overflow latched status, clear-on-read
OF_61 : Input FIFO 61 overflow latched status, clear-on-read
OF_60 : Input FIFO 60 overflow latched status, clear-on-read
OF_59 : Input FIFO 59 overflow latched status, clear-on-read
OF_58 : Input FIFO 58 overflow latched status, clear-on-read
OF_57 : Input FIFO 57 overflow latched status, clear-on-read
OF_56 : Input FIFO 56 overflow latched status, clear-on-read
OF_55 : Input FIFO 55 overflow latched status, clear-on-read
OF_54 : Input FIFO 54 overflow latched status, clear-on-read
OF_53 : Input FIFO 53 overflow latched status, clear-on-read
OF_52 : Input FIFO 52 overflow latched status, clear-on-read
OF_51 : Input FIFO 51 overflow latched status, clear-on-read
OF_50 : Input FIFO 50 overflow latched status, clear-on-read
OF_49 : Input FIFO 49 overflow latched status, clear-on-read

Table 21. OFLOW_CL Register (0x587)

ADDRESS	0x587							
REGISTER NAME	OFLOW_CL							
BIT	15	14	13	12	11	10	9	8
NAME	OF_80	OF_79	OF_78	OF_77	OF_76	OF_75	OF_74	OF_73
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	OF_72	OF_71	OF_70	OF_69	OF_68	OF_67	OF_66	OF_65
DEFAULT VALUE	0	0	0	0	0	0	0	0

OF_80 : Input FIFO 80 overflow latched status, clear-on-read
OF_79 : Input FIFO 79 overflow latched status, clear-on-read
OF_78 : Input FIFO 78 overflow latched status, clear-on-read
OF_77 : Input FIFO 77 overflow latched status, clear-on-read
OF_76 : Input FIFO 76 overflow latched status, clear-on-read
OF_75 : Input FIFO 75 overflow latched status, clear-on-read
OF_74 : Input FIFO 74 overflow latched status, clear-on-read
OF_73 : Input FIFO 73 overflow latched status, clear-on-read
OF_72 : Input FIFO 72 overflow latched status, clear-on-read
OF_71 : Input FIFO 71 overflow latched status, clear-on-read
OF_70 : Input FIFO 70 overflow latched status, clear-on-read
OF_69 : Input FIFO 69 overflow latched status, clear-on-read
OF_68 : Input FIFO 68 overflow latched status, clear-on-read
OF_67 : Input FIFO 67 overflow latched status, clear-on-read
OF_66 : Input FIFO 66 overflow latched status, clear-on-read
OF_65 : Input FIFO 65 overflow latched status, clear-on-read

Table 22. OFLOW_CH Register (0x588)

ADDRESS	0x588							
REGISTER NAME	OFLOW_CH							
BIT	15	14	13	12	11	10	9	8
NAME	OF_96	OF_95	OF_94	OF_93	OF_92	OF_91	OF_90	OF_89
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	OF_88	OF_87	OF_86	OF_85	OF_84	OF_83	OF_82	OF_81
DEFAULT VALUE	0	0	0	0	0	0	0	0

OF_96 : Input FIFO 96 overflow latched status, clear-on-read
OF_95 : Input FIFO 95 overflow latched status, clear-on-read
OF_94 : Input FIFO 94 overflow latched status, clear-on-read
OF_93 : Input FIFO 93 overflow latched status, clear-on-read
OF_92 : Input FIFO 92 overflow latched status, clear-on-read
OF_91 : Input FIFO 91 overflow latched status, clear-on-read
OF_90 : Input FIFO 90 overflow latched status, clear-on-read
OF_89 : Input FIFO 89 overflow latched status, clear-on-read
OF_88 : Input FIFO 88 overflow latched status, clear-on-read
OF_87 : Input FIFO 87 overflow latched status, clear-on-read
OF_86 : Input FIFO 86 overflow latched status, clear-on-read
OF_85 : Input FIFO 85 overflow latched status, clear-on-read
OF_84 : Input FIFO 84 overflow latched status, clear-on-read
OF_83 : Input FIFO 83 overflow latched status, clear-on-read
OF_82 : Input FIFO 82 overflow latched status, clear-on-read
OF_81 : Input FIFO 81 overflow latched status, clear-on-read

Table 23. OFLOW_DL Register (0x589)

ADDRESS	0x589							
REGISTER NAME	OFLOW_DL							
BIT	15	14	13	12	11	10	9	8
NAME	OF_112	OF_111	OF_110	OF_109	OF_108	OF_107	OF_106	OF_105
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	OF_104	OF_103	OF_102	OF_101	OF_100	OF_99	OF_98	OF_97
DEFAULT VALUE	0	0	0	0	0	0	0	0

OF_112: Input FIFO 112 overflow latched status, clear-on-read
OF_111: Input FIFO 111 overflow latched status, clear-on-read
OF_110: Input FIFO 110 overflow latched status, clear-on-read
OF_109: Input FIFO 109 overflow latched status, clear-on-read
OF_108: Input FIFO 108 overflow latched status, clear-on-read
OF_107: Input FIFO 107 overflow latched status, clear-on-read
OF_106: Input FIFO 106 overflow latched status, clear-on-read
OF_105: Input FIFO 105 overflow latched status, clear-on-read
OF_104: Input FIFO 104 overflow latched status, clear-on-read
OF_103: Input FIFO 103 overflow latched status, clear-on-read
OF_102: Input FIFO 102 overflow latched status, clear-on-read
OF_101: Input FIFO 101 overflow latched status, clear-on-read
OF_100: Input FIFO 100 overflow latched status, clear-on-read
OF_99: Input FIFO 99 overflow latched status, clear-on-read
OF_98: Input FIFO 98 overflow latched status, clear-on-read
OF_97: Input FIFO 97 overflow latched status, clear-on-read

Table 24. OFLOW_DH Register (0x58A)

ADDRESS	0x58A							
REGISTER NAME	OFLOW_DH							
BIT	15	14	13	12	11	10	9	8
NAME	OF_128	OF_127	OF_126	OF_125	OF_124	OF_123	OF_122	OF_121
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	OF_120	OF_119	OF_118	OF_117	OF_116	OF_115	OF_114	OF_113
DEFAULT VALUE	0	0	0	0	0	0	0	0

OF_128 : Input FIFO 128 overflow latched status, clear-on-read
OF_127 : Input FIFO 127 overflow latched status, clear-on-read
OF_126 : Input FIFO 126 overflow latched status, clear-on-read
OF_125 : Input FIFO 125 overflow latched status, clear-on-read
OF_124 : Input FIFO 124 overflow latched status, clear-on-read
OF_123 : Input FIFO 123 overflow latched status, clear-on-read
OF_122 : Input FIFO 122 overflow latched status, clear-on-read
OF_121 : Input FIFO 121 overflow latched status, clear-on-read
OF_120 : Input FIFO 120 overflow latched status, clear-on-read
OF_119 : Input FIFO 119 overflow latched status, clear-on-read
OF_118 : Input FIFO 118 overflow latched status, clear-on-read
OF_117 : Input FIFO 117 overflow latched status, clear-on-read
OF_116 : Input FIFO 116 overflow latched status, clear-on-read
OF_115 : Input FIFO 115 overflow latched status, clear-on-read
OF_114 : Input FIFO 114 overflow latched status, clear-on-read
OF_113 : Input FIFO 113 overflow latched status, clear-on-read

Table 25. UFLOW_AL Register (0x58B)

ADDRESS	0x58B							
REGISTER NAME	UFLOW_AL							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	UF_16	UF_15	UF_14	UF_13	UF_12	UF_11	UF_10	UF_9
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	UF_8	UF_7	UF_6	UF_5	UF_4	UF_3	UF_2	UF_1
DEFAULT VALUE	0	0	0	0	0	0	0	0

UF_16 : Input FIFO 16 underflow latched status, clear-on-read
UF_15 : Input FIFO 15 underflow latched status, clear-on-read
UF_14 : Input FIFO 14 underflow latched status, clear-on-read
UF_13 : Input FIFO 13 underflow latched status, clear-on-read
UF_12 : Input FIFO 12 underflow latched status, clear-on-read
UF_11 : Input FIFO 11 underflow latched status, clear-on-read
UF_10 : Input FIFO 10 underflow latched status, clear-on-read
UF_9 : Input FIFO 9 underflow latched status, clear-on-read
UF_8 : Input FIFO 8 underflow latched status, clear-on-read
UF_7 : Input FIFO 7 underflow latched status, clear-on-read
UF_6 : Input FIFO 6 underflow latched status, clear-on-read
UF_5 : Input FIFO 5 underflow latched status, clear-on-read
UF_4 : Input FIFO 4 underflow latched status, clear-on-read
UF_3 : Input FIFO 3 underflow latched status, clear-on-read
UF_2 : Input FIFO 2 underflow latched status, clear-on-read
UF_1 : Input FIFO 1 underflow latched status, clear-on-read

Table 26. UFLOW_AH Register (0x58C)

ADDRESS	0x58C							
REGISTER NAME	UFLOW_AH							
BIT	15	14	13	12	11	10	9	8
NAME	UF_32	UF_31	UF_30	UF_29	UF_28	UF_27	UF_26	UF_25
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	UF_24	UF_23	UF_22	UF_21	UF_20	UF_19	UF_18	UF_17
DEFAULT VALUE	0	0	0	0	0	0	0	0

UF_32 : Input FIFO 32 underflow latched status, clear-on-read
UF_31 : Input FIFO 31 underflow latched status, clear-on-read
UF_30 : Input FIFO 30 underflow latched status, clear-on-read
UF_29 : Input FIFO 29 underflow latched status, clear-on-read
UF_28 : Input FIFO 28 underflow latched status, clear-on-read
UF_27 : Input FIFO 27 underflow latched status, clear-on-read
UF_26 : Input FIFO 26 underflow latched status, clear-on-read
UF_25 : Input FIFO 25 underflow latched status, clear-on-read
UF_24 : Input FIFO 24 underflow latched status, clear-on-read
UF_23 : Input FIFO 23 underflow latched status, clear-on-read
UF_22 : Input FIFO 22 underflow latched status, clear-on-read
UF_21 : Input FIFO 21 underflow latched status, clear-on-read
UF_20 : Input FIFO 20 underflow latched status, clear-on-read
UF_19 : Input FIFO 19 underflow latched status, clear-on-read
UF_18 : Input FIFO 18 underflow latched status, clear-on-read
UF_17 : Input FIFO 17 underflow latched status, clear-on-read

Table 27. UFLOW_BL Register (0x58D)

ADDRESS	0x58D							
REGISTER NAME	UFLOW_BL							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	UF_48	UF_47	UF_46	UF_45	UF_44	UF_43	UF_42	UF_41
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	UF_40	UF_39	UF_38	UF_37	UF_36	UF_35	UF_34	UF_33
DEFAULT VALUE	0	0	0	0	0	0	0	0

UF_48 : Input FIFO 48 underflow latched status, clear-on-read
UF_47 : Input FIFO 47 underflow latched status, clear-on-read
UF_46 : Input FIFO 46 underflow latched status, clear-on-read
UF_45 : Input FIFO 45 underflow latched status, clear-on-read
UF_44 : Input FIFO 44 underflow latched status, clear-on-read
UF_43 : Input FIFO 43 underflow latched status, clear-on-read
UF_42 : Input FIFO 42 underflow latched status, clear-on-read
UF_41 : Input FIFO 41 underflow latched status, clear-on-read
UF_40 : Input FIFO 40 underflow latched status, clear-on-read
UF_39 : Input FIFO 39 underflow latched status, clear-on-read
UF_38 : Input FIFO 38 underflow latched status, clear-on-read
UF_37 : Input FIFO 37 underflow latched status, clear-on-read
UF_36 : Input FIFO 36 underflow latched status, clear-on-read
UF_35 : Input FIFO 35 underflow latched status, clear-on-read
UF_34 : Input FIFO 34 underflow latched status, clear-on-read
UF_33 : Input FIFO 33 underflow latched status, clear-on-read

Table 28. UFLOW_BH Register (0x58E)

ADDRESS	0x58E							
REGISTER NAME	UFLOW_BH							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	UF_64	UF_63	UF_62	UF_61	UF_60	UF_59	UF_58	UF_57
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	UF_56	UF_55	UF_54	UF_53	UF_52	UF_51	UF_50	UF_49
DEFAULT VALUE	0	0	0	0	0	0	0	0

UF_64 : Input FIFO 64 underflow latched status, clear-on-read
UF_63 : Input FIFO 63 underflow latched status, clear-on-read
UF_62 : Input FIFO 62 underflow latched status, clear-on-read
UF_61 : Input FIFO 61 underflow latched status, clear-on-read
UF_60 : Input FIFO 60 underflow latched status, clear-on-read
UF_59 : Input FIFO 59 underflow latched status, clear-on-read
UF_58 : Input FIFO 58 underflow latched status, clear-on-read
UF_57 : Input FIFO 57 underflow latched status, clear-on-read
UF_56 : Input FIFO 56 underflow latched status, clear-on-read
UF_55 : Input FIFO 55 underflow latched status, clear-on-read
UF_54 : Input FIFO 54 underflow latched status, clear-on-read
UF_53 : input FIFO 53 underflow latched status, clear-on-read
UF_52 : Input FIFO 52 underflow latched status, clear-on-read
UF_51 : Input FIFO 51 underflow latched status, clear-on-read
UF_50 : Input FIFO 50 underflow latched status, clear-on-read
UF_49 : Input FIFO 49 underflow latched status, clear-on-read

Table 29. UFLOW_CL Register (0x58F)

ADDRESS	0x58F							
REGISTER NAME	UFLOW_CL							
BIT	15	14	13	12	11	10	9	8
NAME	UF_80	UF_79	UF_78	UF_77	UF_76	UF_75	UF_74	UF_73
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	UF_72	UF_71	UF_70	UF_69	UF_68	UF_67	UF_66	UF_65
DEFAULT VALUE	0	0	0	0	0	0	0	0

UF_80 : Input FIFO 80 underflow latched status, clear-on-read
UF_79 : Input FIFO 79 underflow latched status, clear-on-read
UF_78 : Input FIFO 78 underflow latched status, clear-on-read
UF_77 : Input FIFO 77 underflow latched status, clear-on-read
UF_76 : Input FIFO 76 underflow latched status, clear-on-read
UF_75 : Input FIFO 75 underflow latched status, clear-on-read
UF_74 : Input FIFO 74 underflow latched status, clear-on-read
UF_73 : Input FIFO 73 underflow latched status, clear-on-read
UF_72 : Input FIFO 72 underflow latched status, clear-on-read
UF_71 : Input FIFO 71 underflow latched status, clear-on-read
UF_70 : Input FIFO 70 underflow latched status, clear-on-read
UF_69 : Input FIFO 69 underflow latched status, clear-on-read
UF_68 : Input FIFO 68 underflow latched status, clear-on-read
UF_67 : Input FIFO 67 underflow latched status, clear-on-read
UF_66 : Input FIFO 66 underflow latched status, clear-on-read
UF_65 : Input FIFO 65 underflow latched status, clear-on-read

Table 30. UFLOW_CH Register (0x590)

ADDRESS	0x590							
REGISTER NAME	UFLOW_CH							
BIT	15	14	13	12	11	10	9	8
NAME	UF_96	UF_95	UF_94	UF_93	UF_92	UF_91	UF_90	UF_89
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	UF_88	UF_87	UF_86	UF_85	UF_84	UF_83	UF_82	UF_81
DEFAULT VALUE	0	0	0	0	0	0	0	0

UF_96 : Input FIFO 96 underflow latched status, clear-on-read
UF_95 : Input FIFO 95 underflow latched status, clear-on-read
UF_94 : Input FIFO 94 underflow latched status, clear-on-read
UF_93 : Input FIFO 93 underflow latched status, clear-on-read
UF_92 : Input FIFO 92 underflow latched status, clear-on-read
UF_91 : Input FIFO 91 underflow latched status, clear-on-read
UF_90 : Input FIFO 90 underflow latched status, clear-on-read
UF_89 : Input FIFO 89 underflow latched status, clear-on-read
UF_88 : Input FIFO 88 underflow latched status, clear-on-read
UF_87 : Input FIFO 87 underflow latched status, clear-on-read
UF_86 : Input FIFO 86 underflow latched status, clear-on-read
UF_85 : Input FIFO 85 underflow latched status, clear-on-read
UF_84 : Input FIFO 84 underflow latched status, clear-on-read
UF_83 : Input FIFO 83 underflow latched status, clear-on-read
UF_82 : Input FIFO 82 underflow latched status, clear-on-read
UF_81 : Input FIFO 81 underflow latched status, clear-on-read

Table 31. UFLOW_DL Register (0x591)

ADDRESS	0x591							
REGISTER NAME	UFLOW_DL							
BIT	15	14	13	12	11	10	9	8
NAME	UF_112	UF_111	UF_110	UF_109	UF_108	UF_107	UF_106	UF_105
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	UF_104	UF_103	UF_102	UF_101	UF_100	UF_99	UF_98	UF_97
DEFAULT VALUE	0	0	0	0	0	0	0	0

UF_112 : Input FIFO 112 underflow latched status, clear-on-read
UF_111 : Input FIFO 111 underflow latched status, clear-on-read
UF_110 : Input FIFO 110 underflow latched status, clear-on-read
UF_109 : Input FIFO 109 underflow latched status, clear-on-read
UF_108 : Input FIFO 108 underflow latched status, clear-on-read
UF_107 : Input FIFO 107 underflow latched status, clear-on-read
UF_106 : Input FIFO 106 underflow latched status, clear-on-read
UF_105 : Input FIFO 105 underflow latched status, clear-on-read
UF_104 : Input FIFO 104 underflow latched status, clear-on-read
UF_103 : Input FIFO 103 underflow latched status, clear-on-read
UF_102 : Input FIFO 102 underflow latched status, clear-on-read
UF_101 : Input FIFO 101 underflow latched status, clear-on-read
UF_100 : Input FIFO 100 underflow latched status, clear-on-read
UF_99 : Input FIFO 99 underflow latched status, clear-on-read
UF_98 : Input FIFO 98 underflow latched status, clear-on-read
UF_97 : Input FIFO 97 underflow latched status, clear-on-read

Table 32. UFLOW_DH Register (0x592)

ADDRESS	0x592							
REGISTER NAME	UFLOW_DH							
BIT	15	14	13	12	11	10	9	8
NAME	UF_128	UF_127	UF_126	UF_125	UF_124	UF_123	UF_122	UF_121
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	UF_120	UF_119	UF_118	UF_117	UF_116	UF_115	UF_114	UF_113
DEFAULT VALUE	0	0	0	0	0	0	0	0

UF_128 : Input FIFO 128 underflow latched status, clear-on-read
UF_127 : Input FIFO 127 underflow latched status, clear-on-read
UF_126 : Input FIFO 126 underflow latched status, clear-on-read
UF_125 : Input FIFO 125 underflow latched status, clear-on-read
UF_124 : Input FIFO 124 underflow latched status, clear-on-read
UF_123 : Input FIFO 123 underflow latched status, clear-on-read
UF_122 : Input FIFO 122 underflow latched status, clear-on-read
UF_121 : Input FIFO 121 underflow latched status, clear-on-read
UF_120 : Input FIFO 120 underflow latched status, clear-on-read
UF_119 : Input FIFO 119 underflow latched status, clear-on-read
UF_118 : Input FIFO 118 underflow latched status, clear-on-read
UF_117 : Input FIFO 117 underflow latched status, clear-on-read
UF_116 : Input FIFO 116 underflow latched status, clear-on-read
UF_115 : Input FIFO 115 underflow latched status, clear-on-read
UF_114 : Input FIFO 114 underflow latched status, clear-on-read
UF_113 : Input FIFO 113 underflow latched status, clear-on-read

Table 33. CHAN_IN_CFG Registers

There is a CHAN_IN_CFG register for each of the 128 channels.

ADDRESS	0x500 + ch#, ch# = 1 to 128							
REGISTER NAME	CHAN_IN_CF_ch#							
DESCRIPTION	channel configuration							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	—	GBL_RST	LCL_RST	MUTE
DEFAULT VALUE	0	0	0	0	0	0	0	1
BIT	7	6	5	4	3	2	1	0
NAME	—	—	SLOT[5]	SLOT[4]	SLOT[3]	SLOT[2]	SLOT[1]	SLOT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

GBL_RST: Global FIFO reset enable.
LCL_RST: Local FIFO reset pulse, self-clearing.
MUTE: Mute the channel.
1: Channel off (muted)
0: Channel on (active)
SLOT[5:0]: Time slot [5:0].

Table 34. COMB8 Registers

There are 16 COMB8 registers, one for each of the 8-channel block combiners.

ADDRESS	0x100 + ((blk8# -1) * 0x40), blk8# = 1 to 16							
REGISTER NAME	COMB8_blk#							
BIT	15	14	13	12	11	10	9	8
NAME	FCW2[20]	FCW2[19]	FCW2[18]	FCW2[17]	FCW2[16]	SPARE2	SPARE1	LD_FCW2
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G3[7]	G3[6]	G3[5]	G3[4]	G3[3]	G3[2]	G3[1]	G3[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

FCW2[20:16]: NCO2 frequency control word MSB, bits [20:16].
FCW2 is in signed magnitude format.
SPARE2: Spare bit.
SPARE1: Spare bit.
LD_FCW2: Frequency control word 2 load pulse (self-clearing), resets NCO2.
G3[7:0]: G3 gain value [7:0].

Table 35. NCO2LSB Registers

There are 16 NCO2LSB registers, one for each of the 8-channel block combiners.

ADDRESS	0x101 + ((blk8# -1) * 0x40), blk8# = 1 to 16							
REGISTER NAME	NCO2LSB_blk#							
BIT	15	14	13	12	11	10	9	8
NAME	FCW2[15]	FCW2[14]	FCW2[13]	FCW2[12]	FCW2[11]	FCW2[10]	FCW2[9]	FCW2[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	FCW2[7]	FCW2[6]	FCW2[5]	FCW2[4]	FCW2[3]	FCW2[2]	FCW2[1]	FCW2[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

FCW2[15:0] : NCO2 frequency control word LSBs, bits [15:0].
FCW2 is in signed magnitude format.

Table 36. G3_IPWR Registers

There are 16 G3_IPWR registers, one for each of the 8-channel block combiners.

ADDRESS	0x102 + ((blk8# -1) * 0x40), blk8# = 1 to 16							
REGISTER NAME	G3_IPWR_blk#							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[11:0] : Power monitor threshold count, I path.

Table 37. G3_QPWR Registers

There are 16 G3_QPWR registers, one for each of the 8-channel block combiners.

ADDRESS	0x103 + ((blk8# -1) * 0x40), blk8# = 1 to 16							
REGISTER NAME	G3_QPWR_blk#							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[11:0] : Power monitor threshold count, Q path.

Table 38. KF_LF_MSB_1 Registers

There are 16 KF_LF_MSB_1 registers, one for each of the 8-channel block combiners. It contains the upper KF and LF bits (MSBs) for each individual channel. KF/LF values are in unsigned integer number format.

ADDRESS	0x104 + ((blk8# -1) * 0x40), blk8# = 1 to 16							
REGISTER NAME	KF_LF_MSB_1_blk8#							
BIT	15	14	13	12	11	10	9	8
NAME	KF_ Ch8[26]	KF_ Ch8[25]	KF_ Ch8[24]	LF_ Ch8[26]	LF_ Ch8[25]	LF_ Ch8[24]	KF_ Ch7[26]	KF_ Ch7[25]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	KF_ Ch7[24]	LF_ Ch7[26]	LF_ Ch7[25]	LF_ Ch7[24]	KF_ Ch6[26]	KF_ Ch6[25]	KF_ Ch6[24]	LF_ Ch6[26]
DEFAULT VALUE	0	0	0	0	0	0	0	0

KF_Ch8[26:24] : Upper MSBs of the KF value.
LF_Ch8[26:24] : Upper MSBs of the LF value.
KF_Ch7[26:24] : Upper MSBs of the KF value.
LF_Ch7[26:24] : Upper MSBs of the LF value.
KF_Ch6[26:24] : Upper MSBs of the KF value.
LF_Ch6[26] : Bit [26] of the LF value.

There are sixteen channel combiners (blk8# = 1 to 16) each of which is associated with eight channels (see Figure 27). The channel notation KF_ChN and LF_ChN (where N = 1..8) refers to a particular blk8# combiner's channel. The actual channel identifier would be calculated as: channel# = N + (blk8# -1) * 8 (e.g. blk#= 2, Ch3 (N= 3) would equate to channel 11).

Table 39. KF_LF_MSB_2 Registers

There are 16 KF_LF_MSB_2 registers, one for each of the 8-channel block combiners. It contains the upper KF and LF bits (MSBs) for each individual channel.

ADDRESS	0x105 + ((blk8# -1) * 0x40), blk8# = 1 to 16							
REGISTER NAME	KF_LF_MSB_2_blk8#							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	LF_ Ch6[25]	LF_ Ch6[24]	KF_ Ch5[26]	KF_ Ch5[25]	KF_ Ch5[24]	LF_ Ch5[26]	LF_ Ch5[25]	LF_ Ch5[24]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	KF_ Ch4[26]	KF_ Ch4[25]	KF_ Ch4[24]	LF_ Ch4[26]	LF_ Ch4[25]	LF_ Ch4[24]	KF_ Ch3[26]	KF_ Ch3[25]
DEFAULT VALUE	0	0	0	0	0	0	0	0

LF_Ch6[25:24] : Bits [25:24] of the LF value.
KF_Ch5[26:24] : Upper MSBs of the KF value.
LF_Ch5[26:24] : Upper MSBs of the LF value.
KF_Ch4[26:24] : Upper MSBs of the KF value.
LF_Ch4[26:24] : Upper MSBs of the LF value.
KF_Ch3[26:25] : Bits [26:25] of the KF value.
There are sixteen channel combiners (blk8# = 1 to 16) each of which is associated with eight channels (see Figure 27). The channel notation KF_ChN and LF_ChN (where N = 1..8) refers to a particular blk8# combiner's channel. The actual channel identifier would be calculated as: channel# = N + (blk8# -1) * 8 (e.g. blk#= 2, Ch3 (N= 3) would equate to channel 11).

Table 40. KF_LF_MSB_3 Registers

There are 16 KF_LF_MSB_3 registers, one for each of the 8-channel block combiners. It contains the upper KF and LF bits (MSBs) for each individual channel.

ADDRESS	0x106 + ((blk8# -1) * 0x40), blk8# = 1 to 16							
REGISTER NAME	KF_LF_MSB_3_blk8#							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	KF_ Ch3[24]	LF_ Ch3[26]	LF_ Ch3[25]	LF_ Ch3[24]	KF_ Ch2[26]	KF_ Ch2[25]	KF_ Ch2[24]	LF_ Ch2[26]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	LF_ Ch2[25]	LF_ Ch2[24]	KF_ Ch1[26]	KF_ Ch1[25]	KF_ Ch1[24]	LF_ Ch1[26]	LF_ Ch1[25]	LF_ Ch1[24]
DEFAULT VALUE	0	0	0	0	0	0	0	0

KF_Ch3[24] : Bit [24] of the KF value.
LF_Ch3[26:24] : Upper MSBs of the LF value.
KF_Ch2[26:24] : Upper MSBs of the KF value.
LF_Ch2[26:24] : Upper MSBs of the LF value.
KF_Ch1[26:24] : Upper MSBs of the KF value.
LF_Ch1[26:24] : Upper MSBs of the LF value.
There are sixteen channel combiners (blk8# = 1 to 16) each of which is associated with eight channels Figure 27. The channel notation KF_ChN and LF_ChN (where N = 1..8) refers to a particular blk8# combiner's channel. The actual channel identifier would be calculated as: channel# = N + (blk8# -1) * 8 (e.g. blk#= 2, Ch3 (N= 3) would equate to channel 11).

Table 41. SYMIF Registers

There is a SYMIF register for each of the 128 channels.

ADDRESS	0x108 + ((ch# - 1) * 0x07) + (int ((ch#-1) / 8) * 0x08), ch# = 1 to 128							
REGISTER NAME	SYMIF_ch#							
DESCRIPTION	Channel_121 Symbol Interface							
BIT	15	14	13	12	11	10	9	8
NAME	LD_FCW	LD_KFLF	GLB	PRBS	ALPHA[1]	ALPHA[0]	QOFF	QAM[2]
DEFAULT VALUE	0	0	0	0	0	0	0	1
BIT	7	6	5	4	3	2	1	0
NAME	QAM[1]	QAM[0]	SPARE1	D2	D1[3]	D1[2]	D1[1]	D1[0]
DEFAULT VALUE	1	1	0	0	0	0	0	0

LD_FCW: Channel_1 frequency control word local load pulse, self-clearing.
LD_KFLF: LF/KF control word load pulse, self-clearing.
GLB: Enable global LF/KF load.
PRBS: Enable PRBS this channel (seed in separate register).
ALPHA[1:0]: RRC alpha select [1:0].
00 = Alpha 0.12
01 = Alpha 0.13
10 = Alpha 0.15
11 = Alpha 0.18
QOFF: Enable QAM offset bit.
QAM[2:0]: QAM map select (default is bypass) [2:0].
000 = TCM 256-QAM
001 = TCM 64-QAM
010 = Diff Grey 16-QAM
011 = Diff Grey 32-QAM
100 = Diff Grey 64-QAM
101 = Diff Grey 128-QAM
110 = Diff Grey 256-QAM
111 = 10-Bit Bypass Mode with Offset Bit Register
SPARE1: Spare bit.
D2: Enable half symbol delay, D2 delay.
D1[3:0]: Value for D1 delay, bits [3:0].
When in PRBS mode, these 6 bits are part of the 12-bit PRBS SEED value.

Table 42. KFA Registers

There is a KFA register for each of the 128 channels. KF/LF values are in unsigned integer number format.

ADDRESS	0x109 + ((ch# - 1) * 0x07) + (int ((ch#-1) / 8) * 0x08), ch# = 1 to 128							
REGISTER NAME	KFA_ch#							
DESCRIPTION	KFA register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	KF[15]	KF[14]	KF[13]	KF[12]	KF[11]	KF[10]	KF[9]	KF[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	KF[7]	KF[6]	KF[5]	KF[4]	KF[3]	KF[2]	KF[1]	KF[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

KF[15:0]: KF LSB bits [15:0].

Table 43. KFLF Registers

There is a KFLF register for each of the 128 channels.

ADDRESS	0x10A + ((ch# - 1) * 0x07) + (int ((ch#-1) / 8) * 0x08), ch# = 1 to 128							
REGISTER NAME	KFLF_ch#							
DESCRIPTION	KFLF register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	KF[23]	KF[22]	KF[21]	KF[20]	KF[19]	KF[18]	KF[17]	KF[16]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	LF[23]	LF[22]	LF[21]	LF[20]	LF[19]	LF[18]	LF[17]	LF[16]
DEFAULT VALUE	0	0	0	0	0	0	0	0

KF[23:16]: KF MSB, bits [23:16].
LF[23:16]: LF MSB, bits [23:16].

Table 44. LFA Registers

There is a LFA register for each of the 128 channels.

ADDRESS	0x10B + ((ch# - 1) * 0x07) + (int ((ch#-1) / 8) * 0x08), ch# = 1 to 128							
REGISTER NAME	LFA_ch#							
DESCRIPTION	LFA register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	LF[15]	LF[14]	LF[13]	LF[12]	LF[11]	LF[10]	LF[9]	LF[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	LF[7]	LF[6]	LF[5]	LF[4]	LF[3]	LF[2]	LF[1]	LF[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

LF[15:0]: LF LSBs, bits [15:0].

Table 45. NCOA Registers

There is a NCOA register for each of the 128 channels. The frequency word is formatted in signed magnitude format.

ADDRESS	0x10C + ((ch# - 1) * 0x07) + (int ((ch#-1) / 8) * 0x08), ch# = 1 to 128							
REGISTER NAME	NCOA_ch#							
DESCRIPTION	NCOA register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	FCW1[15]	FCW1[14]	FCW1[13]	FCW1[12]	FCW1[11]	FCW1[10]	FCW1[9]	FCW1[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	FCW1[7]	FCW1[6]	FCW1[5]	FCW1[4]	FCW1[3]	FCW1[2]	FCW1[1]	FCW1[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

FCW1[15:0]: NCO 1 control word LSBs, bits [15:0].

Table 46. NCOB Registers

There is a NCOB register for each of the 128 channels. The frequency word is formatted in signed magnitude format.

ADDRESS	0x10D + ((ch# - 1) * 0x07) + (int ((ch#-1) / 8) * 0x08), ch# = 1 to 128							
REGISTER NAME	NCOB_ch#							
DESCRIPTION	NCOB register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]
DEFAULT VALUE	1	1	1	1	1	1	1	1
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	—	—	FCW1[18]	FCW1[17]	FCW1[16]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G2[7:0]: Post modulator gain factor, bits [7:0].
FCW1[18:16]: NCO 1 control word, MSBs, bits [18:16].

Table 47. RRC Registers

There is a RRC register for each of the 128 channels.

ADDRESS	0x10E + ((ch# - 1) * 0x07) + (int ((ch#-1) / 8) * 0x08), ch# = 1 to 128							
REGISTER NAME	RRC_ch#							
DESCRIPTION	RRC register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	—	—	—	G1[10]	G1[9]	G1[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G1[10:0] : RRC gain factor [10:0]. Gain values are unsigned (positive) values.

CHAN32 REGISTERS

Table 48. CHAN32 Registers

There are four CHAN32 registers, one for each of the 32-channel block combiners.

ADDRESS	0x020 + ((blk32# - 1) * 0x08), blk32# = 1 to 4							
REGISTER NAME	CHAN32_blk32#							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	—	SPARE2	SPARE1	LD_FCW
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G4[7]	G4[6]	G4[5]	G4[4]	G4[3]	G4[2]	G4[1]	G4[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

SPARE2: Spare bit.
SPARE1: Spare bit.
LD_FCW: Frequency control word load pulse generated when a 1 is written to this bit, self-clearing.
G4[7:0]: G4 gain value [7:0] Gain values are unsigned (positive) values.

Table 49. NCO3A Registers

There are four NCO3A registers, one for each of the 32-channel block combiners.

ADDRESS	0x021 + ((blk32# - 1) * 0x08), blk32# = 1 to 4							
REGISTER NAME	NCO3A_blk32#							
BIT	15	14	13	12	11	10	9	8
NAME	FCW3[15]	FCW3[14]	FCW3[13]	FCW3[12]	FCW3[11]	FCW3[10]	FCW3[9]	FCW3[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	FCW3[7]	FCW3[6]	FCW3[5]	FCW3[4]	FCW3[3]	FCW3[2]	FCW3[1]	FCW3[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

FCW3[15:0] : Modulator 3 frequency control word LSB's [15:0].
FCW values are signed magnitude format.

Table 50. NCO3B Registers

There are four NCO3B registers, one for each of the 32-channel block combiners.

ADDRESS	0x022 + ((blk32# - 1)* 0x08), blk32# = 1 to 4							
REGISTER NAME	G4_IPWR_blk32#							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	—	—	—	—
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	—	FCW3[19]	FCW3[18]	FCW3[17]	FCW3[16]
DEFAULT VALUE	0	0	0	0	0	0	0	0

FCW3[19:16]: Modulator 3 frequency control word MSBs [19:16].
FCW values are signed magnitude format.

Table 51. G4_IPWR Registers

There are four G4_IPWR registers, one for each of the 32-channel block combiners.

ADDRESS	0x023 + ((blk32# - 1) * 0x08), blk32# = 1 to 4							
REGISTER NAME	NC03B_blk32#							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[11:0]: Power monitor threshold count, I path [11:0].

Table 52. G4_QPWR Registers

There are four G4_QPWR registers, one for each of the 32-channel block combiners.

ADDRESS	0x024 + ((blk32# - 1) * 0x08), blk32# = 1 to 4							
REGISTER NAME	G4_QPWR_blk32#							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[11:0] : Power monitor threshold count, Q path [11:0]

CHAN128 REGISTERS

Table 53. HS_CFG Register (0x040)

ADDRESS	0x040							
REGISTER NAME	HS_CFG							
DESCRIPTION	Configuration for output circuits.							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	MOD	ENXCLK	MISR_CNT[1]	MISR_CNT[0]	MCFG[1]	MCFG[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	—	SPARE	XOR	SYNC	LD_FCW
DEFAULT VALUE	0	0	0	0	0	0	1	0

MOD: Complement B and D outputs.
ENXCLK: Enable XOR to output DATACK/16 clock.
MISR_CNT[1:0]: MISR sample clock select - 00: /12, 01: /9, 10: /10, 11: /11.
MCFG[1:0]: Output Test, bits [1:0], 00: bypass, 01: MISR, 10: data/clk, 11: SPI value.
SPARE: Spare.
XOR: Enable modulating data outputs with LFSR pattern.
SYNC: Enable LFSR pattern on sync.
LD_FCW: Frequency control word load pulse, self-clearing.

Table 54. GAIN5 Register (0x041)

ADDRESS	0x041							
REGISTER NAME	GAIN5							
DESCRIPTION	Gain control for 128 channel combiner output							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	—	—	—	—	—	G5[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	G5[7]	G5[6]	G5[5]	G5[4]	G5[3]	G5[2]	G5[1]	G5[0]
DEFAULT VALUE	1	1	1	1	1	1	1	1

G5[8:0] : G5 gain control [8:0]. Gain values are unsigned (positive) values.

Table 55. NCO4A Register (0x042)

ADDRESS	0x042							
REGISTER NAME	NCO4A							
DESCRIPTION	NCO 4 frequency control word (LSB)							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	FCW4[15]	FCW4[14]	FCW4[13]	FCW4[12]	FCW4[11]	FCW4[10]	FCW4[9]	FCW4[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	FCW4[7]	FCW4[6]	FCW4[5]	FCW4[4]	FCW4[3]	FCW4[2]	FCW4[1]	FCW4[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

FCW4[15:0]: nco4 LSB frequency control word, bits [15:0].

Table 56. NCO4B Register (0x043)

ADDRESS	0x043							
REGISTER NAME	NCO4B							
DESCRIPTION	NCO 4 frequency control word (MSB)							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	—	—	—	—	—	—
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	-—	FCW4[20]	FCW4[19]	FCW4[18]	FCW4[17]	FCW4[16]
DEFAULT VALUE	0	0	0	0	0	0	0	0

FCW4[20:16] : nco4 MSB frequency control word, bits [20:16]
FCW values are signed magnitude format.

Table 57. G5_PWR Register (0x044)

ADDRESS	0x044							
REGISTER NAME	G5_PWR							
DESCRIPTION	Gain 5 power monitor counter							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	—	—	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[11:0]: Power monitor threshold count [11:0].

Table 58. GAIN6 Register (0x050)

ADDRESS	0x050							
REGISTER NAME	GAIN6							
DESCRIPTION	Final output gain stage							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	—	—	—	—	—	G6[8]
DEFAULT VALUE	0	0	0	0	0	0	0	1
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	G6[7]	G6[6]	G6[5]	G6[4]	G6[3]	G6[2]	G6[1]	G6[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G8[8:0] : G6 gain control [8:0]. Gain values are unsigned (positive) values.
The default is a gain of 1 (100h).

Table 59. GAIN6_PWR Register (0x051)

ADDRESS	0x051							
REGISTER NAME	G6_PWR							
DESCRIPTION	Gain 6 power monitor counter							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[11:0]: Power monitor threshold count [11:0].

Table 60. PWRMON_CFG Register (0x046)

ADDRESS	0x046							
REGISTER NAME	PWRMON_CFG							
DESCRIPTION	Power monitor control register							
BIT	15	14	13	12	11	10	9	8
NAME	THLD[7]	THLD[6]	THLD[5]	THLD[4]	THLD[3]	THLD[2]	THLD[1]	THLD[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	—	—	PM	MODE	RESET
DEFAULT VALUE	0	0	0	0	0	0	0	0

THLD[7:0]: Power monitor threshold value, bits [7:0] (two's complement format).
PM: Enable power monitor data collection.
MODE: selects above threshold (1) or below threshold (0).
MODE=1, should be used with the positive threshold values, and MODE=0, should be used with the negative threshold values.
RESET: reset counters and initiates the power monitoring process. RESET should be applied each time to start a new power monitor cycle.

Table 61. PWRMON_1 Register (0x047)

ADDRESS	0x047							
REGISTER NAME	PWRMON_1							
DESCRIPTION	Power monitor 48-bit timer register							
BIT	15	14	13	12	11	10	9	8
NAME	COUNT[15]	COUNT[14]	COUNT[13]	COUNT[12]	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[15:0]: Power monitor start count, LSBs, bits [15:0].

Table 62. PWRMON_2 Register (0x048)

ADDRESS	0x048							
REGISTER NAME	PWRMON_2							
DESCRIPTION	Power monitor 48-bit timer register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	COUNT[31]	COUNT[30]	COUNT[29]	COUNT[28]	COUNT[27]	COUNT[26]	COUNT[25]	COUNT[24]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	COUNT[23]	COUNT[22]	COUNT[21]	COUNT[20]	COUNT[19]	COUNT[18]	COUNT[17]	COUNT[16]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[31:16] : Power monitor start count, bits [31:16]

Table 63. PWRMON_3 Register (0x049)

ADDRESS	0x049							
REGISTER NAME	PWRMON_3							
DESCRIPTION	Power monitor 48-bit timer register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	COUNT[47]	COUNT[46]	COUNT[45]	COUNT[44]	COUNT[43]	COUNT[42]	COUNT[41]	COUNT[40]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	COUNT[39]	COUNT[38]	COUNT[37]	COUNT[36]	COUNT[35]	COUNT[34]	COUNT[33]	COUNT[32]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[47:32]: Power monitor start count, MSBs, bits [47:32].

Table 64. XOR_CFG Register (0x04A)

ADDRESS	0x04A							
REGISTER NAME	XOR_CFG							
DESCRIPTION	XOR tap select register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	TAP[15]	TAP[14]	TAP[13]	TAP[12]	TAP[11]	TAP[10]	TAP[9]	TAP[8]
DEFAULT VALUE	0	0	0	0	0	1	0	1
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	TAP[7]	TAP[6]	TAP[5]	TAP[4]	TAP[3]	TAP[2]	TAP[1]	TAP[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

TAP[15:0] : Enable feedback from LFSR MSB to low order bit positions [15:0]

Table 65. SYNC_CFG Register (0x04B)

ADDRESS	0x04B							
REGISTER NAME	SYNC_CFG							
DESCRIPTION	Sync tap select register							
BIT	15	14	13	12	11	10	9	8
NAME	TAP[15]	TAP[14]	TAP[13]	TAP[12]	TAP[11]	TAP[10]	TAP[9]	TAP[8]
DEFAULT VALUE	0	0	0	0	0	1	0	1
BIT	7	6	5	4	3	2	1	0
NAME	TAP[7]	TAP[6]	TAP[5]	TAP[4]	TAP[3]	TAP[2]	TAP[1]	TAP[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

TAP[15:0] : Enable feedback from LFSR MSB to low order bit positions [15:0]

Table 66. TEST_PORTA Register (0x04C)

ADDRESS	0x04C							
REGISTER NAME	TEST_PORTA							
DESCRIPTION	Test: LVDS A and XOR SPI static output values							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	PORTA[13]	PORTA[12]	PORTA[11]	PORTA[10]	PORTA[9]	PORTA[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	PORTA[7]	PORTA[6]	PORTA[5]	PORTA[4]	PORTA[3]	PORTA[2]	PORTA[1]	PORTA[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

PORTA[13] : Test value for port A LVDS output bit [13]. This bit value is inverted on the output.
PORTA[12:0] : Test value for port A LVDS output bus [12:0].

Table 67. TEST_PORTB Register (0x04D)

ADDRESS	0x04D							
REGISTER NAME	TEST_PORTB							
DESCRIPTION	Test: LVDS B and SYNC SPI static output values							
BIT	15	14	13	12	11	10	9	8
NAME	—	SYNC	PORTB[13]	PORTB[12]	PORTB[11]	PORTB[10]	PORTB[9]	PORTB[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	PORTB[7]	PORTB[6]	PORTB[5]	PORTB[4]	PORTB[3]	PORTB[2]	PORTB[1]	PORTB[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

SYNC : Test value for SYNC pin
PORTB[13] : Test value for port B LVDS output bit [13].
This bit value is inverted on the output.
PORTB[12:0] : Test value for port B LVDS output bus [12:0].

Table 68. TEST_PORTC Register (0x04E)

ADDRESS	0x04E							
REGISTER NAME	TEST_PORTC							
DESCRIPTION	Test: LVDS C and PAR SPI static output values							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	PARITY	PORTC[13]	PORTC[12]	PORTC[11]	PORTC[10]	PORTC[9]	PORTC[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	PORTC[7]	PORTC[6]	PORTC[5]	PORTC[4]	PORTC[3]	PORTC[2]	PORTC[1]	PORTC[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

PARITY : Test value for Parity pin
PORTC[13] : Test value for port C LVDS output bit [13]. This bit value is inverted on the output.
PORTC[12:0] : Test value for port C LVDS output bus [12:0].

Table 69. TEST_PORTD Register (0x04F)

ADDRESS	0x04F							
REGISTER NAME	TEST_PORTD							
DESCRIPTION	Test: LVDS D SPI static output values							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	XOR	PORTD[13]	PORTD[12]	PORTD[11]	PORTD[10]	PORTD[9]	PORTD[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	PORTD[7]	PORTD[6]	PORTD[5]	PORTD[4]	PORTD[3]	PORTD[2]	PORTD[1]	PORTD[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

XOR : Test value for XOR pin
PORTD[13] : SPI test value for port D LVDS output bit [13].
This bit value is inverted on the output.
PORTD[12:0] : SPI test value for port D LVDS output bus [12:0].

DPD REGISTERS

Table 70. DPDCFG Register (0x081)

ADDRESS	0x081							
REGISTER NAME	DPDCFG							
DESCRIPTION	DPD Configuration							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	—	—	—	BR1_ACT	BR2_ACT	BR3_ACT
DEFAULT VALUE	0	0	0	0	0	1	1	1
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	BR4_ ACT	SPARE	SIGN_FDAC_ BY2_2FOUT	PREFILT_ BYPASS	A_C_ OFF	B_D_OFF	DAC_EVEN_ SAMP	BYPASS
DEFAULT VALUE	1	0	0	0	0	0	0	0

BR1_ACT - DPD fdac_by2_3fout branch active - default is 1 (branch active).
BR2_ACT - DPD hd3 & hd2 branch active - default is 1 (branch active).
BR3_ACT - DPD interleaving error comp branch active - default is 1 (branch active).
BR4_ACT - DPD fdac_by2_2fout branch active - default is 1 (branch active).
SPARE: DPD spare.
PREFILT_BYPASS: Prefilter bypassing in Fdac/2-2Fout DPD.
SIGN_FDAC_BY2_2FOUT: Sign of Fdac/2-2Fout comp for RF-DAC ports A,B,C,D.
A_C_OFF: Output buses A and C off.
B_D_OFF: Output buses B and D off.
DAC_EVEN_SAMP: RF-DAC even-sampling.
BYPASS: Enable DPD bypass.

Table 71. DPD_2 Register (0x082)

ADDRESS	0x082							
REGISTER NAME	DPD_2							
DESCRIPTION	DPD Delay 1							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	—	—	—	—	—	—
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	—	D1[3]	D1[2]	D1[1]	D1[0]
DEFAULT VALUE	0	0	0	0	0	0	0	1

D1[3:0] : DPD Delay 1 [3:0]

Table 72. DPD_3 Register (0x083)

ADDRESS	0x083							
REGISTER NAME	DPD_3							
DESCRIPTION	DPD Delay 2							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	—	—	—	—	—	—
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	—	D2[3]	D2[2]	D2[1]	D2[0]
DEFAULT VALUE	0	0	0	0	1	1	0	0

D2[3:0] : DPD Delay 2 [3:0]

Table 73. DPD_4 Register (0x084)

ADDRESS	0x084							
REGISTER NAME	DPD_4							
DESCRIPTION	DPD Delay 3							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	—	—	—	—	—	—
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	—	D3[3]	D3[2]	D3[1]	D3[0]
DEFAULT VALUE	0	0	0	0	0	1	1	0

D3[3:0] : DPD Delay 3 [3:0]

Table 74. DPD_5 Register (0x085)

ADDRESS	0x085							
REGISTER NAME	DPD_5							
DESCRIPTION	DPD gain 1							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	—	—	—	—	G1[11]	G1[10]	G1[9]	G1[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G1[11:0]: DPD gain 1 [11:0] (two's complement data format).

Table 75. DPD_6 Register (0x086)

ADDRESS	0x086							
REGISTER NAME	DPD_6							
DESCRIPTION	DPD gain 2							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	G2[11]	G2[10]	G2[9]	G2[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G2[11:0]: DPD gain 2 [11:0] (two's complement data format).

Table 76. DPD_7 Register (0x087)

ADDRESS	0x087							
REGISTER NAME	DPD_7							
DESCRIPTION	DPD gain 3							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	G3[11]	G3[10]	G3[9]	G3[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G3[7]	G3[6]	G3[5]	G3[4]	G3[3]	G3[2]	G3[1]	G3[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G3[11:0]: DPD gain 3 [11:0] (two's complement data format).

Table 77. DPD_8 Register (0x088)

ADDRESS	0x088							
REGISTER NAME	DPD_8							
DESCRIPTION	DPD gain 4							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	G4[11]	G4[10]	G4[9]	G4[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G4[7]	G4[6]	G4[5]	G4[4]	G4[3]	G4[2]	G4[1]	G4[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G4[11:0]: DPD gain 4 [11:0] (two's complement data format).

Table 78. DPD_9 Register (0x089)

ADDRESS	0x089							
REGISTER NAME	DPD_9							
DESCRIPTION	DPD gain 5							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	G5[11]	G5[10]	G5[9]	G5[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G5[7]	G5[6]	G5[5]	G5[4]	G5[3]	G5[2]	G5[1]	G5[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G4[11:0]: DPD gain 4 [11:0] (two's complement data format).

Table 79. DPD_10 Register (0x08A)

ADDRESS	0x08A							
REGISTER NAME	DPD_10							
DESCRIPTION	DPD gain 6							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	G6[11]	G6[10]	G6[9]	G6[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G6[7]	G6[6]	G6[5]	G6[4]	G6[3]	G6[2]	G6[1]	G6[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G6[11:0]: DPD gain 6 [11:0] (two's complement data format).

Table 80. DPD_11 Register (0x08B)

ADDRESS	0x08B							
REGISTER NAME	DPD_11							
DESCRIPTION	DPD gain 7							
BIT	15	14	13	12	11	10	9	8
NAME	SPARE[3]	SPARE[2]	SPARE[1]	SPARE[0]	G7[11]	G7[10]	G7[9]	G7[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G7[7]	G7[6]	G7[5]	G7[4]	G7[3]	G7[2]	G7[1]	G7[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G7[11:0]: DPD gain 7 [11:0] (two's complement data format).
SPARE[3:0]: Spare.

Table 81. DPD_12 Register (0x08C)

ADDRESS	0x08C							
REGISTER NAME	DPD_12							
DESCRIPTION	DPD gain 8							
BIT	15	14	13	12	11	10	9	8
NAME	SPARE[3]	SPARE[2]	SPARE[1]	SPARE[0]	G8[11]	G8[10]	G8[9]	G8[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G8[7]	G8[6]	G8[5]	G8[4]	G8[3]	G8[2]	G8[1]	G8[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G8[11:0]: DPD gain 8 [11:0] (two's complement data format).
SPARE[3:0]: Spare.

Table 82. DPD_13 Register (0x08D)

ADDRESS	0x08D							
REGISTER NAME	DPD_13							
DESCRIPTION	DPD gain 9							
BIT	15	14	13	12	11	10	9	8
NAME	SPARE[7]	SPARE[6]	SPARE[5]	SPARE[4]	SPARE[3]	SPARE[2]	SPARE[1]	SPARE[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G9[7]	G9[6]	G9[5]	G9[4]	G9[3]	G9[2]	G9[1]	G9[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G9[7:0]: DPD gain 9 [7:0] (two's complement data format).
SPARE[7:0]: Spare.

Table 83. DPD_14 Register (0x08E)

ADDRESS	0x08E							
REGISTER NAME	DPD_14							
DESCRIPTION	DPD gain 10							
BIT	15	14	13	12	11	10	9	8
NAME	SPARE[7]	SPARE[6]	SPARE[5]	SPARE[4]	SPARE[3]	SPARE[2]	SPARE[1]	SPARE[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	G10[7]	G10[6]	G10[5]	G10[4]	G10[3]	G10[2]	G10[1]	G10[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

G10[7:0]: DPD gain 10 [7:0] (two's complement data format).
SPARE[7:0]: Spare.

CHAN8 PWR REGISTERS

Table 84. RRC_I_PWR Registers

There is a RRC_I_PWR register for each of the 128 channels.

ADDRESS	0x600 + ((ch# -1) * 0x04), ch# = 1 to 128							
REGISTER NAME	RRC_I_PWR_ch#							
DESCRIPTION	Channel RRC I power							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[11:0] : Power monitor threshold count, I path

Table 85. RRC_Q_PWR Registers

There is a RRC_Q_PWR register for each of the 128 channels.

ADDRESS	0x601 + ((ch# -1) * 0x04), ch# = 1 to 128							
REGISTER NAME	RRC_Q_PWR_ch#							
DESCRIPTION	Channel RRC Q power							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[11:0] : Power monitor threshold count, Q path

Table 86. MOD1_I_PWR Registers

There is a MOD1_I_PWR register for each of the 128 channels.

ADDRESS	0x602 + ((ch# -1) * 0x04), ch# = 1 to 128							
REGISTER NAME	MOD1_I_PWR_ch#							
DESCRIPTION	Channel MOD1 I power							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[11:0] : Power monitor threshold count, I path

Table 87. MOD_1_Q_PWR Registers

There is a MOD1_Q_PWR register for each of the 128 channels.

ADDRESS	0x603 + ((ch# -1) * 0x04), ch# = 1 to 128							
REGISTER NAME	MOD1_Q_PWR_ch#							
DESCRIPTION	Channel MOD1 Q power							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	COUNT[11]	COUNT[10]	COUNT[9]	COUNT[8]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

COUNT[11:0] : Power monitor threshold count, Q path

PRBS REGISTERS

Table 88. PRBS Registers

There are 64 PRBS seed registers, each containing two seeds (for a total of 128 seeds, one per channel).

ADDRESS	0xA00 + int((ch# - 1)/2) + int ((ch# - 1)/8) *4, ch# = 1 to 128							
REGISTER NAME	PRBS							
DESCRIPTION	PRBS Seed register							
BIT	15	14	13	12	11	10	9	8
NAME	SEEDB[7]	SEEDB[6]	SEEDB[5]	SEEDB[4]	SEEDB[3]	SEEDB[2]	SEEDB[1]	SEEDB[0]
BIT	7	6	5	4	3	2	1	0
NAME	SEEDA[7]	SEEDA[6]	SEEDA[5]	SEEDA[4]	SEEDA[3]	SEEDA[2]	SEEDA[1]	SEEDA[0]

SEEDA[7:0]: 8-channel seed A [7:0].
SEEDB[7:0]: 8-channel seed B [7:0].
Seed register = 0xA00 + int ((ch# - 1) / 2) , ch# = 1 to 128.
SEEDB (bits 15:8]) is the even-channel seed (2, 4, 6, 8, 10, etc.).
SEEDA (bits 7:0]) is the odd-channel seed (1, 3, 5, 7, 9, etc.).
The d1 delay bits of the SYMIF register (one set per channel) are also used for the seed.

EFUSE REGISTERS

Table 89. MASTER_KEY_1 Register (0x010)

ADDRESS	0x010							
REGISTER NAME	MASTER_KEY_1							
BIT	15	14	13	12	11	10	9	8
NAME	MKEY[15]	MKEY[14]	MKEY[13]	MKEY[12]	MKEY[11]	MKEY[10]	MKEY[9]	MKEY[8]
BIT	7	6	5	4	3	2	1	0
NAME	MKEY[7]	MKEY[6]	MKEY[5]	MKEY[4]	MKEY[3]	MKEY[2]	MKEY[1]	MKEY[0]

MKEY[15:0] : Master key, low order word, bits [15:0], read-only

Table 90. MASTER_KEY_2 Register (0x011)

ADDRESS	0x011							
REGISTER NAME	MASTER_KEY_2							
BIT	15	14	13	12	11	10	9	8
NAME	MKEY[31]	MKEY[30]	MKEY[29]	MKEY[28]	MKEY[27]	MKEY[26]	MKEY[25]	MKEY[24]
BIT	7	6	5	4	3	2	1	0
NAME	MKEY[23]	MKEY[22]	MKEY[21]	MKEY[20]	MKEY[19]	MKEY[18]	MKEY[17]	MKEY[16]

MKEY[31:16] : Master key, bits [31:16], read-only

Table 91. MASTER_KEY_3 Register (0x012)

ADDRESS	0x012							
REGISTER NAME	MASTER_KEY_3							
BIT	15	14	13	12	11	10	9	8
NAME	MKEY[47]	MKEY[46]	MKEY[45]	MKEY[44]	MKEY[43]	MKEY[42]	MKEY[41]	MKEY[40]
BIT	7	6	5	4	3	2	1	0
NAME	MKEY[39]	MKEY[38]	MKEY[37]	MKEY[36]	MKEY[35]	MKEY[34]	MKEY[33]	MKEY[32]

MKEY[47:32] : Master key, bits [47:32], read-only

Table 92. MASTER_KEY_4 Register (0x013)

ADDRESS	0x013							
REGISTER NAME	MASTER_KEY_4							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	—	—	—	—
BIT	7	6	5	4	3	2	1	0
NAME	MKEY[55]	MKEY[54]	MKEY[53]	MKEY[52]	MKEY[51]	MKEY[50]	MKEY[49]	MKEY[48]

MKEY[55:48] : Master key, high order word, bits [55:48], read-only

Table 93. FACTORY_CAP Register (0x014)

ADDRESS	0x014							
REGISTER NAME	FACTORY_CAP							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	—	—	—	—
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	INFO[3]	INFO[2]	INFO[1]	INFO[0]	FCAP[3]	FCAP[2]	FCAP[1]	FCAP[0]
DEFAULT VALUE	INFO	INFO	INFO	INFO	FCAP	FCAP	FCAP	FCAP

INFO[3:0]: Maximum channel capacity information, bits [3:0].
0001 = 8-channel max capacity (not upgradable)
0010 = 16-channel max capacity (not upgradable)
0011 = 24-channel max capacity (not upgradable)
0100 = 32-channel max capacity (not upgradable)
0101 to 1111 = Reserved
FCAP[3:0]: Factory-programmed channel capacity, bits [3:0].
0000 = 8 channels
0001 = 16 channels
0010 = 24 channels
0011 = 32 channels

Table 94. KEY_STATUS Register (0xA98)

ADDRESS	0xA98							
REGISTER NAME	KEY_STATUS							
DESCRIPTION	Key status and current channel capacity.							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	—	—	—	—	—
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	—	—	COMP	MATCH	CCAP[3]	CCAP[2]	CCAP[1]	CCAP[0]
DEFAULT VALUE	0	0	0	0	FCAP	FCAP	FCAP	FCAP

COMP: When 1, the upgraded channel capacity is in use instead of the factory-default capacity.
MATCH: When 1, the upgrade key is valid.
CCAP[3:0] - Current maximum channel capacity displayed in 8-channel increments:
0000 = 8 channels
0001 = 16 channels
0010 = 24 channels
0011 = 32 channels

The default value for CCAP[3:0] is FC[3:0] which is the factory-default channel capacity.

Table 95. UPGRADE_CAP Register (0x015)

ADDRESS	0x015							
REGISTER NAME	UPGRADE_CAP							
BIT	15	14	13	12	11	10	9	8
NAME	—	—	—	DFLAG	DCAP[3]	DCAP[2]	DCAP[1]	DCAP[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	—	UCAP[3]	UCAP[2]	UCAP[1]	UCAP[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

DFLAG: When 1 indicates, downsized capacity is in use.
DCAP[3:0]: Downsized channel capacity , bits [3;0].
UCAP[3:0]: Soft upgrade capacity value, bits [3:0].

DLL REGISTERS

Table 96. DLLCTRL Register (0xA80)

ADDRESS	0xA80							
REGISTER NAME	DLLCTRL							
DESCRIPTION	DLL Control Register							
BIT	15	14	13	12	11	10	9	8
NAME	BW	POL	ICP[1]	ICP[0]	PH[3]	PH[2]	PH[1]	PH[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	7	6	5	4	3	2	1	0
NAME	OFF	EFUSE	EVREF	AMUX	FRNG[1]	FRNG[0]	ILVDS	LOCK
DEFAULT VALUE	1	0	0	0	0	0	0	0

BW: DLL loop bandwidth.
0: Normal 16 bits integrator
1: High bandwidth 12 bits integration
POL: Internally inverts DLL clock.
0: Normal
1: DLL clock output inverted
ICP[1:0]: DLL2 P-source adjustment [1:0].
PH[3:0]: DUC data and dataclk adjustment bits [3:0].
OFF: DLL on/off control.
0: DLL on
1: DLL off and held in reset
EFUSE: Select trim value.
1: SPI
0: eFuse (+)
EVREF:
1: Default selecting internal 1.25 reference
1: Select external reference
AMUX: Trim current output.
0: Analog mux is off
1: Analog mux is on for ITRIMP output,
FRNG[1:0]: DLL frequency range select [1:0].
00: Normal
01: One step down
10: One step up
11: Two steps up <rsvd> [1:0]
ILVDS: Transmit LVDS current select.
0: Default 3.5mA
1: Half current 1.75mA
LOCK: DLL lock indicator.
1: DLL locked
0: DLL unlocked

Table 97. DLLTRIM Register (0xA88)

ADDRESS	0xA88							
REGISTER NAME	DLLTRIM							
DESCRIPTION	DLL Trim Register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	VTRIM[2]	VTRIM[1]	VTRIM[0]	ITRIM[1]	ITRIM[0]	ITRIMP[2]	ITRIMP[1]	ITRIMP[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	EFUSE[7]	EFUSE[6]	EFUSE[5]	EFUSE[4]	EFUSE[3]	EFUSE[2]	EFUSE[1]	EFUSE[0]
DEFAULT VALUE	T	T	T	T	T	T	T	T

VTRIM[2:0]: internal band-gap trim bits [2:0].
ITRIM[4:3]: Ibc biasing current trim [1;0].
ITRIMP[2:0]: Ibp biasing current trim [2:0].
EFUSE[7:0]: DLL trim value stored in EFUSE. [7:0].
T = Trim bit value set during manufacturing test.

Table 98. DLL Register (0xA89)

ADDRESS	0xA89							
REGISTER NAME	DLL							
DESCRIPTION	DLL clock select and trim enable code register							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	BCLK	—	TEN[2]	TEN[1]	TEN[0]	—	—	—
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	—	—	—	—	—
DEFAULT VALUE	0	0	0	0	0	0	0	0

BCLK : When 0, use CLKOUT from DLL (instead of LCLK).
TEN[13:11] : Trim enable switch (Manufacturing test only)
A value of 101 and dllctrl_efuse high allows selecting trim value from SPI registers.

Table 99. OEM_TEST Register (0x003)

ADDRESS	0x003							
REGISTER NAME	OEM_TEST							
DESCRIPTION	Test the full bandwidth (up to 128 channels) of the MAX5862 by using the channel PRBS generators or by streaming data from one of eight port/time slots.							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NAME	CW[3]	CW[2]	CW[1]	CW[0]	—	—	—	—
DEFAULT VALUE	0	0	0	0	0	0	0	0
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	—	—	—	SGRP[1]	SGRP[0]
DEFAULT VALUE	0	0	0	0	0	0	0	0

CW[3:0]: Control Word - Set to “1101” to enable OEM_TEST function.
Any other data in CW[3:0] disables this test function.
SGRP[1:0]: Select Slot Group (Group of 8 enabled timeslots).
00: timeslots 1–8
01: timeslots 9–16
10: timeslots 17–24
11: timeslots 25–32

Static Performance Parameter Definitions

Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two midscale digital input codes, with respect to the full scale of the DAC. This error affects all codes by the same amount.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Dynamic Performance Parameter Definitions

Noise Spectral Density

The DAC output noise is the sum of the quantization noise and other noise sources. Noise spectral density is the noise power in a 1Hz bandwidth.

Two-/Four-Tone Intermodulation Distortion (IMD)

The two-/four-tone IMD is the ratio expressed in dBc (or dBFS) of the worst 3rd-order (or higher) IMD products to any output tone.

Adjacent Channel Power (ACP)

Adjacent channel power is commonly used in combination with DOCSIS-compliant QAM signals. ACP is the ratio in dB between the power in a channel at a specified frequency offset from the edge of the transmitted channel block, and power in the lowest frequency channel of the transmitted block. ACP provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

Ordering Information

PART*	TEMP RANGE	PIN-PACKAGE	FUNCTION
MAX5862AUXH+	0°C to +110°C	280 FCBGA	8-Channel QAM Modulator
MAX5862BUXH+	0°C to +110°C	280 FCBGA	16-Channel QAM Modulator
MAX5862CUXH+	0°C to +110°C	280 FCBGA	24-Channel QAM Modulator
MAX5862DUXH+	0°C to +110°C	280 FCBGA	32-Channel QAM Modulator

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
280 FCBGA	X28027FM+1	**21-0652**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/13	Initial release	—

