EVALUATION KIT AVAILABLE

MAX8967

Dual 2A Step-Down Converters with 6 LDOs for Baseband and Applications Processor

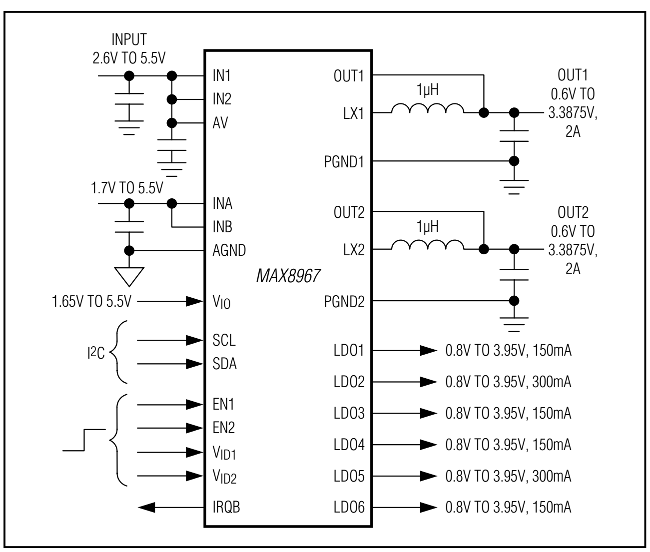
General Description

The MAX8967 is an μPMIC with two DC-to-DC step-down switching converters and six remote capacitor-capable LDOs. The step-down converters deliver up to 2A of output current independently. Two of the LDOs deliver a load current up to 300mA, while the remaining four deliver up to 150mA. Both step-down converters have remote sense, allowing loads to be placed away from the IC. The IC operates over a 2.6V to 5.5V input supply range.

Fixed-frequency 4.4MHz PWM operation and clocks that are 180° out of phase permit the use of small external components. Under light load conditions, the step-down converters automatically switch to skip mode operation. In skip mode operation, switching occurs only as needed, allowing efficient operation. Placing either of the step-down converters into green mode reduces the quiescent current consumption of that converter to 5μA (typ).

The IC supports dynamic adjustment of the output voltage through its I^2C interface. Each step-down converter has two register settings for output voltage and a setting for ramp rate. Also, each step-down converter has a dedicated enable pin and a dedicated V_{ID} pin to toggle between the two programmed output voltages. Additionally, an interrupt output is provided, allowing the IC to signal its master.

Typical Operating Circuit



Benefits and Features

- Multi-Output PMIC in a Compact Package
  - Two 2A Step-Down Converters with Remote Output Voltage Sensing
  - Two 300mA LDOs
  - Four 150mA LDOs
  - < 1μA Shutdown Current
  - 2.32mm x 2.44mm Package
- Versatile Step-Down Converters
  - Programmable Output Voltage (0.6V to 3.3875V) Through I^2C Bus
  - Programmable Output Voltage Slew Rate (12.5mV/μs to 50mV/μs)
  - Dynamic Switching Between Two Output Voltages Through $V_{ID\_}$ Pins
- Efficient Step-Down Converters
  - Over 95% Efficiency with Internal Synchronous Rectifier
  - Automatic Skip Mode at Light Loads
  - Low 61μA (typ) Quiescent Current
  - 5μA (typ) Green Mode per Step-Down Converter
- Programmable LDOs
  - Programmable Output Voltage (0.8V to 3.95V in 50mV Steps)
  - Programmable Soft-Start Slew Rate (5mV/μs–100mV/μs)
- Reduces Component Size and Board Area Solution
  - 4.4MHz Step-Down Switching Allows for 1μH Inductors
  - C_{OUT} = 1μF for All LDOs
  - Reduced Board Space with Remote Capacitor LDOs
  - Internal Feedback for Step-Down Converters and LDOs

Applications

Cellular Handsets and Smartphones

Tablets

Portable Devices

***Ordering Information* appears at end of data sheet.**

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to:* ***www.maximintegrated.com/errata****.*

ABSOLUTE MAXIMUM RATINGS

IN1, IN2, INA, INB, AV, OUT1, OUT2, ,SCL, SDA, SNSP1, SNSN1, SNSP2, SNSN2 to AGND....................-0.3V to +6.0V
EN1, EN2, $V_{ID\_}$, V_{IO}, IRQB to AGND...... -0.3V to (V_{AV} + 0.3V)
LDO1, LDO2, LDO3 to AGND.................-0.3V to (V_{INA} + 0.3V)
LDO4, LDO5, LDO6 to AGND.................-0.3V to (V_{INB} + 0.3V)
PGND1, PGND2 to AGND ....-0.3V to +0.3V
LX1, LX2 Current ....2.0A_{RMS}

Continuous Power Dissipation (T_A = +70°C)
30-Bump, 2.32mm x 2.44mm WLP (derate 20.4mW/°C above +70°C)............................1632mW
Operating Temperature..................................... -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range............................ -65°C to +150°C
Soldering Temperature (reflow) ....+260°C

CAUTION! ESD SENSITIVE DEVICE

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA})..........49°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....9°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Input Voltage Range	V_{INPUT}	V_{IN1} = V_{IN2} = V_{AV}		2.6		5.5	V
Overvoltage Lockout	OVP	V_{AV} rising, 100mV hysteresis		5.70	5.85	6.00	V
AV Undervoltage Lockout (UVLO)	UVLO	V_{AV} rising, 55mV hysteresis		2.3	2.4	2.5	V
V_{IO} Operating Range	V_{IO}			1.65		5.5	V
V_{IO} Enable Threshold High				1.4			V
V_{IO} Enable Threshold Low						0.4	V
V_{IO} Enable Hysteresis					100		mV
V_A Shutdown Current		V_{AV} > 2.6V, V_{IO} < 0.4V, EN1 = EN2 = 0	T_A = +25°C	-5	+0.1	+0.5	µA
			T_A = +85°C		0.1		
V_A Standby Current		V_{AV} > 2.6V, V_{IO} > 1.4V, EN1 = EN2 = 0			28		µA
V_{IO} Supply Current		All logic in high or low state			0.1		µA
Quiescent Current (Green Mode)		No switching, $V_{OUT\_}$ = 1.2V, step-down converter in green mode, all LDOs off			5		µA
Quiescent Current (Step-Down Converters On)		No switching, $V_{OUT\_}$ = 1.2V remote sense off			61	85	µA
Quiescent Current (All On Normal Mode)		No switching, $V_{OUT\_}$ = 1.2V, remote sense off, both step-down converters in normal mode, all LDOs on			176		µA
Quiescent Current (Step-Down Converters On, Normal Mode Remote sense ON)		No switching, $V_{OUT\_}$ = 1.2V, remote sense on, both step-down converters on			75	120	µA

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current (All On Green Mode)		No switching, $V_{OUT\_}$= 1.2V, both step-down converters in green mode, all LDOs on			40		µA
FPWM Current		Forced PWM, one step-down converter on only, I_{OUT} = 0A, C_{OUT1} = C_{OUT2} = 22µF, L1 = L2 = 1µH, V_{OUT} = 1.2V			9		mA
Thermal Shutdown		T_A rising, 20°C hysteresis			+160		°C
STEP-DOWN CONVERTER 1							
Output Current		L = 1µH		2			A
Adjustable Output Voltage Range		12.5mV steps		0.6000		3.3875	V
Settling Time		FPWM, I_{OUT1} = 0.2A C_{OUT1} = 22µF, L = 1µH, measure from V_{OUT1} = 1V to V_{OUT1} = 1.2V		20			µs
Output Voltage Accuracy (FPWM)		V_{OUT1} = 1.2V, FPWM, V_{OUT1} < 0.95 x V_{IN}, remote sense disabled (Note 3)		1.176	1.20	1.224	V
Output Voltage Accuracy (Green Mode)		Green mode, I_{OUT1} ≤ 5mA (Note 3)		1.152	1.200	1.248	V
Line Regulation		V_{OUT1} = 1.2V, I_{OUT1} = 0.2A, C_{OUT1} = 22µF, L = 1µH			0.04		%/V
Load Regulation		V_{OUT1} = 1.2V, 0 ≤ I_{OUT1} ≤ 2A			+0.125		%/A
Switching Frequency				3.96	4.40	4.84	MHz
Peak Current Limit		FPWM mode		2500	3000	3600	mA
Valley Current Limit		FPWM mode			1800		mA
Negative Current limit		FPWM mode			1		A
Zero-Crossing Current Threshold		Used in skip mode and green mode			20		mA
PMOS On-Resistance		$V_{IN\_}$ = 3.6V, I_{OUT1} = 190mA			60		mΩ
NMOS On-Resistance		$V_{IN\_}$ = 3.6V, I_{OUT1} = 190mA			50		mΩ
LX Leakage		V_{LX1} = V_{IN} , 0V	T_A = +25°C	-1	0.1	+1	µA
			T_A = +85°C		1		
Output Discharge Resistor in Shutdown		Feature must be active, see the *Register Definitions* section			100		Ω

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_} = V_{AV} = 3.6V$, $V_{IO} = 1.8V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are $T_A = +25°C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Step Ramp Rate		Slew_ _[7:6] = 00, see Table 15		12.5		mV/µs
		Slew_ _[7:6] = 01, see Table 15		25		
		Slew_ _[7:6] = 10, see Table 15		50		
Load Transient FPWM		FPWM mode, V_{OUT1} = 1.2V, load steps between 0.2 to 1.2A in 30ns, C_{OUT1} = 22µF, L = 1µH		40		mV
Load Transient (Skip Mode)		Skip mode, V_{OUT} = 1.2V, load steps between 0.2 to 1.2A in 30ns, C_{OUT1} = 22µF, L = 1µH		40		mV
Line Transient		V_{OUT} = 1.2V, I_{OUT1} = 1.2A, C_{OUT1} = 22µF, L = 1µH.		0.25		%/V
Overshoot		Transitions between output voltage states 1.0 and 1.4V, I_{OUT1} = 400mA, C_{OUT1} = 22µF, L = 1µH		40		mV
Chip Enable Time		From chip standby state until first output voltage ramp starts		250		µs
Enable Time		From enabling until voltage ramp starts, the IC is in normal operating state with previous state shut down, $I_{OUT1} \leq$ 100mA, L = 1µH, C_{OUT1} = 22µF		25		µs
Output POK Threshold		V_{OUT1} falling, 1.2V nominal setting	86	90	94	$\%V_{OUT1}$
Output POK Threshold Hysteresis				3		%
Minimum Output Capacitance				12		µF
Minimum Inductance		1µH inductor with 30% duration		1		µH
STEP-DOWN CONVERTER 2						
Output Current		L = 1µH	2			A
Adjustable Output Voltage Range		12.5mV steps	0.6000		3.3875	V
Settling Time		FPWM, I_{OUT2} = 0.2A, C_{OUT2} = 22µF, L = 1µH, measure from V_{OUT2} = 1V to V_{OUT2} = 1.2V		20		µs
Output Voltage Accuracy (FPWM)		V_{OUT2} = 1.2V, FPWM, V_{OUT2} < 0.95 x V_{IN}, remote sense disabled (Note 3)	1.176	1.20	1.224	V
Output Voltage Accuracy (Green Mode)		Green mode, $I_{OUT2} \leq$ 5mA (Note 3)	1.152	1.200	1.248	V
Line Regulation		V_{OUT2} = 1.2V, I_{OUT2} = 0.2A, C_{OUT2} = 22µF, L = 1µH		0.04		%/V

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation		V_{OUT2} = 1.2V, 0 ≤ I_{OUT2} ≤ 2A			+0.125		%/A
Switching Frequency				3.96	4.40	4.84	MHz
Peak Current Limit		FPWM mode		2500	3000	3600	mA
Valley Current Limit		FPWM mode			1800		mA
Negative Current Limit		FPWM mode			1		A
Zero-Crossing Current Threshold		Used in skip mode and green mode			20		mA
PMOS On-Resistance		$V_{IN\_}$ = 3.6V, I_{OUT2} = 190mA			60		mΩ
NMOS On-Resistance		$V_{IN\_}$ = 3.6V, I_{OUT2} = 190mA			50		mΩ
LX Leakage		V_{LX2} = V_{IN} ,0V	T_A = +25°C	-1	0.1	+1	µA
			T_A = +85°C		1		
Output Discharge Resistor in Shutdown		Feature must be active, see the *Register Definitions* section			100		Ω
Output Step Ramp Rate		Slew_ _[7:6] = 00, see Table 15			12.5		mV/µs
		Slew_ _[7:6] = 01, see Table 15			25		
		Slew_ _[7:6] = 10, see Table 15			50		
Load Transient FPWM		FPWM mode, V_{OUT2} = 1.2V, load steps between 0.2 to 1.2A in 30ns, C_{OUT2} = 22µF, L = 1µH			40		mV
Load Transient (Skip Mode)		Skip mode, V_{OUT2} = 1.2V, load steps between 0.2 to 1.2A in 30ns, C_{OUT2} = 22µF, L = 1µH			40		mV
Line Transient		V_{OUT2} = 1.2V, I_{OUT2} = 1.2A, C_{OUT2} = 22µF, L = 1µH			0.25		%/V
Overshoot		Transitions between output voltage states 1.0V and 1.4V, I_{OUT21} = 400mA, C_{OUT2} = 22µF, L = 1µH			40		mV
Chip Enable Time		From chip standby state until first output voltage ramp starts			250		µs
Enable Time		From enabling until voltage ramp starts; the IC is in normal operating state with previous state shut down, I_{OUT2} ≤ 100mA, L = 1µH, C_{OUT2} = 22µF			25		µs
Output POK Threshold		V_{OUT2} falling, 1.2V nominal setting		86	90	94	%V_{OUT2}
Output POK Threshold Hysteresis					3		%
Minimum Output Capacitance					12		µF
Minimum Inductance		1µH inductor with 30% duration			1		µH

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO1							
Input Voltage Range	$V_{IN,LDO1}$			1.7		5.5	V
Undervoltage Lockout	$V_{UVLO,LDO1}$	$V_{IN,LDO1}$ rising, 100mV hysteresis			1.6	1.7	V
Output Voltage Range	$V_{OUT,LDO1}$	V_{INLDO1} is the maximum of 3.7V or $V_{OUT,LDO1}$ + 0.3V		0.8		3.95	V
Maximum Output Current	$I_{MAX,LDO1}$	Normal mode		150			mA
		Green mode		5			
Minimum Output Capacitance	$C_{OUT,LDO1}$	(Note 4)	Normal mode		0.7		µF
			Green mode		0.7		
Bias Enable Time	t_{LBIAS1}	Time to enable LDO bias only, central bias is already enabled			90		µs
Bias Enable Currents	I_{QBIAS1}	LDO bias enabled, LDOBIASEN = 1			10		µA
AV Supply Current	$I_{AV,LDO1}$	No load	Shutdown, T_A = +25°C (Note 5)		0		µA
			Normal regulation		3	6	
			Green mode		0.5	3	
INA Input Supply Current	$I_{IN,LDO1}$	No load	Shutdown, T_A = +25°C (Note 6)		0		µA
			Normal regulation		15	30	
			Green mode		1	3	
Output Voltage Accuracy		Normal mode	$V_{IN,LDO1}$ = V_{NOM} + 0.3V to 5.5V with 1.7V minimum, $I_{OUT,LDO1}$ = 0.1mA to $I_{MAX,LDO1}$, $V_{NOM,LDO1}$ set to any voltage	-3		+3	%
		Green mode	$V_{IN,LDO1}$ = $V_{NOM,LDO1}$ + 0.3V to 5.5V with 2.4V minimum, $I_{OUT,LDO1}$ = 0.1mA to 5mA, $V_{NOM,LDO1}$ set to any voltage	-5		+5	

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Load Regulation (Note 7)		Normal mode	$I_{OUT,LDO1}$ = 0.1mA to $I_{MAX,LDO1}$, $V_{IN,LDO1}$ = $V_{NOM,LDO1}$ + 0.3V with 1.7V minimum, $V_{NOM,LDO1}$ set to any voltage			0.1		%
		Green mode	$I_{OUT,LDO1}$ = 0.1mA to 5mA, $V_{IN,LDO1}$ = $V_{NOM,LDO1}$ + 0.3V with 2.4V minimum, $V_{NOM,LDO1}$ set to any voltage			0.2		
Line Regulation (Note 7)		Normal mode	$V_{IN,LDO1}$ = $V_{NOM,LDO1}$ + 0.3V to 5.5V with 1.7V minimum, $I_{OUT,LDO1}$ = 0.1mA, $V_{NOM,LDO1}$ set to any voltage			0.03		%/V
		Green mode	$V_{IN,LDO1}$ = $V_{NOM,LDO1}$ + 0.3V to 5.5V with 2.4V minimum, $I_{OUT,LDO1}$ = 0.1mA, $V_{NOM,LDO1}$ set to any voltage			0.1		
Dropout Voltage	$V_{DO,LDO1}$	Normal mode	$I_{OUT,LDO1}$ = $I_{MAX,LDO1}$	$V_{IN,LDO1}$ = 3.7V		60	120	mV
				$V_{IN,LDO1}$ = 1.7V		150	300	
		Green mode	$I_{OUT,LDO1}$ = 5mA, $V_{IN,LDO1}$ = 3.7V			50	100	
Output Current Limit	$I_{LIM,LDO1}$	$V_{OUT,LDO1}$ = 0V			150	225	375	mA
Output Load Transient (LDO1OVCLMP_EN = 1) (Notes 4, 7)		Normal mode, $V_{IN,LDO1}$ = $V_{NOM,LDO1}$ + 0.3V to 5.5V with 1.7V absolute minimum, $I_{OUT,LDO1}$ = 1% to 100% to 1% of $I_{MAX,LDO1}$, $V_{NOM,LDO1}$ set to any voltage, t_{R1} = t_{F1} = 1µs, LDO1COMP[5:4] = 01				66		mV
		Green mode, $V_{IN,LDO1}$ = $V_{NOM,LDO1}$ + 0.3V to 5.5V with 2.4V absolute minimum, $I_{OUT,LDO1}$ = 0.05mA to 5mA to 0.05mA, $V_{NOM,LDO1}$ set to any voltage, t_{R1} = t_{F1} = 1µs				25		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Line Transient (Notes 3, 6)		Normal mode, $V_{IN,LDO1}$ = $V_{NOM,LDO1}$ + 0.3V to $V_{NOM,LDO1}$ + 0.8V to $V_{NOM,LDO1}$ + 0.3V with 1.7V absolute minimum, t_{R1} = t_{F1} = 1µs, $I_{OUT,LDO1}$ = $I_{MAX,LDO1}$, $V_{NOM,LDO1}$ set to any voltage		5		mV
		Green mode, $V_{IN,LDO1}$ = $V_{NOM,LDO1}$ + 0.3V to $V_{NOM,LDO1}$ + 0.8V to $V_{NOM,LDO1}$ + 0.3V with 2.4V absolute minimum, t_{R1} = t_{F1} = 1µs, $I_{OUT,LDO1}$ = 5mA, $V_{NOM,LDO1}$ set to any voltage		5		
Power-Supply Rejection	$PSRR_{LDO1}$	Rejection from $V_{IN,LDO1}$ to $V_{OUT,LDO1}$ $I_{OUT,LDO1}$ = 10% of $I_{MAX,LDO1}$; $V_{INLDO1DC}$ = $V_{NOM,LDO1}$ + 0.3V, $V_{INLDO1AC}$ = 50mV; f = 1kHz		63		dB
		f = 10kHz		51		
		f = 100kHz		44		
		f = 1000kHz		57		
		f = 4450kHz		33		
		Green mode, $I_{OUT,LDO1}$ = 1mA, f = 1kHz, rejection from $V_{IN,LDO1}$ to $V_{OUT,LDO1}$		50		
Output Noise		f = 10Hz to 100kHz, $I_{OUT,LDO1}$ = 10% of $I_{MAX,LDO1}$; $V_{OUT,LDO1}$ = 0.8V		45		µV_{RMS}
		$V_{OUT,LDO1}$ = 1.8V		45		
		$V_{OUT,LDO1}$ = 3.7V		60		
Startup Ramp Rate	$t_{SS,LDO1}$	After enabling; LDO1SS = 0		100		mV/µs
		LD01SS = 1		5		
Active-Discharge Resistance		$V_{OUT,LDO1}$ = 1V, output disabled; Active discharge enabled, LDO1ADE = 1		0.16	0.3	kΩ
		Active discharge disabled, LDO1ADE = 0	1000			

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clamp Active Regulation Voltage		Clamp active (LDO1OVCLMP_EN = 1), LDO output sinking 0.1mA			$V_{NOM,LDO1}$		V
Clamp Disabled Overvoltage Sink Current		$V_{OUT,LDO1}$ = $V_{NOM,LDO1}$ x 110%			2.2		µA
Enable Delay (Note 4)	$t_{LON,LDO1}$	Time from LDO enable command received to the output starting to slew	Ramp rate = 100mV/µs		10		µs
			Ramp rate = 5mV/µs		60		
Disable Delay (Note 4)		After LDO is disabled; the LDO output voltage discharges based on load and C_{OUT}; to ensure fast discharge times, enable the active discharge resistor			0.1		µs
Transition Time from Green Mode to Normal Mode					10		µs
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
Power-OK Threshold	$V_{POKTHL1}$	$V_{OUT,LDO1}$ when V_{POK} switches	$V_{OUT,LDO1}$ rising		92	95	%
			$V_{OUT,LDO1}$ falling	84	87		
Power-OK Noise Pulse Immunity	V_{POKNF1}	$V_{OUT,LDO1}$ pulsed from 100% to 80% of regulation			25		µs
LDO2							
Input Voltage Range	$V_{IN,LDO2}$			1.7		5.5	V
Undervoltage Lockout	$V_{UVLO,LDO2}$	$V_{IN,LDO2}$ rising, 100mV hysteresis			1.6	1.7	V
Output Voltage Range	$V_{OUT,LDO2}$	$V_{IN,LDO2}$ is the maximum of 3.7V or $V_{OUT,LDO2}$ + 0.3V		0.8		3.95	V
Maximum Output Current	$I_{MAX,LDO2}$	Normal mode		300			mA
		Green mode		5			
Minimum Output Capacitance	$C_{OUT,LDO2}$	(Note 3)	Normal mode		0.7		µF
			Green mode		0.7		
Bias Enable Time	t_{LBIAS2}	Time to enable LDO bias only, central bias is already enabled			90		µs
Bias Enable Current	I_{LBIAS2}	LDO bias enabled			10		µA

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AV Supply Current	$I_{AV,LDO2}$	No load	Shutdown, T_A = +25°C (Note 5)		0		µA
			Normal regulation		3	6	
			Green mode		0.5	3	
INA Supply Current	$I_{IN,LDO2}$	No load	Shutdown, T_A = +25°C (Note 5)		0		µA
			Normal regulation		17	30	
			Green mode		1	3	
Output Voltage Accuracy		Normal mode	$V_{IN,LDO2}$ = $V_{NOM,LDO2}$ + 0.3V to 5.5V with 1.7V minimum, $I_{OUT,LDO2}$ = 0.1mA to $I_{MAX,LDO2}$, $V_{NOM,LDO2}$ set to any voltage	-3		+3	%
		Green mode	$V_{IN,LDO2}$ = $V_{NOM,LDO2}$ + 0.3V to 5.5V with 2.4V minimum, $I_{OUT,LDO2}$ = 0.1mA to 5mA, $V_{NOM,LDO2}$ set to any voltage	-5		+5	
Load Regulation (Note 6)		Normal mode	$I_{OUT,LDO2}$ = 0.1mA to $I_{MAX,LDO2}$, $V_{IN,LDO2}$ = $V_{NOM,LDO2}$ + 0.3V with 1.7V minimum, $V_{NOM,LDO2}$ set to any voltage		0.1		%
		Green mode	$I_{OUT,LDO2}$ = 0.1mA to 5mA, $V_{IN,LDO2}$ = $V_{NOM,LDO2}$ + 0.3V with 2.4V minimum, $V_{NOM,LDO2}$ set to any voltage		0.2		
Line Regulation (Note 6)		Normal mode	$V_{IN,LDO2}$ = $V_{NOM,LDO2}$ + 0.3V to 5.5V with 1.7V minimum; $I_{OUT,LDO2}$ = 0.1mA, $V_{NOM,LDO2}$ set to any voltage		0.03		%/V
		Green mode	$V_{IN,LDO2}$ = $V_{NOM,LDO2}$ + 0.3V to 5.5V with 2.4V minimum; $I_{OUT,LDO2}$ = 0.1mA, $V_{NOM,LDO2}$ set to any voltage		0.1		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Dropout Voltage	$V_{DO,LDO2}$	Normal mode	$I_{OUT,LDO2}$ = $I_{MAX,LDO2}$	$V_{IN,LDO2}$ = 3.7V		50	100	mV
				$V_{IN,LDO2}$ = 1.7V		150	450	
		Green mode	$I_{OUT,LDO2}$ = 5mA, $V_{IN,LDO2}$ = 3.7V			150	300	
Output Current Limit	$I_{LIM,LDO2}$	$V_{OUT,LDO2}$ = 0V			300	450	750	mA
Output Load Transient (LDO2OVCLMP_EN = 1) (Notes 3, 6)		Normal mode, $V_{IN,LDO2}$ = $V_{NOM,LDO2}$ + 0.3V to 5.5V with 1.7V absolute minimum; $I_{OUT,LDO2}$ = 1% to 100% to 1% of $I_{MAX,LDO2}$, $V_{NOM,LDO2}$ set to any voltage, t_{R2} = t_{F2} = 1µs, LDO2COMP[5:4] = 01				66		mV
		Green mode, $V_{IN,LDO2}$ = $V_{NOM,LDO2}$ + 0.3V to 5.5V with 2.4V absolute minimum; $I_{OUT,LDO2}$ = 0.05mA to 5mA to 0.05mA, $V_{NOM,LDO2}$ set to any voltage, t_{R2} = t_{F2} = 1µs				25		
Output Line Transient (Notes 3, 6)		Normal mode, $V_{IN,LDO2}$ = $V_{NOM,LDO2}$ + 0.3V to $V_{NOM,LDO2}$ + 0.8V to $V_{NOM,LDO2}$ + 0.3V with 1.7V absolute minimum; t_{R2} = t_{F2} = 1µs, $I_{OUT,LDO2}$ = $I_{MAX,LDO2}$, $V_{NOM,LDO2}$ set to any voltage				5		mV
		Green mode, $V_{IN,LDO2}$ = $V_{NOM,LDO2}$ + 0.3V to $V_{NOM,LDO2}$ + 0.8V to $V_{NOM,LDO2}$ + 0.3V with 2.4V absolute minimum; t_{R2} = t_{F2} = 1µs, $I_{OUT,LDO2}$ = 5mA, $V_{NOM,LDO2}$ set to any voltage				5		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection	$PSRR_{LDO2}$	Rejection from $V_{IN,LDO2}$ to $V_{OUT,LDO2}$ $I_{OUT,LDO2}$ = 10% of $I_{MAX,LDO2}$; $V_{INLDO2DC}$ = $V_{NOM,LDO2}$ +0.3V $V_{INLDO2AC}$ = 50mV; f = 1kHz		63		dB
		f = 10kHz		51		
		f = 100kHz		44		
		f = 1000kHz		57		
		f = 4450kHz		33		
		Green mode, $I_{OUT,LDO2}$ = 1mA, f = 1kHz, rejection from $V_{IN,LDO2}$ to $V_{OUT,LDO2}$		50		
Output Noise		f = 10Hz to 100kHz, $I_{OUT,LDO2}$ = 10% of $I_{MAX,LDO2}$; $V_{OUT,LDO2}$ = 0.8V		45		μV_{RMS}
		$V_{OUT,LDO2}$ = 1.8V		45		
		$V_{OUT,LDO2}$ = 3.7V		60		
Startup Ramp Rate	t_{SS22}	After enabling; LDO2SS = 0		100		mV/µs
		LDO2SS = 1		5		
Active-Discharge Resistance		$V_{OUT,LDO2}$ = 1V, output disabled; Active discharge enabled, LDO2ADE = 1		0.16	0.3	kΩ
		Active discharge disabled, LDO2ADE = 0	1000			
Clamp Active Regulation Voltage		Clamp active (LDO2OVCLMP_EN = 1), LDO output sinking 0.1mA		$V_{NOM,LDO2}$		V
Clamp Disabled Overvoltage Sink Current		$V_{OUT,LDO2}$ = $V_{NOM,LDO2}$ x 110%		2.2		µA
Enable Delay (Note 3)	t_{LON2}	Time from LDO enable command received to the output starting to slew; Ramp rate = 100mV/µs		10		µs
		Ramp rate = 5mV/µs		60		
Disable Delay (Note 3)		After LDO is disabled; the LDO output voltage discharges based on load and C_{OUT}; to ensure fast discharge times, enable the active discharge resistor		0.1		µs

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Transition Time from Green Mode to Normal Mode					10		µs
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
Power-OK Threshold	$V_{POKTHL2}$	$V_{OUT,LDO2}$ when V_{POK} switches	$V_{OUT,LDO2}$ rising		92	95	%
			$V_{OUT,LDO2}$ falling	84	87		
Power-OK Noise Pulse Immunity	V_{POKNF2}	$V_{OUT,LDO2}$ pulsed from 100% to 80% of regulation			25		µs
LDO3							
Input Voltage Range	$V_{IN,LDO3}$			1.7		5.5	V
Undervoltage Lockout	$V_{UVLO,LDO3}$	$V_{IN,LDO3}$ rising, 100mV hysteresis			1.6	1.7	V
Output Voltage Range	$V_{OUT,LDO3}$	$V_{IN,LDO3}$ is the maximum of 3.7V or $V_{OUT,LDO3}$ + 0.3V		0.8		3.95	V
Maximum Output Current	$I_{MAX,LDO3}$	Normal mode		150			mA
		Green mode		5			
Minimum Output Capacitance	$C_{OUT,LDO3}$	(Note 3)	Normal mode		0.7		µF
			Green mode		0.7		
Bias Enable Time	t_{LBIAS3}	Time to enable LDO bias only, central bias is already enabled			90		µs
Bias Enable Currents	I_{QBIAS3}	LDO bias enabled			10		µA
AV Supply Current	$I_{AV,LDO3}$	No load	Shutdown, T_A = +25°C (Note 4)		0		µA
			Normal regulation		3	6	
			Green mode		0.5	3	
INA Supply Current	$I_{IN,LDO3}$	No load	Shutdown, T_A = +25°C (Note 5)		0		µA
			Normal regulation		15	30	
			Green mode		1	3	

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage Accuracy		Normal mode	$V_{IN,LDO3}$ = $V_{NOM,LDO3}$ + 0.3V to 5.5V with 1.7V minimum, $I_{OUT,LDO3}$ = 0.1mA to $I_{MAX,LDO3}$, $V_{NOM,LDO3}$ set to any voltage		-3		+3	%
		Green mode	$V_{IN,LDO3}$ = $V_{NOM,LDO3}$ + 0.3V to 5.5V with 2.4V minimum, $I_{OUT,LDO3}$ = 0.1mA to 5mA, $V_{NOM,LDO3}$ set to any voltage		-5		+5	
Load Regulation (Note 6)		Normal mode	$I_{OUT,LDO3}$ = 0.1mA to $I_{MAX,LDO3}$, $V_{IN,LDO3}$ = $V_{NOM,LDO3}$ + 0.3V with 1.7V minimum, $V_{NOM,LDO3}$ set to any voltage			0.1		%
		Green mode	$I_{OUT,LDO3}$ = 0.1mA to 5mA, $V_{IN,LDO3}$ = $V_{NOM,LDO3}$ + 0.3V with 2.4V minimum, $V_{NOM,LDO3}$ set to any voltage			0.2		
Line Regulation (Note 6)		Normal mode	$V_{IN,LDO3}$ = $V_{NOM,LDO3}$ + 0.3V to 5.5V with 1.7V minimum, $I_{OUT,LDO3}$ = 0.1mA, $V_{NOM,LDO3}$ set to any voltage			0.03		%/V
		Green mode	$V_{IN,LDO3}$ = $V_{NOM,LDO3}$ + 0.3V to 5.5V with 2.4V minimum, $I_{OUT,LDO3}$ = 0.1mA, $V_{NOM,LDO3}$ set to any voltage			0.1		
Dropout Voltage	$V_{DO,LDO3}$	Normal Mode	$I_{OUT,LDO3}$ = $I_{MAX,LDO3}$	$V_{IN,LDO3}$ = 3.7V		60	120	mV
				$V_{IN,LDO3}$ = 1.7V		150	300	
		Green Mode	$I_{OUT,LDO3}$ = 5mA, $V_{IN,LDO3}$ = 3.7V			50	100	
Output Current Limit	$I_{LIM,LDO3}$	V_{OUT} = 0V			150	225	375	mA

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Load Transient (LDO3OVCLMP_EN = 1) (Notes 3, 6)		Normal mode, $V_{IN,LDO3}$ = $V_{NOM,LDO3}$ + 0.3V to 5.5V with 1.7V absolute minimum, $I_{OUT,LDO3}$ = 1% to 100% to 1% of $I_{MAX,LDO3}$, $V_{NOM,LDO3}$ set to any voltage, t_{R3} = t_{F3} = 1µs, LDO3COMP[5:4] = 01				66		mV
		Green mode, $V_{IN,LDO3}$ = $V_{NOM,LDO3}$ + 0.3V to 5.5V with 2.4V absolute minimum, $I_{OUT,LDO3}$ = 0.05mA to 5mA to 0.05mA, $V_{NOM,LDO3}$ set to any voltage, t_{R3} = t_{F3} = 1µs				25		
Output Line Transient (Notes 3, 6)		Normal mode, $V_{IN,LDO3}$ = $V_{NOM,LOD3}$ + 0.3V to $V_{NOM,LDO3}$ + 0.8V to $V_{NOM,LDO3}$ + 0.3V with 1.7V absolute minimum, t_{R3} = t_{F3} = 1µs, $I_{OUT,LOD3}$ = $I_{MAX,LDO3}$, $V_{NOM,LOD3}$ set to any voltage				5		mV
		Green mode, $V_{IN,LDO3}$ = $V_{NOM,LOD3}$ + 0.3V to $V_{NOM,LDO3}$ + 0.8V to $V_{NOM,LDO3}$ + 0.3V with 2.4V absolute minimum, t_{R3} = t_{F3} =1µs, $I_{OUT,LOD3}$ = 5mA, $V_{NOM,LOD3}$ set to any voltage				5		
Power-Supply Rejection	$PSRR_{LDO3}$	Rejection from $V_{IN,LDO3}$ to $V_{OUT,IDO3}$ $I_{OUT,LDO3}$ = 10% of $I_{MAX,LDO3}$	$V_{INLDO3DC}$ = $V_{NOM,LDO3}$ + 0.3V $V_{INLDO3AC}$ = 50mV	f = 1kHz		63		dB
				f = 10kHz		51		
				f = 100kHz		44		
				f = 1000kHz		57		
				f = 4450kHz		33		
		Green mode, $I_{OUT,LDO3}$ = 1mA, f = 1kHz, rejection from $V_{IN,LDO3}$ to $V_{OUT,LDO3}$				50		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 10% of $I_{MAX,LDO3}$	$V_{OUT,LDO3}$ = 0.8V		45		μV_{RMS}
			$V_{OUT,LDO3}$ = 1.8V		45		
			$V_{OUT,LDO3}$ = 3.7V		60		
Startup Ramp Rate	t_{SS3}	After enabling	LDO3SS = 0		100		mV/µs
			LDO3SS = 1		5		
Active-Discharge Resistance		$V_{OUT,LDO3}$ = 1V, output disabled	Active discharge enabled, LDO3ADE = 1		0.16	0.3	kΩ
			Active discharge disabled, LDO3ADE = 0	1000			
Clamp Active Regulation Voltage		Clamp active (LDO3OVCLMP_EN = 1), LDO output sinking 0.1mA			$V_{NOM,LDO3}$		V
Clamp Disabled Overvoltage Sink Current		$V_{OUT,LDO3}$ = $V_{NOM,LDO3}$ x110%			2.2		µA
Enable Delay (Note 3)	t_{LON3}	Time from LDO enable command received to the output starting to slew	Ramp rate = 100mV/µs		10		µs
			Ramp rate = 5mV/µs		60		
Disable Delay (Note 3)		After LDO is disabled; the LDO output voltage discharges based on Load and $C_{OUT,LDO3}$; to ensure fast discharge times enable the active discharge resistor			0.1		µs
Transition Time from Green Mode to Normal Mode					10		µs
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
Power-OK Threshold	$V_{POKTHL3}$	$V_{OUT,LDO3}$ when V_{POK} switches	$V_{OUT,LDO3}$ rising		92	95	%
			$V_{OUT,LDO3}$ falling	84	87		
Power-OK Noise Pulse Immunity	V_{POKNF3}	$V_{OUT,LDO3}$ pulsed from 100% to 80% of regulation			25		µs
LDO4							
Input Voltage Range	$V_{IN,LDO4}$			1.7		5.5	V
Undervoltage Lockout	$V_{UVLO,LDO4}$	$V_{IN,LDO4}$ rising, 100mV hysteresis			1.6	1.7	V
Output Voltage Range	$V_{OUT,LDO4}$	$V_{IN,LDO4}$ is the maximum of 3.7V or $V_{OUT,LDO4}$ + 0.3V		0.8		3.95	V
Maximum Output Current	$I_{MAX,LDO4}$	Normal mode		150			mA
		Green mode		5			
Minimum Output Capacitance	$C_{OUT,LDO4}$	(Note 3)	Normal mode		0.7		µF
			Green mode		0.7		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Bias Enable Time	t_{LBIAS4}	Time to enable LDO bias only, central bias is already enabled			90		µs
Bias Enable Currents	I_{QBIAS4}	LDO bias enabled			10		µA
AV Supply Current	$I_{AV,LDO4}$	No load	Shutdown, T_A = +25°C (Note 4)		0		µA
			Normal regulation		3	6	
			Green mode		0.5	3	
INB Supply Current	$I_{IN,LDO4}$	No load	Shutdown, T_A = +25°C (Note 5)		0		µA
			Normal regulation		15	30	
			Green mode		1	3	
Output Voltage Accuracy		Normal mode	$V_{IN,LDO4}$ = $V_{NOM,LDO4}$ + 0.3V to 5.5V with 1.7V minimum, $I_{OUT,LDO4}$ = 0.1mA to $I_{MAX,LD04}$, $V_{NOM,LDO4}$ set to any voltage	-3		+3	%
		Green mode	$V_{IN,LDO4}$ = $V_{NOM,LDO4}$ + 0.3V to 5.5V with 2.4V minimum, $I_{OUT,LDO4}$ = 0.1mA to 5mA, $V_{NOM,LDO4}$ set to any voltage	-5		+5	
Load Regulation (Note 6)		Normal mode	$I_{OUT,LDO4}$ = 0.1mA to $I_{MAX,LD04}$, V_{IN} = $V_{NOM,LDO4}$ + 0.3V with 1.7V minimum, $V_{NOM,LDO4}$ set to any voltage		0.1		%
		Green mode	$I_{OUT,LDO4}$ = 0.1mA to 5mA, V_{IN} = $V_{NOM,LDO4}$ + 0.3V with 2.4V minimum, $V_{NOM,LDO4}$ set to any voltage		0.2		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Line Regulation (Note 6)		Normal mode	$V_{IN,LDO4}$ = $V_{NOM,LDO4}$ + 0.3V to 5.5V with 1.7V minimum, $I_{OUT,LDO4}$ = 0.1mA, $V_{NOM,LDO4}$ set to any voltage			0.03		%/V
		Green mode	$V_{IN,LDO4}$ = $V_{NOM,LDO4}$ + 0.3V to 5.5V with 2.4V minimum, $I_{OUT,LDO4}$ = 0.1mA, $V_{NOM,LDO4}$ set to any voltage			0.1		
Dropout Voltage	$V_{DO,LDO4}$	Normal mode	$I_{OUT,LDO4}$ = $I_{MAX,LD04}$	$V_{IN,LDO4}$ = 3.7V		60	120	mV
				$V_{IN,LDO4}$ = 1.7V		150	300	
		Green mode	$I_{OUT,LDO4}$ = 5mA, $V_{IN,LDO4}$ = 3.7V			50	100	
Output Current Limit	$I_{LIM,LDO4}$	$V_{OUT,LDO4}$ = 0V			150	225	375	mA
Output Load Transient (LDO4OVCLMP_EN = 1) (Notes 3, 6)		Normal mode, $V_{IN,LDO4}$ = $V_{NOM,LDO4}$ + 0.3V to 5.5V with 1.7V absolute minimum. $I_{OUT,LDO4}$ = 1% to 100% to 1% of $I_{MAX,LDO4}$, $V_{NOM,LD04}$ set to any voltage, t_{R4} = t_{F4} = 1µs, LDO4COMP[5:4] = 01				66		mV
		Green mode, $V_{IN,LDO4}$ = $V_{NOM,LDO4}$ + 0.3V to 5.5V with 2.4V absolute minimum, $I_{OUT,LDO4}$ = 0.05mA to 5mA to 0.05mA, $V_{NOM,LDO4}$ set to any voltage, t_{R4} = t_{F4} = 1µs				25		
Output Line Transient (Notes 3, 6)		Normal mode, $V_{IN,LDO4}$ = $V_{NOM,LDO4}$ + 0.3V to $V_{NOM,LDO4}$ + 0.8V to $V_{NOM,LDO4}$ + 0.3V with 1.7V absolute minimum, t_{R4} = t_{F4} = 1µs, $I_{OUT,LDO4}$ = $I_{MAX,LDO4}$, $V_{NOM,LDO4}$ set to any voltage				5		mV
		Green mode, $V_{IN,LDO4}$ = $V_{NOM,LDO4}$ + 0.3V to $V_{NOM,LDO4}$ + 0.8V to $V_{NOM,LDO4}$ + 0.3V with 2.4V absolute minimum, t_{R4} = t_{F4} = 1µs, $I_{OUT,LDO4}$ = 5mA, $V_{NOM,LDO4}$ set to any voltage				5		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Power-Supply Rejection	$PSRR_{LDO4}$	Rejection from $V_{IN,LDo4}$ to $V_{OUT,LDO4}$ $I_{OUT,LDO4}$ = 10% of $I_{MAX,LDO4}$	$V_{INLDO4DC}$ = $V_{NOM,LDO4}$ + 0.3V, $V_{INLDO4AC}$ = 50mV	f = 1kHz		63		dB
				f = 10kHz		51		
				f = 100kHz		44		
				f = 1000kHz		57		
				f = 4450kHz		33		
		Green mode, $I_{OUT,LDO4}$ = 1mA, f = 1kHz, rejection from $V_{IN,LDO4}$ to $V_{OUT,LDO4}$				50		
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{OUT} = 0.8V			45		μV_{RMS}
			V_{OUT} = 1.8V			45		
			V_{OUT} = 3.7V			60		
Startup Ramp Rate	t_{SS4}	After enabling	LDO4SS = 0			100		mV/µs
			LDO4SS = 1			5		
Active-Discharge Resistance		$V_{OUT,LDO4}$ = 1V, output disabled	Active discharge enabled, LDO4ADE = 1			0.16	0.3	kΩ
			Active discharge disabled, LDO4ADE = 0		1000			
Clamp Active Regulation Voltage		Clamp active (LDO4OVCLMP_EN = 1), LDO output sinking 0.1mA				$V_{NOM, LDO4}$		V
Clamp Disabled Overvoltage Sink Current		$V_{OUT,LDO4}$ = $V_{NOM,LDO4}$ x 110%				2.2		µA
Enable Delay (Note 3)	t_{LON4}	Time from LDO enable command received to the output starting to slew	Ramp rate = 100mv/µs			10		µs
			Ramp rate = 5mv/µs			60		
Disable Delay (Note 3)		After LDO is disabled; the LDO output voltage discharges based on load and $C_{OUT,LDO4}$; to ensure fast discharge times enable the active discharge resistor				0.1		µs
Transition time from Green Mode to Normal Mode						10		µs
Thermal Shutdown		Output disabled or enabled	T_J rising			165		°C
			T_J falling			150		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-OK Threshold	$V_{POKTHL4}$	$V_{OUT,LDO4}$ when V_{POK} switches	$V_{OUT,LDO4}$ rising		92	95	%
			$V_{OUT,LDO4}$ falling	84	87		
Power-OK Noise Pulse Immunity	V_{POKNF4}	$V_{OUT,LDO4}$ pulsed from 100% to 80% of regulation			25		µs
LDO5							
Input Voltage Range	$V_{IN,LDO5}$			1.7		5.5	V
Undervoltage Lockout	$V_{UVLO,LDO5}$	$V_{IN,LDO5}$ rising, 100mV hysteresis			1.6	1.7	V
Output Voltage Range	$V_{OUT,LDO5}$	$V_{IN,LDO5}$ is the maximum of 3.7V or $V_{OUT,LDO5}$ + 0.3V		0.8		3.95	V
Maximum Output Current	$I_{MAX,LDO5}$	Normal mode		300			mA
		Green mode		5			
Minimum Output Capacitance	$C_{OUT,LDO5}$	(Note 3)	Normal mode		0.7		µF
			Green mode		0.7		
Bias Enable Time	t_{LBIAS5}	Time to enable LDO bias only, central bias is already enabled			90		µs
Bias Enable Currents	I_{QBIAS5}	LDO bias enabled			10		µA
AV Supply Current	$I_{AV,LDO5}$	No load	Shutdown, T_A = +25°C (Note 4)		0		µA
			Normal regulation		3	6	
			Green mode		0.5	3	
INB Supply Current	$I_{IN,LDO5}$	No load	Shutdown, T_A = +25°C (Note 5)		0		µA
			Normal regulation		17	30	
			Green mode		1	3	
Output Voltage Accuracy		Normal mode	$V_{IN,LDO5}$ = $V_{NOM,LDO5}$ + 0.3V to 5.5V with 1.7V minimum, $I_{OUT,LDO5}$ = 0.1mA to $I_{MAX,LDO5}$, $V_{NOM,LDO5}$ set to any voltage	-3		+3	%
		Green mode	$V_{IN,LDO5}$ = $V_{NOM,LDO5}$ + 0.3V to 5.5V with 2.4V minimum, $I_{OUT,LDO5}$ = 0.1mA to 5mA, $V_{NOM,LDO5}$ set to any voltage	-5		+5	

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Load Regulation (Note 6)		Normal mode	$I_{OUT,LDO5}$ = 0.1mA to $I_{MAX,LDO5}$, $V_{IN,LDO5}$ = $V_{NOM,LDO5}$ + 0.3V with 1.7V minimum, $V_{NOM,LDO5}$ set to any voltage			0.1		%
		Green mode	$I_{OUT,LDO5}$ = 0.1mA to 5mA, $V_{IN,LDO5}$ = $V_{NOM,LDO5}$ + 0.3V with 2.4V minimum, $V_{NOM,LDO5}$ set to any voltage			0.2		
Line Regulation (Note 6)		Normal mode	$V_{IN,LDO5}$ = $V_{NOM,LDO5}$ + 0.3V to 5.5V with 1.7V minimum. $I_{OUT,LDO5}$ = 0.1mA, $V_{NOM,LDO5}$ set to any voltage			0.03		%/V
		Green mode	$V_{IN,LDO5}$ = $V_{NOM,LDO5}$ + 0.3V to 5.5V with 2.4V minimum. $I_{OUT,LDO5}$ = 0.1mA, $V_{NOM,LDO5}$ set to any voltage			0.1		
Dropout Voltage	$V_{DO,LDO5}$	Normal mode	$I_{OUT,LDO5}$ = $I_{MAX,LDO5}$	$V_{IN,LDO5}$ = 3.7V		50	100	mV
				$V_{IN,LDO5}$ = 1.7V		150	450	
		Green mode	$I_{OUT,LDO5}$ = 5mA, $V_{IN,LDO5}$ = 3.7V			150	300	
Output Current Limit	$I_{LIM,LDO5}$	$V_{OUT,LDO5}$ = 0V			300	450	750	mA
Output Load Transient (LDO5OVCLMP_EN = 1) (Notes 3, 6)		Normal mode, $V_{IN,LDO5}$ = $V_{NOM,LDO5}$ + 0.3V to 5.5V with 1.7V absolute minimum, $I_{OUT,LDO5}$ = 1% to 100% to 1% of $I_{MAX,LDO5}$, $V_{NOM,LDO5}$ set to any voltage, t_{R5} = t_{F5} = 1µs, LDO5COMP[5:4] = 01				66		mV
		Green mode, $V_{IN,LDO5}$ = $V_{NOM,LDO5}$ + 0.3V to 5.5V with 2.4V absolute minimum, $I_{OUT,LDO5}$ = 0.05mA to 5mA to 0.05mA, $V_{NOM,LDO5}$ set to any voltage, t_{R5} = t_{F5} = 1µs				25		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Line Transient (Notes 3, 6)		Normal mode, $V_{IN,LOD5}$ = $V_{NOM,LDO5}$ + 0.3V to $V_{NOM,LDO5}$ + 0.8V to $V_{NOM,LDO5}$ + 0.3V with 1.7V absolute minimum, t_{R5} = t_{F5} = 1µs, $I_{OUT,LDO5}$ = $I_{MAX,LDO5}$, $V_{NOM,LDO5}$ set to any voltage		5		mV
		Green mode, $V_{IN,LDO5}$ = $V_{NOM,LDO5}$ + 0.3V to $V_{NOM,LDO5}$ + 0.8V to $V_{NOM,LDO5}$ + 0.3V with 2.4V absolute minimum, t_{R5} = t_{F5} = 1µs, $I_{OUT,LDO5}$ = 5mA, $V_{NOM,LDO5}$ set to any voltage		5		
Power-Supply Rejection	$PSRR_{LDO5}$	Rejection from $V_{IN,LDO5}$ to $V_{OUT,LDO5}$ $I_{OUT,LDO5}$ = 10% of $I_{MAX,LDO5}$; $V_{INLDO5DC}$ = $V_{NOM,LDO5}$ + 0.3V $V_{INLDO5AC}$ = 50mV; f = 1kHz		63		dB
		f = 10kHz		51		
		f = 100kHz		44		
		f = 1000kHz		57		
		f = 4450kHz		33		
		Green mode, I_{OUT} = 1mA, f = 1kHz, rejection from $V_{IN,LDO5}$ to $V_{OUT,LDO5}$		50		
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 10% of $I_{MAX,LDO5}$; $V_{OUT,LDO5}$ = 0.8V		45		$µV_{RMS}$
		$V_{OUT,LDO5}$ = 1.8V		45		
		$V_{OUT,LDO5}$ = 3.7V		60		
Startup Ramp Rate	t_{SS5}	After enabling; LDO5SS = 0		100		mV/µs
		LDO5SS = 1		5		
Active-Discharge Resistance		$V_{OUT,LDO5}$ = 1V, output disabled; Active discharge enabled, LDO5ADE = 1		0.16	0.3	kΩ
		Active discharge disabled, LDO5ADE = 0	1000			
Clamp Active Regulation Voltage		Clamp active (LDO5OVCLMP_EN = 1), LDO output sinking 0.1mA		$V_{NOM,LD05}$		V

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clamp Disabled Overvoltage Sink Current		$V_{OUT,LDO5}$ = $V_{NOM,LDO5}$ x 110%			2.2		µA
Enable Delay (Note 3)	t_{LON5}	Time from LDO enable command received to the output starting to slew	Ramp rate =100mV/µs		10		µs
			Ramp rate = 5mV/µs		60		
Disable Delay (Note 3)		After LDO is disabled; the LDO output voltage discharges based on load and C_{OUT}; to ensure fast discharge times, enable the active discharge resistor			0.1		µs
Transition Time from Green Mode to Normal Mode					10		µs
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
Power-Ok Threshold	V_{POKTHL}	$V_{OUT,LDO5}$ when V_{POK} switches	$V_{OUT,LDO5}$ rising		92	95	%
			$V_{OUT,LDO5}$ falling	84	87		
Power-Ok Noise Pulse Immunity	V_{POKNF}	$V_{OUT,LDO5}$ pulsed from 100% to 80% of regulation			25		µs
LDO6							
Input Voltage Range	$V_{IN,LDO6}$			1.7		5.5	V
Undervoltage Lockout	$V_{UVLO,LDO6}$	Rising, 100mV hysteresis			1.6	1.7	V
Output Voltage Range	$V_{OUT,LDO6}$	$V_{IN,LDO6}$ is the maximum of 3.7V or $V_{OUT,LDO6}$ + 0.3V		0.8		3.95	V
Maximum Output Current	$I_{MAX,LDO6}$	Normal mode		150			mA
		Green mode		5			
Minimum Output Capacitance	$C_{OUT,LDO6}$	(Note 3)	Normal mode		0.7		µF
			Green mode		0.7		
Bias Enable Time	t_{LBIAS6}	Time to enable LDO bias only, central bias is already enabled			90		µs
Bias Enable Currents	I_{QBIAS6}	LDO bias enabled			10		µA
AV Supply Current	$I_{AV,LDO6}$	No load	Shutdown, T_A = +25°C (Note 4)		0		µA
			Normal regulation		3	6	
			Green mode		0.5	3	
INB Supply Current	$I_{IN,LDO6}$	No load	Shutdown, T_A = +25°C (Note 5)		0		µA
			Normal regulation		15	30	
			Green mode		1	3	

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage Accuracy		Normal mode	$V_{IN,LDO6}$ = $V_{NOM,LDO6}$ + 0.3V to 5.5V with 1.7V minimum, $I_{OUT,LDO6}$ = 0.1mA to $I_{MAX,LDO6}$, $V_{NOM,LDO6}$ set to any voltage		-3		+3	%
		Green mode	$V_{IN,LDO6}$ = $V_{NOM,LDO6}$ + 0.3V to 5.5V with 2.4V minimum, $I_{OUT,LDO6}$ = 0.1mA to 5mA, $V_{NOM,LDO6}$ set to any voltage		-5		+5	
Load Regulation (Note 6)		Normal mode	$I_{OUT,LDO6}$ = 0.1mA to $I_{MAX,LDO6}$, $V_{IN,LDO6}$ = $V_{NOM,LDO6}$ + 0.3V with 1.7V minimum, $V_{NOM,LDO6}$ set to any voltage			0.1		%
		Green mode	$I_{OUT,LDO6}$ = 0.1mA to 5mA, $V_{IN,LDO6}$ = $V_{NOM,LDO6}$ + 0.3V with 2.4V minimum, $V_{NOM,LDO6}$ set to any voltage			0.2		
Line Regulation (Note 6)		Normal mode	$V_{IN,LDO6}$ = $V_{NOM,LDO6}$ + 0.3V to 5.5V with 1.7V minimum, $I_{OUT,LDO6}$ = 0.1mA, $V_{NOM,LDO6}$ set to any voltage			0.03		%/V
		Green mode	$V_{IN,LDO6}$ = $V_{NOM,LDO6}$ + 0.3V to 5.5V with 2.4V minimum, $I_{OUT,LDO6}$ = 0.1mA, $V_{NOM,LDO6}$ set to any voltage			0.1		
Dropout Voltage	$V_{DO,LDO6}$	Normal mode	$I_{OUT,LDO6}$ = $I_{MAX,LDO6}$	$V_{IN,LDO6}$ = 3.7V		60	120	mV
				$V_{IN,LDO6}$ = 1.7V		150	300	
		Green mode	$I_{OUT,LDO6}$ = 5mA, $V_{IN,LDO6}$ = 3.7V			50	100	
Output Current Limit	$I_{LIM,LDO6}$	$V_{OUT,LDO6}$ = 0V			150	225	375	mA

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Load Transient (LDO6OVCLMP_EN = 1) (Notes 3, 6)		Normal mode, $V_{IN,LDO6}$ = $V_{NOM,LDO6}$ + 0.3V to 5.5V with 1.7V absolute minimum, $I_{OUT,LDO6}$ = 1% to 100% to 1% of $I_{MAX,LDO6}$, $V_{NOM,LDO6}$ set to any voltage, t_{R6} = t_{F6} = 1µs, LDO6COMP[5:4] = 01				66		mV
		Green mode, $V_{IN,LDO6}$ = $V_{NOM,LDO6}$ +0.3V to 5.5V with 2.4V absolute minimum, $I_{OUT,LDO6}$ = 0.05mA to 5mA to 0.05mA, $V_{NOM,LDO6}$ set to any voltage, t_{R6} = t_{F6} = 1µs				25		
Output Line Transient (Notes 3, 6)		Normal mode, $V_{IN,LDO6}$ = $V_{NOM,LDO6}$ + 0.3V to $V_{NOM,DLo6}$ + 0.8V to $V_{NOM,LDO6}$ + 0.3V with 1.7V absolute minimum, t_{R6} = t_{F6} = 1µs, $I_{OUT,LDO6}$ = $I_{MAX,LDO6}$, $V_{NOM,LDO6}$ set to any voltage				5		mV
		Normal mode, $V_{IN,LDO6}$ = $V_{NOM,LDO6}$ + 0.3V to $V_{NOM,DLo6}$ + 0.8V to $V_{NOM,LDO6}$ + 0.3V with 2.4V absolute minimum, t_{R6} = t_{F6} = 1µs, $I_{OUT,LDO6}$ = 5mA, $V_{NOM,LDO6}$ set to any voltage				5		
Power-Supply Rejection	$PSRR_{LDO6}$	Rejection from $V_{IN,LDO6}$ to $V_{OUT,LDO06}$ $I_{OUT,LDO6}$ = 10% of $I_{MAX,LDO6}$	$V_{INLOD6DC}$ = $V_{NOM,LDO6}$ + 0.3V, $V_{INLDO6AC}$ = 50mV	f = 1kHz		63		dB
				f = 10kHz		51		
				f = 100kHz		44		
				f = 1000kHz		57		
				f = 4450kHz		33		
		Green mode, $I_{OUT,LDO6}$ = 1mA, f = 1kHz, rejection from $V_{IN,LDO6}$ to $V_{OUT,LDO6}$				50		

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise		f = 10Hz to 100kHz, $I_{OUT,LDO6}$ = 10% of $I_{MAX,LDO6}$	$V_{OUT,LDO06}$ = 0.8V		45		μV_{RMS}
			$V_{OUT,LDO06}$ = 1.8V		45		
			$V_{OUT,LDO06}$ = 3.7V		60		
Startup Ramp Rate	$t_{SS,LDO6}$	After enabling	LDO6SS = 0		100		mV/µs
			LDO6SS = 1		5		
Active-Discharge Resistance		$V_{OUT,LDO6}$ = 1V, output disabled	Active discharge enabled, LDO6ADE = 1		0.16	0.3	kΩ
			Active discharge disabled, LDO6ADE = 0	1000			
Clamp Active Regulation Voltage		Clamp active (LDO6OVCLMP_EN = 1), LDO output sinking 0.1mA			$V_{NOM,LDO6}$		V
Clamp Disabled Overvoltage Sink Current		$V_{OUT,LDO6}$ = $V_{NOM,LDO6}$ x 110%			2.2		µA
Enable Delay (Note 3)	t_{LON6}	Time from LDO enable command received to the output starting to slew	Ramp rate = 100mV/µs		10		µs
			Ramp rate = 5mV/µs		60		
Disable Delay (Note 3)		After LDO is disabled, the LDO output voltage discharges based on load and $C_{OUT,LDO6}$; to ensure fast discharge times, enable the active discharge resistor			0.1		µs
Transition Time from Green mode to Normal Mode					10		µs
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
Power-OK Threshold	$V_{POKTHL6}$	$V_{OUT,LDO6}$ when V_{POK} switches	$V_{OUT,LDO6}$ rising		92	95	%
			$V_{OUT,LDO6}$ falling	84	87		
Power-OK Noise Pulse Immunity	V_{POKNF6}	$V_{OUT,LDO6}$ pulsed from 100% to 80% of regulation			25		µs
DIGITAL I/O							
Logic Input High Voltage Threshold	V_{IH}	$V_{ID\_}$, EN_, SDA, SCL, V_{IN1} = V_{IN2} = V_{AV} = 2.6V to 5.5V V_{IO} = 1.65V to 3.6V		1.4			V
Logic Input Low Voltage Threshold	V_{IL}	$V_{ID\_}$, EN_, SDA, SCL, V_{IN1} = V_{IN2} = V_{AV} = 2.6V to 5.5V V_{IO} = 1.65V to 3.6V				0.4	V

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input Current (SDA, SCL)		V_{IL} = 0V or V_{IH} = 3.6V, EN_ = AGND	T_A = +25°C	-1		+1	µA
			T_A = +85°C		0.1		
Logic Input Current ($V_{ID\_}$, EN_)		V_{IL} = 0V, EN_ = AGND	T_A = +25°C	-1		+1	µA
			T_A = +85°C		0.1		
$V_{ID\_}$, EN_ Logic Input Pulldown Resistor				400			kΩ
I²C INTERFACE							
SDA Output Low Voltage		I_{SDA} = 3mA				0.1	V
I²C Clock Frequency						400	kHz
Bus-Free Time Between START and STOP	t_{BUF}	See Figure 7 in the *Digital I/O* section		1.3			µs
Hold Time Repeated START Condition	t_{HD_STA}	See Figure 7 in the *Digital I/O* section		0.6	0.1		µs
SCL Low Period	t_{LOW}	See Figure 7 in the *Digital I/O* section		1.3	0.2		µs
SCL High Period	t_{HIGH}	See Figure 7 in the *Digital I/O* section		0.6	0.1		µs
Setup Time Repeated START Condition	t_{SU_STA}	See Figure 7 in the *Digital I/O* section		0.6	0.1		µs
SDA Hold Time	t_{HD_DAT}	See Figure 7 in the *Digital I/O* section		0	-0.01		µs
SDA Setup Time	t_{SU_DAT}	See Figure 7 in the *Digital I/O* section		0.1	0.05		µs
Glitch Filter		Maximum pulse width of spikes that must be suppressed by the input filter of both the DATA and CLK pins			50		ns
Setup Time for STOP Condition	t_{SU_STO}	See Figure 7 in the *Digital I/O* section		0.6	0.1		µs

Note 2: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. LDO_COMP = 01 (default).

Note 3: V_{OUT} is limited to approximately: V_{IN} - (inductor DCR + output trace resistance + 100mΩ) x I_{OUT}.

Note 4: Values are based on simulations and bench testing; they are not production tested.

Note 5: System shutdown current is guaranteed by testing the combined current part in shutdown in the main bias section.

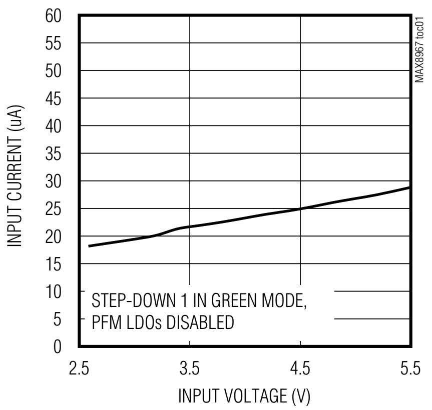
Note 6: IN shutdown current is guaranteed by testing the combined current of all IN_ and LDO_ pins in shutdown to a 5µA (max).

Note 7: Does not include ESR of the capacitance or trace resistance of the module/PCB.

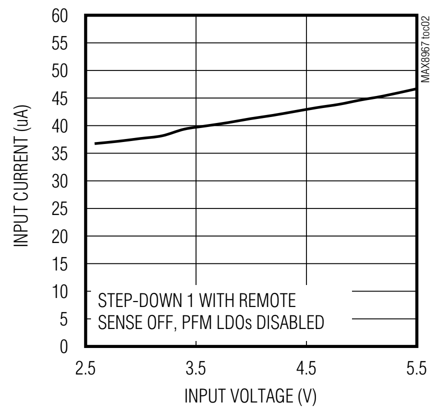
Typical Operating Characteristics

($V_{IN\_} = V_{AV} = 3.6V$, $V_{IO} = 1.8V$, *Typical Application Circuit*, $T_A = +25°C$, unless otherwise noted.)

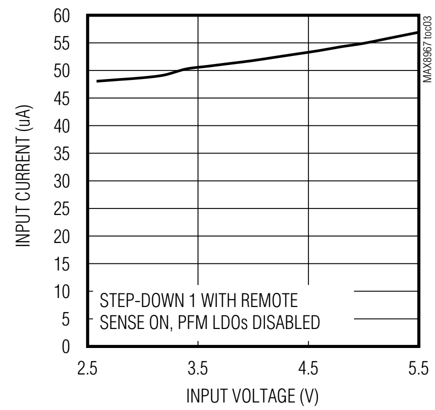
INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



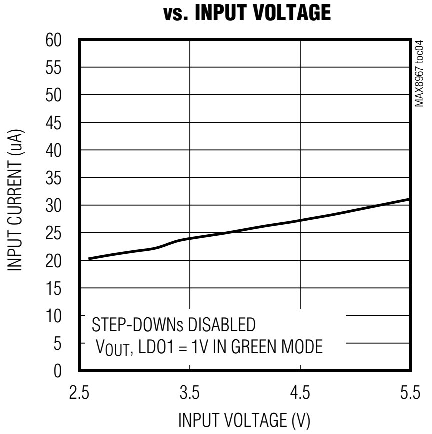
INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



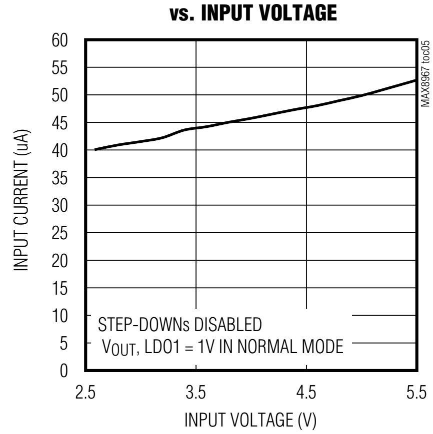
INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



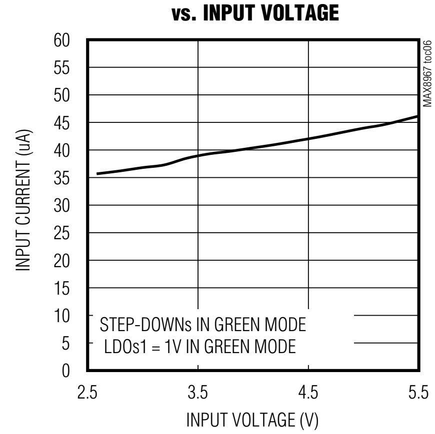
INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



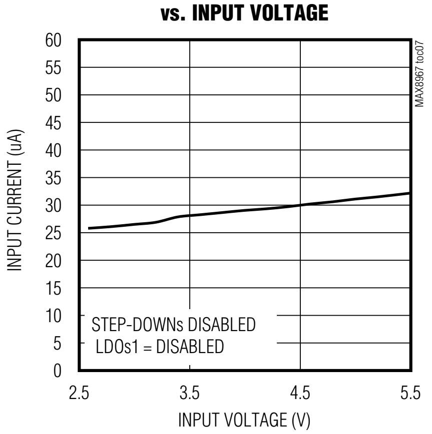
INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



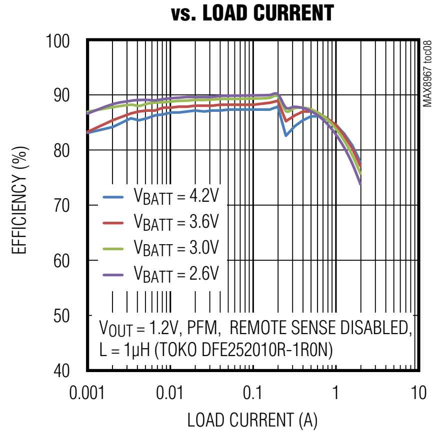
INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



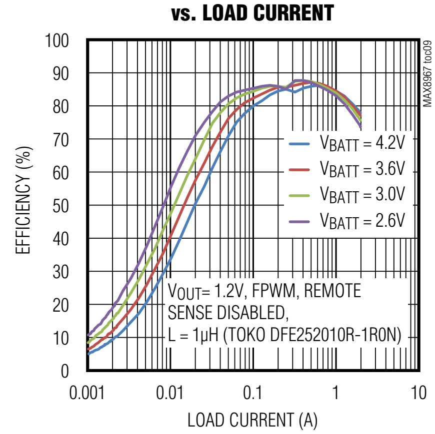
STANDBY CURRENT vs. INPUT VOLTAGE



STEP-DOWN EFFICIENCY vs. LOAD CURRENT



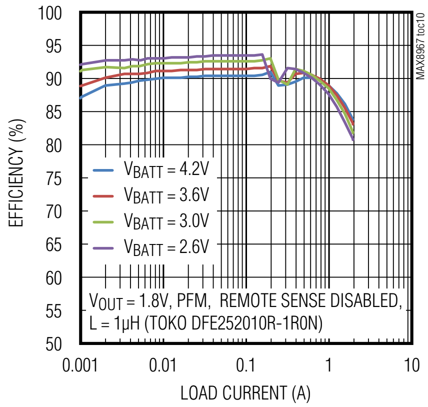
STEP-DOWN EFFICIENCY vs. LOAD CURRENT



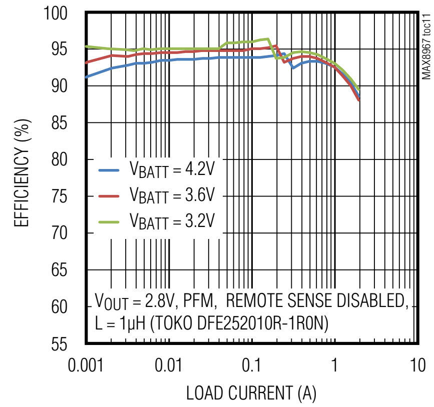
Typical Operating Characteristics (continued)

($V_{IN\_}$ = V_{AV} = 3.6V, V_{IO} = 1.8V, *Typical Application Circuit*, T_A = +25°C, unless otherwise noted.)

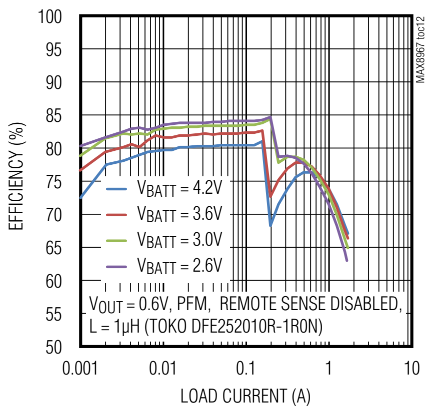
STEP-DOWN EFFICIENCY vs. LOAD CURRENT



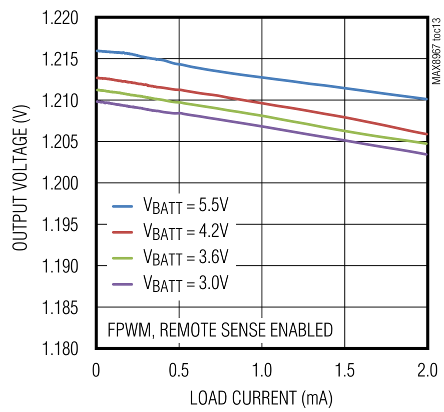
STEP-DOWN EFFICIENCY vs. LOAD CURRENT



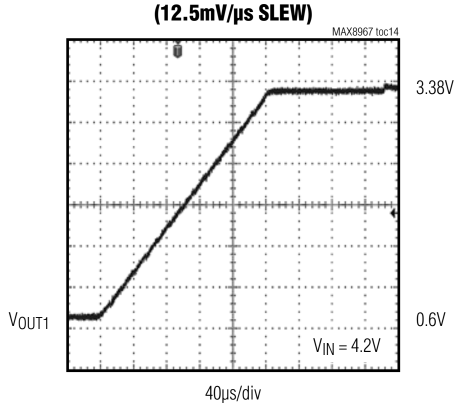
STEP-DOWN EFFICIENCY vs. LOAD CURRENT



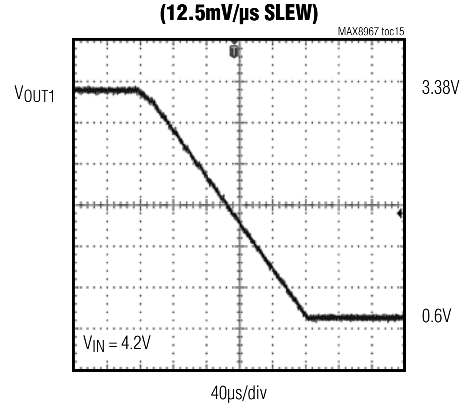
STEP-DOWN LOAD REGULATION



V_{ID} TRANSTION (12.5mV/µs SLEW)



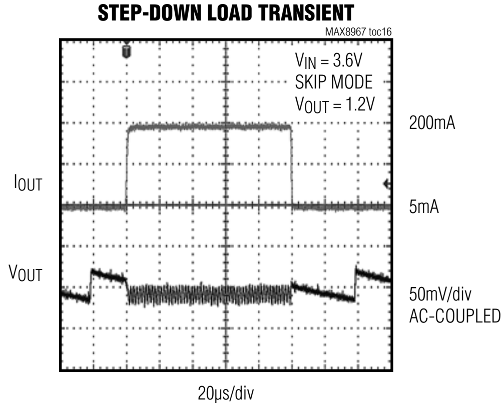
V_{ID} TRANSTION (12.5mV/µs SLEW)



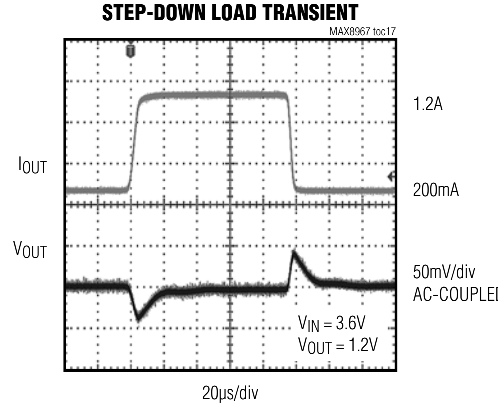
Typical Operating Characteristics (continued)

($V_{IN\_} = V_{AV} = 3.6V$, $V_{IO} = 1.8V$, *Typical Application Circuit*, $T_A = +25°C$, unless otherwise noted.)

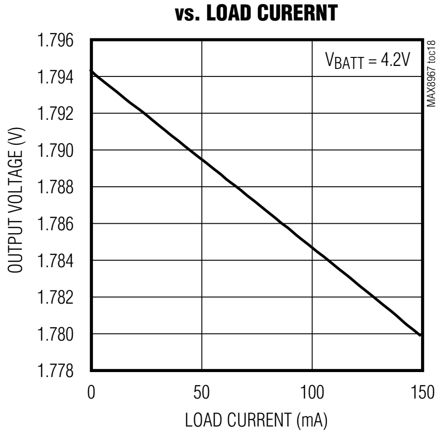
STEP-DOWN LOAD TRANSIENT



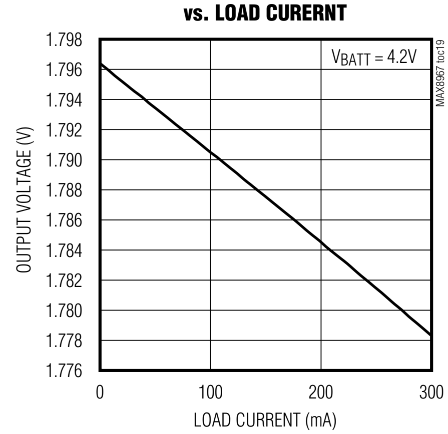
STEP-DOWN LOAD TRANSIENT



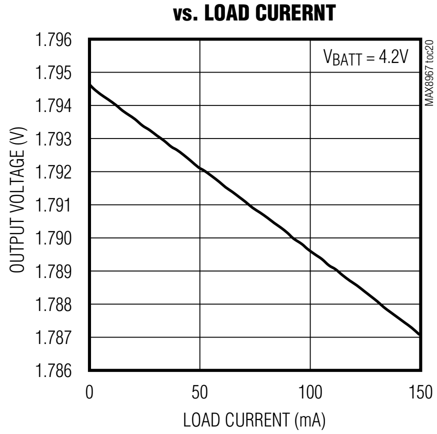
LDO1 OUTPUT VOLTAGE vs. LOAD CURERNT



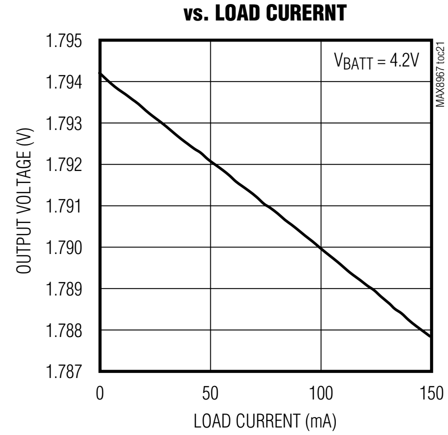
LDO2 OUTPUT VOLTAGE vs. LOAD CURERNT



LDO3 OUTPUT VOLTAGE vs. LOAD CURERNT



LDO4 OUTPUT VOLTAGE vs. LOAD CURERNT



Typical Operating Characteristics (continued)

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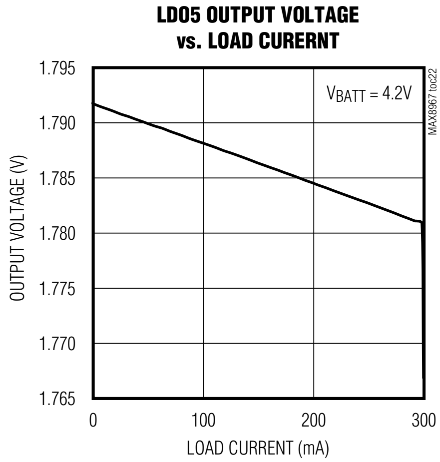

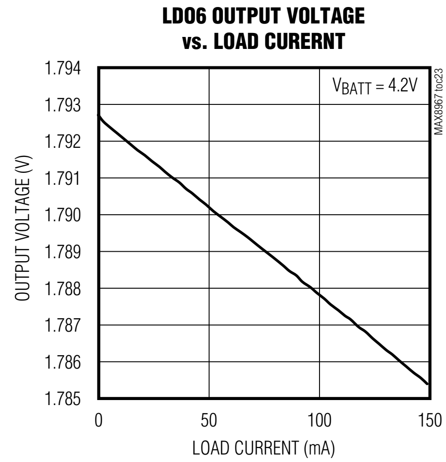

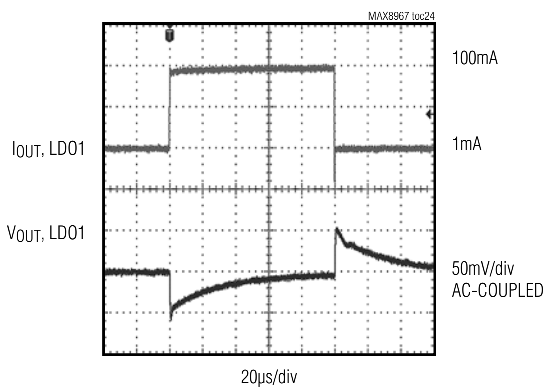

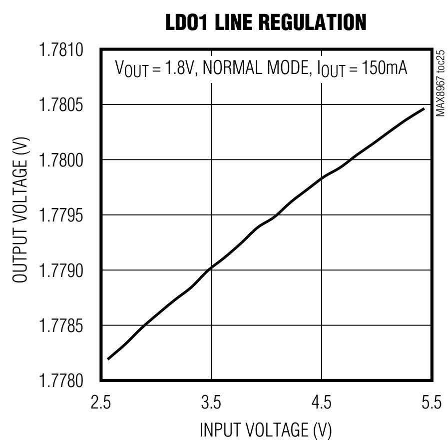

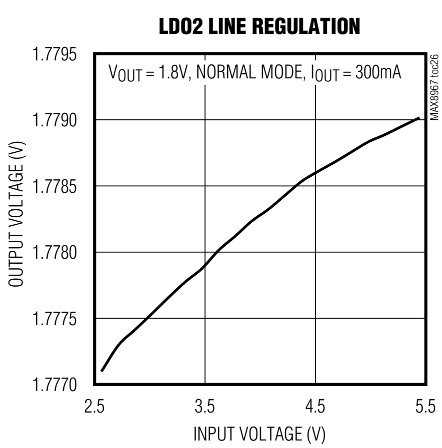

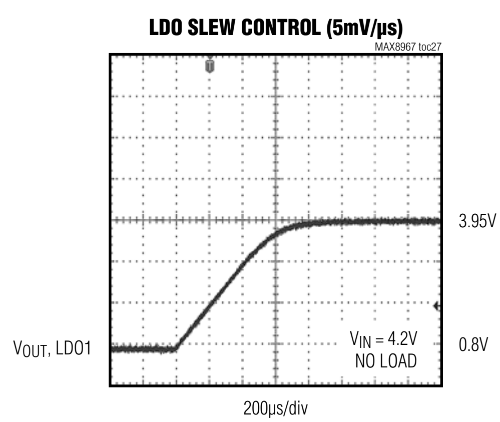

Typical Operating Characteristics (continued)

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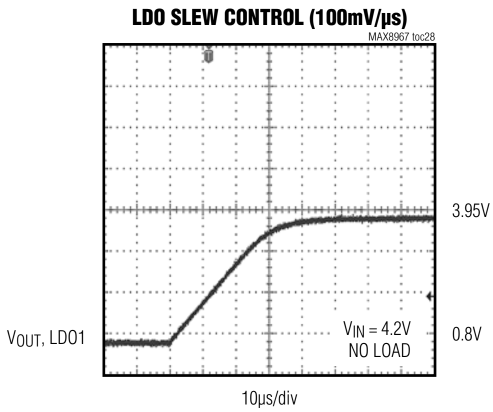
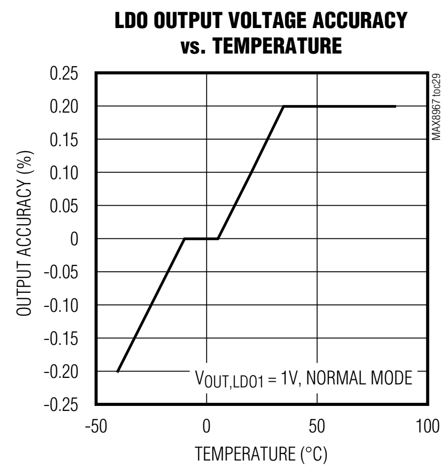
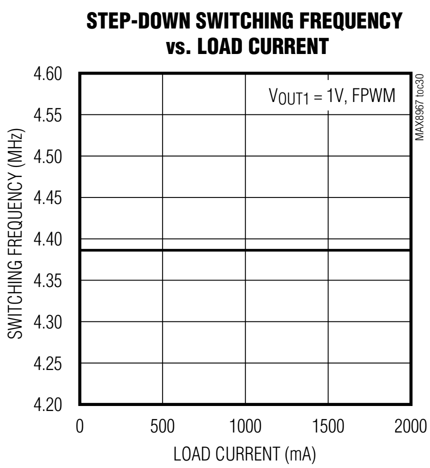
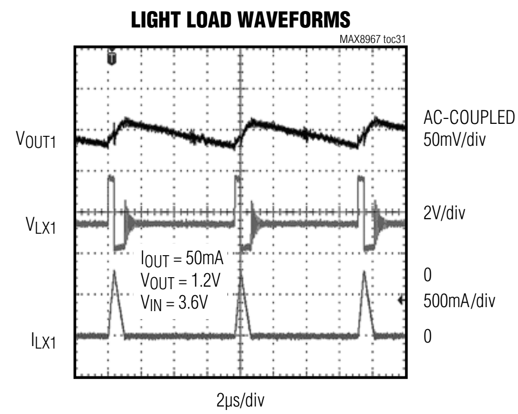
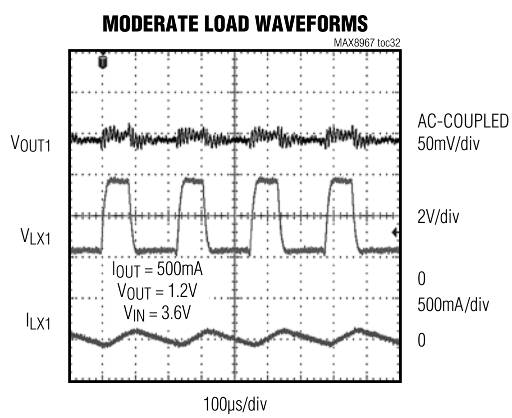
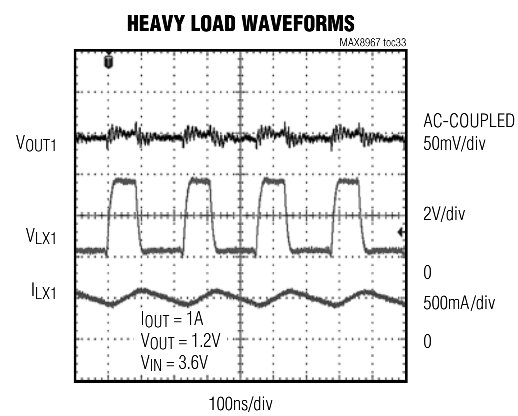




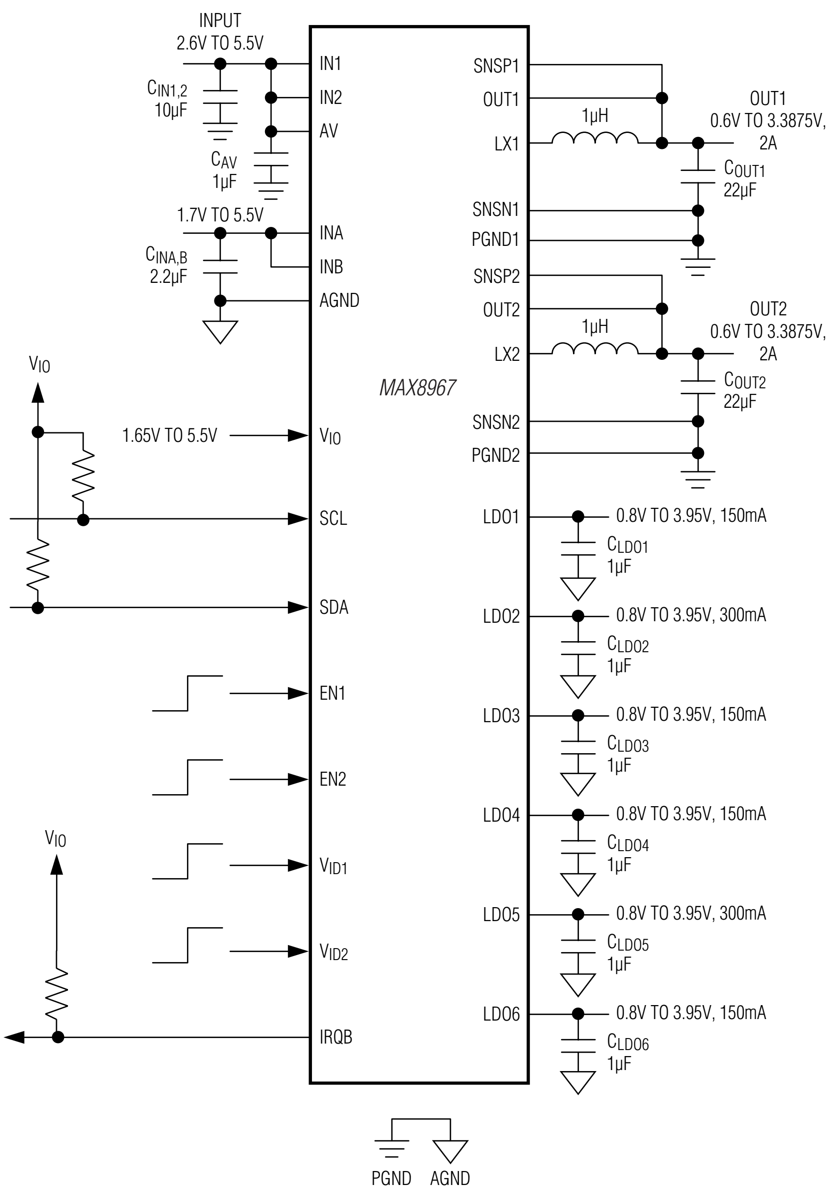




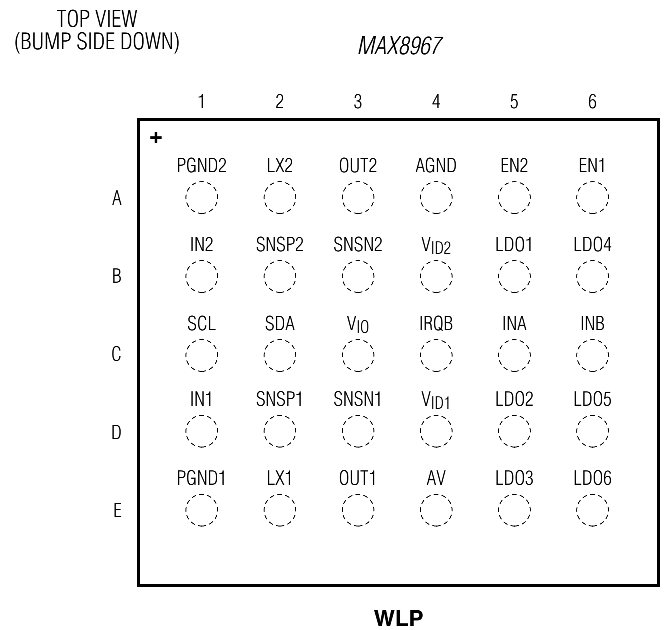




Typical Applications Circuit



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
A1	PGND2	Step-Down Converter 2 Power Ground. Bypass IN2 to PGND2 with a 10µF ceramic capacitor as close as possible to the IC.
A2	LX2	Step-Down Converter 2 Inductor Switching Node. Connect a 1µH inductor from LX2 to OUT2. LX2 is high impedance when disabled.
A3	OUT2	Step-Down Converter 2 Output Sense and Discharge Connection. Bypass OUT2 to PGND2 with a 22µF ceramic capacitor. OUT2 can also be connected to ground through an internal 100Ω resistor using an I^2C command when disabled.
A4	AGND	Analog Ground. Connect AGND to PGND_.
A5	EN2	Enable Logic Input for Step-Down Converter 2. Step-down converter 2 can also be enabled through I^2C. EN2 has an internal 800kΩ pulldown resistor.
A6	EN1	Enable Logic Input for Step-Down Converter 1. Step-down converter 1 can also be enabled through I^2C. EN1 has an internal 800kΩ pulldown resistor.
B1	IN2	Step-Down Converter 2 Input Supply. Bypass IN2 to PGND2 with a 10µF ceramic capacitor as close as possible to the IC. Connect IN2 to both IN1 and AV.
B2	SNSP2	Step-Down Converter 2 Positive Remote Voltage Sense. Connect SNSP2 to the positive terminal of the OUT2 bypass capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
B3	SNSN2	Step-Down Converter 2 Negative Remote Voltage Sense. Connect SNSN2 to the negative terminal of the OUT2 bypass capacitor.
B4	V_{ID2}	Voltage Identification Digital 2. To toggle between two step-down converter 2 output voltages, toggle V_{ID2} logic-high and logic-low. V_{ID2} has an internal 800kΩ pulldown resistor.
B5	LDO1	LDO1 Output. Bypass LDO1 to AGND with a 1µF ceramic capacitor.
B6	LDO4	LDO4 Output. Bypass LDO4 to AGND with a 1µF ceramic capacitor.
C1	SCL	I^2C Clock Signal. Connect SCL to V_{IO} with a 2.2kΩ pullup resistor.
C2	SDA	I^2C Data Signal. Connect SCA to V_{IO} with a 2.2kΩ pullup resistor.
C3	V_{IO}	I/O Input Supply. Connect V_{IO} to the I^2C bus master's power supply.
C4	IRQB	Interrupt Open-Drain Active-Low Output. IRQB signals if there is a fault. Connect IRQB to V_{IO} with a 100kΩ pullup resistor.
C5	INA	Input Supply for LDOs 1, 2, and 3. Bypass INA to AGND with a 2.2µF ceramic capacitor as close as possible to the IC.
C6	INB	Input Supply for LDOs 4, 5, and 6. Bypass INB to AGND with a 2.2µF ceramic capacitor as close as possible to the IC.
D1	IN1	Power input for Step-Down Converter 1. Bypass IN1 to PGND1 as close as possible to the IC. Connect IN1 to both IN2 and AV.
D2	SNSP1	Step-Down Converter 1 Positive Remote Voltage Sense. Connect SNSP1 to the positive terminal of the OUT1 bypass capacitor.
D3	SNSN1	Step-Down Converter 1 Negative Remote Voltage Sense. Connect SNSN1 to the negative terminal of the OUT1 bypass capacitor.
D4	V_{ID1}	Voltage Identification Digital 1. To toggle between two different step-down converter 1 output voltages toggle V_{ID1} logic-high and logic-low. V_{ID1} has an internal 800kΩ pulldown resistor.
D5	LDO2	LDO2 Output. Bypass LDO2 to AGND with a 1µF ceramic capacitor.
D6	LDO5	LDO5 Output. Bypass LDO5 to AGND with a 1µF ceramic capacitor.
E1	PGND1	Step-Down Converter 1 Power Ground. Bypass IN1 to PGND1 with a 10µF ceramic capacitor as close as possible to the IC.
E2	LX1	Inductor Connection for Buck 1. LX is high impedance when disabled.
E3	OUT1	Step-Down Converter 1 Output Sense and Discharge Connection. Bypass OUT1 to PGND1 with a 22µF ceramic capacitor. OUT1 can also be connected to ground through an internal 100Ω resistor using an I^2C command when disabled.
E4	AV	Analog Input Supply. Connect AV to IN1 and IN2. Bypass AV to AGND with 1µF ceramic capacitor as close as possible to the IC.
E5	LDO3	LDO3 Output. Bypass LDO3 to AGND with a 1µF ceramic capacitor.
E6	LDO6	LDO6 Output. Bypass LDO6 to AGND with a 1µF ceramic capacitor.

General Description

The MAX8967's two ultra-low I_Q step-down converters are ideal for powering modems, applications processor cores, memory, system I/O, and portable devices. In normal operation, these step-down converters consume only 16μA (typ) of quiescent current. In green mode, the quiescent current is reduced to 5μA (typ) per converter with reduced load capability. Each step-down converter can be independently put into green mode by writing a bit in its control register.

Step-Down Converters

Each step-down converter provides internal feedback, minimizing external component count. Both step-down converter output voltages are programmed through the IC's serial interface. A 4.4MHz switching frequency minimizes external component size. Dynamic voltage scaling is available to reduce power consumption. Both step-down converters feature automatic transition from skip mode to FPWM operation. Forced PWM operation can be enabled by writing a bit in a control register.

Interleaved Switching

The step-down converter's high-side switches turn on during opposite clock edges of the oscillator. This helps minimize input current ripple, thus reducing the input capacitance required to reduce input voltage ripple.

Skip Mode/FPWM Operation

In the normal operating state, both step-down converters automatically transition from skip mode to fixed-frequency operation as load current increases. For operating modes where lowest output ripple is required, forced PWM switching behavior can be enabled by writing a bit in the appropriate FPWM_ register. See Table 3 and Table 15.

Voltage Control Using V_{ID}

Both step-down converters feature V_{ID} control to reduce power consumption in the loads such as modem and applications processor cores. Each V_{ID} control allows the converter to transition between two states setup in advance using I^2C. Essentially two voltage states are accessible without the overhead associated with I^2C control. V_{ID} control allows the core voltages to be reduced when the processor clock is throttled back. When exiting sleep mode (by changing the state of V_{ID}), the normal core voltages are restored, providing the optimal operating condition for best system performance.

Remote Output Voltage Sensing

Each step-down converter's output features remote output voltage sensing for improved output voltage accuracy. The remote sense accommodates a distance that incures up to a 200mV correction in the output voltage. The SNSP_ and SNSN_ inputs connect directly across the load, with the SNSN_ connected to a quiet analog ground near the load, and SNSP_ connected directly to the output bypass capacitor.

The remote sense feature requires a 1V or greater difference between AV and OUT_ for best performance. The remote sense feature can be disabled through registers to reduce quiescent current consumption. In addition, this feature is disabled during green mode operation.

Output Voltage Slew Rate

Both step-down converters feature an adjustable slew rate when increasing or decreasing output voltage. The nominal slew rate is 12.5mV/μs. Two additional slew rates are provided (25mV/μs and 50mV/μs), so that faster and slower slew rates can be programmed. An option for fastest possible ramp rate is also provided to allow the converter to operate at current limit for the fastest possible slew rate.

When decreasing the output voltage, two settings are provided with a single register bit. When this control bit is set, the converter operates in forced PWM (FPWM) mode with negative inductor current so that the output voltage can be decreased in finite steps at the selected slew rate. When this control bit is reset, the converter operates in skip mode, and the actual slew rate of the output is dependent on the external load, and might not necessarily track the slew rate set for falling output voltages.

Output Ripple

For normal operation (not in green mode), output ripple should be < $20mV_{P-P}$ for an output current < 50mA. Ripple can be further reduced by increasing output capacitance above the minimum for stable operation. Transition from skip to PWM operation should occur at current levels below 50mA. In green mode, the output ripple can increase to $40mV_{P-P}$ (max) for $V_{OUT\_}$ = 0.7V. This value can be decreased by adding additional output capacitance.

Green Mode Operation

In green mode, the quiescent current of each of the step-down converters are reduced from 16µA (typ) to 5µA (typ). If the output voltages are adjusted during green mode slew rate is very slow. Also, output current is limited to 5mA. Green mode is enabled by setting bits PWR_[5:4] = 10 in the appropriate converter's control register. See Table 3. Each converter can be individually selected to enter green mode.

Discharge Resistance

The IC provides an internal 100Ω discharge resistor for each disabled step-down converter. The discharge resistor connection can be enabled and disabled through the nADEN_ register bit for maximum flexibility. See Table 3.

LDO Detailed Description

The IC provides six LDOs with adjustable outputs as shown in Table 1.

Shutdown, Standby, and Reset

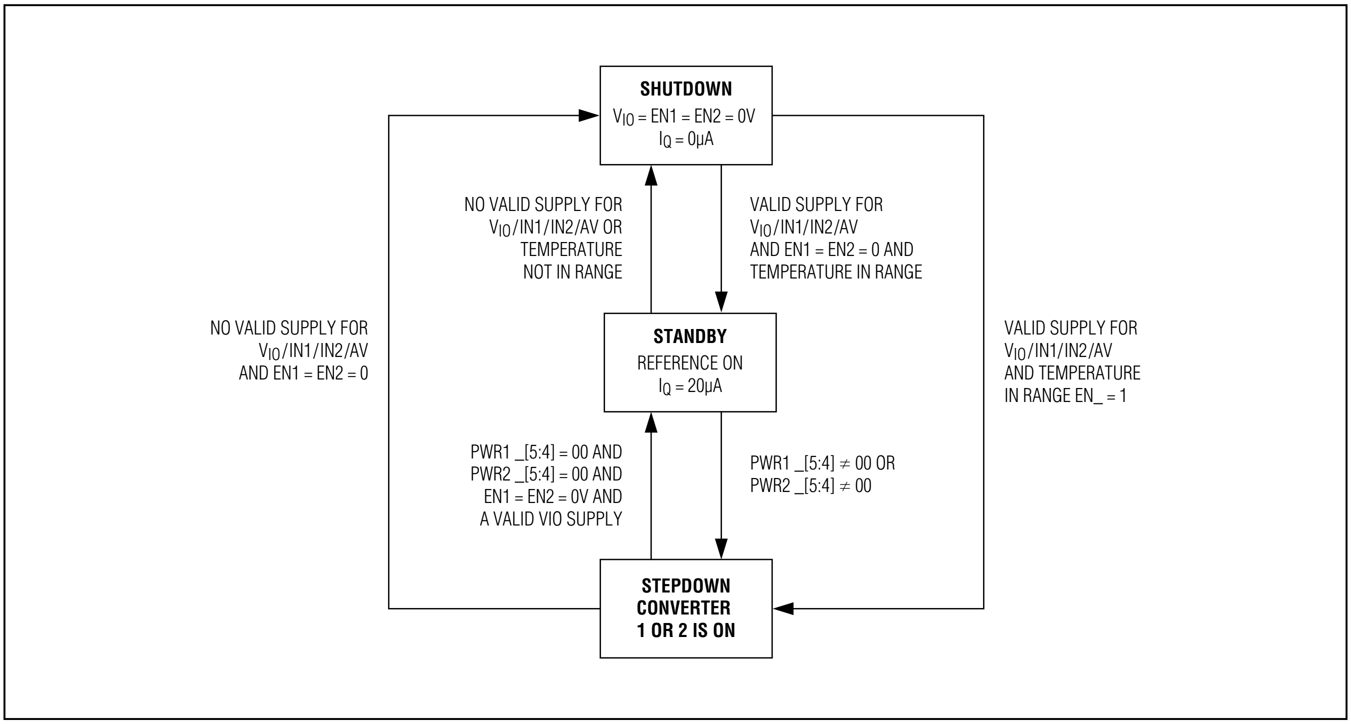


Figure 1. Power Mode State Diagram

Table 1. LDO Description

LDO	$V_{IN\_}$ RANGE (V)	INPUT SUPPLY	V_{OUT} RANGE (V)	MAXIMUM OUTPUT CURRENT (mA)	C_{OUT} (µF)
LDO1	1.7 to 5.5	INA	0.8 to 3.95	150	1
LDO2	1.7 to 5.5	INA	0.8 to 3.95	300	1
LDO3	1.7 to 5.5	INA	0.8 to 3.95	150	1
LDO4	1.7 to 5.5	INB	0.8 to 3.95	150	1
LDO5	1.7 to 5.5	INB	0.8 to 3.95	300	1
LDO6	1.7 to 5.5	INB	0.8 to 3.95	150	1

LDO Power Modes

All LDO regulators have independent enable and disable control through their LDO_PWR[7:6] bits. In addition, each LDO has a special green mode that reduces the quiescent current to 1.5µA (typ). In green mode, each regulator supports a load of up to 10mA. The load regulation performance degrades proportionally with the reduced load current.

Several usage options are available for green mode. To force individual regulators to green mode set LDO_PWR[7:6] = 10.

Soft-Start and Dynamic Voltage Change

The LDO regulators have a programmable soft-start rate. When an LDO is enabled, the output voltage ramps to its final voltage at a slew rate of either 5mV/Fs or 100mV/Fs, depending on the state of the LDO_SS bit. See Table 3 and Table 20.

The 5mV/µs ramp rate limits the input inrush current to around 5mA on a 300mA regulator with a 1µF output capacitor and no load. The 100mV/µs ramp rate results in a 100mA inrush current with a 1µF output capacitor and no load, but achieves regulation within 50µs. The soft-start ramp rate is also the rate of change at the output when switching dynamically between two output voltages without disabling.

The soft-start circuitry of the LDOs supports starting into a prebiased output.

Power-OK Comparator

Each regulator includes a power-OK (POK) comparator. The POK comparator signals (LDO_POK) indicate when each output has lost regulation (i.e., the output voltage is below V_{POKTHL}). The POK signal has a 25µs noise immunity filter ($V_{POKNF\_}$). The POK comparator is disabled in green mode to save power. When any of the POK signals (LDO_POK) go low, then an interrupt is generated.

Note that the LDOs implement a proprietary POK scheme that allows the POK comparator to operate correctly even while the LDO is in its soft-start period. If the LDO is overloaded when it is in its soft-start period, POK is low. If it is not overloaded during its soft-start period, POK is high.

Active Discharge

Each linear regulator has an active-discharge resistor feature that can be enabled/disabled with the LDO_ADE bit. See Table 3 and Table 20. Enabling the active discharge feature helps ensure a complete and timely power-down of all system peripherals. The default condition of the active-discharge resistor feature is enabled so that whenever VUVLO,LDO_ is below its UVLO threshold, all regulators are disabled with their active discharge resistors turned on. When VUVLO,LDO_ is less than 1.0V, the NMOS transistors that control the active discharge resistors lose their gate drive and become open.

When the regulator is disabled while the active discharge is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load.

When the regulator is enabled, the internal active-discharge resistor is not connected to its output. When the regulator is disabled while the active discharge is enabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance.

Adjustable Compensation

All six LDOs have adjustable compensation to facilitate remote capacitor capability. This feature can be used to adjust the compensation of the LDO based on the resistance and inductance to the remote capacitor. This ability allows each LDO to be programmed for optimal load transient performance based on the location of its remote capacitor. See Table 20 for more details. The LDO compensation should be switched only when that LDO is off. If the compensation switches when the LDO is enabled, it causes unknown output glitches, due to switching in uncharged capacitors as compensation changes.

Overvoltage Clamp

Each LDO has an overvoltage clamp that allows it to sink current when the output voltage is above its target voltage. This overvoltage clamp is default enabled but can be disabled with LDO_OVCLMP_EN. See Table 3 and Table 15. The following list briefly describes three typical applications scenarios that pertain to the overvoltage clamp.

- **LDO's Load Leaking Current into the LDO's Output:** Some LDO loads leak current into an LDO output during certain operating modes. This is typically seen with microprocessor loads. For example, a microprocessor with 3.3V, 2.5V, 1.8V, and 1.0V supply rails is running in standby mode. In this mode, the higher voltage rails can leak currents of several mA into the lower voltage rails. If the 1.0V rail is supplied by an LDO, the LDO output voltage rises based on the amount of leakage current. With the LDO overvoltage clamp enable, when the output voltage rises above its target regulation voltage, the overvoltage clamp sinks current from the output capacitor to bring the output voltage back within regulation.
- **Negative Load Transient to 0A:** When the LDO load current quickly ramps to 0A (i.e., 300mA to 0A load transient with 1µs transition time), the output voltage can overshoot (i.e., soar). Since the LDO cannot turn off its pass device immediately, the LDO output voltage overshoots. In this instance, when the output voltage sores above target regulation voltage, the overvoltage clamp sinks current from the output capacitor to bring the output voltage back within regulation.
- **Negative Dynamic Voltage Transition:** When the LDO output target voltage is decreased (i.e., 1.2V to 0.8V) when the system loading is light, the energy in the output capacitor tends to hold the output voltage up. When the output voltage is above its target regulation voltage, the overvoltage clamp sinks current from the output capacitor to bring the output voltage back within regulation.

LDO Interrupt

The power-OK comparators outputs drive a set of interrupts. Each regulator is capable of generating an interrupt, when the output goes out of regulation in normal operation. In green mode, the POK comparators are disabled and the regulators do not generate interrupts.

Thermal Considerations

In most applications, the IC does not dissipate much heat due to its high efficiency. But in applications where the IC runs at high ambient temperature with heavy loads, the heat dissipated can exceed the maximum junction temperature of the part. If the junction temperature reaches approximately +165°C, the thermal overload protection is activated.

The IC maximum power dissipation depends on the thermal resistance of the IC package and circuit board. The power dissipated in the device is:

$$PD = P_{OUT1} \times (1/\eta 1 - 1) + P_{OUT2} \times (1/\eta 2 - 1)$$

where $\eta 1$ and $\eta 2$ are the efficiencies of each converter while P_{OUT1} and P_{OUT2} are the output power of each converter.

The maximum allowed power dissipation is:

$$P_{MAX} = (T_{JMAX} - T_A)/\theta_{JA}$$

$T_{JMAX} - T_A$ is the temperature difference between the IC's maximum rated junction temperature and the surrounding air, θ_{JA} is the thermal resistance of the junction through the PCB, copper traces, and other materials to the surrounding air.

Digital Interface

The IC has four types of digital interface:

- Two enable pins (EN_), one for each step-down converter
- Two V_{ID} pins ($V_{ID\_}$), one for each step-down converter
- An interrupt pin, IRQB
- A two-wire I²C interface

The I²C interface is use to set the state of the IC while the two enable and two V_{ID} pins, one set for each step-down converter, are used to rapidly transition between on/off and two voltage and mode states previously defined using I²C communication.

Enable (EN_)

Two enable logic input pins are provided to allow rapid transitions between on and off for each step-down converter. The enable pins work in conjunction with the I²C step-down converter PWR MD (mode) bits to control on/off, normal or green mode, and enabling/disabling of remote sense per step-down converter. Each converter can be enabled through the dedicated enable pin or through the I²C with a logical OR function.

Voltage Identification Digital ($V_{ID\_}$)

Two $V_{ID\_}$ pins are provided to allow rapid transitions between two previously configured states for each step-down converter. There are multiple registers for output voltage and mode of operation for each converter as well.

IRQB

The IRQB is an active-low, open-drain output that signals a fault on any one or more of the step-down converters or LDOs. Each converter and LDO is individually monitored for its POK status, and thermal shutdown for the entire MAX8967 is monitored.

Table 2. Step-Down Converter Modes

EN_	I²C MD BITS		MODE
0	0	0	Off
0	0	1	On, green
0	1	0	On, normal, remote sense on
0	1	1	On, normal, remote sense off
1	0	0	On, normal, remote sense on
1	0	1	On, green
1	1	0	On, normal, remote sense on
1	1	1	On, normal, remote sense off

I²C Interface

An I²C-compatible, 2-wire serial interface controls the step-down converter output voltage, ramp rate, operating mode, and synchronization. The serial bus consists of a bidirectional serial-data line (SDA) and a serial-clock input (SCL). The master initiates data transfer on the bus and generates SCL to permit data transfer.

I²C is an active-low open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional resistors (24Ω) in series with SDA and SCL can protect the device inputs from high-voltage spikes on bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. See Figure 2. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section for more information.

Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is 9 bits long, 8 bits of data followed by the acknowledge bit. The IC supports data transfer rates with SCL frequencies up to 400kHz.

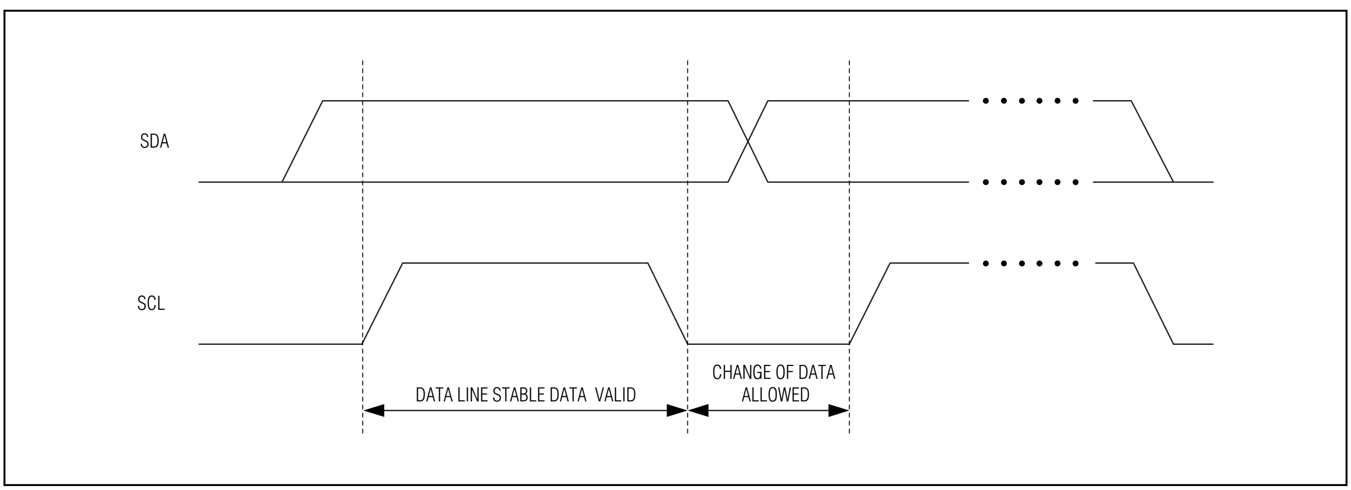


Figure 2. I²C Bit Transfer

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See Figure 3.

A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission by issuing a not-acknowledge (nACK) followed by a STOP condition. See the *Acknowledge* section for more information. The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP command to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the IC internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

System Configuration

A device on the I²C bus that generates a message is called a transmitter and a device that receives the message is a receiver. The device that controls the message is the master and the devices that are controlled by the master are called slaves.

Acknowledge

The number of data bytes between the START and STOP conditions for the transmitter and receiver are unlimited. Each 8-bit byte is followed by an acknowledge bit. The acknowledge bit is a high-level signal put on SDA by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the DATA line during the acknowledge clock pulse, so that the DATA line is stable low during the high period of the acknowledge clock pulse (setup and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a STOP condition.

Update of Output Operation Mode

If updating the output voltage or operation mode register for the mode that the is currently operating in, the output voltage/operation mode is updated at the same time the IC sends the acknowledge for the I²C data byte.

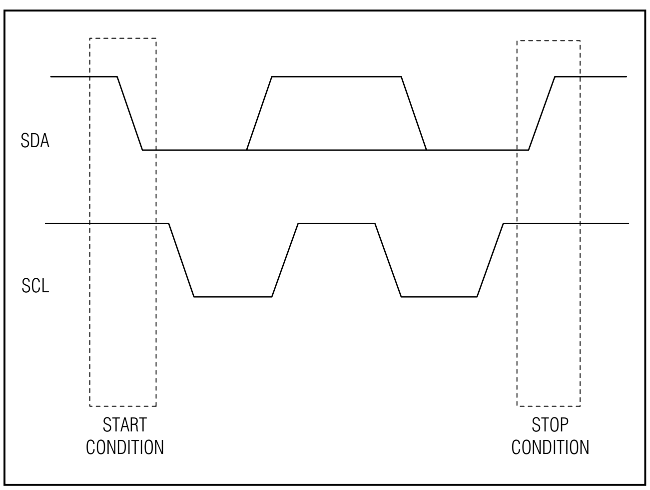


Figure 3. I²C START and STOP Conditions

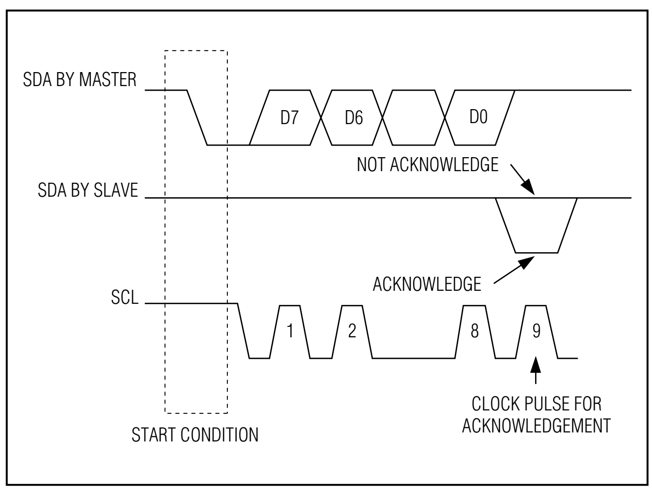


Figure 4. I²C Acknowledge

Slave Address

A bus master initiates communication IC by issuing a START condition followed by the slave address. The slave address byte consists of 7 address bits (1100011x) and a read/write bit (R/$\overline{W}$). After receiving the proper address, the IC issues an acknowledge by pulling SDA low during the ninth clock cycle.

The IC uses a default I²C slave address of C6h. There are two other slave addresses (C8h and CAh) that can be assigned. Contact the factory for details. See the *Selector Guide*.

Write Operations

The IC recognizes the write byte protocol as defined in the SMBus specification. The write byte protocol allows the I²C master device to send 1 byte of data to the slave device. The write byte protocol requires a register pointer address for the subsequent write. The IC acknowledges any register pointer even though only a subset of those registers actually exists in the device. The write byte protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte.
8) The slave updates with the new data.
9) The master sends a STOP condition.

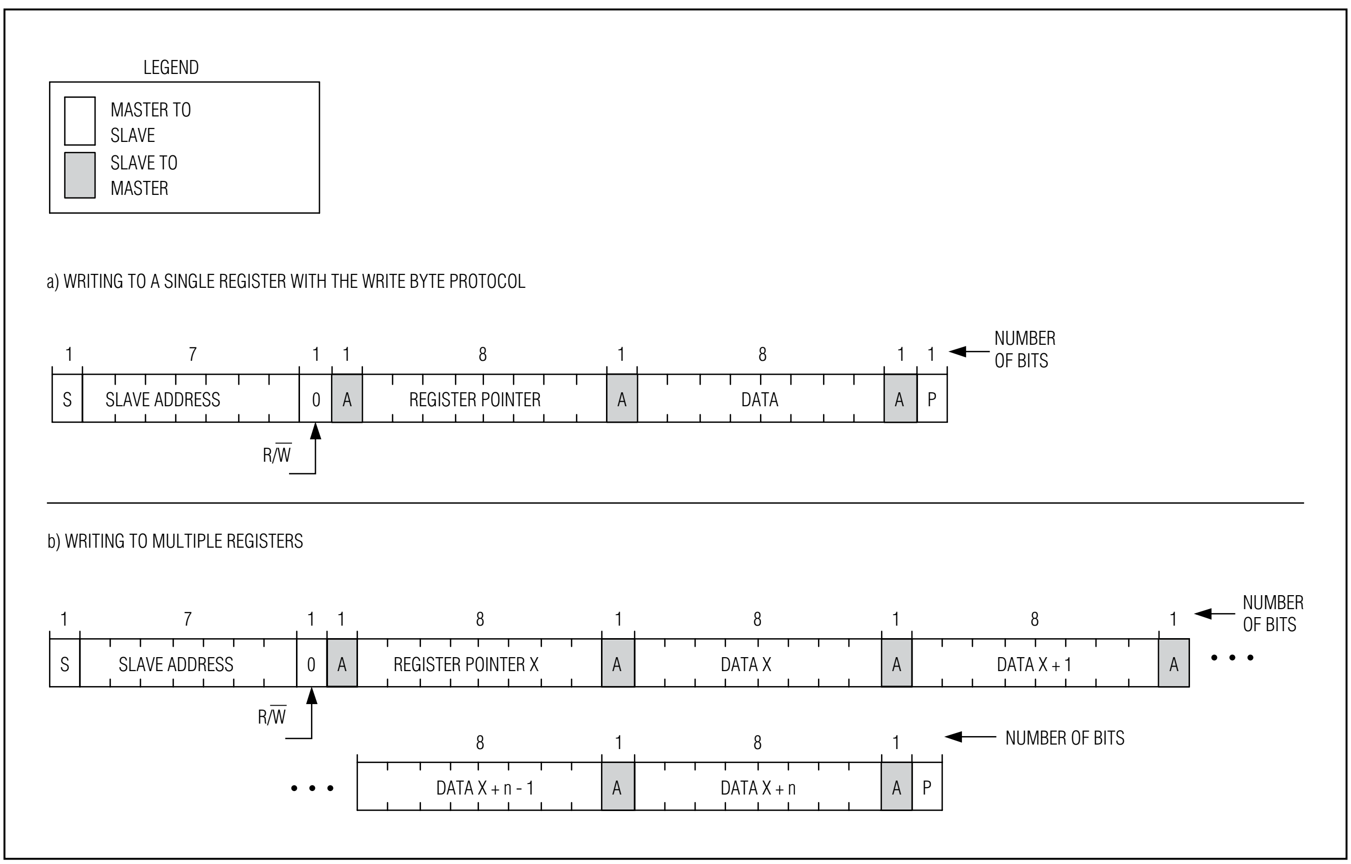


Figure 5. I²C Write Operation

In addition to the write-byte protocol, the IC can write to multiple registers as shown in Figure 5. This protocol allows the I2C master device to address the slave only once and then send data to a sequential block of registers starting at the specified register pointer.

Use the following procedure to write to a sequential block of registers:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends the 8-bit register pointer of the first register to write.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte.
8) The slave updates with the new data.
9) Steps 6 to 8 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
10) The master sends a STOP condition.

Read Operations

The method for reading a single register (byte) is shown below. To read a single register:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated START condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave assets an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master assets a not acknowledge by keeping SDA high.
11) The master sends a STOP condition.

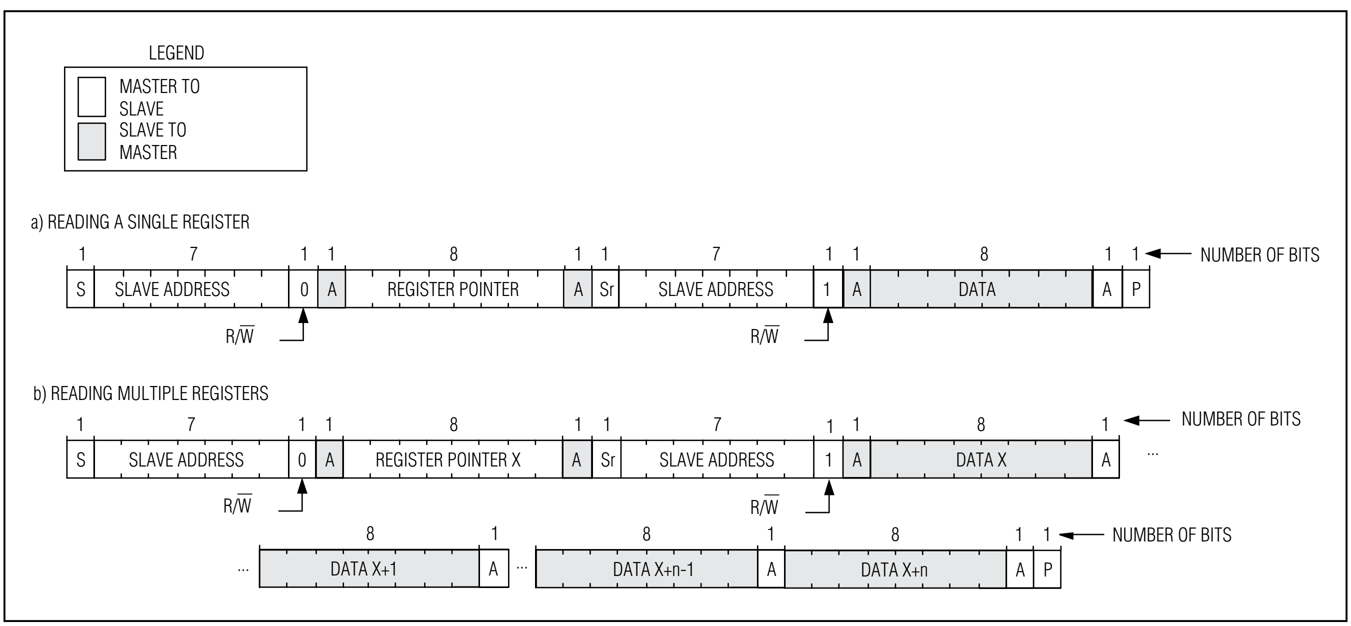


Figure 6. I2C Read Operation

In addition, the IC can read a block of multiple sequential registers as shown in section B of Figure 6. Use the following procedure to read a sequential block of registers:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer of the first register in the block.
5) The slave acknowledges the register pointer.
6) The master sends a repeated START condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave assets an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master assets an acknowledge by pulling SDA low when there is more data to read, or a not acknowledge by keeping SDA high when all data has been read.
11) Steps 9 and 10 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
12) The master sends a STOP condition.

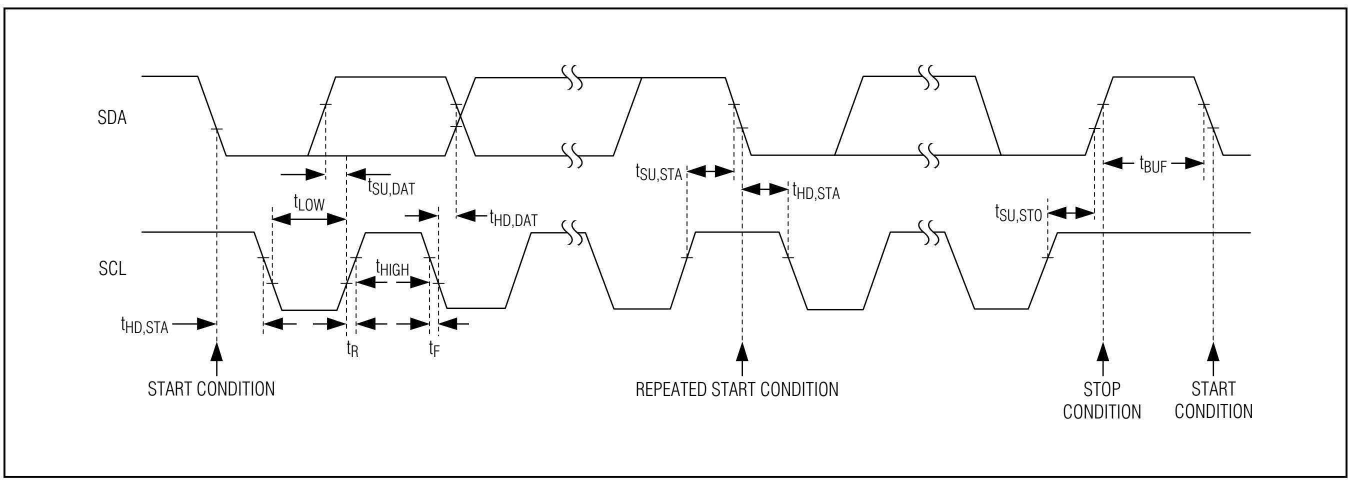


Figure 7. I²C Timing Diagram

I²C Commands

Register Reset

All resisters associated with the IC's I²C interface are reset to their default values when the voltage applied to V_{IO} drops below the 0.4V threshold. See the *Electrical Characteristics* table. The slave address of the IC is 0xC6.

I²C High Level Register Map

Table 3. I²C High Level Register Map

REGISTER	DESCRIPTION	BIT 7 MSB	6	5	4	3	2	1	0 LSB
0x00	ID	ID[7:0]							
0x01	Chip Configuration	FREQ[2:0]			RSVD	RSVD	RSVD	RSVD	RSVD
0x02	Step-Down 1 Voltage V_{ID} High	VOUT_B1_VIDH[7:0]							
0x03	Step-Down 1 Voltage V_{ID} Low	VOUT_B1_VIDL[7:0]							
0x04	Step-Down 1 Configuration V_{ID} High	SLEW1H[7:6]		PWR1H[5:4]		nADEN1H	FPWM1H	RSVD	FALL SLEW1H
0x05	Step-Down 1 Configuration V_{ID} Low	SLEW1L[7:6]		PWR1L[5:4]		nADEN1L	FPWM1L	RSVD	FALL SLEW1L
0x06	Step-Down 2 Voltage V_{ID} High	VOUT_B2_VIDH[7:0]							
0x07	Step-Down 2 Voltage V_{ID} Low	VOUT_B2_VIDL[7:0]							
0x08	Step-Down 2 Configuration V_{ID} High	SLEW2H[7:6]		PWR2H[5:4]		nADEN2H	FPWM2H	RSVD	FALL SLEW2H
0x09	Step-Down 2 Configuration V_{ID} Low	SLEW2L[7:6]		PWR2L[5:4]		nADEN2L	FPWM2L	RSVD	FALL SLEW2L
0x0B	Status	PNOK1	PNOK2	TH	LDO_ PNOK	RSVD	RSVD	RSVD	RSVD
0x0C	Interrupt	PNOK1_ INT	PNOK2_ INT	TH_INT	LDO_ PNOK_ INT	RSVD	RSVD	RSVD	RSVD
0x0D	Interrupt Mask	PNOK1M	PNOK2M	THM	LDO_ PNOKM	RSVD	RSVD	RSVD	RSVD
0x0E	LDO 1 Configuration 1	LDO1PWR[7:6]		LDO1TV[5:0]					
0x0F	LDO 1 Configuration 2	LDO1OV CLMP_EN	RSVD	LDO1COMP[5:4]		LDO1POK	RSVD	LDO1 ADE	LDO1SS
0x10	LDO 2 Configuration 1	LDO2PWR[7:6]		LDO2TV[5:0]					
0x11	LDO 2 Configuration 2	LDO2OV CLMP_EN	RSVD	LDO2COMP[5:4]		LDO2POK	RSVD	LDO2 ADE	LDO2SS
0x12	LDO 3 Configuration 1	LDO3PWR[7:6]		LDO3TV[5:0]					
0x13	LDO 3 Configuration 2	LDO3OV CLMP_EN	RSVD	LDO3COMP[5:4]		LDO3POK	RSVD	LDO3 ADE	LDO3SS

Table 3. I²C High Level Register Map (continued)

REGISTER	DESCRIPTION	BIT							
		7 MSB	6	5	4	3	2	1	0 LSB
0x14	LDO 4 Configuration 1	LDO4PWR[7:6]		LDO4TV[5:0]					
0x15	LDO 4 Configuration 2	LDO4OV CLMP_EN	RSVD	LDO4COMP[5:4]		LDO4POK	RSVD	LDO4 ADE	LDO4SS
0x16	LDO 5 Configuration 1	LDO5PWR[7:6]		LDO5TV[5:0]					
0x17	LDO 5 Configuration 2	LDO5OV CLMP_EN	RSVD	LDO5COMP[5:4]		LDO5POK	RSVD	LDO5 ADE	LDO5SS
0x18	LDO 6 Configuration 1	LDO6PWR[7:6]		LDO6TV[5:0]					
0x19	LDO 6 Configuration 2	LDO6OV CLMP_EN	RSVD	LDO6COMP[5:4]		LDO6POK	RSVD	LDO6 ADE	LDO6SS
0x1B	LDO INT	RSVD		L06_INT	L05_INT	L04_INT	L03_INT	L02_INT	L01_INT
0x1C	LDO INTM	RSVD		L06_INTM	L05_INTM	L04_INTM	L03_INTM	L02_INTM	L01_INTM

Table 4. ID Register

COMMAND NAME	ID
I²C address	MAX8967 I²C address
Command code	**0x00**
Access type	Read only
Reset condition	Hard wired, not reset

BIT	NAME	DESCRIPTION	DEFAULT
7–0	ID[7:0]	Code is a unique chip version identifier	0x66

Table 5. Chip Configuration Register

COMMAND NAME	CHIP CONFIGURATION
I²C address	MAX8967 I²C address
Command code	**0x01**
Access type	Read/write
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7, 6, 5	FREQ[2:0]	Switching frequency selection bits 000 = 4.4MHz 100 = 4.2MHz 001 = 4.8MHz 101 = RSVD 010 = 4.0MHz 110 = 4.6MHz 011 = RSVD 111 = RSVD	0b000
4–0	Reserved	—	0b0

Table 6. Step-Down 1 Output Voltage VID High

COMMAND NAME	STEP-DOWN CONVERTER 1 VOLTAGE VID HIGH
I²C address	MAX8967 I²C address
Command code	**0x02**
Access type	Read/write
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7:0	VOUT_ B1_VIDH [7:0]	See Table 14	0x00

Table 7. Step-Down 1 Output Voltage VID Low

COMMAND NAME	STEP-DOWN CONVERTER 1 VOLTAGE VID LOW
I²C address	MAX8967 I²C address
Command code	**0x03**
Access type	Read/write
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7–0	VOUT_B1_VIDL [7:0]	See Table 14	0x30

Table 8. Step-Down 1 Configuration Register VID High

COMMAND NAME	STEP-DOWN CONVERTER 1 CONFIGURATION VID HIGH
I²C address	MAX8967 I²C address
Command code	**0x04**
Access type	Read/write
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7–0	See Table 15	See Table 15	0x00

Table 9. Step-Down 1 Configuration Register VID Low

COMMAND NAME	STEP-DOWN CONVERTER 1 CONFIGURATION VID LOW
I²C address	MAX8967 I²C address
Command code	**0x05**
Access type	Read/write
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7–0	See Table 15	See Table 15	0x00

Table 10. Step-Down 2 Voltage Register VID High

COMMAND NAME	STEP-DOWN 2 VOLTAGE VID HIGH
I²C address	MAX8967 I²C address
Command code	**0x06**
Access type	Read/write
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7–0	VOUT_B2_VIDH[7:0]	See Table 14	0x00

Table 11. Step-Down 2 Output Voltage VID Low

COMMAND NAME	STEP-DOWN 2 VOLTAGE VID LOW
I²C address	MAX8967 I²C address
Command code	**0x07**
Access type	Read/write
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7–0	VOUT_B2_VIDL[7:0]	See Table 14	0x30

Table 12. Step-Down 2 Configuration Register VID High

COMMAND NAME	STEP-DOWN 2 CONFIGURATION VID HIGH
I²C address	MAX8967 I²C address
Command code	**0x08**
Access type	Read/write
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7–0	See Table 15	See Table 15	0x00

Table 13. Step-Down 2 Configuration Register VID Low

COMMAND NAME	STEP-DOWN 2 CONFIGURATION VID LOW
I²C address	MAX8967 I²C address
Command code	**0x09**
Access type	Read/write
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7–0	See Table 15	See Table 15	0x00

Table 14. Step-Down Output Voltage Table

BIT	DESCRIPTION							DEFAULT
VOUT_B_ VID_[7:0]	0x00 = 0.6000V	0x20 = 1.0000V	0x40 = 1.4000V	0x60 = 1.8000V	0x80 = 2.2000V	0xA0 = 2.6000V	0xC0 = 3.0000V	See the *Electrical Characteristics* table.
	0x01 = 0.6125V	0x21 = 1.0125V	0x41 = 1.4125V	0x61 = 1.8125V	0x81 = 2.2125V	0xA1 = 2.6125V	0xC1 = 3.0125V	
	0x02 = 0.6250V	0x22 = 1.0250V	0x42 = 1.4250V	0x62 = 1.8250V	0x82 = 2.2250V	0xA2 = 2.6250V	0xC2 = 3.0250V	
	0x03 = 0.6375V	0x23 = 1.0375V	0x43 = 1.4375V	0x63 = 1.8375V	0x83 = 2.2375V	0xA3 = 2.6375V	0xC3 = 3.0375V	
	0x04 = 0.6500V	0x24 = 1.0500V	0x44 = 1.4500V	0x64 = 1.8500V	0x84 = 2.2500V	0xA4 = 2.6500V	0xC4 = 3.0500V	
	0x05 = 0.6625V	0x25 = 1.0625V	0x45 = 1.4625V	0x65 = 1.8625V	0x85 = 2.2625V	0xA5 = 2.6625V	0xC5 = 3.0625V	
	0x06 = 0.6750V	0x26 = 1.0750V	0x46 = 1.4750V	0x66 = 1.8750V	0x86 = 2.2750V	0xA6 = 2.6750V	0xC6 = 3.0750V	
	0x07 = 0.6875V	0x27 = 1.0875V	0x47 = 1.4875V	0x67 = 1.8875V	0x87 = 2.2875V	0xA7 = 2.6875V	0xC7 = 3.0875V	
	0x08 = 0.7000V	0x28 = 1.1000V	0x48 = 1.5000V	0x68 = 1.9000V	0x88 = 2.3000V	0xA8 = 2.7000V	0xC8 = 3.1000V	
	0x09 = 0.7125V	0x29 = 1.1125V	0x49 = 1.5125V	0x69 = 1.9125V	0x89 = 2.3125V	0xA9 = 2.7125V	0xC9 = 3.1125V	
	0x0A = 0.7250V	0x2A = 1.1250V	0x4A = 1.5250V	0x6A = 1.9250V	0x8A = 2.3250V	0xAA = 2.7250V	0xCA = 3.1250V	
	0x0B = 0.7375V	0x2B = 1.1375V	0x4B = 1.5375V	0x6B = 1.9375V	0x8B = 2.3375V	0xAB = 2.7375V	0xCB = 3.1375V	
	0x0C = 0.7500V	0x2C = 1.1500V	0x4C = 1.5500V	0x6C = 1.9500V	0x8C = 2.3500V	0xAC = 2.7500V	0xCC = 3.1500V	
	0x0D = 0.7625V	0x2D = 1.1625V	0x4D = 1.5625V	0x6D = 1.9625V	0x8D = 2.3625V	0xAD = 2.7625V	0xCD = 3.1625V	
	0x0E = 0.7750V	0x2E = 1.1750V	0x4E = 1.5750V	0x6E = 1.9750V	0x8E = 2.3750V	0xAE = 2.7750V	0xCE = 3.1750V	
	0x0F = 0.7875V	0x2F = 1.1875V	0x4F = 1.5875V	0x6F = 1.9875V	0x8F = 2.3875V	0xAF = 2.7875V	0xCF = 3.1875V	
	0x10 = 0.8000V	0x30 = 1.2000V	0x50 = 1.6000V	0x70 = 2.0000V	0x90 = 2.4000V	0xB0 = 2.8000V	0xD0 = 3.2000V	
	0x11 = 0.8125V	0x31 = 1.2125V	0x51 = 1.6125V	0x71 = 2.0125V	0x91 = 2.4125V	0xB1 = 2.8125V	0xD1 = 3.2125V	
	0x12 = 0.8250V	0x32 = 1.2250V	0x52 = 1.6250V	0x72 = 2.0250V	0x92 = 2.4250V	0xB2 = 2.8250V	0xD2 = 3.2250V	
	0x13 = 0.8375V	0x33 = 1.2375V	0x53 = 1.6375V	0x73 = 2.0375V	0x93 = 2.4375V	0xB3 = 2.8375V	0xD3 = 3.2375V	

Table 14. Step-Down Output Voltage Table (continued)

BIT	DESCRIPTION							DEFAULT
VOUT_ B_ VID_[7:0]	0x14 = 0.8500V	0x34 = 1.2500V	0x54 = 1.6500V	0x74 = 2.0500V	0x94 = 2.4500V	0xB4 = 2.8500V	0xD4 = 3.2500V	See the *Electrical Characteristics* table.
	0x15 = 0.8625V	0x35 = 1.2625V	0x55 = 1.6625V	0x75 = 2.0625V	0x95 = 2.4625V	0xB5 = 2.8625V	0xD5 = 3.2625V	
	0x16 = 0.8750V	0x36 = 1.2750V	0x56 = 1.6750V	0x76 = 2.0750V	0x96 = 2.4750V	0xB6 = 2.8750V	0xD6 = 3.2750V	
	0x17 = 0.8875V	0x37 = 1.2875V	0x57 = 1.6875V	0x77= 2.0875V	0x97 = 2.4875V	0xB7 = 2.8875V	0xD7 = 3.2875V	
	0x18 = 0.9000V	0x38 = 1.3000V	0x58 = 1.7000V	0x78 = 2.1000V	0x98 = 2.5000V	0xB8 = 2.9000V	0xD8 = 3.3000V	
	0x19 = 0.9125V	0x39 = 1.3125V	0x59 = 1.7125V	0x79 = 2.1125V	0x99 = 2.5125V	0xB9 = 2.9125V	0xD9 = 3.3125V	
	0x1A = 0.9250V	0x3A = 1.3250V	0x5A = 1.7250V	0x7A = 2.1250V	0x9A = 2.5250V	0xBA = 2.9250V	0xDA = 3.3250V	
	0x1B = 0.9375V	0x3B = 1.3375V	0x5B = 1.7375V	0x7B = 2.1375V	0x9B = 2.5375V	0xBB = 2.9375V	0xDB = 3.3375V	
	0x1C = 0.9500V	0x3C = 1.3500V	0x5C = 1.7500V	0x7C = 2.1500V	0x9C = 2.5500V	0xBC = 2.9500V	0xDC = 3.3500V	
	0x1D = 0.9625V	0x3D = 1.3625V	0x5D = 1.7625V	0x7D = 2.1625V	0x9D = 2.5625V	0xBD = 2.9625V	0xDD = 3.3625V	
	0x1E = 0.9750V	0x3E = 1.3750V	0x5E = 1.7750V	0x7E = 2.1750V	0x9E = 2.5750V	0xBE = 2.9750V	0xDE = 3.3750V	
	0x1F = 0.9875V	0x3F = 1.3875V	0x5F = 1.7875V	0x7F = 2.1875V	0x9F = 2.5875V	0xBF = 2.9875V	0xDF = 3.3875V	

Table 15. Step-Down Configuration Table

BIT	NAME	DESCRIPTION	DEFAULT
0	FALLSLEW_	**Active-Low Step-Down Converter Falling Slew Rate Enable** 0 = The slew rate control circuit is active when the output voltage is decreased. The desired regulation voltage is decreased in 12.5mV steps, and forced PWM mode is enabled so that negative inductor current can be used to pull energy out of the output capacitor. 1 = The slew rate control circuit is disabled when the output voltage is decreased. The desired regulation voltage is decreased in 12.5mV steps, but it is up to the external load to drain energy from the output capacitor in order to pull down on the output voltage.	0b0
1	RSVD	Reserved	0b0
2	FPWM_	**Step-Down Forced PWM Mode Enable** 0 = Step-Down Converter automatically skips pulses under light load conditions, and transfers to fixed frequency operation as the load current increases. 1 = Step-Down Converter operates with fixed frequency under all load conditions.	0b0
3	nADEN_	**Active-Low Buck Converter Active Discharge Enable** 0 = The active discharge function is enabled. When the buck converter is disabled, an internal 100Ω discharge resistor is connected to the output to discharge the energy stored in the output capacitor. When the buck converter is enabled, the discharge resistor is disconnected from the output. 1 = The active discharge function is disabled. When the buck converter is disabled, the internal 100Ω discharge resistor is not connected to the output, and the discharge rate is dependent on the output capacitance and the load present. When the buck converter is enabled, the discharge resistor is disconnected from the output.	0b0
5:4	PWR_[5:4]	**Step-Down Power Mode Configuration.** These bits determine the mode of operation for this converter. 00 = Disabled 01 = Normal operation mode with remote sense disabled 10 = Green mode 11 = Normal operation mode with remote sense enabled	0b00
7:6	SLEW_[7:6]	**Step-Down Rising Slew Rate** 00 = 12.5mV/µs ramp rate 01 = 25mV/µs ramp rate 10 = 50mV/µs ramp rate 11 = No slew rate control. Output voltage increases as fast as the current limit allows.	0b00

Table 16. Status

COMMAND NAME	STATUS
I²C address	MAX8967 I²C address
Command code	**0x0B**
Access type	Read only. Status is masked by the interrupt mask register and is cleared by reading related interrupt register bits.
Reset condition	Power-up/chip reset/0b1 written to bit

BIT	NAME	DESCRIPTION	DEFAULT
7	PNOK1	0 = Step-down converter 1 is on. 1 = Step-down converter 1 is off or faulted.	0b1
6	PNOK2	0 = Step-down converter 2 is on. 1 = Step-down converter 2 is off or faulted.	0b1
5	TH	0 = Temperature is below the thermal shutdown threshold. 1 = Temperature exceeds the thermal shutdown threshold.	0b0
4	LDO_PNOK	0 = One or more LDOs are off or above the POK threshold. 0 = One or more LDOs are on and below the POK threshold.	0b0
3	RSVD	Reserved	0b1
2	RSVD	Reserved	0b1
1	RSVD	Reserved	0b1
0	RSVD	Reserved	0b1

Table 17. Interrupt

COMMAND NAME	INTERRUPT
I²C address	MAX8967 I²C address
Command code	**0x0C**
Access type	Read—clear on read
Reset condition	Power-up/chip reset/0b1 written to bit

BIT	NAME	DESCRIPTION	DEFAULT
7	PNOK1_INT	**Step-Down 1 Interrupt Bit** 0 = Output is normal 1 = Output has fallen below the power-OK threshold.	0b0
6	PNOK2_INT	**Step-Down 2 Interrupt Bit** 0 = Output is normal 1 = Output has fallen below the power-OK threshold.	0b0
5	TH_INT	**Thermal Interrupt Bit** 0 = Die temperature is normal 1 = Die temperature has exceeded thermal shutdown threshold	0b0
4	LDO_PNOK_INT	One or more LDO power-OK levels have not been maintained.	0b0
3	RSVD	Reserved	0b0
2	RSVD	Reserved	0b0
1	RSVD	Reserved	0b0
0	RSVD	Reserved	0b0

Table 18. Interrupt Mask

COMMAND NAME	INTERRUPT MASK
I²C address	MAX8967 I²C address
Command code	**0x0D**
Access type	Read–clear on read
Reset condition	Power-up/chip reset/0b1 written to bit

BIT	NAME	DESCRIPTION	DEFAULT
7	PNOK1M	**Step-Down 1 Interrupt Mask Bit** 0 = Interrupt is unmasked. 1 = Interrupt is masked.	0b1
6	PNOK2M	**Step-Down 2 Interrupt Mask Bit** 0 = Interrupt is unmasked. 1 = Interrupt is masked.	0b1
5	THM	**Thermal Interrupt Mask Bit** 0 = Interrupt is unmasked. 1 = Interrupt is masked.	0b1
4	LDO_PNOKM	**LDO Interrupt Mask Bit** 0 = Interrupt is unmasked. 1 = Interrupt is masked.	0b1
3	RSVD	Reserved	0b1
2	RSVD	Reserved	0b0
1	RSVD	Reserved	0b0
0	RSVD	Reserved	0b0

Table 19. LDO_ Configuration 1 Register

REGISTER NAME	LDO_ CONFIGURATION 1
Register address	See Table 3
Access type	Read/write
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7, 6	LDO_PWR [7:6]	**LDO Power Mode Configuration** 00 = Output disabled 01 = Output disabled 10 = Green mode 11 = Normal mode	0b00
5–0	LDO_TV[5:0]	**Sets the Target Voltage of the LDO.** Programmed in 0.05V steps. 0x00 = 0.80V, 0x0A = 1.30V, 0x14 = 1.80V, 0x1E = 2.30V, 0x28 = 2.80V, 0x32 = 3.30V, 0x3C = 3.80V 0x01 = 0.85V, 0x0B = 1.35V, 0x15 = 1.85V, 0x1F = 2.35V, 0x29 = 2.85V, 0x33 = 3.35V, 0x3D = 3.85V 0x02 = 0.90V, 0x0C = 1.40V, 0x16 = 1.90V, 0x20 = 2.40V, 0x2A = 2.90V, 0x34 = 3.40V, 0x3E = 3.90V 0x03 = 0.95V, 0x0D = 1.45V, 0x17 = 1.95V, 0x21 = 2.45V, 0x2B = 2.95V, 0x35 = 3.45V, 0x3F = 3.95V 0x04 = 1.00V, 0x0E = 1.50V, 0x18 = 2.00V, 0x22 = 2.50V, 0x2C = 3.00V, 0x36 = 3.50V 0x05 = 1.05V, 0x0F = 1.55V, 0x19 = 2.05V, 0x23 = 2.55V, 0x2D = 3.05V, 0x37 = 3.55V 0x06 = 1.10V, 0x10 = 1.60V, 0x1A = 2.10V, 0x24 = 2.60V, 0x2E = 3.10V, 0x38 = 3.60V 0x07 = 1.15V, 0x11 = 1.65V, 0x1B = 2.15V, 0x25 = 2.65V, 0x2F = 3.15V, 0x39 = 3.65V 0x08 = 1.20V, 0x12 = 1.70V, 0x1C = 2.20V, 0x26 = 2.70V, 0x30 = 3.20V, 0x3A = 3.70V 0x09 = 1.25V, 0x13 = 1.75V, 0x1D = 2.25V, 0x27 = 2.75V, 0x31 = 3.25V, 0x3B = 3.75V	0b00

Table 20. LDO_ Configuration 2 Register

REGISTER NAME	LDO_ CONFIGURATION 2
Register address	See Table 3.
Access type	Read only for bit 3, and read/write for the rest
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7	LDO_OVCLMP_EN	**Overvoltage Clamp Enable** 0 = Overvoltage clamp disabled. 1 = Overvoltage clamp enabled.	0b1
6	RSVD	Reserved	0b0
5, 4	LDO_COMP	**LDO Compensation** 00 = Assume 50mΩ/5nH trace impedance to remote capacitor. 01 = Assume 100mΩ/10nH trace impedance to remote capacitor. 10 = Assume 50mΩ to 200mΩ /5nH to 20nH trace impedance to remote capacitor. 11 = Assume 100mΩ to 400mΩ /10nH to 40nH trace impedance to remote capacitor. **Note:** The LDO_COMP bits should only be changed with the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.	0b01
3	LDO_POK	**Voltage OK Status Bit** 0 = The voltage is less than the POK threshold and the device is in normal mode. 1 = The voltage is above the POK threshold or the LDO is operating in its green mode or the LDO is disabled.	0b0
2	RSVD	Reserved	—
1	LDO_ADE	**Active Discharge Enable** 0 = The active discharge function is disabled. 1 = The active discharge function is enabled.	0b1
0	LDO_SS	**Sets the LDO Soft-Start Slew Rate** (Applies to both startup and output voltage setting changes) 0 = Fast Startup and Dynamic Voltage Change—100mV/µs. 1 = Slow Startup and Dynamic Voltage Change—5mV/µs.	0b1

Table 21. LDO_INT Register

REGISTER NAME	LDO_INT
Register address	**0x1B**
Access type	Read—clear on read
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7, 6	RSVD	Reserved	
5	L06_INT	**LDO6 Interrupt Bit** 0 = LDO output is normal. 1 = LDO output has fallen below the power-OK threshold.	0b0
4	L05_INT	**LDO5 Interrupt Bit** 0 = LDO output is normal. 1 = LDO output has fallen below the power-OK threshold.	0b0
3	L04_INT	**LDO4 Interrupt Bit** 0 = LDO output is normal. 1 = LDO output has fallen below the power-OK threshold.	0b0
2	L03_INT	**LDO3 Interrupt Bit** 0 = LDO output is normal. 1 = LDO output has fallen below the power-OK threshold.	0b0
1	L02_INT	**LDO2 Interrupt Bit** 0 = LDO output is normal. 1 = LDO output has fallen below the power-OK threshold.	0b0
0	L01_INT	**LDO1 Interrupt Bit** 0 = LDO output is normal. 1 = LDO output has fallen below the power-OK threshold.	0b0

Table 22. LDO_INTM Register

REGISTER NAME	LDO_INTM
Register address	0x1C
Access type	Read—clear on read
Reset condition	Power-up/chip reset

BIT	NAME	DESCRIPTION	DEFAULT
7, 6	RSVD	Reserved	0b11
5	L06_INTM	**LDO6 Interrupt Mask Bit** 0 = Interrupt is unmasked. 1 = Interrupt is masked.	0b1
4	L05_INTM	**LDO5 Interrupt Mask Bit** 0 = Interrupt is unmasked. 1 = Interrupt is masked.	0b1
3	L04_INTM	**LDO4 Interrupt Mask Bit** 0 = Interrupt is unmasked. 1 = Interrupt is masked.	0b1
2	L03_INTM	**LDO3 Interrupt Mask Bit** 0 = Interrupt is unmasked. 1 = Interrupt is masked.	0b1
1	L02_INTM	**LDO2 Interrupt Mask Bit** 0 = Interrupt is unmasked. 1 = Interrupt is masked.	0b1
0	L01_INTM	**LDO1 Interrupt Mask Bit** 0 = Interrupt is unmasked. 1 = Interrupt is masked.	0b1

Applications Information

Inductor Selection

Each step-down converter operates with a 1µH nominal inductance. It is recommended to use an inductor with a DCR less than 50mΩ to reduce I^2R losses.

Output Capacitor Selection

The IC is designed to operate with at least a 22µF ceramic capacitor (X5R rated) connected to each step-down converter output. Note that a significant share of each output's capacitance can be placed as bypassing at the load.

A 1µF (X5R rated ceramic capacitor is required for each LDO output. The capacitor can be remotely placed away from the IC and the appropriate compensation can be selected through an I^2C command. See Table 20.

Input Capacitor Selection

Since ripple cancelation is used, the worst case condition is if one supply is operating at near its 2A maximum while the other supply is providing very little current. Since the IC can normally be connected to a node with significant capacitance, only 4.7µF need be applied locally. A 10µF ceramic capacitor with X5R rating is recommended.

PCB Layout

Nearly all noise generated by the IC is found across IN1, IN2, and PGND_ pins. The bypass capacitors for these pins should be placed closest to the IC. PGND_ and AGND should be connected only after the PGND_ pins connect to its corresponding step-down converter's input capacitor. Both step-down converters have remote sensing which accommodates a distance that incurs up to a 200mV correction in the output voltage. Refer to the MAX8967 EV kit for more details.

Ordering Information

PART	PIN-PACKAGE	TEMP RANGE	BUCK OUT1 (V)	BUCK OUT2 (V)
MAX8967EWV+T	30 WLP	-40°C to +85°C	1.20	1.20
MAX8967AEWV+T	30 WLP	-40°C to +85°C	1.20	1.80
MAX8967BEWV+T	30 WLP	-40°C to +85°C	1.20	2.80
MAX8967CEWV+T	30 WLP	-40°C to +85°C	1.20	3.20

+Denotes a lead (Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
30 WLP	W302B2+2	**21-0548**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/12	Initial release	—