19-5800; Rev 0; 3/11

EVALUATION KIT AVAILABLE

MAX9266

HDCP Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

General Description

The MAX9266 gigabit multimedia serial link (GMSL) deserializer features an LVDS system interface and high-bandwidth digital content protection (HDCP) decryption for content protection of DVD and Blu-ray™ video and audio data. The deserializer pairs with any HDCP-GMSL serializer to form a digital serial link for the transmission of control data and HDCP-encrypted video and audio data. GMSL is an interface approved by Digital Content Protection, LLC (DCP).

The deserializer features 3-channel and 4-channel modes. The 3-channel mode outputs three lanes of LVDS data (21 bits), UART control signals, and three audio outputs. The 4-channel mode outputs four lanes of LVDS data (28 bits), UART control signals, three audio outputs, and auxiliary control signals. The three audio outputs are for I²S audio, supporting an 8kHz to 192kHz sampling frequency and a sample depth of 4 to 32 bits. The embedded control channel forms a full-duplex differential 9.6kbps to 1Mbps UART link between the serializer and the deserializer. An electronic control unit (ECU) or microcontroller (µC) can be located on the serializer side of the link (typical for video display), on the deserializer side of the link (typical for image sensing), or on both sides. The control channel enables ECU/µC control of peripherals on the remote side, providing such functions as backlight control, touch-screen input, and HDCP-related operations.

The serial link signaling is AC-coupled current-mode logic (CML) with scrambled 8b/10b coding. For driving longer cables, GMSL serializers have programmable pre/deemphasis, and the deserializer has a programmable channel equalizer. For reduced EMI, the deserializer has programmable spread spectrum on the LVDS and control outputs. The serial link inputs and the LVDS output meet ISO 10605 and IEC 61000-4-2 ESD standards. The deserializer's core supply is 3.3V and the I/O supply is 1.8V to 3.3V. The device is available in a 48-pin TQFP package with an exposed pad and is specified over the -40°C to +105°C automotive temperature range.

Features

- **HDCP Encryption Enable/Disable Programmable Through Control Channel**
- **Control Channel Handles All HDCP Protocol Transactions—Separate Control Bus Not Required**
- **HDCP Keys Preprogrammed in Secure On-Chip Nonvolatile Memory**
- **2.5Gbps Payload Data Rate (3.125Gbps with Overhead)**
- **AC-Coupled Serial Link with Scrambled 8b/10b Line Coding**
- **8.33MHz to 104MHz (3-Channel LVDS) or 6.25MHz to 78MHz (4-Channel LVDS) Pixel Clock**
- **4-Bit to 32-Bit Word Length, 8kHz to 192kHz I²S Audio Channel Supports High-Definition Audio**
- **Embedded Half-/Full-Duplex Bidirectional Control Channel**
- **9.6kbps to 1Mbps Base Mode and Bypass Mode**
- **Interrupt Supports Touch-Screen Displays**
- **Remote-End I²C Master for Peripherals**
- **Programmable Channel Equalizer for 15m Cable Drive at 3.125Gbps**
- **Programmable Spread Spectrum on Serial Outputs Reduces EMI**
- **Serial-Data Clock Recovery Eliminates External Reference Clock**
- **Auto Data-Rate Detection Allows On-The-Fly Data-Rate Change**
- **Built-In PRBS Checker for BER Testing of the Serial Link**
- **ISO 10605 and IEC 61000-4-2 ESD Tolerance**

Applications

High-Resolution Automotive Navigation

Rear-Seat Infotainment

Blu-ray is a trademark of Blu-ray Disc Association.

Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to: ***www.maxim-ic.com/MAX9266.related***

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.5V to +3.9V
DVDD to GND .....-0.5V to +3.9V
IOVDD to GND .....-0.5V to +3.9V
Any Ground to Any Ground .....-0.5V to +0.5V
IN+, IN- to AGND .....-0.5V to +1.9V
TXOUT_, TXCLKOUT_ to AGND .....-0.5V to +3.9V
All Other Pins to GND ..... -0.5V to (V_{IOVDD} + 0.5V)
TXOUT_, TXCLKOUT_ Short Circuit
to AGND or AVDD.....Continuous

Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP (derate 36.2mW/°C above +70°C) 2898.6mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

Junction-to-Case Thermal Resistance (θ_{JC}) .....2°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}).....27.6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS*

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{OVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (BWS, INT, CDS, EQS, MS, $\overline{PWDN}$, SSEN, DRS)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
SINGLE-ENDED OUTPUTS (WS, SCK, SD/CNTL0, CNTL1, CNTL2/MCLK)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA	DCS = 0	V_{IOVDD} - 0.3			V
			DCS = 1	V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA	DCS = 0			0.3	V
			DCS = 1			0.2	
Output Short-Circuit Current	I_{OS}	V_{OUT} = V_{GND}, DCS = 0	V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
			V_{IOVDD} = 1.7V to 1.9V	3	7	13	
		V_{OUT} = V_{GND}, DCS = 1	V_{IOVDD} = 3.0V to 3.6V	20	35	63	
			V_{IOVDD} = 1.7V to 1.9V	5	10	21	

*The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

DC ELECTRICAL CHARACTERISTICS* (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{OVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²C AND UART I/O, OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL, LOCK, $\overline{ERR}$, GPIO_)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0V to V_{IOVDD} (Note 2)	RX/SDA, TX/SCL	-110		+1	µA
			LOCK, $\overline{ERR}$, GPIO_	-80		+1	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
DIFFERENTIAL OUTPUT FOR REVERSE CONTROL CHANNEL (IN+, IN-)							
Differential High Output Peak Voltage, (V_{IN+}) - (V_{IN-})	V_{ROH}	No high-speed data transmission (Figure 1)		30		60	mV
Differential Low Output Peak Voltage, (V_{IN+}) - (V_{IN-})	V_{ROL}	No high-speed data transmission (Figure 1)		-60		-30	mV
DIFFERENTIAL INPUTS (IN+, IN-)							
Differential High Input Threshold (Peak) Voltage, (V_{IN+}) - (V_{IN-})	$V_{IDH(P)}$	Figure 2			40	90	mV
Differential Low Input Threshold (Peak) Voltage, (V_{IN+}) - (V_{IN-})	$V_{IDL(P)}$	Figure 2		-90	-40		mV
Input Common-Mode Voltage ((V_{IN+}) + (V_{IN-}))/2	V_{CMR}			1	1.3	1.6	V
Differential Input Resistance (Internal)	R_I			80	100	130	Ω
THREE-LEVEL LOGIC INPUTS (ADD0, ADD1)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Midlevel Input Current	I_{INM}	ADD0 and ADD1 open or connected to a driver with output in high impedance (Note 3)		-10		+10	µA
Input Current	I_{IN}	ADD0 and ADD1 = high or low, $\overline{PWDN}$ = high or low		-150		+150	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
LVDS OUTPUTS (TXOUT__, TXCLKOUT_)							
Differential Output Voltage	V_{OD}	Figure 3		250		450	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 3				25	mV

*The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

DC ELECTRICAL CHARACTERISTICS* (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{OVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Offset Voltage	V_{OS}	Figure 3		1.125		1.375	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 3				25	mV
Output Short-Circuit Current	I_{OS}	V_{OUT} = 0V or 3.6V	3.5mA LVDS output	-7.5		+7.5	mA
			7mA LVDS output	-15		+15	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	3.5mA LVDS output				7.5	mA
		7mA LVDS output				15	
Output High-Impedance Current	I_{OZ}	ADD0 and ADD1 = high or low, $\overline{PWDN}$ = high or low		-0.5		+0.5	µA
POWER SUPPLY							
Worst-Case Supply Current (Figure 4) (Note 4)	I_{WCS}	BWS = low, $f_{TXCLKOUT\_}$ = 16.6MHz			149	190	mA
		BWS = low, $f_{TXCLKOUT\_}$ = 33.3MHz			159	212	
		BWS = low, $f_{TXCLKOUT\_}$ = 66.6MHz			190	255	
		BWS = low, $f_{TXCLKOUT\_}$ = 104MHz			228	295	
Sleep-Mode Supply Current	I_{CCS}				80	248	µA
Power-Down Current	I_{CCZ}	$\overline{PWDN}$ = GND			25	178	µA
ESD PROTECTION							
IN+, IN-	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 5)		±8			kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF (Note 6)	Contact Discharge	±10			
			Air-Gap Discharge	±12			
		ISO 10605, R_D = 2kΩ, C_S = 330pF (Note 6)	Contact Discharge	±8			
			Air-Gap Discharge	±15			
TX0UT_, TXCLKOUT_	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 5)		±8			kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF (Note 6)	Contact Discharge	±8			
			Air-Gap Discharge	±20			
		ISO 10605, R_D = 2kΩ, C_S = 330pF (Note 6)	Contact Discharge	±8			
			Air-Gap Discharge	±30			
All Other Pins	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 5)		±4			kV

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AC ELECTRICAL CHARACTERISTICS*

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{OVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS CLOCK OUTPUTS (TXCLKOUT+, TXCLKOUT-)							
Clock Frequency	$f_{TXCLKOUT\_}$	BWS = GND, V_{DRS} = V_{IOVDD}		8.33		16.66	MHz
		BWS = GND, DRS = GND		16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}		6.25		12.5	
		V_{BWS} = V_{IOVDD}, DRS = GND		12.5		78	
I²C/UART PORT TIMING							
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD (Figure 5)		20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD (Figure 5)		20		150	ns
Input Setup Time	t_{SET}	I²C only (Figure 5) (Note 7)		100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 5) (Note 7)		0			ns
SWITCHING CHARACTERISTICS (Note 7)							
CNTL_ Output Rise-and-Fall Time	t_R, t_F	20% to 80%, C_L = 10pF, DCS = 1 (Figure 6)	V_{IOVDD} = 1.7V to 1.9V	0.5		3.1	ns
			V_{IOVDD} = 3.0V to 3.6V	0.3		2.2	
		20% to 80%, C_L = 5pF, DCS = 0 (Figure 6)	V_{IOVDD} = 1.7V to 1.9V	0.6		3.8	
			V_{IOVDD} = 3.0V to 3.6V	0.4		2.4	
LVDS Output Rise Time	t_R	20% to 80%, R_L = 100Ω (Figure 3)			200	350	ps
LVDS Output Fall Time	t_F	80% to 20%, R_L = 100Ω (Figure 3)			200	350	ps
LVDS Output Pulse Position	t_{PPOSN}	N = 0 to 6, t_{CLK} = 1/$f_{TXCLKOUT\_}$, $f_{TXCLKOUT\_}$ = 104MHz (Figure 7)	$f_{TXCLKOUT\_}$ = 12.5MHz	N/7 x t_{CLK} - 250	N/7 x t_{CLK}	N/7 x t_{CLK} + 250	ps
			$f_{TXCLKOUT\_}$ = 33MHz	N/7 x t_{CLK} - 200	N/7 x t_{CLK}	N/7 x t_{CLK} + 200	
			$f_{TXCLKOUT\_}$ = 78MHz	N/7 x t_{CLK} - 125	N/7 x t_{CLK}	N/7 x t_{CLK} + 125	
			$f_{TXCLKOUT\_}$ = 104MHz	N/7 x t_{CLK} - 100	N/7 x t_{CLK}	N/7 x t_{CLK} + 100	
LVDS Output Enable Time	t_{LVEN}	From the last bit of the enable UART packet to V_{OS} = 1125mV				100	µs
LVDS Output Disable Time	t_{LVDS}	From the last bit of the enable UART packet to V_{OS} = 0V				100	µs
Deserializer Delay	t_{SD}	Figure 8 (Note 8)				3660	Bits
Reverse Control-Channel Output Rise Time	t_R	No forward-channel data transmission (Figure 1)		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward-channel data transmission (Figure 1)		180		400	ns
Lock Time	t_{LOCK}	Figure 9				3.6	ms
Power-Up Time	t_{PU}	Figure 10				9.4	ms

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AC ELECTRICAL CHARACTERISTICS* (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{OVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²S OUTPUT TIMING (Note 7)							
WS Jitter	t_{AJ-WS}	t_{WS} = 1/f_{WS}, rising (falling) edge to falling (rising) edge (Note 5)	f_{WS} = 48kHz or 44.1kHz		$0.4e^{-3}$ x t_{WS}	$0.5e^{-3}$ x t_{WS}	ns
			f_{WS} = 96kHz		$0.8e^{-3}$ x t_{WS}	$1e^{-3}$ x t_{WS}	
			f_{WS} = 192kHz		$1.6e^{-3}$ x t_{WS}	$2e^{-3}$ x t_{WS}	
SCK Jitter	t_{AJ-SCK}	t_{SCK} = 1/f_{SCK}, rising edge to rising edge	n_{WS} = 16 bits, f_{WS} = 48kHz or 44.1kHz		$13e^{-3}$ x t_{SCK}	$16e^{-3}$ x t_{SCK}	ns
			n_{WS} = 24 bits, f_{WS} = 96kHz		$39e^{-3}$ x t_{SCK}	$48e^{-3}$ x t_{SCK}	
			n_{WS} = 32 bits, f_{WS} = 192kHz		0.1 x t_{SCK}	0.13 x t_{SCK}	
Audio Skew Relative to Video	t_{ASK}	Video and audio synchronized			3 x t_{WS}	4 x t_{WS}	µs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%	C_L = 10pF, DCS = 1	0.3		3.1	ns
			C_L = 5pF, DCS = 0	0.4		3.8	
SD, WS Valid Time Before SCK	t_{DVB}	t_{SCK} = 1/f_{SCK} (Figure 11)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK	t_{DVA}	t_{SCK} = 1/f_{SCK} (Figure 11)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns

Note 2: Minimum I_{IN} due to voltage drop across the internal pullup resistor.

Note 3: To provide a midlevel, leave the input unconnected, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.

Note 4: HDCP enabled.

Note 5: Tested terminal to all grounds.

Note 6: Tested terminal to AGND.

Note 7: Guaranteed by design and not production tested.

Note 8: Measured in CML bit times. Bit time = 1/(30 x $f_{TXCLKOUT\_}$) for BWS = GND. Bit time = 1/(40 x $f_{TXCLKOUT\_}$) for V_{BWS} = V_{IOVDD}.

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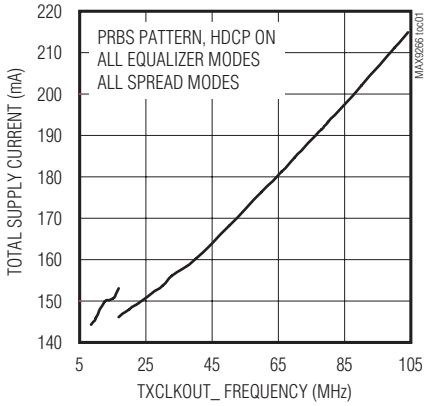
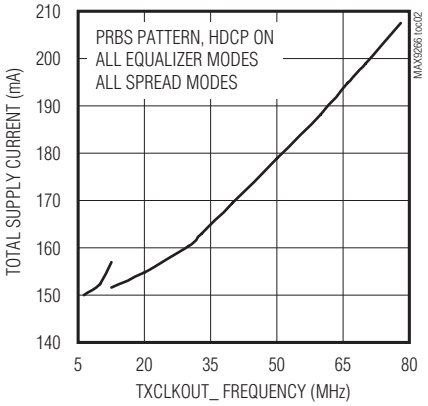
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C, unless otherwise noted.)

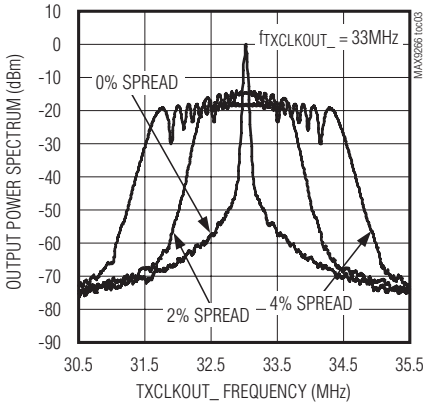
TOTAL SUPPLY CURRENT vs. TXCLKOUT_ FREQUENCY (3-CHANNEL MODE)



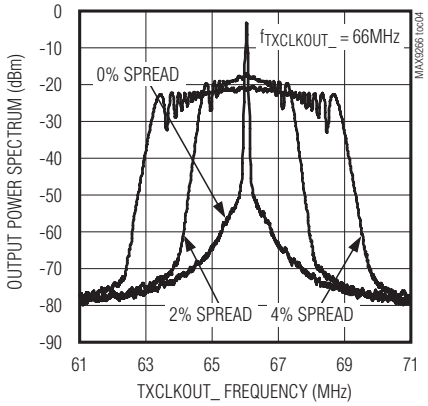
TOTAL SUPPLY CURRENT vs. TXCLKOUT_ FREQUENCY (4-CHANNEL MODE)



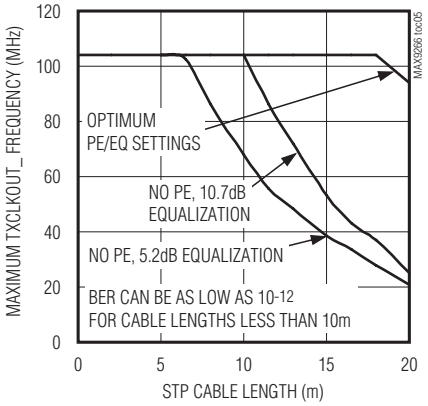
OUTPUT POWER SPECTRUM vs. TXCLKOUT_ FREQUENCY (VARIOUS SPREAD)



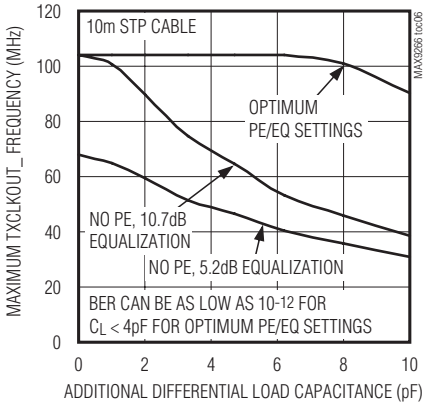
OUTPUT POWER SPECTRUM vs. TXCLKOUT_ FREQUENCY (VARIOUS SPREAD)



MAXIMUM TXCLKOUT_ FREQUENCY vs. STP CABLE LENGTH (BER < 10^{-9})

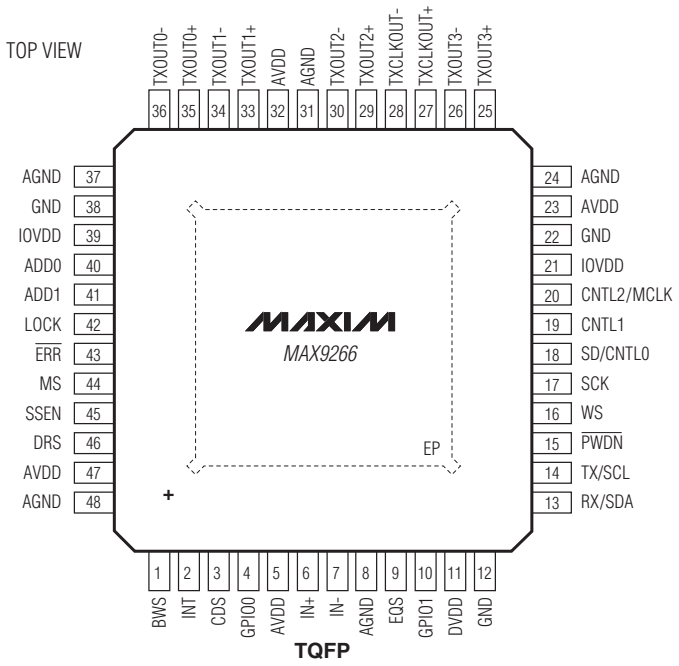


MAXIMUM TXCLKOUT_ FREQUENCY vs. ADDITIONAL DIFFERENTIAL C_L (BER < 10^{-9})



HDCP Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	BWS	Bus-Width Select. BWS requires external pulldown or pullup resistor. Set BWS = low for 3-channel mode. Set BWS = high for 4-channel mode.
2	INT	Interrupt Input. INT requires external pullup or pulldown resistor. A transition on the deserializer's INT input toggles the GMSL serializer's INT output.
3	CDS	Control Direction Selection. Control link direction selection input requires external pulldown or pullup resistor. Set CDS = high for UART connection of a µC as control-channel master. Set CDS = low for peripheral connection as a control-channel I²C or UART slave.
4	GPIO0	General-Purpose I/O 0. Open-drain GPIO with internal 60kΩ pullup resistor to IOVDD. GPIO0 is high impedance during power-up and when $\overline{PWDN}$ = low.
5, 23, 32, 47	AVDD	3.3V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
6, 7	IN+, IN-	Differential CML Input +/−. Differential inputs of the serial link.
8, 24, 31, 37, 48	AGND	Analog Ground

Pin Description (continued)

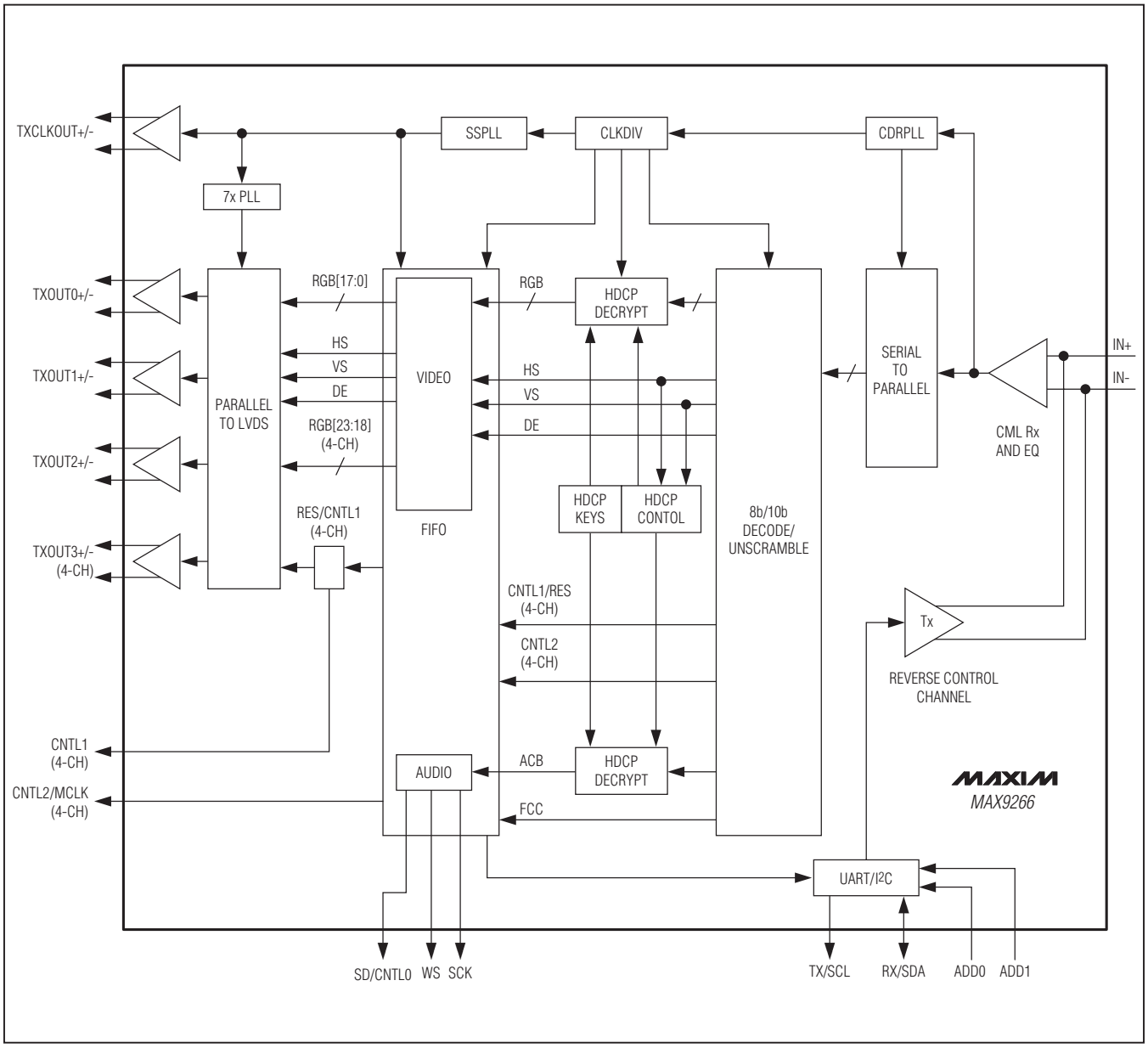
PIN	NAME	FUNCTION
9	EQS	Equalizer Select Input. EQS requires external pulldown or pullup resistor. The state of EQS latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set EQS = low for 10.7dB equalizer boost (EQTUNE = 1001). Set EQS = high for 5.2dB equalizer boost (EQTUNE = 0100).
10	GPIO1	General-Purpose I/O 1. Open-drain GPIO with an internal 60kΩ pullup resistor to IOVDD. GPIO1 is high impedance during power-up and when $\overline{PWDN}$ = low.
11	DVDD	3.3V Digital Power Supply. Bypass DVDD to DGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to DVDD.
12, 22, 38	GND	Digital and I/O Ground
13	RX/SDA	Receive/Serial Data. UART receive or I²C serial-data input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the deserializer's UART. In I²C mode, RX/SDA is the SDA input/output of the deserializer's I²C master. RX/SDA has an open-drain driver and requires a pullup resistor.
14	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the deserializer's UART. In I²C mode, TX/SCL is the SCL output of the deserializer's I²C master. TX/SCL is an open-drain driver and requires a pullup resistor.
15	$\overline{PWDN}$	Active-Low, Power-Down Input. $\overline{PWDN}$ requires external pulldown or pullup resistor.
16	WS	I²S Word-Select Output
17	SCK	I²S Serial-Clock Output
18	SD/CNTL0	I²S Serial-Data Output/Control Output 0. Disable I²S to use SD/CNTL0 as an additional control output. SD/CNTL0 is encrypted when HDCP is enabled.
19	CNTL1	Control Output 1. CNTL1 is active in 3-channel mode and remains low. To use CNTL1, set BWS = high (4-channel mode) and set DISCNTL = 0. CNTL1 is mapped from DOUT27. CNTL1 is not encrypted when HDCP is enabled (see Table 3).
20	CNTL2/MCLK	Control Output 2/Data Output 28/MCLK. CNTL2/MCLK is not active in 3-channel mode and remains low. To use CNTL2/MCLK, set BWS = high (4-channel mode). CNTL2/MCLK is not encrypted when HDCP is enabled (see Table 3). CNTL2/MCLK can be used to output MCLK (see the *Additional MCLK Output for Audio Applications* section).
21, 39	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to IOVDD.
25, 26, 29, 30, 33–36	TXOUT_+, TXOUT_-	Differential LVDS Data Outputs. Set BWS = low (3-channel mode) to use TXOUT0_ to TXOUT2_. Set BWS = high (4-channel mode) to use TXOUT0_ to TXOUT3_.
27, 28	TXCLKOUT+, TXCLKOUT-	Differential LVDS Output for the LVDS Clock
40	ADD0	Address Selection Input 0. Three-level input to select the deserializer's device address (see Table 2). The state of ADD0 latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low).

Pin Description (continued)

PIN	NAME	FUNCTION
41	ADD1	Address Selection Input 1. Three-level input to select the deserializer's device address (see Table 2). The state of ADD1 latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low).
42	LOCK	Open-Drain Lock Output with Internal 60kΩ Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK remains low when the configuration link is active. LOCK is high impedance when $\overline{PWDN}$ = low. LOCK is an open-drain driver and requires a pullup resistor.
43	$\overline{ERR}$	Active-Low, Open-Drain Video Data Error Output with Internal 60kΩ Pullup to IOVDD. $\overline{ERR}$ goes low when the number of decoding errors during normal operation exceeds a programmed error threshold, or when at least one PRBS error is detected during a PRBS test. $\overline{ERR}$ is high impedance when $\overline{PWDN}$ = low. $\overline{ERR}$ is an open-drain driver and requires a pullup resistor.
44	MS	Mode Select. Control-channel mode-selection input requires external pulldown or pullup resistor. MS sets the control-link mode when CDS = high (see the *Control Channel and Register Programming* section). MS sets autostart mode when CDS = low (see Table 9).
45	SSEN	Spread-Spectrum Enable Input. Serial link spread-spectrum enable input requires external pulldown or pullup resistor. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set SSEN = high for ±2% spread spectrum on the LVDS and control outputs. Set SSEN = low to use the LVDS and control outputs without spread spectrum.
46	DRS	Data-Rate Select. Data-rate range-selection input requires external pulldown or pullup resistor. The state of DRS latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set DRS = high for TXCLKOUT_ frequencies of 8.33MHz to 16.66MHz (3-channel mode) or 6.25MHz to 12.5MHz (4-channel mode). Set DRS = low for TXCLKOUT_ frequencies of 16.66MHz to 104MHz (3-channel mode) or 12.5MHz to 78MHz (4-channel mode).
—	EP	Exposed Pad. EP is internally connected to AGND. **MUST** externally connect EP to the AGND plane for proper thermal and electrical performance.

HDCP Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

Functional Diagram



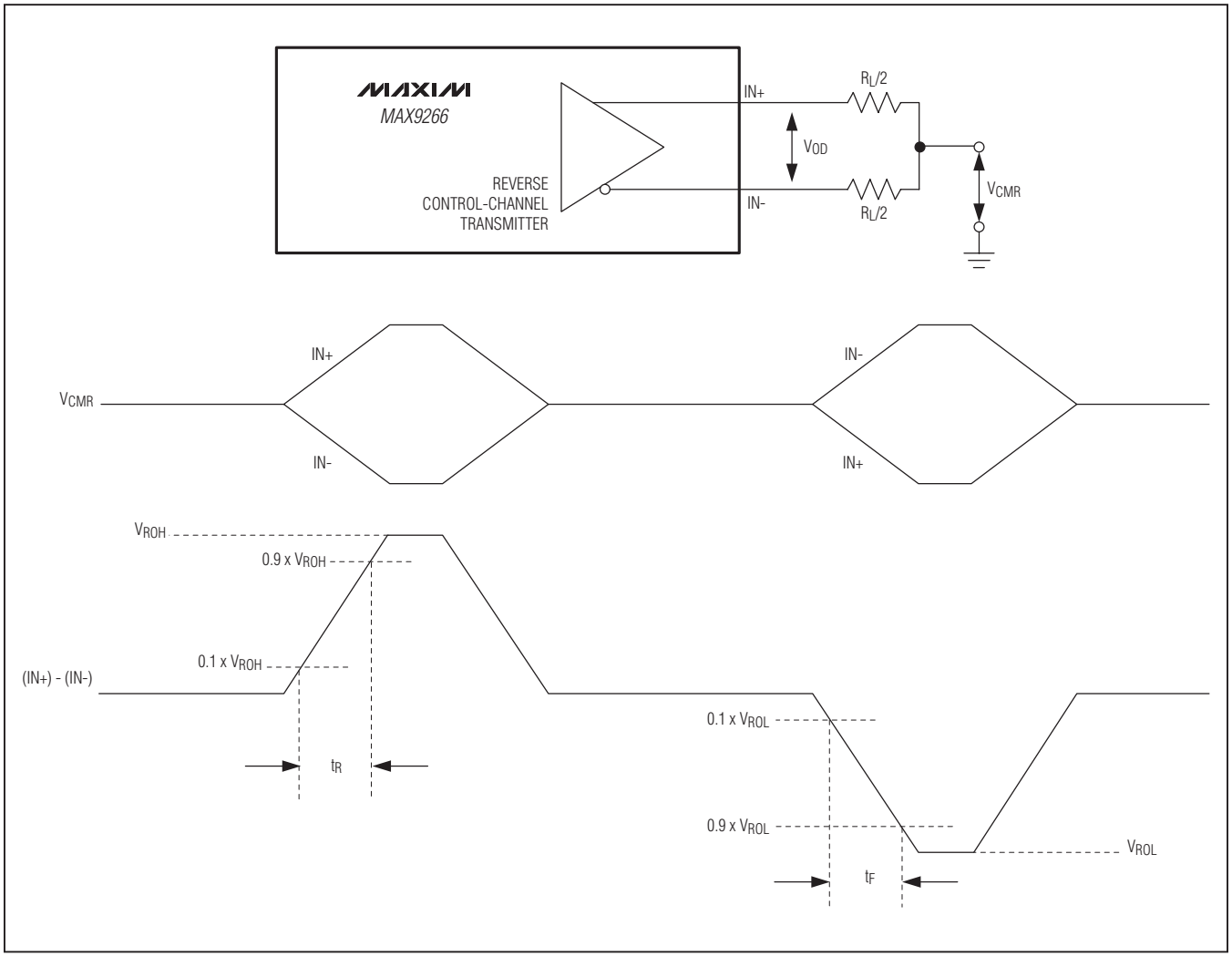


Figure 1. Reverse Control-Channel Output Parameters

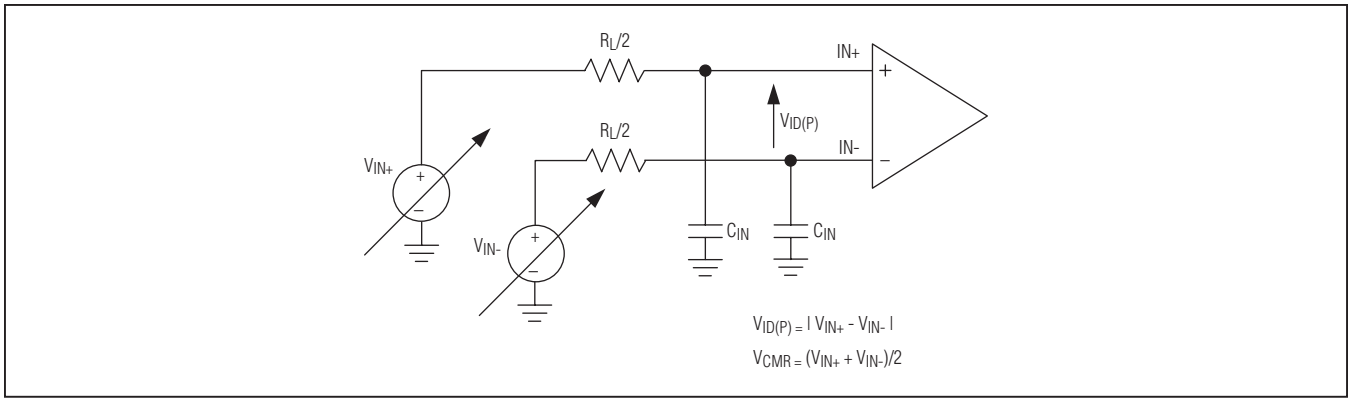


Figure 2. Test Circuit for Differential Input Measurement

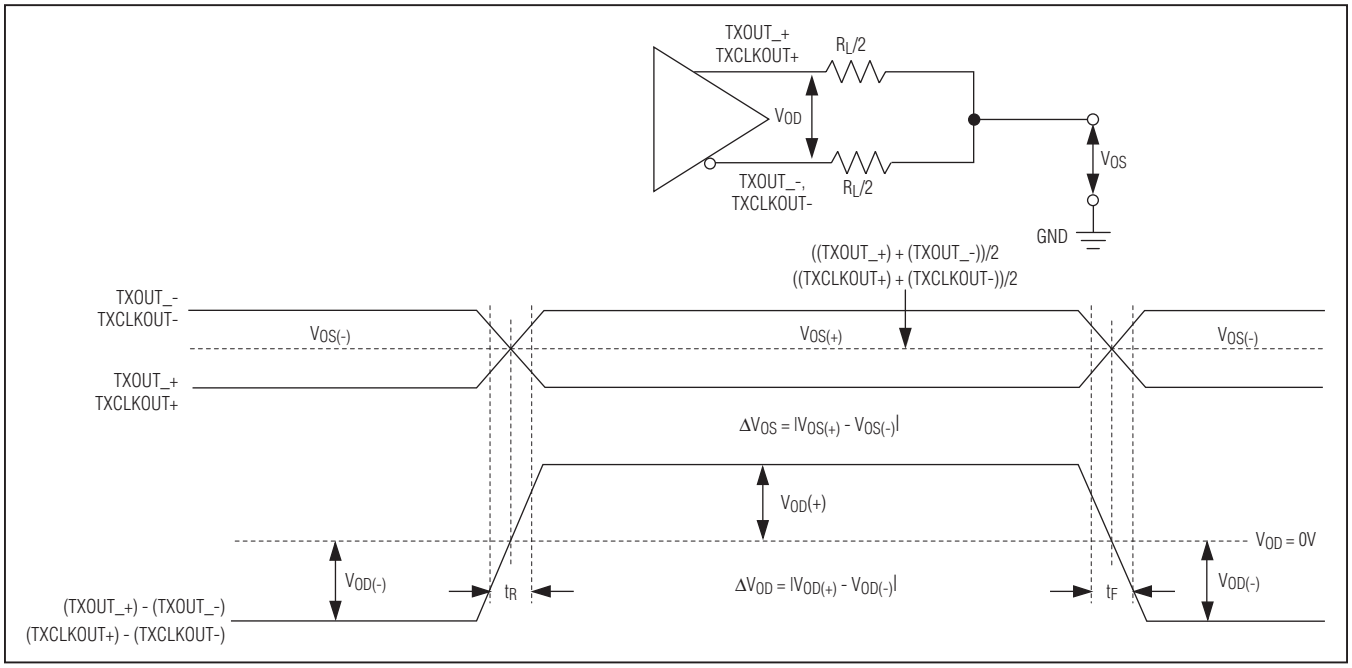


Figure 3. LVDS Output Parameters

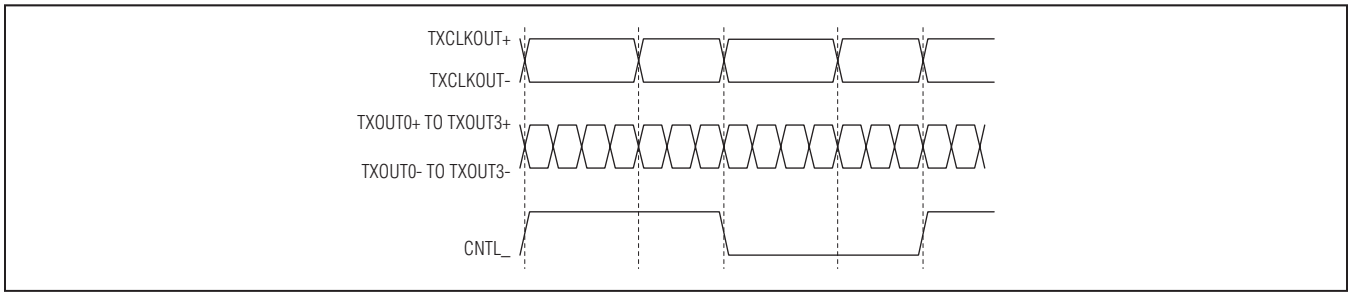


Figure 4. Worst-Case Pattern Output

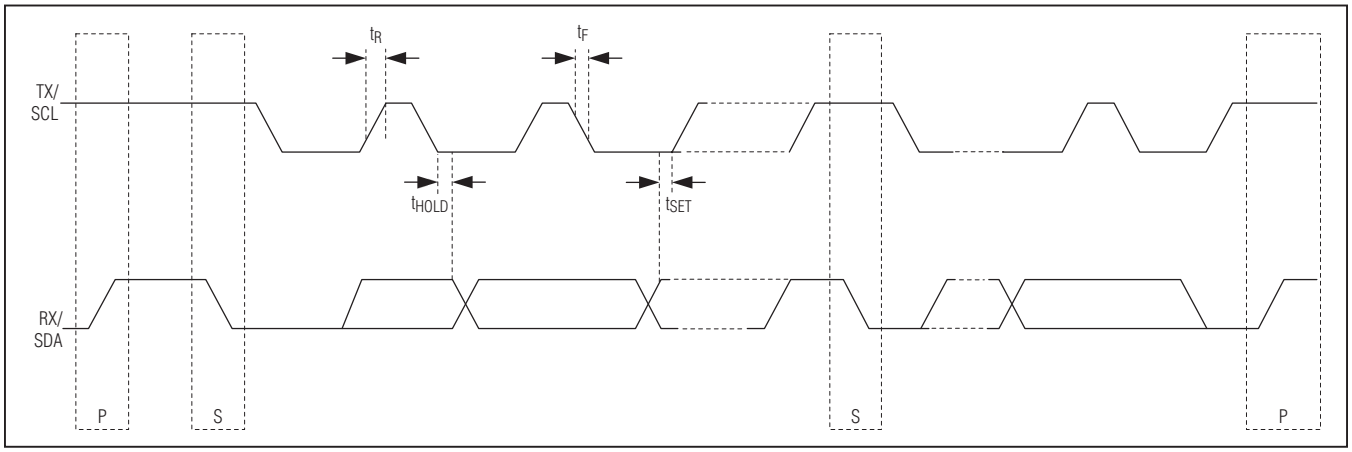


Figure 5. I²C Timing Parameters

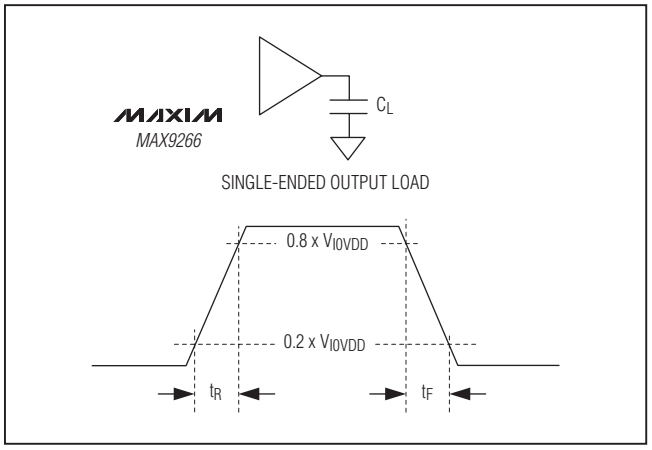


Figure 6. Single-Ended Output High and Low Times

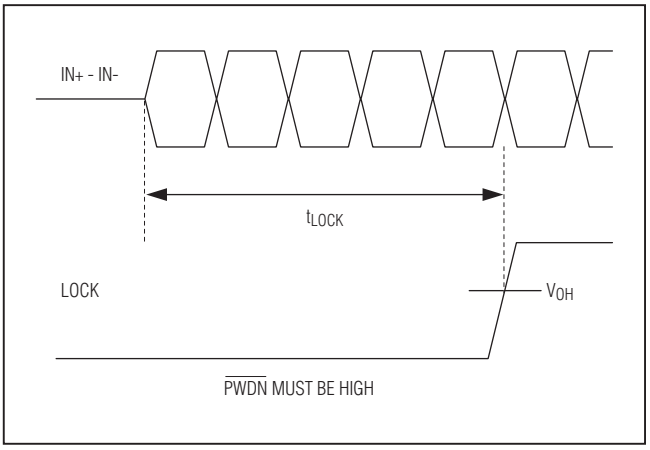


Figure 9. Lock Time

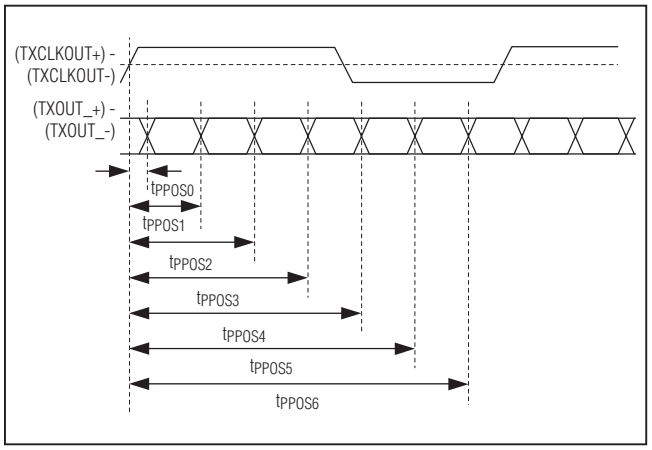


Figure 7. LVDS Output Pulse Position Measurement

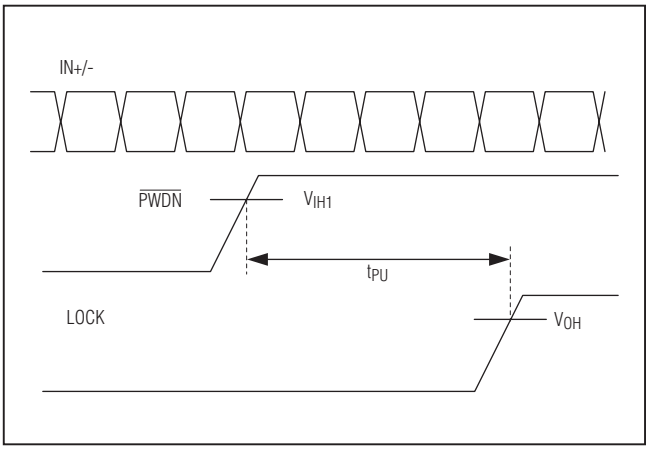


Figure 10. Power-Up Delay

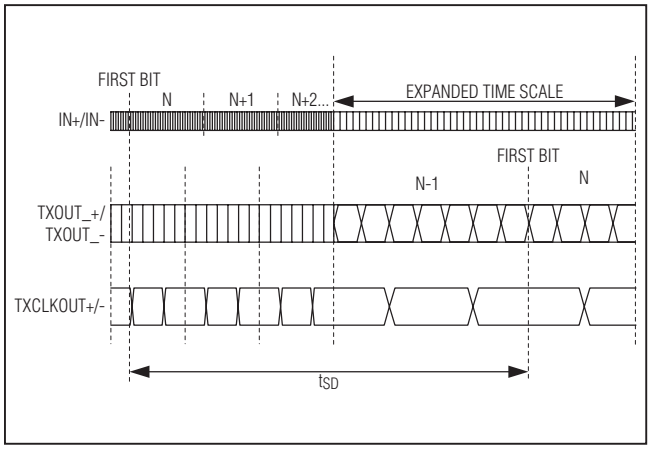


Figure 8. Deserializer Delay

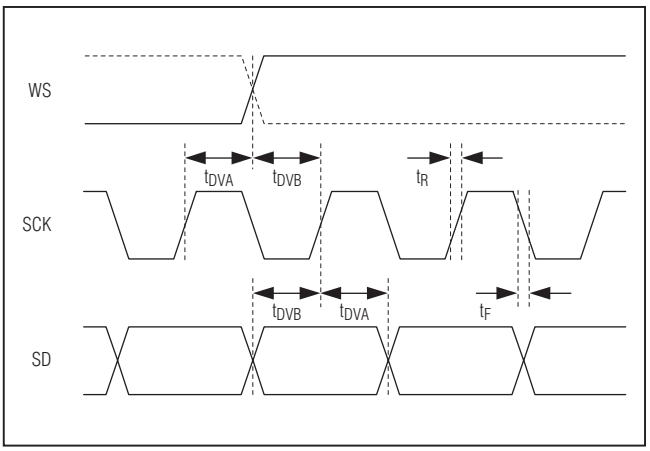


Figure 11. Output I²S Timing Parameters

Detailed Description

The MAX9266 GMSL deserializer with LVDS interface utilizes Maxim's gigabit multimedia serial link (GMSL) technology and high-bandwidth digital content protection (HDCP). When HDCP is enabled, the deserializer decrypts video and audio data on the serial link. The deserializer is backward compatible with the MAX9268 LVDS output deserializer.

The deserializer has a maximum serial payload data rate of 2.5Gbps for 15m or more of shielded twisted-pair (STP) cable. The deserializer operates up to a maximum input clock of 104MHz for 3-channel mode, or 78MHz for 4-channel mode, respectively. This serial link supports a wide range of display panels from QVGA (320 x 240) to WXGA (1280 x 800) and higher with 24-bit color.

The 3-channel mode handles three lanes of LVDS data (21 bits), UART control signals, and three audio signals. The 4-channel mode handles four lanes of LVDS data (28 bits), UART control signals, three audio signals, and auxiliary control outputs. The audio outputs form a standard I²S interface, supporting 8kHz to 192kHz sample rates and audio word lengths of 4 to 32 bits. The embedded control channel forms a full-duplex, differential 9.6kbps to 1Mbps UART link between the serializer and the deserializer for HDCP-related control operations. In addition, the control channel enables electronic control unit (ECU) or microcontroller (µC) control of peripherals on the remote side, such as backlight control, grayscale gamma correction, camera module, and touch screen. An ECU/µC can be located on the serializer side of the link (typical for video display), on the deserializer side of the link (typical for image sensing), or on both sides. Base-mode communication with peripherals uses either I²C or the GMSL UART format. A bypass mode enables full-duplex communication using a user-defined UART format.

The GMSL serializer pre/deemphasis, along with the deserializer channel equalizer, extends the link length and enhances the link reliability. Spread spectrum is available to reduce EMI on the LVDS and control outputs. The serial inputs comply with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

The µC configures various operating conditions of the GMSL serializer and the deserializer through internal registers. Table 1 lists the default register values. The device addresses are stored in registers 0x00 and 0x01 of both the GMSL serializer and the deserializer. Write to registers 0x00 and 0x01 in both devices to change the device address of the GMSL serializer or the deserializer.

Table 1. Power-Up Default Register Map (see Tables 16 and 17)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x40, 0x44, 0x48, 0x80, 0x84, 0x88, 0xC0, 0xC4, 0xC8	SERID = XX00XX0, serializer device address is determined by ADD1 and ADD0 (Table 2) RESERVED = 0
0x01	0x50, 0x54, 0x58, 0x90, 0x94, 0x98, 0xD0, 0xD4, 0xD8	DESID = XX01XX0, deserializer device address is determined by ADD1 and ADD0 (Table 2) CFGBLOCK = 0, registers 0x00 to 0x1F are read/write
0x02	0x1F or 0x5F	SS = 00 (SSEN = low), SS = 01 (SSEN = high), spread-spectrum settings depend on SSEN pin state at power-up RESERVED = 0 AUDIOEN = 1, I²S channel enabled PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect the serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking RESERVED = 0 SDIV = 00000, autocalibrate sawtooth divider

Table 1. Power-Up Default Register Map (see Tables 16 and 17) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x04	0x03, 0x13, 0x43, 0x53	LOCKED = 0, LOCK output is low (read only) OUTENB = 0 ($\overline{\text{ENABLE}}$ = low), OUTENB = 1 ($\overline{\text{ENABLE}}$ = high), OUTENB default depends on ENABLE pin state at power-up PRBSEN = 0, PRBS test disabled SLEEP = 0 or 1, SLEEP setting default depends on CDS and MS pin state at power-up (see the *Link Startup Procedure* section) INTTYPE = 00, base mode uses I^2C REVCCEN = 1, reverse control channel active (sending) FWDCCEN = 1, forward control channel active (receiving)
0x05	0x24 or 0x29	I2CMETHOD = 0, I^2C master sends the register address HPFTUNE = 01, 3.75MHz equalizer highpass cutoff frequency PDHF = 0, high-frequency boosting disabled EQTUNE = 0100 (EQS = high, 5.2dB), EQTUNE = 1001 (EQS = low, 10.7dB), EQTUNE default setting depends on EQS pin state at power-up
0x06	0x0F	RESERVED = 0, outputs are staggered AUTORST = 0, error registers/output autoreset disabled DISINT = 0, INT transmission enabled INT = 0, INT output is low (read only) GPIO1OUT = 1, GPIO1 output set to high GPIO1 = 1, GPIO1 input = high (read only) GPIO0OUT = 1, GPIO0 output set to high GPIO0 = 1, GPIO0 input = high (read only)
0x07	0x54	RESERVED = 01010100
0x08	0x30	RESERVED = 001100 DISVSFILT = 0, VSYNC glitch filter active DISHSFILT = 0, HSYNC glitch filter active
0x09	0xC8	RESERVED = 11001000
0x0A	0x12	RESERVED = 00010010
0x0B	0x20	RESERVED = 00100000
0x0C	0x00	ERRTHR = 00000000, error threshold set to zero for decoding errors
0x0D	0x00 (read only)	DECERR = 00000000, zero decoding errors detected
0x0E	0x00 (read only)	PRBSERR = 00000000, zero PRBS errors detected
0x12	0x00	MCLKSRC = 0, MCLK is derived from TXCLKOUT_ (see Table 5) MCLKDIV = 0000000, MCLK output is disabled
0x13	0x10	RESERVED = 00010000

Table 1. Power-Up Default Register Map (see Tables 16 and 17) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x14	0x09	INVVSYNC = 0, deserializer does not invert VSYNC INVHSYNC = 0, deserializer does not invert HSYNC FORCELVDS = 0, normal LVDS operation DCS = 0, normal CMOS driver current DISCNTL = 1, CNTL1 forced low DISRES = 0, serial-data bit 27 is mapped to RES ILVDS = 01, 3.5mA LVDS current
0x1E	0x08 (read only)	ID = 00001000, device ID is 0x08
0x1F	0x1X (read only)	RESERVED = 000 CAPS = 1, HDCP capable REVISION = XXXX
0x80 to 0x84	0xXXXXXXXXXX (read only)	BKSV = 0xXXXXXXXXXX, HDCP receiver KSV is 0xXXXXXXXXXX
0x85, 0x86	0xXXXX (read only)	RI' = 0xXXXX, RI' of the transmitter is 0xXXXX
0x87	0xXX (read only)	PJ' = 0xXXXX, PJ' of the transmitter is 0xXX
0x88 to 0x8F	0x00000000 00000000	AN = 0000000000000000, session random number is 0000000000000000
0x90 to 0x94	0x00000000 00000000	AKSV = 0x0000000000, HDCP transmitter KSV is 0x0000000000000000
0x95	0x00	PD_HDCP = 0, HDCP circuits powered up RESERVED = 000 GPIO1_FUNCTION = 0, normal GPIO1 function GPIO0_FUNCTION = 0, normal GPIO0 function AUTH_STARTED = 0, HDCP authentication not started ENCRYPTION_ENABLE = 0, HDCP encryption disabled
0x96	0x00	RESERVED = 000000 NEW_DEV_CONN = 0, no new devices connected KSV_LIST_READY = 0, KSV list is not ready
0x97	0x00	RESERVED = 0000000 REPEATER = 0, HDCP receiver is not a repeater
0x98 to 0x9F	0x00000000 00000000 (read only)	RESERVED = 0x0000000000000000
0xA0 to 0xA3	0xXXXXXXXX (read only)	H0 part of SHA-1 hash value is 0xXXXXXXXX
0xA04 to 0xA7	0xXXXXXXXX (read only)	H1 part of SHA-1 hash value is 0xXXXXXXXX

Table 1. Power-Up Default Register Map (see Tables 16 and 17) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0xA8 to 0xAB	0xXXXXXXXX (read only)	H2 part of SHA-1 hash value is 0xXXXXXXXX
0xAC to 0xAF	0xXXXXXXXX (read only)	H3 part of SHA-1 hash value is 0xXXXXXXXX
0xB0 to 0xB3	0xXXXXXXXX (read only)	H4 part of SHA-1 hash value is 0xXXXXXXXX
0xB4	0x00	Reserved = 0000 MAX_CASCADE_EXCEEDED = 0, seven or fewer cascaded HDCP devices attached DEPTH = 000, device cascade depth is zero
0xB5	0x00	MAX_DEVS_EXCEEDED = 0, 14 or fewer HDCP devices attached DEVICE_COUNT = 0000000, zero attached devices
0xB6	0x00	GPMEM = 00000000, 0x00 stored in general-purpose memory
0xB7 to 0xB9	0x000000 (read only)	Reserved = 0x000000
0xBA to 0xFF	All zero	KSV_LIST = all zero, no KSVs stored

X = Indeterminate.

Table 2. Device Address Defaults (Register 0x00, 0x01)

PIN		DEVICE ADDRESS (bin)								SERIALIZER DEVICE ADDRESS (hex)	DESERIALIZER DEVICE ADDRESS (hex)
ADD1	ADD0	D7	D6	D5	D4	D3	D2	D1	D0		
Low	Low	1	0	0	X*	0	0	0	R/$\overline{W}$	80	90
Low	High	1	0	0	X*	0	1	0	R/$\overline{W}$	84	94
Low	Open	1	0	0	X*	1	0	0	R/$\overline{W}$	88	98
High	Low	1	1	0	X*	0	0	0	R/$\overline{W}$	C0	D0
High	High	1	1	0	X*	0	1	0	R/$\overline{W}$	C4	D4
High	Open	1	1	0	X*	1	0	0	R/$\overline{W}$	C8	D8
Open	Low	0	1	0	X*	0	0	0	R/$\overline{W}$	40	50
Open	High	0	1	0	X*	0	1	0	R/$\overline{W}$	44	54
Open	Open	0	1	0	X*	1	0	0	R/$\overline{W}$	48	58

**X = 0 for the serializer address, X = 1 for the deserializer address.*

HDCP Bitmapping and Bus-Width Selection

The LVDS output has two selectable widths: 3-channel and 4-channel. Serial data is mapped to outputs on the deserializer according to Figure 12 and Figure 13. In 3-channel mode, TXOUT3_ and CNTL1, CNTL2/MCLK are not available. For both modes, the SD/CNTL0, SCK, and WS pins are for I²S audio when audio is enabled. With audio disabled, SD/CNTL0 becomes control signal CNTL0. The deserializer outputs 8.33MHz to 104MHz clock rates for 3-channel mode and 6.25MHz to 78MHz for 4-channel mode

Table 3 lists the HDCP bit mapping for the LVDS interface output. DOUT18 and DOUT19 are reserved for HSYNC and VSYNC, respectively. The deserializer has HDCP decryption on DOUT[17:0] and the I²S output. 4-channel mode has additional HDCP decryption on DOUT[26:21].

DOUT[28:27] and DOUT[20:18] do not have HDCP decryption. SD, when used as an additional data output (AUDIOEN = 0), also does not have HDCP decryption.

Table 3. LVDS, HDCP Mapping and Bus-Width Selection (See Figures 12 and 13)

OUTPUT BITS	3-CHANNEL MODE (BWS = LOW)			4-CHANNEL MODE (BWS = HIGH)		
	TYPICAL BIT-MAPPING	AUXILIARY SIGNALS MAPPING	HDCP DE-CRYPTION CAPABILITY	TYPICAL BIT-MAPPING	AUXILIARY SIGNALS MAPPING	HDCP DE-CRYPTION CAPABILITY
DOUT[0:5]	R[0:5]	—	Yes	R[0:5]	—	Yes
DOUT[6:11]	G[0:5]	—	Yes	G[0:5]	—	Yes
DOUT[12:17]	B[0:5]	—	Yes	B[0:5]	—	Yes
DOUT[18:20]	HS, VS, DE	—	No	HS, VS, DE	—	No
DOUT[21:22]	Not available	—	—	R6, R7	—	Yes
DOUT[23:24]	Not available	—	—	G6, G7	—	Yes
DOUT[25:26]	Not available	—	—	B6, B7	—	Yes
DOUT27	Not available	Not available	—	RES*	CNTL1*	No
DOUT28	—	Not available	—	—	CNTL2	No
SD	—	SD/CNTL0	I²S**	—	SD/CNTL0	I²S**

**See the Reserved Bit (RES)/CNTL1 section for details.*
***HDCP decryption on SD when used as an I²S signal.*

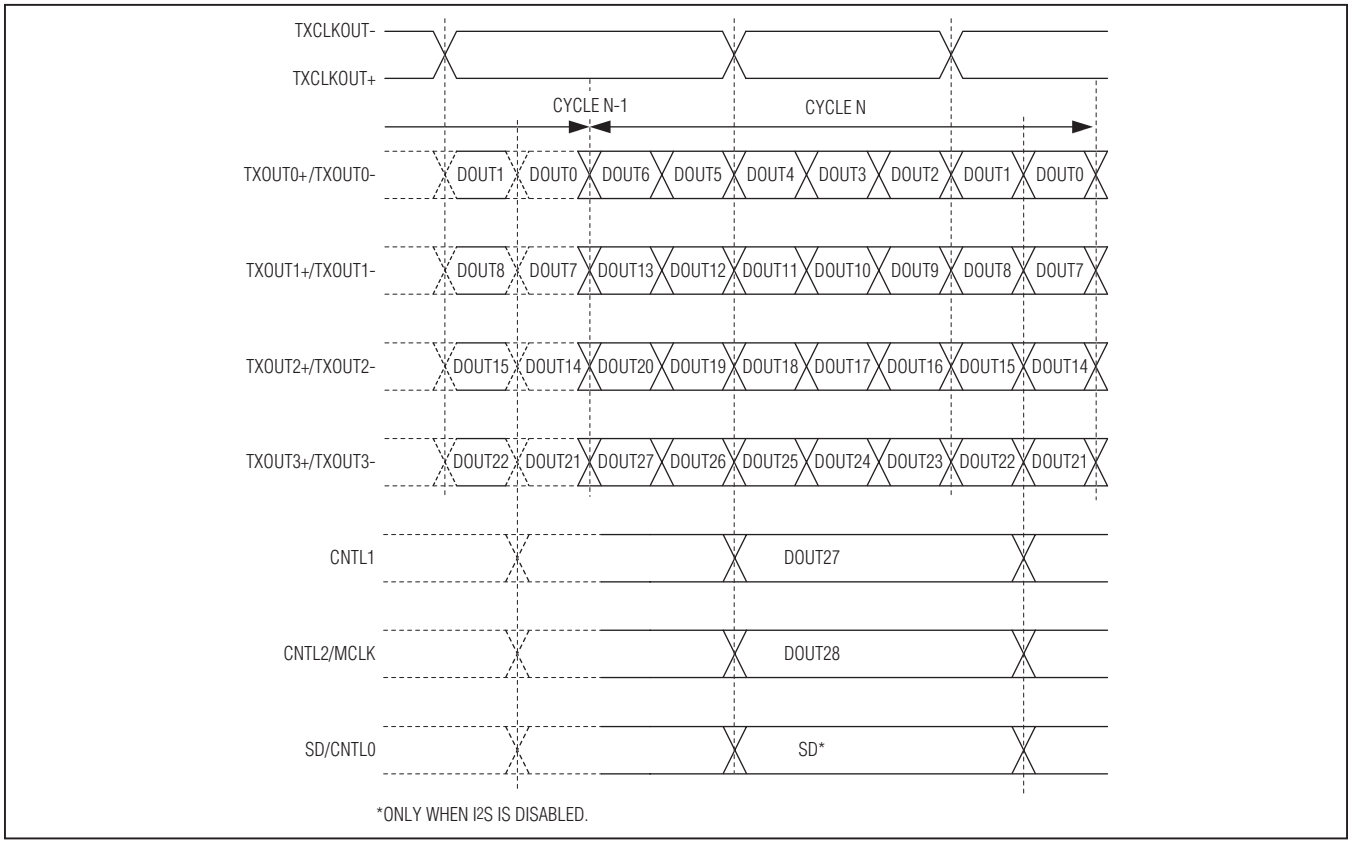


Figure 12. LVDS Output Timing

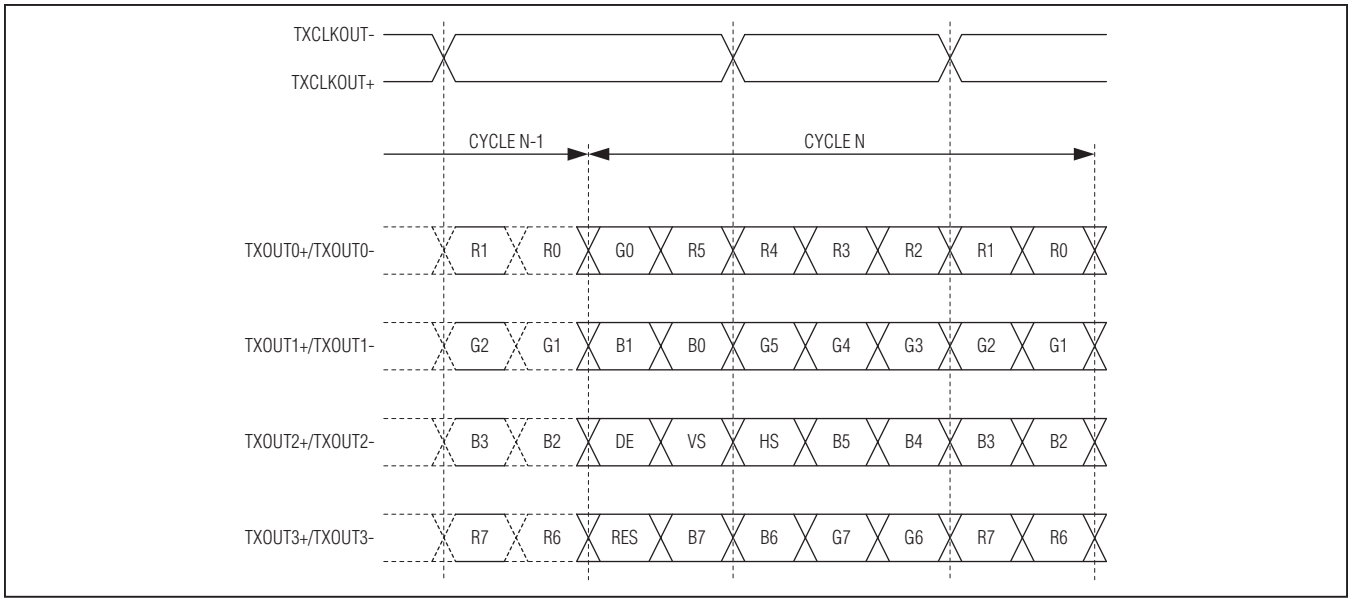


Figure 13. Typical Panel Clock and Bit Assignment

Serial Link Signaling and Data Format

The GMSL serializer uses CML signaling with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization. Together, the GMSL link can operate at full speed over STP cable lengths to 15m or more.

The GMSL serializer scrambles and encodes the input data and sends the 8b/10b coded signal through the serial link. The deserializer recovers the embedded serial clock and then samples, decodes, and descrambles before outputting the data. Figure 14 and 15 show the serial-data packet format after unscrambling and 8b/10b decoding. In 3-channel or 4-channel mode, 21 or 29 bits map to the high-speed output. The audio channel bit (ACB) contains an encoded audio signal derived from the three I²S signals (SD, SCK, and WS). The forward control-channel (FCC) bit carries the forward control data. The last bit (PCB) is the parity bit of the previous 23 or 31 bits.

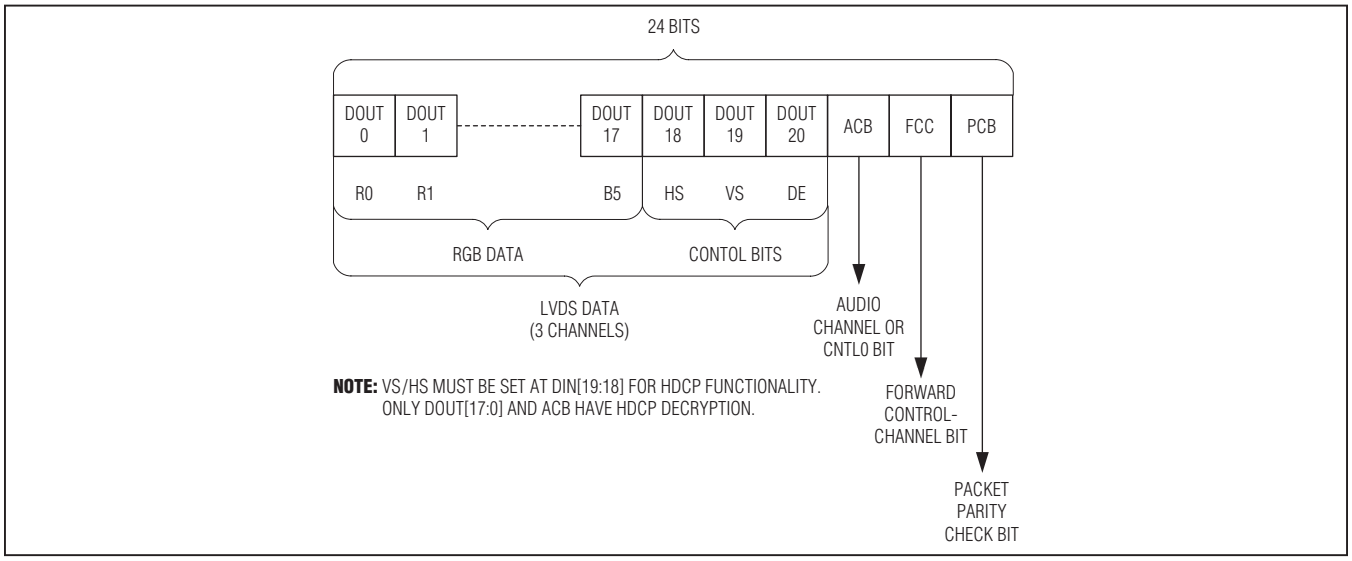


Figure 14. 3-Channel Mode Serial Link Data Format

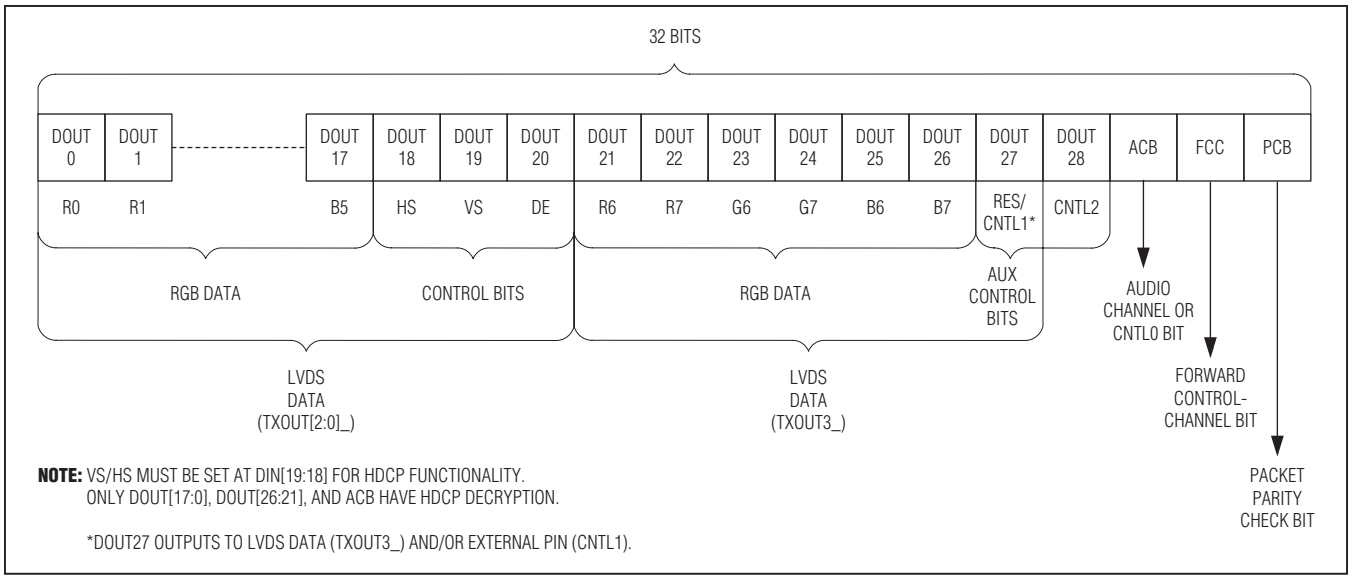


Figure 15. 4-Channel Mode Serial Link Data Format

Reverse Control Channel

The GMSL serializer uses the reverse control channel to receive I²C/UART and interrupt signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same twisted pair forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 500µs after power-up. The GMSL serializer temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

Reserved Bit (RES)/CNTL1

In 4-channel mode, the deserializer by default deserializes serial data bit 27 to RES (DISRES = 0) while CNTL is forced low (DISCNTL = 1). Setting DISRES (D2 of register 0x14) = 1 forces RES low. Setting DISCNTL1 (D3 of register 0x14) = 0 maps data bit 27 to CNTL1.

Data-Rate Selection

The deserializer uses the DRS input to set the TXCLKOUT_ frequency range. Set DRS high for a 6.25MHz to 12.5MHz TXCLKOUT_ frequency range (4-channel mode) or 8.33MHz to 16.66MHz (3-channel mode). Set DRS low for normal operation with a 12.5MHz to 78MHz TXCLKOUT_ frequency range (4-channel mode) or 16.66MHz to 104MHz (3-channel mode).

Audio Channel

The I²S audio channel supports 8kHz to 192kHz audio sampling rates and audio word lengths from 4 bits to 32 bits. The audio bit clock (SCK) does not have to be synchronized with TXCLKOUT_. The GMSL serializer automatically encodes audio data into a single bit stream synchronous with TXCLKOUT_. The deserializer decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I²S format. The audio channel is enabled by default. When the audio channel is disabled, the SD/CNTL0 on the GMSL serializer and deserializer is treated as an additional control signal (CNTL0).

Since the audio data sent through the serial link is synchronized with TXCLKOUT_, low TXCLKOUT_ frequencies limit the maximum audio sampling rate. Table 4 lists the maximum audio sampling rate for various TXCLKOUT_ frequencies. Spread-spectrum settings do not affect the I²S data rate or WS clock frequency.

Additional MCLK Output for Audio Applications

Some audio DACs, such as the MAX9850, do not require a synchronous main clock (MCLK), while other DACs require MCLK to be a specific multiple of WS. If an audio DAC chip needs the MCLK to be a multiple of WS, use an external PLL to regenerate the required MCLK from TXCLKOUT_ or SCK.

For audio applications that cannot use TXCLKOUT_ directly, the deserializer provides a divided MCLK output on CNTL2/MCLK at the expense of one less control line in 4-channel mode. By default, CNTL2/MCLK operates as a control data output and MCLK is turned off. Set MCLKDIV (deserializer register 0x12, D[6:0]) to a nonzero value to enable the MCLK output. Set MCLKDIV to 0x00 to disable MCLK and set CNTL2/MCLK as a control output.

Table 4. Maximum Audio WS Frequency (kHz) for Various TXCLKOUT_ Frequencies

WORD LENGTH (BITS)	TXCLKOUT_ FREQUENCY (DRS = LOW) (MHz)				TXCLKOUT_ FREQUENCY (DRS = HIGH) (MHz)			
	12.5	15	16.6	> 20	6.25	7.5	8.33	> 10
8	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
16	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
18	185.5	> 192	> 192	> 192	185.5	> 192	> 192	> 192
20	174.6	> 192	> 192	> 192	174.6	> 192	> 192	> 192
24	152.2	182.7	> 192	> 192	152.2	182.7	> 192	> 192
32	123.7	148.4	164.3	> 192	123.7	148.4	164.3	> 192

The output MCLK frequency is:

$$f_{MCLK} = \frac{f_{SRC}}{MCLKDIV}$$

where:

f_{SRC} is the MCLK source frequency (see Table 5)

MCLKDIV is the divider ratio from 1 to 127

Choose MCLKDIV values so that f_{MCLK} is not greater than 60MHz. MCLK frequencies derived from TXCLKOUT_ (MCLKSRC = 0) are not affected by spread-spectrum settings in the deserializer. Enabling spread spectrum in the GMSL serializer, however, introduces spread spectrum into MCLK. Spread-spectrum settings of either device do not affect MCLK frequencies derived from the internal oscillator. The internal oscillator frequency ranges from 100MHz to 150MHz over all process corners and operating conditions.

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. Configuring the CDS pin allows the µC to control the link from either the GMSL serializer or the deserializer side to support video-display or image-sensing applications. The control channel between the µC and GMSL serializer or deserializer runs in base mode or bypass mode according to the mode-selection (MS) input of the device connected to the µC. Base mode is a half-duplex control channel and bypass mode is a full-duplex control channel.

Base Mode

In base mode, the µC accesses the core and HDCP registers of the GMSL serializer and deserializer using the GMSL UART protocol. The µC can also program I²C peripherals on the remote side by sending UART packets that are converted to I²C on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol. The device addresses of the GMSL serializer and deserializer in base mode are programmable. The default value is determined by the pin settings of ADD0 and ADD1 (see Table 2).

When the peripheral interface is I²C (default), the device converts packets to I²C that have device addresses different from those of the GMSL serializer or deserializer. The converted I²C bit rate is the same as the original UART bit rate.

The deserializer uses a proprietary differential line coding to send signals back towards the serializer. The speed of the control channel ranges from 9.6kbps to 1Mbps in both directions. The GMSL serializer and deserializer automatically detect the control-channel bit rate in base mode. When changing the bit rate, the new packet bit rate can vary up to 3.5x from the previous bit rate (see the *Changing the Clock Frequency* section).

Table 5. f_{SRC} Settings

MCLKSRC SETTING (REGISTER 0x12, D7)	DATA-RATE SETTING	BUS-WIDTH SETTING	MCLK SOURCE FREQUENCY (f_{SRC})
0	High speed (DRS = high)	3-channel mode	3 x $f_{TXCLKOUT\_}$
		4-channel mode	4 x $f_{TXCLKOUT\_}$
	Low speed (DRS = low)	3-channel mode	6 x $f_{TXCLKOUT\_}$
		4-channel mode	8 x $f_{TXCLKOUT\_}$
1	—	—	Internal oscillator (120MHz typ)

Figure 16 shows the UART protocol for writing and reading in base mode between the µC and the GMSL serializer/deserializer.

Figure 17 shows the UART data format. Figures 18 and 19 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and interrupt generate transitions on the control channel that should be ignored by the µC. Data written to the GMSL serializer/deserializer registers do not take effect until after the acknowledge byte is sent. This allows the µC to verify write commands received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the µC UART data rate automatically. If the INT or MS inputs of the deserializer toggle while there is control-channel communication, the control-channel communication can be corrupted. In the event of a missed acknowledge, the µC assumes there was an error in the packet when the slave device receives it, or that an error occurred during the response from the slave device. In base mode, the µC must keep the UART Tx/Rx lines high for 16 bit times before sending a new packet.

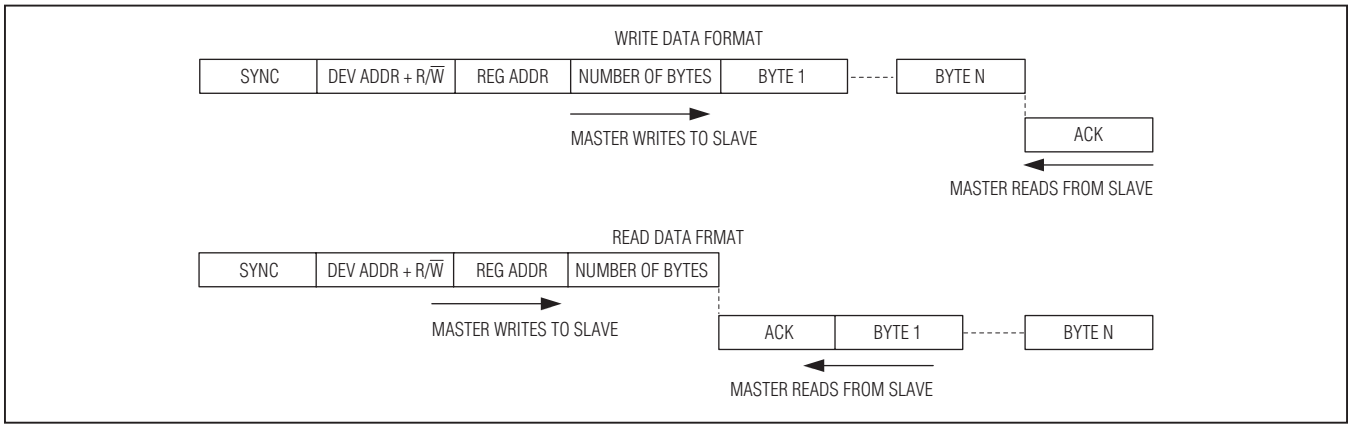


Figure 16. GMSL UART Protocol for Base Mode

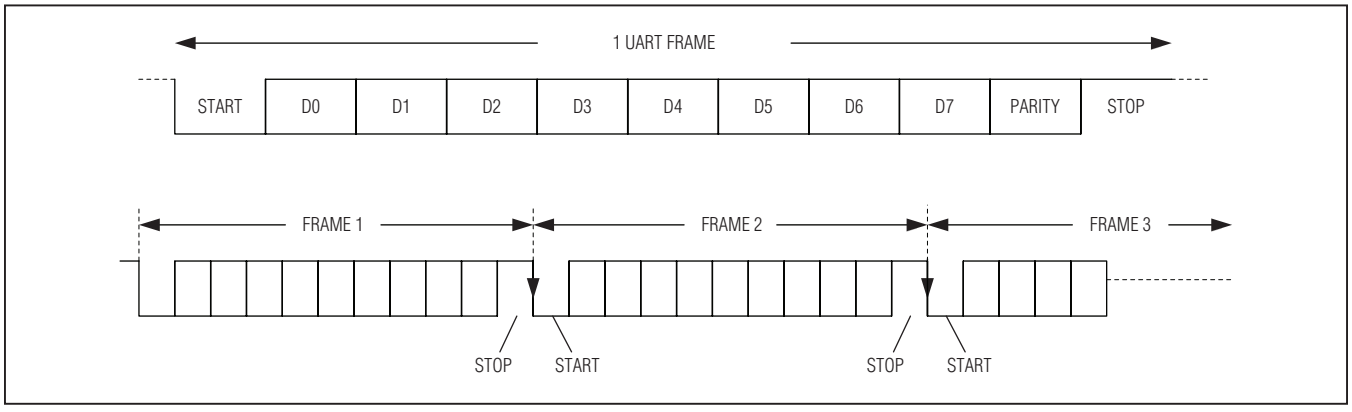


Figure 17. GMSL UART Data Format for Base Mode

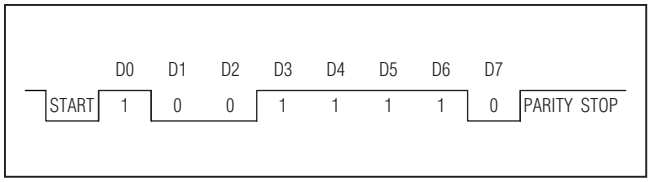


Figure 18. SYNC Byte (0x79)

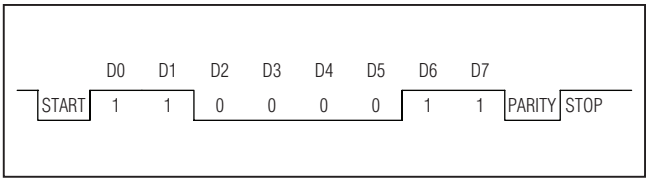


Figure 19. ACK Byte (0xC3)

As shown in Figure 20, the remote-side device converts the packets going to or coming from the peripherals from the UART format to the I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C's data rate is the same as the UART data rate.

Interfacing Command-Byte-Only I²C Devices

The GMSL serializer and deserializer UART-to-I²C conversion interfaces with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 21). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

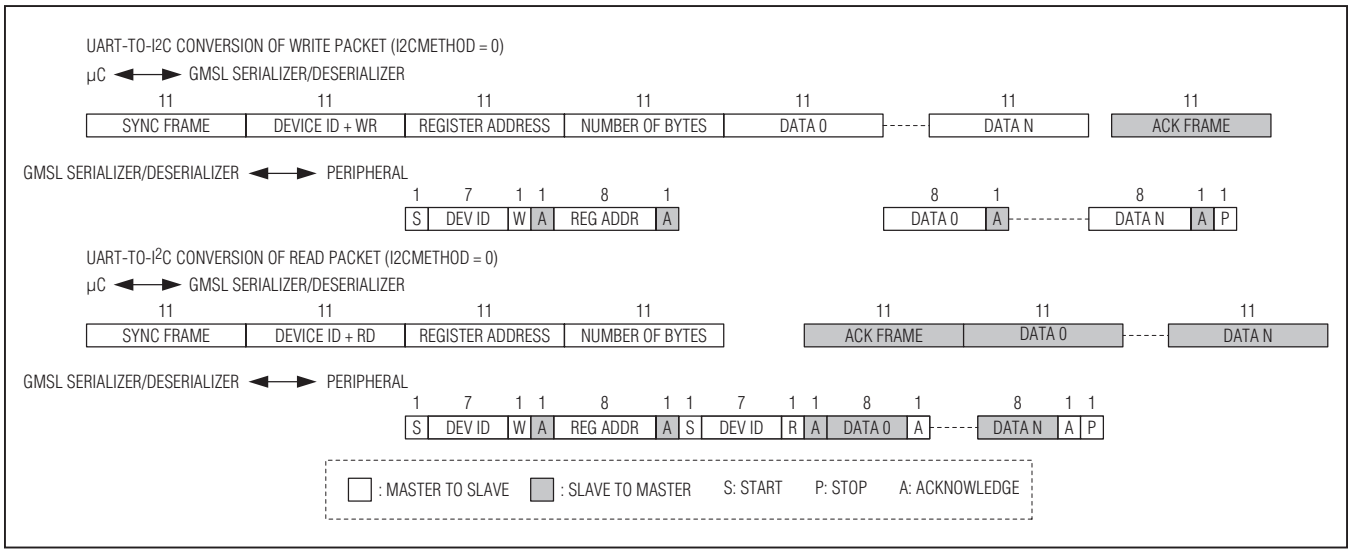


Figure 20. Format Conversion between GMSL UART and I²C with Register Address (I2CMETHOD = 0)

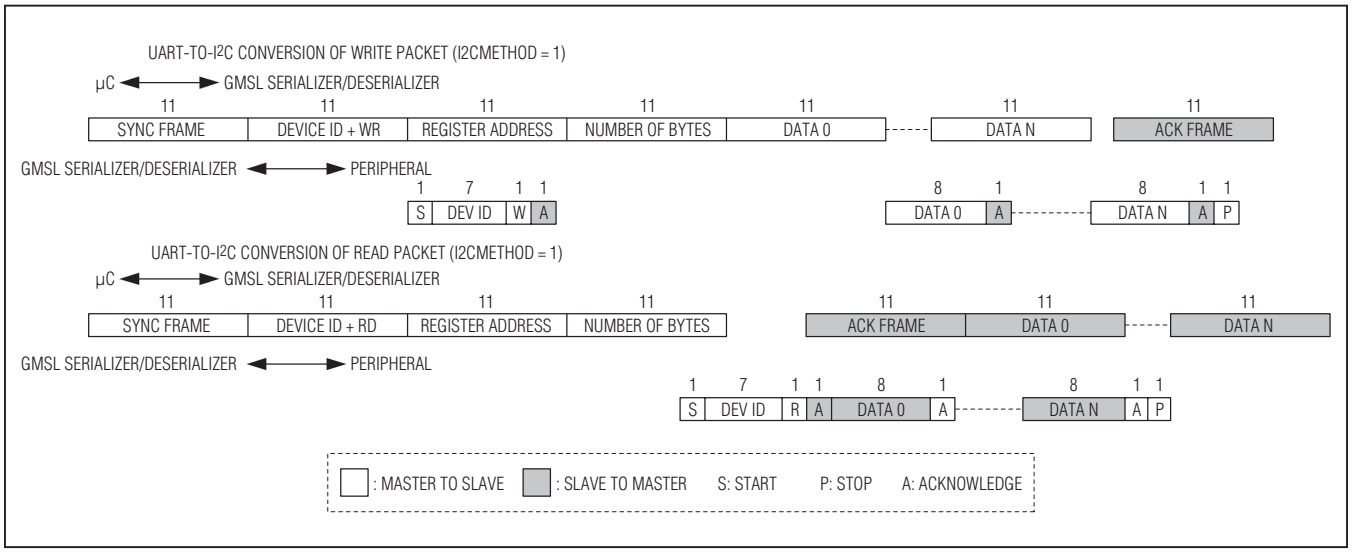


Figure 21. Format Conversion Between GMSL UART and I²C with Register Address (I2CMETHOD = 1)

Bypass Mode

In bypass mode, the GMSL serializer/deserializer ignore UART commands from the µC and the µC communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the GMSL serializer/deserializer's registers in this mode. Peripherals accessed through the forward control channel using the UART interface must tolerate up to one TXCLKOUT_ period ±10ns of jitter due to the asynchronous sampling of the UART signal by TXCLKOUT_. Set MS = high to put the control channel into bypass mode. A 1ms wait time is required between setting MS high on the deserializer and the bypass becoming active. There is no delay when switching to bypass mode on the serializer (CDS = low). Do not send a logic-low longer than 100µs on the control channel in bypass mode if interrupt (INT) is used. Bypass mode accepts bit rates down to 10kbps in either direction.

Interrupt Control

The INT pin of the GMSL serializer is the interrupt output and the INT pin of the deserializer is the interrupt input. Following a transition, the logic state of the interrupt input is reproduced on the interrupt output. The interrupt supports remote-side functions such as touch-screen peripherals, remote power-up, or remote monitoring. An interrupt that occurs when the reverse control channel is disabled, such as during link startup/shutdown, is sent once the reverse control channel becomes available. Bit D4 of register 0x06 in the deserializer stores the interrupt input state. The INT output of the GMSL serializer is low after power-up. The µC can set the INT output by writing the SETINT register bit. Do not low-state data on the control channel longer than 100µs in either base mode or bypass mode to ensure proper interrupt functionality.

Line Equalizer

The deserializer includes an adjustable line equalizer to compensate cable attenuation at high frequencies. The cable equalizer has 11 levels of compensation from 2.1dB to 13dB (see Table 6). The EQS input selects the default equalization level at power-up. The state of EQS is latched upon power-up or when resuming from power-down mode. To select other equalization levels, set the corresponding register bits in the deserializer (0x05 D[3:0]). Use equalization in the deserializer, together with pre/deemphasis in the GMSL serializer to create the most reliable link for a given cable.

Table 6. Deserializer Cable Equalizer Boost Levels

BOOST SETTING (0x05 D[3:0])	TYPICAL BOOST GAIN (dB)
0000	2.1
0001	2.8
0010	3.4
0011	4.2
0100	5.2 **Power-up default (EQS = high)**
0101	6.2
0110	7
0111	8.2
1000	9.4
1001	10.7 **Power-up default (EQS = low)**
1010	11.7
1011	13

Table 7. Output Spread

SS	SPREAD (%)
00	No spread spectrum. **Power-up default when SSEN = low.**
01	±2% spread spectrum. **Power-up default when SSEN = high.**
10	No spread spectrum
11	±4% spread spectrum

Spread Spectrum

To reduce the EMI generated by transitions on the serial link and outputs of the deserializer, the GMSL serializer/deserializer are individually capable of generating spread spectrum. However, turning on spread spectrum in the GMSL serializer spreads the serial link and the deserializer outputs since the deserializer tracks the spread on the serial link. Do not enable spread generation on the GMSL serializer/deserializer at the same time. The amplitudes of the deserializer spread-spectrum generator are ±2% and ±4% (see Table 7).

Set the deserializer SSEN input high to select a ±2% spread at power-up and SSEN input low to select no spread at power-up. The state of SSEN is latched upon power-up or when resuming from power-down mode.

Turning on spread spectrum on the GMSL serializer or deserializer does not spread the audio data stream. The GMSL serializer spreads the deserializer MCLK output if it is derived from TXCLKOUT_ (MCLKSRC = 0).

The deserializer includes a sawtooth divider to control the spread-modulation rate. Autodetection or manual programming of the TXCLKOUT_ operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV, 0x03 D[4:0]) allows the user to set a modulation frequency according to the TXCLKOUT_ frequency. Always keep the modulation frequency between 20kHz and 40kHz to ensure proper operation.

Manual Programming of the Spread-Spectrum Divider

The modulation rate for the deserializer relates to the TXCLKOUT_ frequency as follows:

$$f_M = (1 + DRS)\frac{f_{TXCLKOUT\_}}{MOD \times SDIV}$$

where:

f_M = Modulation frequency

DRS = DRS pin input value (0 or 1)

$f_{TXCLKOUT\_}$ = TXCLKOUT_ frequency

MOD = Modulation coefficient given in Table 8

SDIV = 5-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 8, set SDIV to the maximum value.

Sleep Mode

The deserializer includes a low-power sleep mode to reduce power consumption on the device. Set the SLEEP bit to 1 to initiate sleep mode. The deserializer sleeps after serial link inactivity or 8ms (whichever arrives first) after setting its SLEEP = 1. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

The µC can only put the remote-side device into sleep mode. Use the $\overline{PWDN}$ input pin to bring the µC-side device into a low-power state. Entering sleep mode resets the HDCP registers but not the configuration registers.

Power-Down Mode

The deserializer includes a power-down mode that reduces power consumption more than sleep mode. Set $\overline{PWDN}$ low to enter power-down mode. In power-down mode, the outputs are high impedance. Power-down mode resets the internal registers of the device. Upon exiting power-down mode, the deserializer relatches the state of the SSEN, DRS, and EQS pins.

Configuration Link

GMSL includes a low-speed configuration link to allow control-channel operation in the absence of a clock input. In either display or camera applications, the configuration link can program equalizer, preemphasis, or other registers before establishing the video link. An internal oscillator provides TXCLKOUT_ for establishing the serial configuration link. Set CLINKEN = 1 on the GMSL serializer to turn on the configuration link. The configuration link remains active as long as the video link is not enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Table 8. Modulation Coefficients and Maximum SDIV Settings

SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT (dec)	SDIV UPPER LIMIT (dec)
±4	208	15
±2	208	30

Link Startup Procedure

Table 9 lists four startup cases for display applications. Table 10 lists two startup cases for image-sensing applications. In either application, the control link is available after the video link or the configuration link is established. Then the GMSL registers or the peripherals are ready for programming.

Video-Display Applications

For video-display applications, connect the µC to the GMSL serializer and set CDS = low for both the GMSL serializer and deserializer. Table 9 summarizes the four startup cases based on the settings of $\overline{AUTOS}$ and MS.

Case 1: Autostart Mode

After power-up or when $\overline{PWDN}$ transitions from low to high for both the GMSL serializer and deserializer, the serial link is established if a stable clock is present. The GMSL serializer locks to the clock and sends the serial data to the deserializer. The deserializer then detects activity on the serial link and locks to the input serial data.

Case 2: Standby Start Mode

After power-up or when $\overline{PWDN}$ transitions from low to high for both the GMSL serializer and deserializer, the deserializer starts up in sleep mode, and the GMSL serializer stays in standby mode (does not send serial data). Use the µC and program the GMSL serializer to set SEREN = 1 to establish a video link, or CLINKEN = 1 to establish the configuration link. After locking to a stable clock (for SEREN = 1) or the internal oscillator (for CLINKEN = 1), the GMSL serializer sends a wake-up signal to the deserializer. The deserializer exits sleep mode after locking to the serial data and sets SLEEP = 0. If after 8ms the deserializer does not lock to the input serial data, the deserializer goes back to sleep, and the internal sleep bit remains set (SLEEP = 1).

Case 3: Remote-Side Autostart Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the remote device (deserializer) starts up and tries to lock to an incoming serial signal with sufficient power. The host side (GMSL serializer) is in standby mode and does not try to establish a link. Use the µC and program the GMSL serializer to set SEREN = 1 (and apply a stable clock signal) to establish a video link, or CLINKEN = 1 to establish the configuration link. In this case, the deserializer ignores the short wake-up signal sent from the GMSL serializer.

Table 9. Startup Selection for Display Applications (Both CDS = Low)

CASE	$\overline{AUTOS}$ (GMSL SERIALIZER)	GMSL SERIALIZER POWER-UP STATE	MS (GMSL DESERIALIZER)	GMSL DESERIALIZER POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Low	Normal (SLEEP = 0)	Both devices power up with the serial link active (autostart).
2	High	Serialization disabled	High	Sleep mode (SLEEP = 1)	Serial link is disabled and the deserializer powers up in sleep mode. Set SEREN = 1 or CLINKEN = 1 in the GMSL serializer to start the serial link and wake up the deserializer.
3	High	Serialization disabled	Low	Normal (SLEEP = 0)	Both devices power up in normal mode with the serial link disabled. Set SEREN = 1 or CLINKEN = 1 in the GMSL serializer to start the serial link.
4	Low	Serialization enabled	High	In sleep mode (SLEEP = 1)	The deserializer starts in sleep mode. Link autostarts upon GMSL serializer power-up. Use this case when the deserializer powers up before the GMSL serializer.

Case 4: Remote Side in Sleep Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the remote device (deserializer) starts up in sleep mode. The high-speed link establishes automatically after the GMSL serializer powers up with a stable clock signal and sends a wake-up signal to the deserializer. Use this mode in applications where the deserializer powers up before the GMSL serializer.

Image-Sensing Applications

For image-sensing applications, connect the µC to the deserializer and set CDS = high for both the GMSL serializer and deserializer. The deserializer powers up normally (SLEEP = 0) and continuously tries to lock to a valid serial input. Table 10 summarizes both startup cases, based on the state of the GMSL serializer $\overline{AUTOS}$ pin.

Case 1: Autostart Mode

After power-up, or when $\overline{PWDN}$ transitions from low to high, the GMSL serializer locks to a stable input clock and sends the video data to the deserializer. The deserializer locks to the serial data and outputs the video data and clock.

Case 2: Sleep Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the GMSL serializer starts up in sleep mode. To wake up the serializer, use the µC to send a GMSL protocol UART frame containing at least three rising edges (e.g., 0x66) at a bit rate no greater than 1Mbps. The low-power wake-up receiver of the serializer detects the wake-up frame over the reverse control channel and powers up. Reset the sleep bit (SLEEP = 0) of the GMSL serializer using a control-channel write packet to power up the device. Send the sleep bit reset write packet at least 500µs after the wake-up frame. The GMSL serializer goes back to sleep mode if its sleep bit is not reset within 5ms (min) after detecting a wake-up frame.

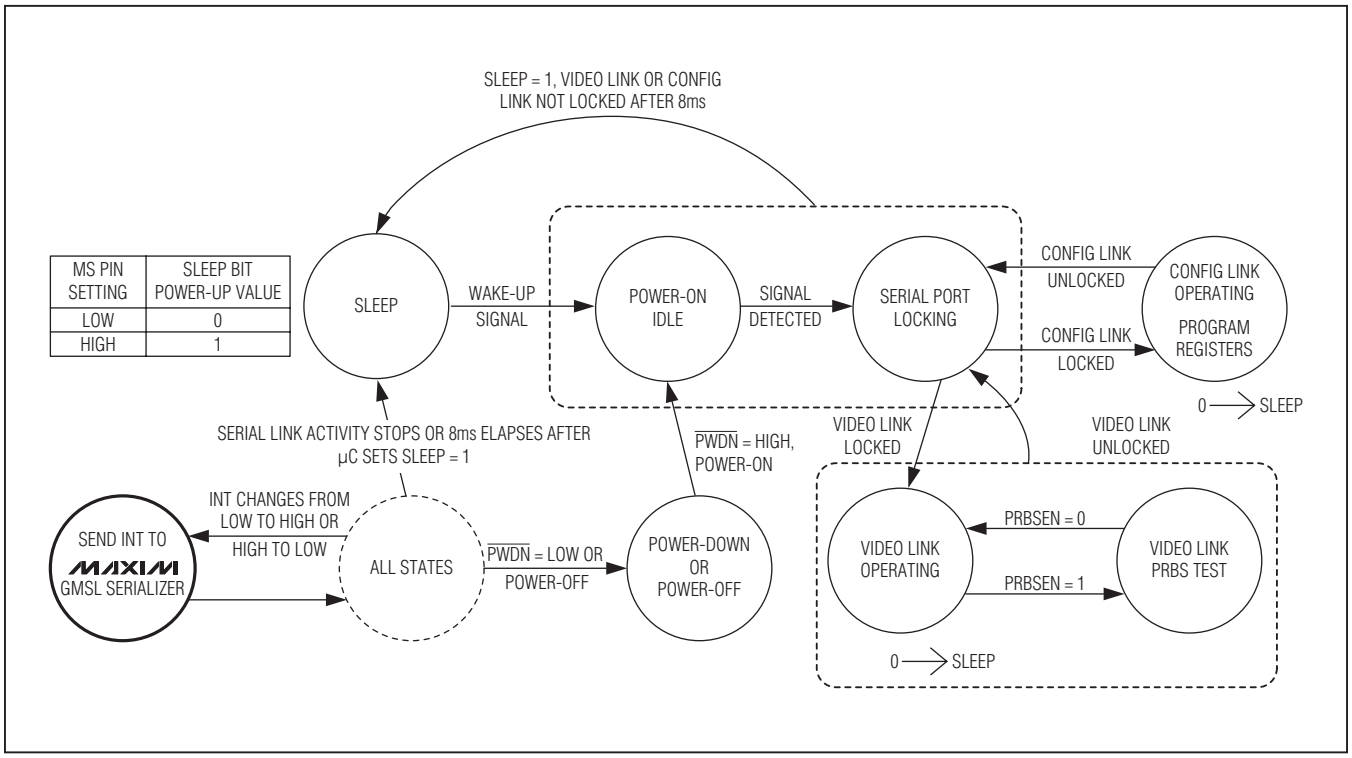


Figure 22. State Diagram, CDS = Low (Display Application)

Table 10. Startup Selection for Image-Sensing Application (Both CDS = High)

CASE	$\overline{\text{AUTOS}}$ (GMSL SERIALIZER)	GMSL SERIALIZER POWER-UP STATE	GMSL DESERIALIZER POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Normal (SLEEP = 0)	Autostart.
2	High	Sleep mode (SLEEP = 1)	Normal (SLEEP = 0)	GMSL serializer is in sleep mode. Wake up the GMSL serializer through the control channel (µC attached to deserializer).

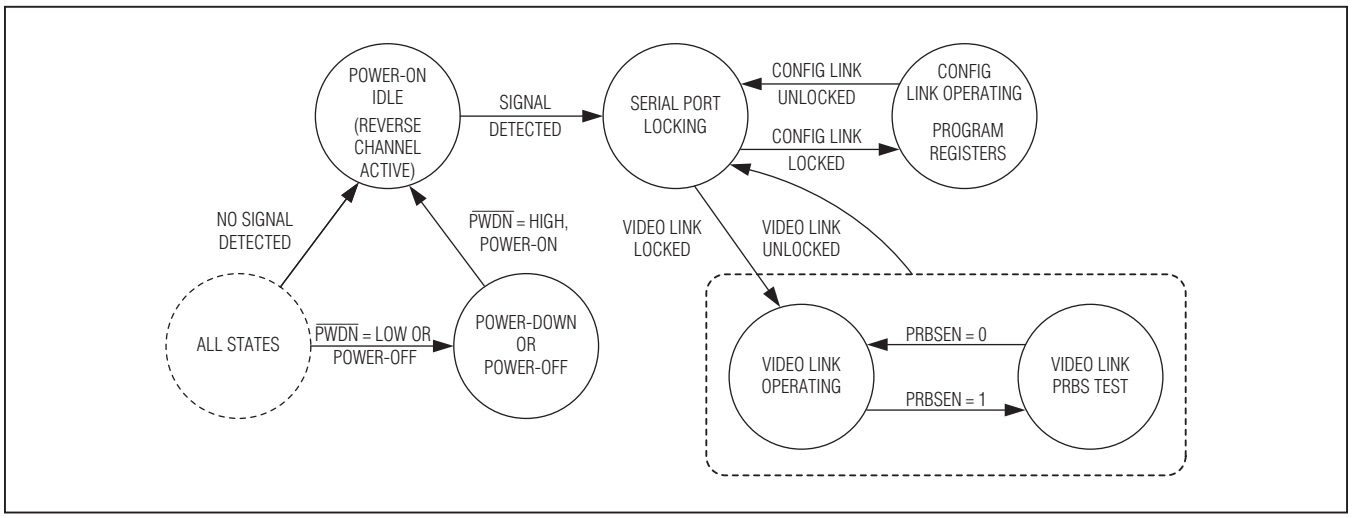


Figure 23. State Diagram, CDS = High (Camera Application)

High-Bandwidth Digital Content Protection (HDCP)

Note: The explanation of HDCP operation in this data sheet is provided as a guide for general understanding. Implementation of HDCP in a product must meet the requirements given in the *HDCP System v1.3 Amendment for GMSL*, which is available from DCP.

HDCP has two main phases of operation: authentication and the link integrity check. The µC starts authentication by writing to the START_AUTHENTICATION bit in the GMSL serializer. The GMSL serializer generates a 64-bit random number. The host µC first reads the 64-bit random number from the GMSL serializer and writes it to the deserializer. The µC then reads the GMSL serializer public key selection vector (AKSV) and writes it to the deserializer. The µC then reads the deserializer KSV (BKSV) and writes it to the GMSL serializer. The µC begins checking BKSV against the revocation list. Using the cipher, the GMSL serializer and deserializer calculate a 16-bit response value, R0 and R0', respectively. The GMSL amendment for HDCP reduces the 100ms minimum wait time allowed for the receiver to generate R0' (specified in HDCP rev 1.3) to 128 pixel clock cycles in the GMSL amendment.

There are two response-value comparison modes: internal comparison and µC comparison. Set EN_INT_COMP = 1 to select internal comparison mode. Set EN_INT_COMP = 0 to select µC comparison mode. In internal comparison mode, the µC reads the deserializer response R0' and writes it to the GMSL serializer. The GMSL serializer compares R0' to its internally generated response value R0, and sets R0_RI_MATCHED. In µC comparison mode, the µC reads and compares the R0/R0' values from the GMSL serializer/deserializer.

During response-value generation and comparison, the host µC checks for a valid BKSV (having 20 1s and 20 0s is also reported in BKSV_INVALID) and checks BKSV against the revocation list. If BKSV is not on the list and the response values match, the host authenticates the link. If the response values do not match, the µC resamples the response values (as described in HDCP rev 1.3, Appendix C). If resampling fails, the µC restarts authentication by setting the RESET_HDCP bit in the GMSL serializer. If BKSV appears on the revocation list, the host cannot transmit data that requires protection. The host knows when the link is authenticated and decides when to output data requiring protection. The µC performs a link integrity check every 128 frames or every 2s ±0.5s. The GMSL serializer/deserializer generate response values every 128 frames. These values are compared internally (internal comparison mode) or can be compared in the host µC.

In addition, the GMSL serializer/deserializer provide response values for the enhanced link verification. Enhanced link verification is an optional method of link verification for faster detection of loss-of-synchronization. For this option, the GMSL serializer and deserializer generate 8-bit enhanced link-verification response values (PJ and PJ') every 16 frames. The host must detect three consecutive PJ/PJ' mismatches before resampling.

Encryption Enable

The GMSL link transfers either encrypted or nonencrypted data. To encrypt data, the host µC sets the encryption enable (ENCRYPTION_ENABLE) bit in both the GMSL serializer and deserializer. The µC must set ENCRYPTION_ENABLE in the same VSYNC cycle in both the GMSL serializer and deserializer (no internal VSYNC falling edges between the two writes). The same timing applies when clearing ENCRYPTION_ENABLE to disable encryption.

Note: ENCRYPTION_ENABLE enables/disables encryption on the GMSL irrespective of the content. To comply with HDCP, the µC must not allow content requiring encryption to cross the GMSL unencrypted.

The µC must complete the authentication process before enabling encryption. In addition, encryption must be disabled before starting a new authentication session.

Synchronization of Encryption

The video vertical sync (VSYNC) synchronizes the start of encryption. Once encryption has started, the GMSL generates a new encryption key for each frame and each line, with the internal falling edge of VSYNC and HSYNC. Rekeying is transparent to data and does not disrupt the encryption of video or audio data.

Repeater Support

The GMSL serializer/deserializer include features to build an HDCP repeater. An HDCP repeater receives and decrypts HDCP content and then encrypts and transmits on one or more downstream links. A repeater can also use decrypted HDCP content (e.g., to display on a screen). To support HDCP repeater-authentication protocol, the deserializer has a REPEATER register bit. This register bit must be set to 1 by a µC (most likely on the repeater module). Both the GMSL serializer and deserializer use SHA-1 hash-value calculation over the assembled KSV lists. HDCP GMSL links support a maximum of 15 receivers (total number including the ones in repeater modules). If the total number of downstream receivers exceeds 14, the µC must set the MAX_DEVS_EXCEEDED register bit when it assembles the KSV list.

HDCP Authentication Procedures

The GMSL serializer generates a 64-bit random number exceeding the HDCP requirement. The GMSL serializer/deserializer internal one-time programmable (OTP) memories contain a unique HDCP keyset programmed at the factory. The host µC initiates and controls the HDCP authentication procedure. The GMSL serializer and deserializer generate HDCP authentication response values for the verification of authentication. Use the following procedures to authenticate the HDCP GMSL encryption (refer to the *HDCP 1.3 Amendment for GMSL* for details). The µC must perform link integrity checks while encryption is enabled (see Table 12). Any event that indicates that the deserializer has lost link synchronization should retrigger authentication. The µC must first write 1 to the RESET_HDCP bit in the GMSL serializer before starting a new authentication attempt.

HDCP Protocol Summary

Table 11, 12, and 13 list the summaries of the HDCP protocol. These tables serve as an implementation guide only. Meet the requirements in the GMSL amendment for HDCP to be in full compliance.

Table 11. Startup, HDCP Authentication, and Normal Operation (Deserializer is not a Repeater)—First Part of the HDCP Authentication Protocol

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	Initial state after power-up.	Powers up waiting for HDCP authentication.	Powers up waiting for HDCP authentication.
2	Makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, uses the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer to mask A/V data at the input of the GMSL serializer. Starts the link by writing SEREN = H or link starts automatically if $\overline{\text{AUTOS}}$ is low.	—	—
3	—	Starts serialization and transmits low-value content A/V data.	Locks to incoming data stream and outputs low-value content A/V data.
4	Reads the locked bit of the deserializer and makes sure the link is established.	—	—
5	Optionally writes a random-number seed to the GMSL serializer.	Combines seed with internally generated random number. If no seed provided, only internal random number is used.	—
6	If HDCP encryption is required, starts authentication by writing 1 to the START_AUTHENTICATION bit of the GMSL serializer.	Generates (stores) AN, and resets the START_AUTHENTICATION bit to 0.	—
7	Reads AN and AKSV from the GMSL serializer and writes to the deserializer.	—	Generates R0' triggered by the µC's write of AKSV.
8	Reads the BKSV and REPEATER bit from and writes to the GMSL serializer.	Generates R0, triggered by the µC's write of BKSV.	—
9	Reads the INVALID_BKSV bit of the GMSL serializer and continues with authentication if it is 0. Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—

Table 11. Startup, HDCP Authentication, and Normal Operation (Deserializer is not a Repeater)—First Part of the HDCP Authentication Protocol (continued)

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
10	Reads R0' from the deserializer and reads R0 from the GMSL serializer. If they match, continues with authentication; otherwise, retries up to two more times (optionally, GMSL serializer comparison can be used to detect if R0/R0' match). Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
11	Waits for the VSYNC falling edge (internal to the GMSL serializer) and then sets the ENCRYPTION_ENABLE bit to 1 in the deserializer and GMSL serializer (if the µC is not able to monitor VSYNC, it can utilize the VSYNC_DET bit in the GMSL serializer).	Encryption enabled after the next VSYNC falling edge.	Decryption enabled after the next VSYNC falling edge.
12	Checks that BKSV is not in the Key Revocation list and continues if it is not. Authentication can be restarted if it fails. **Note:** Revocation list check can start after BKSV is read in step 8.	—	—
13	Starts transmission of A/V content that needs protection.	Performs HDCP encryption on high-value content A/V data.	Performs HDCP decryption on high-value content A/V data.

Table 12. Link Integrity Check (Normal)—Performed Every 128 Frames After Encryption is Enabled

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	—	Generates Ri and updates the RI register every 128 VSYNC cycles.	Generates Ri' and updates the RI' register every 128 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 128 video frames (VSYNC cycles) or every 2s.	—	—
4	Reads RI from the GMSL serializer.	—	—
5	Reads RI' from the deserializer.	—	—
6	Reads RI again from the GMSL serializer and makes sure it is stable (matches the previous RI that it has read from the GMSL serializer). If RI is not stable, go back to step 5.	—	—

Table 12. Link Integrity Check (Normal)—Performed Every 128 Frames After Encryption is Enabled (continued)

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
7	If RI matches RI', the link integrity check is successful; go back to step 3.	—	—
8	If RI does not match RI', the link integrity check fails. After the detection of failure of link integrity check, the µC makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer can be used to mask A/V data input of the GMSL serializer.	—	—
9	Writes 0 to the ENCRYPTION_ENABLE bit of the GMSL serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
10	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the GMSL serializer.	—	—

Table 13. Optional Enhanced Link Integrity Check—Performed Every 16 Frames After Encryption is Enabled

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	—	Generates Pj and updates the PJ register every 16 VSYNC cycles.	Generates Pj' and updates the PJ' register every 16 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 16 video frames, reads PJ from the GMSL serializer and PJ' from the deserializer.	—	—
4	If PJ matches PJ', the enhanced link integrity check is successful; go back to step 3.	—	—

Table 13. Optional Enhanced Link Integrity Check—Performed Every 16 Frames After Encryption is Enabled (continued)

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
5	If there is a mismatch, retry up to two more times from step 3. Enhanced link integrity check fails after 3 mismatches. After the detection of failure of enhanced link integrity check, the µC makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer can be used to mask A/V data input of the GMSL serializer.	—	—
6	Writes 0 to the ENCRYPTION_ENABLE bit of the GMSL serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
7	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the GMSL serializer.	—	—

Example Repeater Network—Two µCs

The example shown in Figure 24 has one repeater and two µCs. Table 14 summarizes the authentication operation.

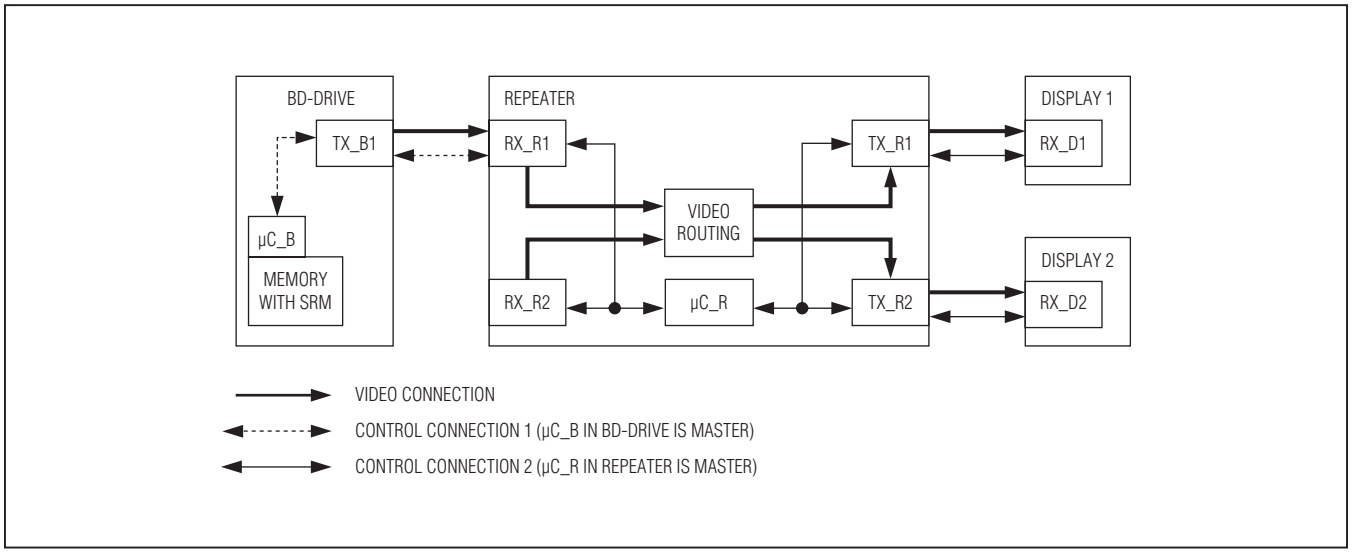


Figure 24. Example Network with One Repeater and Two µCs (Tx = GMSL Serializer's, Rx = Deserializer's)

Table 14. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
1	Initial state after power-up.	Initial state after power-up.	All: Power-up waiting for HDCP authentication.	All: Power-up waiting for HDCP authentication.
2	—	Writes REPEATER = 1 in RX_R1. Retries until proper acknowledge frame received. **Note:** This step must be completed before the first part of authentication is started between TX_B1 and RX_R1 by the µC_B (step 7). For example, to satisfy this requirement, RX_R1 can be held at power-down until µC_R is ready to write the REPEATER bit, or µC_B can poll µC_R before starting authentication.	—	—
3	Makes sure that A/V data not requiring protection (low-value content) is available at the TX_B1 inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of TX_B1 can be used to mask A/V data input of TX_B1. Starts the link between TX_B1 and RX_R1 by writing SEREN = H to TX_B1, or link starts automatically if $\overline{\text{AUTOS}}$ is low.	—	TX_B1: Starts serialization and transmits low-value content A/V data.	RX_R1: Locks to incoming data stream and outputs low-value content A/V data.
4	—	Starts all downstream links by writing SEREN = H to TX_R1, TX_R2, or links start automatically if $\overline{\text{AUTOS}}$ of transmitters are low.	TX_R1, TX_R2: Starts serialization and transmits low-value content A/V data.	RX_D1, RX_D2: Locks to incoming data stream and outputs low-value content A/V data.

Table 14. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0
5	Reads the locked bit of RX_R1 and makes sure the link between TX_B1 and RX_R1 is established.	Reads the locked bit of RX_D1 and makes sure the link between TX_R1 and RX_D1 is established. Reads the locked bit of RX_D2 and makes sure the link between TX_R2 and RX_D2 is established.	—	—
6	Optionally, writes a random number seed to TX_B1.	Writes 1 to the GPIO_0_ FUNCTION and GPIO_1_ FUNCTION bits in RX_R1 to change GPIO functionality used for HDCP purpose. Optionally, writes a random-number seed to TX_R1 and TX_R2.	—	—
7	Starts and completes the first part of the authentication protocol between TX_B1, RX_R1 (see steps 6–10 in Table 11).	—	TX_B1: According to commands from µC_B, generates AN, computes R0.	RX_R1: According to commands from µC_B, computes R0'.
8	—	When GPIO_1 = 1 is detected, starts and completes the first part of the authentication protocol between the (TX_R1, RX_D1) and (TX_R2, RX_D2) links (see steps 6–10 in Table 11).	TX_R1, TX_R2: According to commands from µC_R, generates AN, computes R0.	RX_D1, RX_D2: According to commands from µC_R, computes R0'.
9	Waits for the VSYNC falling edge and then enables encryption on the (TX_B1, RX_R1) link. Full authentication is not complete yet so it makes sure A/V content that needs protection is not transmitted. Since REPEATER = 1 was read from RX_R1, the second part of authentication is required.	—	TX_B1: Encryption enabled after next VSYNC falling edge.	RX_R1: Decryption enabled after next VSYNC falling edge.

Table 14. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
10	—	When GPIO_0 = 1 is detected, enables encryption on the (TX_R1, RX_D1) and (TX_R2, RX_D2) links.	TX_R1, TX_R2: Encryption enabled after next VSYNC falling edge.	RX_D1, RX_D2: Decryption enabled after next VSYNC falling edge.
11	Waits for some time to allow µC_R to make the KSV list ready in RX_R1. Then polls (reads) the KSV_LIST_READY bit of RX_R1 regularly until proper acknowledge frame is received and bit is read as 1.	Blocks control channel from µC_B side by setting REVCCEN = FWDCCEN = 0 in RX_R1. Retries until proper acknowledge frame received.	—	RX_R1: Control channel from serializer side (TX_B1) is blocked after FWDCCEN = REVCCEN = 0 is written.
12		Writes BKSVs of RX_D1 and RX_D2 to the KSV list in RX_R1. Then, calculates and writes the BINFO register of RX_R1.	—	RX_R1: Triggered by µC_R's write of BINFO, calculates hash value (V') on the KSV list, BINFO and the secret-value M0'.
13		Writes 1 to the KSV_LIST_READY bit of RX_R1 and then unblocks the control channel from the µC_B side by setting REVCCEN = FWDCCEN = 1 in RX_R1.	—	RX_R1: Control channel from the serializer side (TX_B1) is unblocked after FWDCCEN = REVCCEN = 1 is written.
14	Reads the KSV list and BINFO from RX_R1 and writes them to TX_B1. If any of the MAX_DEVS_EXCEEDED or MAX_CASCADE_EXCEEDED bits is 1, then authentication fails. **Note:** BINFO must be written after the KSV list.	—	TX_B1: Triggered by µC_B's write of BINFO, calculates hash value (V) on the KSV list, BINFO and the secret-value M0.	—

Table 14. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0
15	Reads V from TX_B1 and V' from RX_R1. If they match, continues with authentication; otherwise, retries up to two more times.	—	—	—
16	Searches for each KSV in the KSV list and BKSV of RX_R1 in the Key Revocation list.	—	—	—
17	If keys are not revoked, the second part of the authentication protocol is completed.	—	—	—
18	Starts transmission of A/V content that needs protection.	—	All: Perform HDCP encryption on high-value A/V data.	All: Perform HDCP decryption on high-value A/V data.

Detection and Action Upon New Device Connection

When a new device is connected to the system, the device must be authenticated and the device's KSV checked against the revocation list. The downstream µCs can set the NEW_DEV_CONN bit of the upstream receiver and invoke an interrupt to notify upstream µCs.

Notification of Start of Authentication and Enable of Encryption to Downstream Links

HDCP repeaters do not immediately begin authentication upon startup or detection of a new device, but instead wait for an authentication request from the upstream transmitter/repeaters.

Use the following procedure to notify downstream links of the start of a new authentication request:

1) Host µC begins authentication with the HDCP repeater's input receiver.
2) When AKSV is written to HDCP repeater's input receiver, its AUTH_STARTED bit is automatically set and its GPIO1 goes high (if GPIO1_FUNCTION is set to high).
3) HDCP repeater's µC waits for a low-to-high transition on HDCP repeater input receiver's AUTH_STARTED bit and/or GPIO1 (if configured) and starts authentication downstream.
4) HDCP repeater's µC resets the AUTH_STARTED bit.

Set GPIO0_FUNCTION to high to have GPIO0 follow the ENCRYPTION_ENABLE bit of the receiver. The repeater µC can use this function for notification when encryption is enabled/disabled by an upstream µC.

Applications Information

Error Checking

The deserializer checks the serial link for errors and stores the number of detected decoding errors in the 8-bit register, DECERR (0x0D). If a large number of 8b/10b decoding or parity errors are detected within a short duration (error rate ≥ 1/4), the deserializer loses lock and stops the error counter. The deserializer then attempts to relock to the serial data. DECERR resets upon successful video link lock, successful readout of DECERR (through UART), or whenever autoerror reset is enabled. The deserializer does not check for decoding or parity errors during the internal PRBS test and DECERR is reset to 0x00.

$\overline{ERR}$ Output

The deserializer has an open-drain $\overline{ERR}$ output. This output asserts low whenever the number of decoding errors exceeds the error threshold ERRTHR (0x0C) during normal operation, or when at least one PRBS error is detected during PRBS test. $\overline{ERR}$ reasserts high whenever DECERR (0x0D) resets due to DECERR readout, video link lock, or autoerror reset.

Autoerror Reset

The default method to reset errors is to read the respective error registers in the deserializer (0x0D, 0x0E). Autoerror reset clears the decoding error counter DECERR and the $\overline{ERR}$ output ~1µs after $\overline{ERR}$ goes low. Autoerror reset is disabled on power-up. Enable autoerror reset through AUTORST (0x06, D6). Autoerror reset does not run when the device is in PRBS test mode.

PRBS Self-Test

The GMSL serializer/deserializer link includes a PRBS pattern generator and a bit-error verification function. First, disable the glitch filters (set DISVSFILT, DISHSFILT to 1) in the deserializer. Next, disable VSYNC/HSYNC inversion in both the GMSL serializer and deserializer (set INVVSYNC, INVHSYNC to 0). Then, set PRBSEN = 1 (0x04, D5) in the GMSL serializer and then the deserializer to start the PRBS self-test. Set PRBSEN = 0 (0x04, D5) first in the deserializer and then the GMSL serializer to exit the PRBS self-test. The deserializer uses an 8-bit register (0x0E) to count the number of detected errors. The control link also controls the start and stop of the error counting. During PRBS mode, the device does not count decoding errors and the deserializer $\overline{ERR}$ output reflects PRBS errors only.

Microcontrollers on Both Sides of the GMSL Link (Dual µC Control)

Usually the microcontroller is either on the GMSL serializer side for video-display applications or on the deserializer side for image-sensing applications. For the former case, both the CDS pins of the GMSL serializer and deserializer are set to low, and for the latter case, the CDS pins are set to high. However, if the CDS pin of the GMSL serializer is low and the same pin of the deserializer is high, then the GMSL serializer/deserializer connect to both µCs simultaneously. In such a case, the µCs on either side can communicate with the GMSL serializer and deserializer.

Contentions of the control link can happen if the µCs on both sides are using the link at the same time. The GMSL serializer/deserializer do not provide the solution for contention avoidance. The serializer/deserializer do not send an acknowledge frame when communication fails due to contention. Users can always implement a higher layer protocol to avoid the contention. In addition, if UART communication across the serial link is not required, the µCs can disable the forward and reverse control channel through the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the GMSL serializer/deserializer. UART communication across the serial link is stopped and contention between µCs no longer occurs. During dual µC operation, if one of the CDS pins on either side changes state, the link resumes the corresponding state described in the *Link Startup Procedure* section.

As an example of dual µC use in an image-sensing application, the GMSL serializer can be in sleep mode and waiting for wake-up by the deserializer. After wake-up, the serializer-side µC sets the GMSL serializer's CDS pin low and assumes master control of the serializer's registers.

HSYNC/VSYNC Glitch Filter

The deserializer contains one-cycle glitch filters on HSYNC and VSYNC. This eliminates single-cycle glitches in HSYNC and VSYNC that can cause a loss of HDCP synchronization between the GMSL serializer and deserializer while encryption is enabled. The glitch filters are on by default. Write to D[1:0] of register 0x08 in the deserializer to disable the glitch filters for HSYNC or VSYNC.

The glitch filter, when active, suppresses all single-cycle-wide pulses sent. Disable the glitch filter before running PRBS BER tests. The internal BER checker assumes that the incoming bit stream is unaltered PRBS data.

Changing the Clock Frequency

Both the video clock rate ($f_{TXCLKOUT\_}$) and the control-channel clock rate (f_{UART}) can be changed on the fly to support applications with multiple clock speeds. It is recommended to enable the serial link after the video clock stabilizes. Stop the video clock for 5µs and restart the serial link or toggle SEREN after each change in the video clock frequency to recalibrate any automatic settings if a clean frequency change cannot be guaranteed. The reverse control channel remains unavailable for 350µs after serial link start or stop. Limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps and then at 100kbps to have reduction ratios of 3 and 3.333, respectively.

Do not interrupt TXCLKOUT_ or change its frequency while encryption is enabled; otherwise, HDCP synchronization is lost and authentication must be repeated. To change the TXCLKOUT_ frequency, stop the high-value content A/V data. Then disable encryption in the GMSL serializer/deserializer within the same VSYNC cycle—encryption stops at the next VSYNC falling edge. TXCLKOUT_ can now be changed/stopped. Reenable encryption before sending any high-value content A/V data.

Fast Detection of Loss-of-Synchronization

A measure of link quality is the recovery time from loss-of-HDCP synchronization. With the GMSL, it is likely that HDCP synchronization will not be lost unless the GMSL synchronization is lost. The host can be quickly notified of loss-of-lock by connecting the deserializer LOCK output to the INT input. If other sources use the interrupt input, such as a touch-screen controller, the µC can implement a routine to distinguish between interrupts from loss-of-sync and normal interrupts. Reverse control-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the GMSL link. LOCK asserts for video link only and not for the configuration link.

Programming the Device Addresses

Both the GMSL serializer and the deserializer have programmable device addresses. This allows multiple GMSL devices along with I²C peripherals to coexist on the same control channel. The serializer device address is stored in register 0x00 of each device, while the deserializer device address is stored in register 0x01 of each device. To change the device address, first write to the device whose address changes (register 0x00 of the GMSL serializer for serializer device-address change, or register 0x01 of the deserializer for deserializer device-address change). Then write the same address into the corresponding register on the other device (register 0x00 of the deserializer for serializer device-address change, or register 0x01 of the GMSL serializer for deserializer device-address change).

3-Level Inputs for Default Device Address

ADD0 and ADD1 are 3-level inputs that control the deserializer's default-device slave addresses (see Table 2). Connect ADD0/ADD1 through a pullup resistor to IOVDD, a pulldown resistor to GND, or a high-impedance connection. For digital control, use three-state logic to drive the 3-level logic inputs.

ADD0/ADD1 set the device addresses in the deserializer only and not the GMSL serializer. Set the GMSL serializer's ADD0/ADD1 inputs to the same settings as the deserializer; alternatively, write to register 0x00 and 0x01 of the GMSL serializer to reflect any changes made due to the 3-level inputs.

Configuration Blocking

The deserializer can block changes to the non-HDCP registers. Set CFGBLOCK to make all non-HDCP registers read only. Once set, the registers remain blocked until the supplies are removed or until $\overline{PWDN}$ is low.

Backward Compatibility

The deserializer is backward compatible with the non-HDCP MAX9268 deserializer with the following exceptions:

- **UART packet delay at power-up:** The µC must wait 2.7ms before sending the first UART packet to the deserializer. This delay is < 200µs for the MAX9268.
- **Glitch filters:** The deserializer includes one-cycle glitch filters on HS and VS. For backward compatibility, disable the glitch filters by setting D[1:0] of register 0x08 to 0.

The pinouts and packages are the same for both devices. See Table 3 and the *Pin Description* section for backward-compatible pin mapping.

Key Memory

Each device has a unique HDCP key set that is stored in secure nonvolatile memory (NVM). The HDCP key set consists of forty 56-bit private keys and one 40-bit public key. The NVM is qualified for automotive applications.

GPIOs

The deserializer has two open-drain GPIOs available. When not used for HDCP purposes (see the *Notification of Start of Authentication and Enable of Encryption to Downstream Links* section), GPIO1OUT and GPIO0OUT (0x06, D3 and D1) set the output state of the GPIOs. The GPIO input buffers are always enabled. The input states are stored in GPIO1 and GPIO0 (0x06, D2 and D0). Set GPIO1OUT/GPIO0OUT to 1 when using GPIO1/GPIO0 as an input.

Internal Input Pulldowns

The control and configuration inputs on the deserializer include an active pulldown to GND. Pulldowns are disabled when the device is shut down ($\overline{PWDN}$ = low) or put into sleep mode. During power-up, keep all inputs driven or use external pullup/pulldown resistors to prevent additional current consumption and undesired configuration due to undefined inputs.

Choosing I²C/UART Pullup Resistors

Both I²C/UART open-drain lines require pullup resistors to provide a logic-high level. There are trade-offs between power dissipation and speed, and a compromise made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times to go from low to high (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *DC Electrical Characteristics* and *AC Electrical Characteristics* tables for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so rise time $t_R = 0.85 \times R_{PULLUP} \times C_{BUS} < 300ns$. The waveforms are not recognized if the transition time becomes too slow. The deserializer supports I²C/UART rates up to 1Mbps.

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Four capacitors (two at the serializer output and two at the deserializer input) are needed for proper link operation and to provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML receiver termination resistor (R_{TR}), the CML driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is $(C \times (R_{TD} + R_{TR}))/4$. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω). This leaves the capacitor selection to change the system time constant. Use at least 0.2µF high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The deserializer uses an AVDD and DVDD of 3.0V to 3.6V. All single-ended inputs and outputs on the deserializer derive power from a 1.7V to 3.6V V_{IOVDD}, which scales with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Twisted-pair and shielded twisted-pair cables tend to generate less EMI due to magnetic-field canceling effects. Balanced cables pick up noise as com-

Table 15. Suggested Connectors and Cables for GMSL

VENDOR	CONNECTOR	CABLE
JAE Electronics, Inc.	MX38-FF	A-BW-Lxxxxx
Nissei Electric Co., Ltd.	GT11L-2S	F-2WME AWG28
Rosenberger Hochfrequenztechnik GmbH	D4S10A-40ML5-Z	Dacar 538

mon mode rejected by the CML receiver. Table 15 lists the suggested cables and connectors used in the GMSL link.

Board Layout

Separate the digital signals and CML/LVDS high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/LVDS, and digital signals. Lay out PCB traces close to each other for a 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together because the impedance goes down when the traces are brought closer.

Route the PCB traces for a CML/LVDS channel (there are two conductors per CML/LVDS channel) in parallel to maintain the differential characteristic impedance. Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

ESD Protection

The deserializer ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial link I/O are tested for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 25). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 26). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 27).

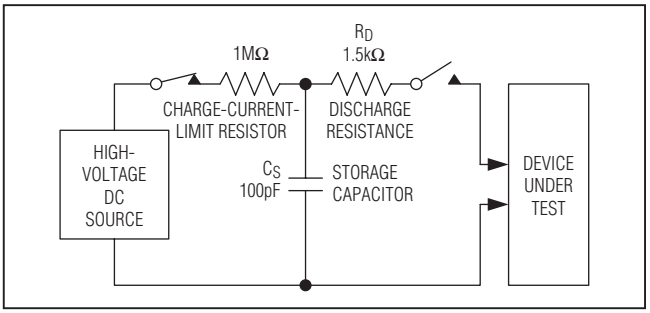


Figure 25. Human Body Model ESD Test Circuit

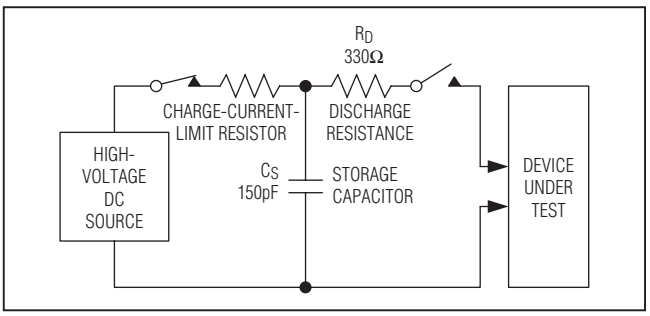


Figure 26. IEC 61000-4-2 Contact Discharge ESD Test Circuit

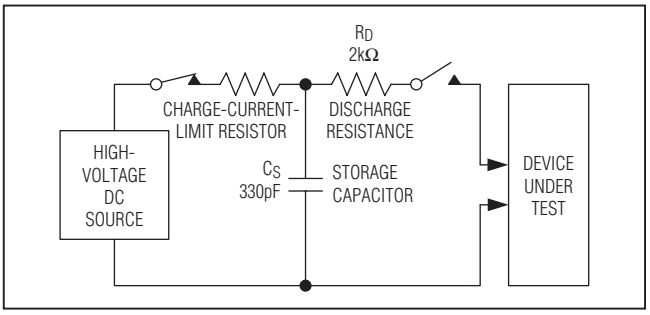


Figure 27. ISO 10605 Contact Discharge ESD Test Circuit

Table 16. GMSL Core Register Table (see Table 1)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address. Power-up default address determined by ADD0 and ADD1 (see Table 2).	1000000
	D0	—	0	Reserved	0
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address. Power-up default address determined by ADD0 and ADD1 (see Table 2).	1001000
	D0	CFGBLOCK	0	Normal operation	0
			1	Registers 0x00 to 0x1F are read only	
0x02	D[7:6]	SS	**00**	No spread spectrum. **Power-up default when SSEN = low.**	00, 01
			01	±2% spread spectrum. **Power-up default when SSEN = high**	
			10	No spread spectrum	
			11	±4% spread spectrum	
	D5	—	0	Reserved	0
	D4	AUDIOEN	0	Disable I²S channel	1
			1	Enable I²S channel	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock	11
			01	25MHz to 50MHz pixel clock	
			10	50MHz to 104MHz pixel clock	
			11	Automatically detect the pixel clock range	
	D[1:0]	SRNG	00	0.5Gbps to 1Gbps serial-data rate	11
			01	1Gbps to 2Gbps serial-data rate	
			10	2Gbps to 3.125Gbps serial-data rate	
			11	Automatically detect serial-data rate	
0x03	D[7:6]	AUTOFM	00	Calibrate spread-modulation rate only once after locking	00
			01	Calibrate spread-modulation rate every 2ms after locking	
			10	Calibrate spread-modulation rate every 16ms after locking	
			11	Calibrate spread-modulation rate every 256ms after locking	
	D5	—	0	Reserved	0
	D[4:0]	SDIV	00000	Autocalibrate sawtooth divider	00000
			XXXXX	Manual SDIV setting (see the *Manual Programming of the Spread-Spectrum Divider* section)	

Table 16. GMSL Core Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x04	D7	LOCKED	0	LOCK output is low	0 (read only)
			1	LOCK output is high	
	D6	OUTENB	0	Enable outputs	0
			1	Disable outputs	
	D5	PRBSEN	0	Disable PRBS test	0
			1	Enable PRBS test	
	D4	SLEEP	0	Normal mode (default value depends on CDS and MS pin values at power-up)	0, 1
			1	Activate sleep mode (default value depends on CDS and MS pin values at power-up)	
	D[3:2]	INTTYPE	00	Base mode uses I²C peripheral interface	00
			01	Base mode uses UART peripheral interface	
			10, 11	Base mode peripheral interface disabled	
	D1	REVCCEN	0	Disable reverse control channel to serializer (sending)	1
			1	Enable reverse control channel to serializer (sending)	
	D0	FWDCCEN	0	Disable forward control channel from serializer (receiving)	1
			1	Enable forward control channel from serializer (receiving)	
0x05	D7	I2CMETHOD	0	I²C conversion sends the register address	0
			1	Disable sending of I²C register address (command-byte-only mode)	
	D[6:5]	HPFTUNE	00	7.5MHz equalizer highpass cutoff frequency	01
			01	3.75MHz cutoff frequency	
			10	2.5MHz cutoff frequency	
			11	1.87MHz cutoff frequency	
	D4	PDHF	0	High-frequency boosting enabled	0
			1	High-frequency boosting disabled	
	D[3:0]	EQTUNE	0000	2.1dB equalizer boost gain	0100, 1001
			0001	2.8dB equalizer boost gain	
			0010	3.4dB equalizer boost gain	
			0011	4.2dB equalizer boost gain	
			0100	5.2dB equalizer boost gain. **Power-up default when EQS = high.**	
			0101	6.2dB equalizer boost gain	
			0110	7dB equalizer boost gain	
			0111	8.2dB equalizer boost gain	
			1000	9.4dB equalizer boost gain	
			1001	10.7dB equalizer boost gain. **Power-up default when EQS = low.**	
			1010	11.7dB equalizer boost gain	
			1011	13dB equalizer boost gain	
			11XX	Do not use	

Table 16. GMSL Core Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x06	D7	—	0	Reserved	0
	D6	AUTORST	0	Do not automatically reset error registers and outputs	0
			1	Automatically reset error registers and outputs	
	D5	DISINT	0	Enable interrupt transmission to serializer	0
			1	Disable interrupt transmission to serializer	
	D4	INT	0	INT input = low (read only)	0 (read only)
			1	INT input = high (read only)	
	D3	GPIO1OUT	0	Output low to GPIO1	1
			1	Output high to GPIO1	
	D2	GPIO1	0	GPIO1 is low	1 (read only)
			1	GPIO1 is high	
	D1	GPIO0OUT	0	Output low to GPIO0	1
			1	Output high to GPIO0	
	D0	GPIO0	0	GPIO0 is low	1 (read only)
			1	GPIO0 is high	
0x07	D[7:0]	—	01010100	Reserved	01010100
0x08	D[7:2]	—	00110000	Reserved	001100
	D1	DISVSFILT	0	VSYNC glitch filter active	0
			1	VSYNC glitch filter disabled	
	D0	DISHSFILT	0	HSYNC glitch filter active	0
			1	HSYNC glitch filter disabled	
0x09	D[7:0]	—	11001000	Reserved	11001000
0x0A	D[7:0]	—	00010010	Reserved	00010010
0x0B	D[7:0]	—	00100000	Reserved	00100000
0x0C	D[7:0]	ERRTHR	XXXXXXXX	Error threshold for decoding errors $\overline{ERR}$ = low when DECERR > ERRTHR	00000000
0x0D	D[7:0]	DECERR	XXXXXXXX	Decoding error counter This counter remains zero while the device is in PRBS test mode	00000000 (read only)
0x0E	D[7:0]	PRBSERR	XXXXXXXX	PRBS error counter	00000000 (read only)
0x12	D7	MCLKSRC	0	MCLK derived from TXCLKOUT_ (see Table 5)	0
			1	MCLK derived from internal oscillator	
	D[6:0]	MCLKDIV	0000000	MCLK disabled	0000000
			XXXXXXX	MCLK divider	
0x13	D[7:5]	—	XXX	Reserved	(read only)
	D[4:0]	—	10000	Reserved	10000

Table 16. GMSL Core Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x14	D7	INVVSYNC	0	Deserializer does not invert VSYNC	0
			1	Deserializer inverts VSYNC	
	D6	INVHSYNC	0	Deserializer does not invert HSYNC	0
			1	Deserializer inverts HSYNC	
	D5	FORCELVDS	0	Normal operation	0
			1	Force LVDS outputs low	
	D4	DCS	0	Normal driver current for CMOS outputs (WS, SCK, SD/CNTL0, CNTL1, CNTL2/MCLK)	0
			1	Strong driver current for CMOS outputs (WS, SCK, SD/CNTL0, CNTL1, CNTL2/MCLK)	
	D3	DISCNTL1	0	Serial-data bit 27 is mapped to CNTL1	1
			1	CNTL1 forced low	
	D2	DISRES	0	Serial-data bit 27 is mapped to RES	0
			1	RES bit forced low	
	D[1:0]	ILVDS	00	1.75mA LVDS current	01
			01	3.5mA LVDS current	
			10	Do not use	
			11	7mA LVDS current	
0x1E	D[7:0]	ID	00001000	Device identifier (MAX9266 = 0x08)	00001000 (read only)
0x1F	D[7:5]	—	000	Reserved	000 (read only)
	D4	CAPS	0	Not HDCP capable	1 (read only)
			1	HDCP capable	
	D[3:0]	REVISION	XXXX	Device revision	(read only)

X = Don't care.

Table 17. HDCP Register Table (see Table 1)

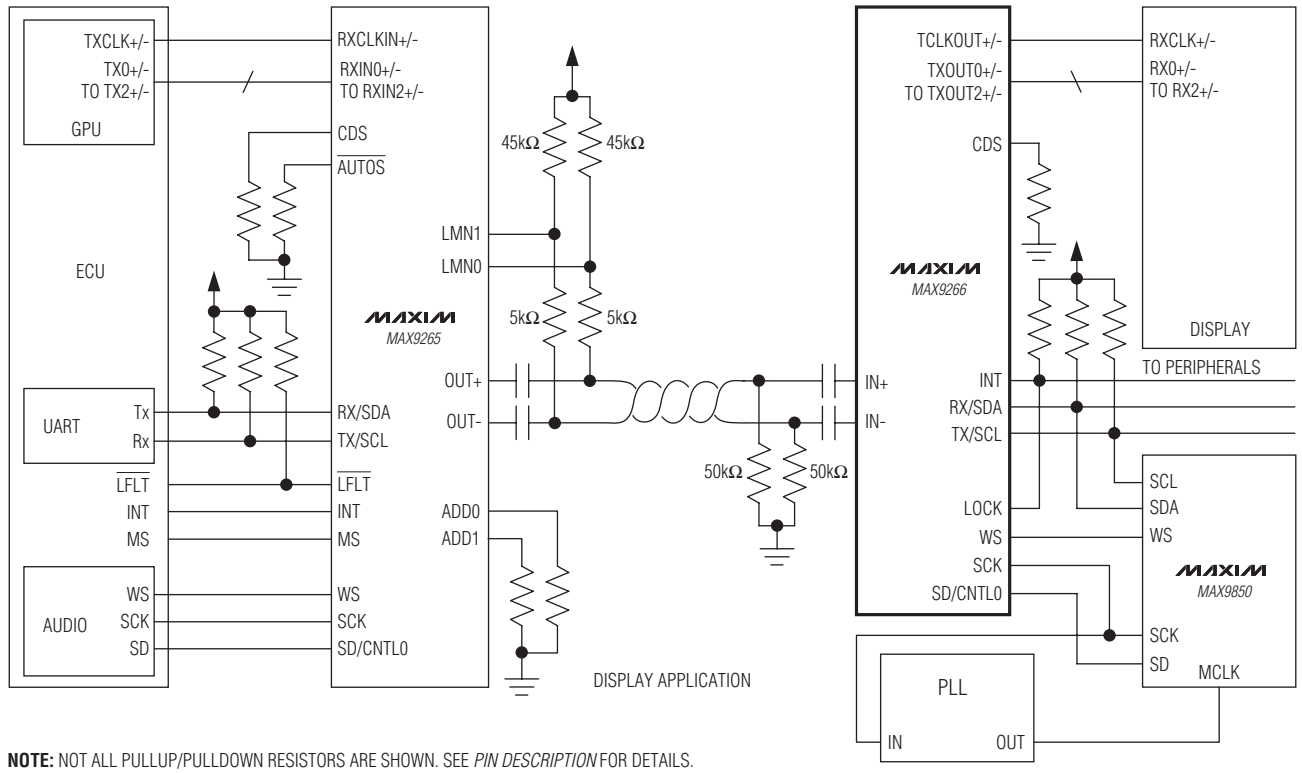
REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x80 to 0x84	5	BKSV	Read only	HDCP receiver KSV	(Read only)
0x85 to 0x86	2	RI'	Read only	Link verification response	(Read only)
0x87	1	PJ'	Read only	Enhanced link verification response	(Read only)
0x88 to 0x8F	8	AN	Read/Write	Session random number	0x0000000000000000
0x90 to 0x94	5	AKSV	Read/Write	HDCP transmitter KSV	0x0000000000
0x95	1	BCTRL	Read/Write	D7 = PD_HDCP 1 = Power down HDCP circuits 0 = HDCP circuits normal	0x00
				D[6:4] = Reserved	
				D3 = GPIO1_FUNCTION 1 = GPIO1 mirrors AUTH_STARTED 0 = Normal GPIO1 operation	
				D2 = GPIO0_FUNCTION 1 = GPIO0 mirrors ENCRYPTION_ENABLE 0 = Normal GPIO0 operation	
				D1 = AUTH_STARTED 1 = Authentication started (triggered by write to AKSV) 0 = Authentication not started	
				D0 = ENCRYPTION_ENABLE 1 = Enable encryption 0 = Disable encryption	
0x96	1	BSTATUS	Read/Write	D[7:2] = Reserved	0x00
				D1 = NEW_DEV_CONN 1 = Set to 1 if a new connected device is detected 0 = Set to 0 if no new device is connected	
				D0 = KSV_LIST_READY 1 = Set to 1 if KSV list and BINFO is ready 0 = Set to 0 if KSV list or BINFO is not ready	
0x97	1	BCAPS	Read/Write	D[7:1] = Reserved	0x00
				D0 = REPEATER 1 = Set to 1 if device is a repeater 0 = Set to 0 if device is not a repeater	
0x98 to 0x9F	8	—	Read Only	Reserved	0x0000000000000000 (read only)

Table 17. HDCP Register Table (see Table 1) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0xA0 to 0xA3	4	V'.H0	Read/Write	H0 part of SHA-1 hash value	0x00000000
0xA4 to 0xA7	4	V'.H1	Read/Write	H1 part of SHA-1 hash value	0x00000000
0xA8 to 0xAB	4	V'.H2	Read/Write	H2 part of SHA-1 hash value	0x00000000
0xAC to 0xAF	4	V'.H3	Read/Write	H3 part of SHA-1 hash value	0x00000000
0xB0 to 0xB3	4	V'.H4	Read/Write	H4 part of SHA-1 hash value	0x00000000
0xB4 to 0xB5	2	BINFO	Read/Write	D[15:12] = Reserved	0x0000
				D11 = MAX_CASCADE_EXCEEDED 1 = Set to 1 if more than seven cascaded devices attached 0 = Set to 0 if seven or fewer cascaded devices attached	
				D[10:8] = DEPTH Depth of cascaded devices	
				D7 = MAX_DEVS_EXCEEDED 1 = Set to 1 if more than 14 devices attached 0 = Set to 0 if 14 or fewer devices attached	
				D[6:0] = DEVICE_COUNT Number of devices attached	
0xB6	1	GPMEM	Read/Write	General-purpose memory byte	0x00
0xB7 to 0xB9	3	—	Read only	Reserved	0x000000
0xBA to 0xFF	70	KSV_LIST	Read/Write	List of KSV's downstream repeaters and receivers (maximum of 14 devices)	All zero

HDCP Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

Typical Application Circuit



NOTE: NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE *PIN DESCRIPTION* FOR DETAILS.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFP-EP	C48E+8	21-0065	90-0138

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9266GCM/V+	-40°C to +105°C	48 TQFP-EP*
MAX9266GCM/V+T	-40°C to +105°C	48 TQFP-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

HDCP Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—