19-0736; Rev 0; 1/07

MAXIM

2:1 Multiplexer and 1:2 Demultiplexer with Loopback

General Description

The MAX9396 consists of a 2:1 multiplexer and a 1:2 demultiplexer with loopback. The multiplexer section (channel B) accepts two differential inputs and generates a single differential output. The demultiplexer section (channel A) accepts a single differential input and generates two parallel differential outputs. The MAX9396 features a loopback mode that connects the input of channel A to the output of channel B and connects the selected input of channel B to the outputs of channel A.

The differential inputs of the MAX9396 accept CML/LVPECL levels and can also accept LVDS inputs with common-mode voltages from +0.6V to (V_{CC} - 0.05V). The differential outputs are LVDS compatible and drive 100Ω loads.

Three LVCMOS/LVTTL logic inputs control the internal connections between inputs and outputs, one for the multiplexer portion of channel B (BSEL), and the other two for loopback control of channels A and B (LB_SELA and LB_SELB). Independent enable inputs for each differential output pair provide additional flexibility.

Fail-safe circuitry forces the outputs to a differential low condition for undriven inputs or when the common-mode voltage is below +0.6V.

Ultra-low 57ps_{P-P} (typ) pseudorandom bit sequence (PRBS) jitter ensures reliable communications in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery, or serializers and deserializers. The high-speed switching performance guarantees 1.25Gbps operation and less than 87ps (max) skew between channels.

The MAX9396 is available in a 32-pin TQFP package and is specified over the -40°C to +85°C extended temperature range.

Applications

High-Speed Telecom/Datacom Equipment

Central Office Backplane Clock Distribution

DSLAMs

Protection Switching

Fault-Tolerant Systems

Pin Configuration and Functional Diagram appear at end of data sheet.

Features

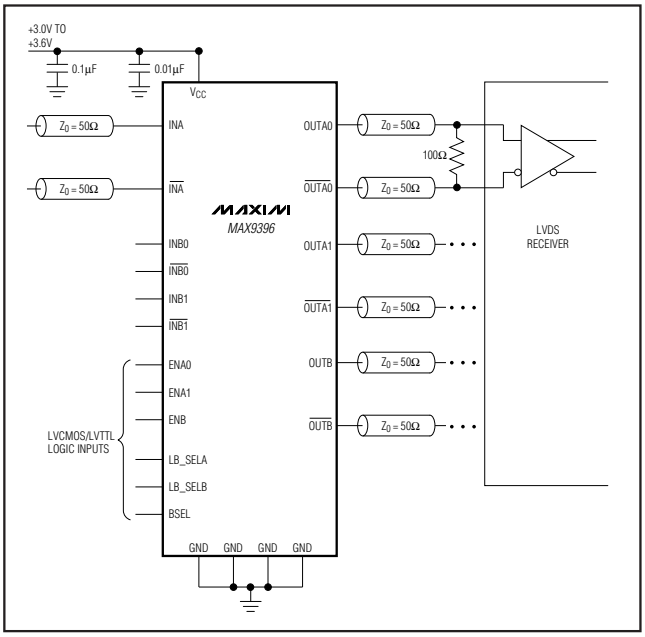
- **Guaranteed 1.25Gbps Operation with 450mV (min) Differential Output Swing**
- **Integrated 100Ω Resistors on Differential Inputs**
- **Simultaneous Loopback Control**
- **2$ps_{(RMS)}$ (max) Random Jitter**
- **AC Specifications Guaranteed for 150mV Differential Input**
- **Signal Inputs Accept Any Differential Signals with V_{CM} = +0.6V to (V_{CC} - 0.05V)**
- **LVDS Outputs for Clock or High-Speed Data**
- **Low-Level Input Fail-Safe Detection**
- **+3.0V to +3.6V Supply Voltage Range**
- **LVCMOS/LVTTL Logic Inputs**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9396EHJ+	-40°C to +85°C	32 TQFP	H32-1

+Denotes a lead-free package.

Typical Operating Circuit



2:1 Multiplexer and 1:2 Demultiplexer with Loopback

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.1V
IN_ _, $\overline{IN}$_ _, OUT_ _, $\overline{OUT}$_ _, EN_ _, BSEL, LB_SEL_
to GND.....-0.3V to (V_{CC} + 0.3V)
IN_ _ to $\overline{IN}$_ _.....±3V
Short-Circuit Duration (OUT_ _, $\overline{OUT}$_ _) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFP (derate 13.1mW/°C above +70°C).....1047mW
Junction-to-Ambient Thermal Resistance in Still Air
32-Pin TQFP.....+76.4°C/W

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection (Human Body Model)
(IN_ _, $\overline{IN}$_ _, OUT_ _, $\overline{OUT}$_ _, EN_ _, BSEL, LB_SEL_)..±2kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, EN_ _ = V_{CC}, V_{CM} = +0.6V to (V_{CC} - 0.05V), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.2V, T_A = +25°C.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVCMOS/LVTTL INPUTS (EN_ _, BSEL, LB_SEL_)						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		0		0.8	V
Input High Current	I_{IH}	V_{IN} = +2.0V to V_{CC}	0		20	µA
Input Low Current	I_{IL}	V_{IN} = 0V to +0.8V	-1		+10	µA
DIFFERENTIAL INPUTS (IN_ _, $\overline{IN}$_ _)						
Differential Input Voltage	V_{ID}	$V_{ILD} \geq$ 0V and $V_{IHD} \leq V_{CC}$, Figure 1	0.1		3.0	V
Input Common-Mode Range	V_{CM}		0.6		V_{CC} - 0.05	V
Single-Ended Input Current	$I_{IN\_\_}$, $I_{\overline{IN}\_\_}$	$\|V_{ID}\| \leq$ 3.0V (V_{IN} = 0V to +V_{CC}, IN_ _, or $\overline{IN}$_ _ open)	-15		+200	µA
Differential Input Termination	R_{IN}	IN_ _ to $\overline{IN}$_ _	80	100	120	Ω
LVDS OUTPUTS (OUT_ _, $\overline{OUT}$_ _)						
Differential Output Voltage	V_{OD}	R_L = 100Ω, Figure 2	450	540	600	mV
Change in Magnitude of V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 2			50	mV
Offset Common-Mode Voltage	V_{OS}	Figure 2	1.4	1.5	1.6	V
Change in Magnitude of V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 2			50	mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, EN_ _ = V_{CC}, V_{CM} = +0.6V to (V_{CC} - 0.05V), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.2V, T_A = +25°C.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current (Output(s) Shorted to GND)	$\|I_{OS}\|$	V_{ID} = ±100mV (Note 4)	$V_{OUT\_\_}$ or $V_{\overline{OUT}\_\_}$ = 0V		28	40	mA
			$V_{OUT\_\_}$ = $V_{\overline{OUT}\_\_}$ = 0V		17	24	
Output Short-Circuit Current (Outputs Shorted Together)	$\|I_{OSB}\|$	V_{ID} = ±100mV, $V_{OUT\_\_}$ = $V_{\overline{OUT}\_\_}$ (Note 4)				12	mA
SUPPLY CURRENT							
Supply Current	I_{CC}	R_L = 100Ω, EN_ _ = V_{CC}			56	75	mA
		R_L = 100Ω, EN_ _ = V_{CC}, switching at 625MHz (1.25Gbps)			56	75	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, $f_{IN} \le$ 625MHz, t_{R_IN} = t_{F_IN} = 125ps, R_L = 100Ω ±1%, $|V_{ID}| \ge$ 150mV, V_{CM} = +0.6V to (V_{CC} - 0.075V), EN_ _ = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.2V, f_{IN} = 625MHz, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEL to Switched Output	t_{SWITCH}	Figure 3			1.1	ns
Disable Time to Differential Output Low	t_{PHD}	Figure 4			1.7	ns
Enable Time to Differential Output High	t_{PDH}	Figure 4			1.7	ns
Data Rate	f_{DR}	$V_{OD} \ge$ 450mV, 2^{23} - 1 PRBS	1.25			Gbps
Low-to-High Propagation Delay	t_{PLH}	Figures 1, 5	250	340	630	ps
High-to-Low Propagation Delay	t_{PHL}	Figures 1, 5	250	355	630	ps
Pulse Skew $\|t_{PLH} - t_{PHL}\|$	t_{SKEW}	Figures 1, 5 (Note 6)		18	86	ps
Output Channel-to-Channel Skew	t_{CCS}	Figure 6 (Note 7)			87	ps
Output Low-to-High Transition Time (20% to 80%)	t_R	$f_{IN\_\_}$ = 100MHz, Figures 1, 5	170	220	350	ps
Output High-to-Low Transition Time (80% to 20%)	t_F	$f_{IN\_\_}$ = 100MHz, Figures 1, 5	170	210	350	ps
Added Random Jitter	t_{RJ}	$f_{IN\_\_}$ = 625MHz, clock pattern (Note 8)		0.45	2	$ps_{(RMS)}$
Added Deterministic Jitter	t_{DJ}	1.25Gbps, 2^{23} - 1 PRBS (Note 8)		57	120	ps_{P-P}

Note 1: Measurements obtained with the device in thermal equilibrium. All voltages referenced to GND except V_{ID}, V_{OD}, and ΔV_{OD}.

Note 2: Current into the device defined as positive. Current out of the device defined as negative.

Note 3: DC parameters are production tested at T_A = +25°C and guaranteed by design and characterization for T_A = -40°C to +85°C.

Note 4: Current through either output.

Note 5: Guaranteed by design and characterization. Limits set at ±6 sigma.

Note 6: t_{SKEW} is the magnitude difference of differential propagation delays for the same output over the same condtions. $t_{SKEW} = |t_{PHL} - t_{PLH}|$.

Note 7: Measured between outputs of the same device at the signal crossing points for a same-edge transition under the same conditions. Does not apply to loopback mode.

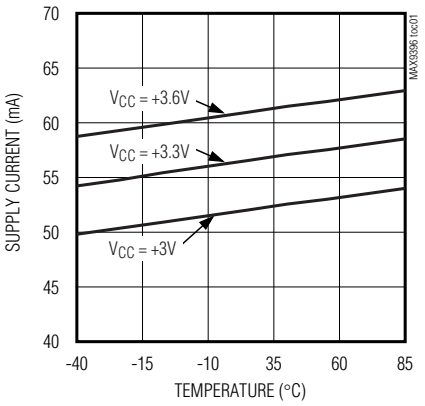
Note 8: Device jitter added to the differential input signal.

2:1 Multiplexer and 1:2 Demultiplexer with Loopback

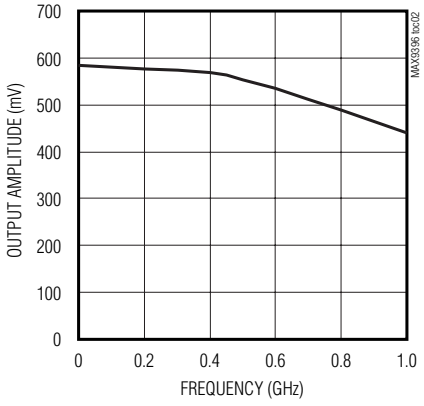
Typical Operating Characteristics

(V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.2V, T_A = +25°C, f_{IN} = 6.25MHz, Figure 5.)

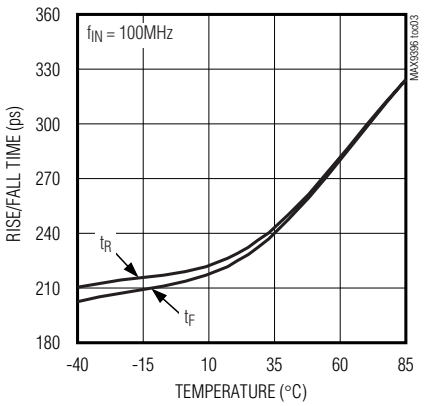
SUPPLY CURRENT vs. TEMPERATURE



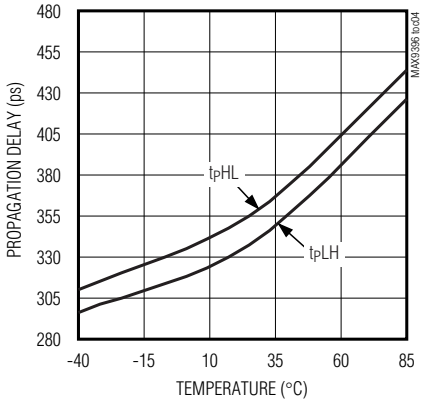
OUTPUT AMPLITUDE vs. FREQUENCY



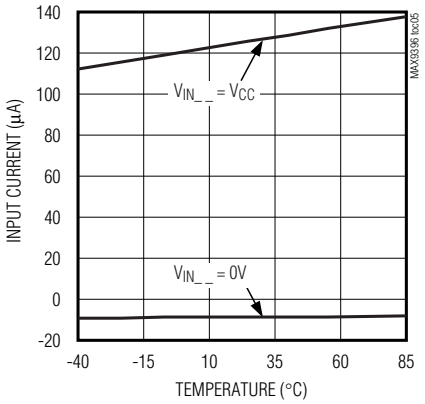
OUTPUT RISE/FALL TIME vs. TEMPERATURE



PROPAGATION DELAY vs. TEMPERATURE



SINGLE-ENDED INPUT CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 2, 3, 30, 31, 32	N.C.	No Connection. Not internally connected.
4, 9, 20, 25	GND	Ground
5	ENB	Channel B Output Enable. Drive ENB high to enable the LVDS outputs for channel B. An internal 435kΩ resistor to GND pulls ENB low when unconnected.
6	OUTB	Channel B LVDS Noninverting Output
7	$\overline{OUTB}$	Channel B LVDS Inverting Output
8, 13, 24, 29	V_{CC}	Power-Supply Input. Bypass each V_{CC} to GND with a 0.1µF and 0.01µF ceramic capacitor. Install both bypass capacitors as close as possible to the device, with the 0.01µF capacitor closest to the device.
10	$\overline{INB0}$	LVPECL/CML Inverting Input. An internal 68kΩ resistor to GND pulls the input low when unconnected.
11	INB0	LVPECL/CML Noninverting Input. An internal 68kΩ resistor to GND pulls the input low when unconnected.
12	LB_SELB	Loopback Select for Channel B Output. Connect LB_SELB to GND or leave unconnected to reproduce the INB_ ($\overline{INB\_}$) differential inputs at OUTB ($\overline{OUTB}$). Connect LB_SELB to V_{CC} to loop back the INA ($\overline{INA}$) differential inputs to OUTB ($\overline{OUTB}$). An internal 435kΩ resistor to GND pulls LB_SELB low when unconnected.
14	$\overline{INB1}$	LVPECL/CML Inverting Input. An internal 68kΩ resistor to GND pulls the input low when unconnected.
15	INB1	LVPECL/CML Noninverting Input. An internal 68kΩ resistor to GND pulls the input low when unconnected.
16	BSEL	Channel B Multiplexer Control Input. Selects the differential input to reproduce at the B channel differential output. Connect BSEL to GND or leave unconnected to select the INB0 ($\overline{INB0}$) set of inputs. Connect BSEL to V_{CC} to select the INB1 ($\overline{INB1}$) set of inputs. An internal 435kΩ resistor to GND pulls BSEL low when unconnected.
17	ENA1	Channel A1 Output Enable. Drive ENA1 high to enable the A1 LVDS outputs. An internal 435kΩ resistor to GND pulls the ENA1 low when unconnected.
18	$\overline{OUTA1}$	Channel A1 LVDS Inverting Output
19	OUTA1	Channel A1 LVDS Noninverting Output

2:1 Multiplexer and 1:2 Demultiplexer with Loopback

Pin Description (continued)

PIN	NAME	FUNCTION
21	ENA0	Channel A0 Output Enable. Drive ENA0 high to enable the A0 LVDS outputs. An internal 435kΩ resistor to GND pulls ENA0 low when unconnected.
22	$\overline{OUTA0}$	Channel A0 LVDS Inverting Output
23	OUTA0	Channel A0 LVDS Noninverting Output
26	INA	LVPECL/CML Noninverting Input. An internal 68kΩ resistor to GND pulls the input low when unconnected.
27	$\overline{INA}$	LVPECL/CML Inverting Input. An internal 68kΩ resistor to GND pulls the input low when unconnected.
28	LB_SELA	Loopback Select for Channel A Output. Connect LB_SELA to GND or leave unconnected to reproduce the INA ($\overline{INA}$) differential inputs at OUTA_ ($\overline{OUTA\_}$). Connect LB_SELA to V_{CC} to loop back the INB_ ($\overline{INB\_}$) differential inputs to OUTA_ ($\overline{OUTA\_}$). An internal 435kΩ resistor to GND pulls LB_SELA low when unconnected.

Detailed Description

The MAX9396 high-speed, low-power 2:1 multiplexer and 1:2 demultiplexer with loopback provides signal redundancy switching in telecom and storage applications. This device selects one of two remote signal sources for local input and buffers a single local output signal to two remote receivers.

The multiplexer section (channel B) accepts two differential inputs and generates a single LVDS-compatible output. The demultiplexer section (channel A) accepts a single differential input and generates two parallel LVDS-compatible outputs. The MAX9396 features a loopback mode that connects the input of channel A to the output of channel B and connects the selected input of channel B to the outputs of channel A. LB_SELA and LB_SELB provide independent loopback control for each channel.

Three LVCMOS/LVTTL logic inputs control the internal connections between inputs and outputs, one for the multiplexer portion of channel B (BSEL), and the other two for loopback control of channels A and B (LB_SELA and LB_SELB). Independent enable inputs for each differential output pair provide additional flexibility.

Input Fail-Safe

The differential inputs of the MAX9396 possess internal fail-safe protection. Fail-safe circuitry forces the outputs to a differential-low condition for undriven inputs or when the common-mode voltage is below +0.6V. The MAX9396 provides low-level input fail-safe detection for LVPECL, CML, and other V_{CC}-referenced differential inputs.

Select Function

BSEL selects the differential input pair to transmit through OUTB ($\overline{OUTB}$) for LB_SELB = GND or through OUTA_ ($\overline{OUTA\_}$) for LB_SELA = V_{CC}. LB_SEL_ controls the loopback function for each channel. Connect LB_SEL_ to GND to select the normal inputs for each channel. Connect LB_SEL_ to V_{CC} to enable the loopback function. The loopback function routes the input of channel A to the output of channel B, and the inputs of channel B to the outputs of channel A. See Tables 1 and 2 for a summary of the input/output routing between channels.

Enable Function

The EN_ _ logic inputs enable and disable each set of differential outputs. For example, connect ENA0 to V_{CC} to enable the OUTA0/$\overline{OUTA0}$ differential output pair or connect ENA0 to GND to disable the OUTA0/$\overline{OUTA0}$ differential output pair. The differential output pairs assert to a differential low condition when disabled.

Applications Information

Differential Inputs

The MAX9396 inputs accept any differential signaling standard within the specified common-mode voltage range. The fail-safe feature detects common-mode input signal levels and generates a differential output low condition for undriven inputs or when the common-mode voltage is below +0.6V. Leave unused inputs unconnected or connect to GND.

Power-Supply Bypassing

Bypass each V_{CC} to GND with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close as possible to the device. Install the 0.01µF capacitor closest to the device.

Differential Traces

Input and output trace characteristics affect the performance of the MAX9396. Connect each input and output to a 50Ω characteristic impedance trace. Maintain the distance between differential traces and eliminate sharp corners to avoid discontinuities in differential impedance and maximize common-mode noise immunity. Minimize the number of vias on the differential input and output traces to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Minimize skew by matching the electrical length of the traces.

Output Termination

Terminate the transmission line with a 100Ω resistor at the receiver inputs for proper operation.

Ensure that the output currents do not exceed the current limits specified in the *Absolute Maximum Ratings*. Observe the total thermal limits of the MAX9396 under all operating conditions.

Cables and Connectors

Use matched differential impedance for transmission media. Use cables and connectors with matched differential impedance to minimize impedance discontinuities. Avoid the use of unbalanced cables.

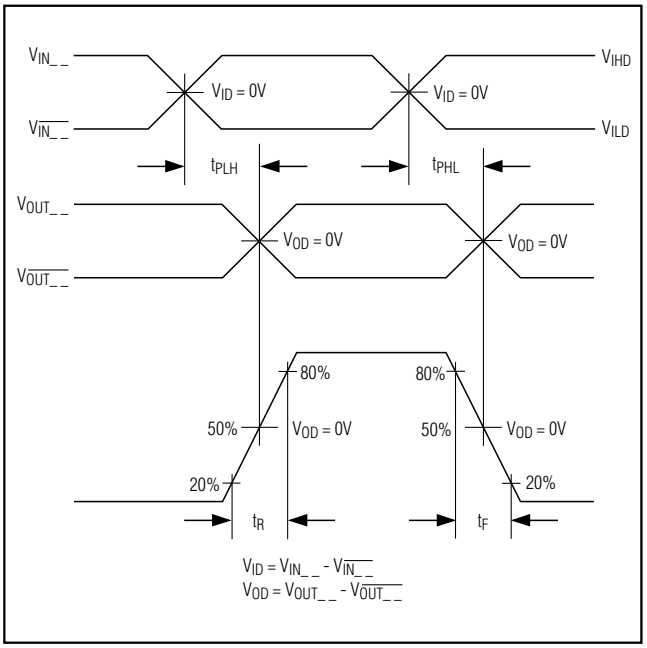


Figure 1. Output Transition Time and Propagation Delay Timing Diagram

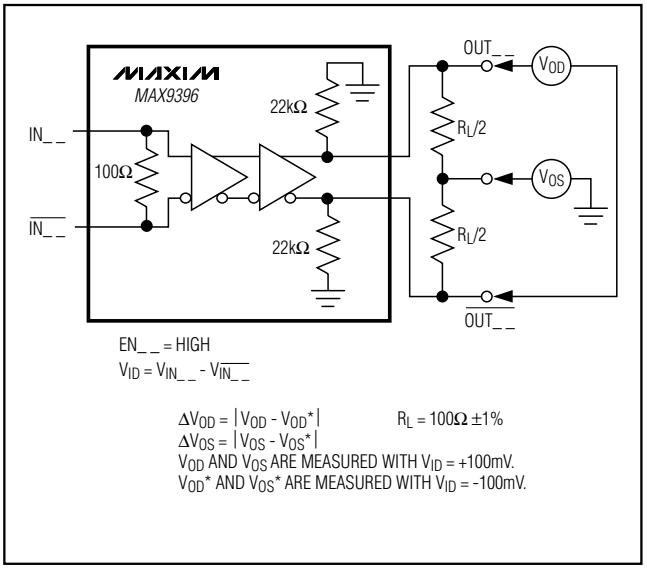


Figure 2. Test Circuit for V_{OD} and V_{OS}

Balanced cables, such as twisted pair, offer superior signal quality and tend to generate less EMI due to canceling effects.

2:1 Multiplexer and 1:2 Demultiplexer with Loopback

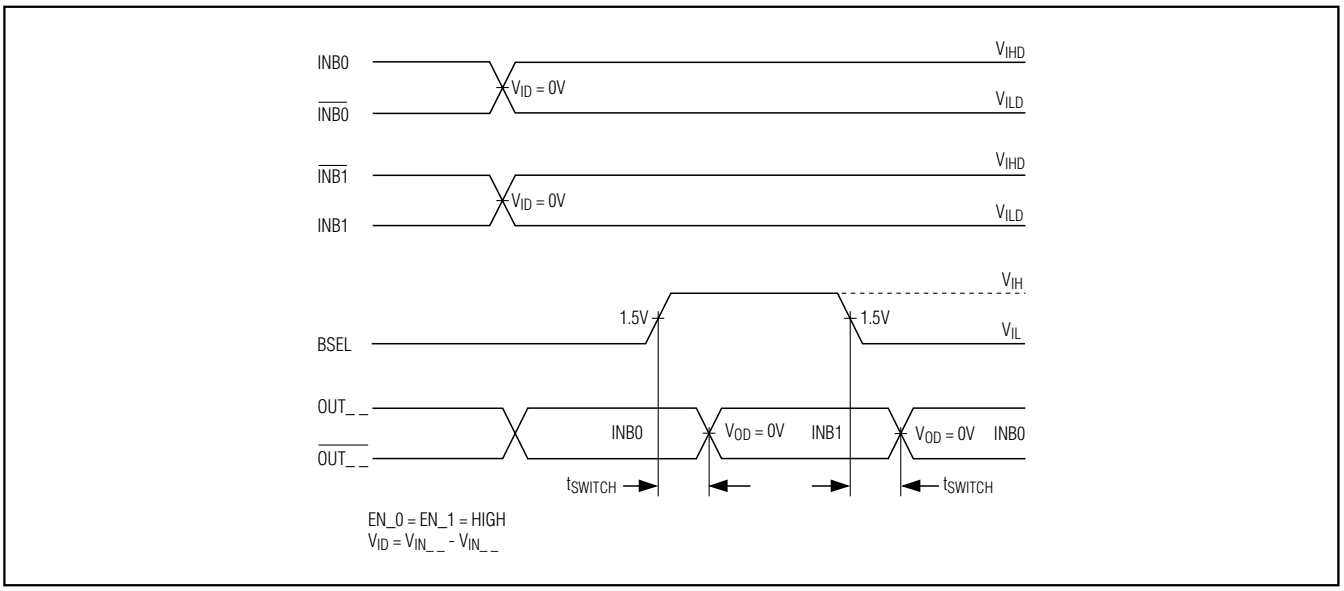


Figure 3. Input to Rising/Falling Edge Select and Mux Switch Timing Diagram

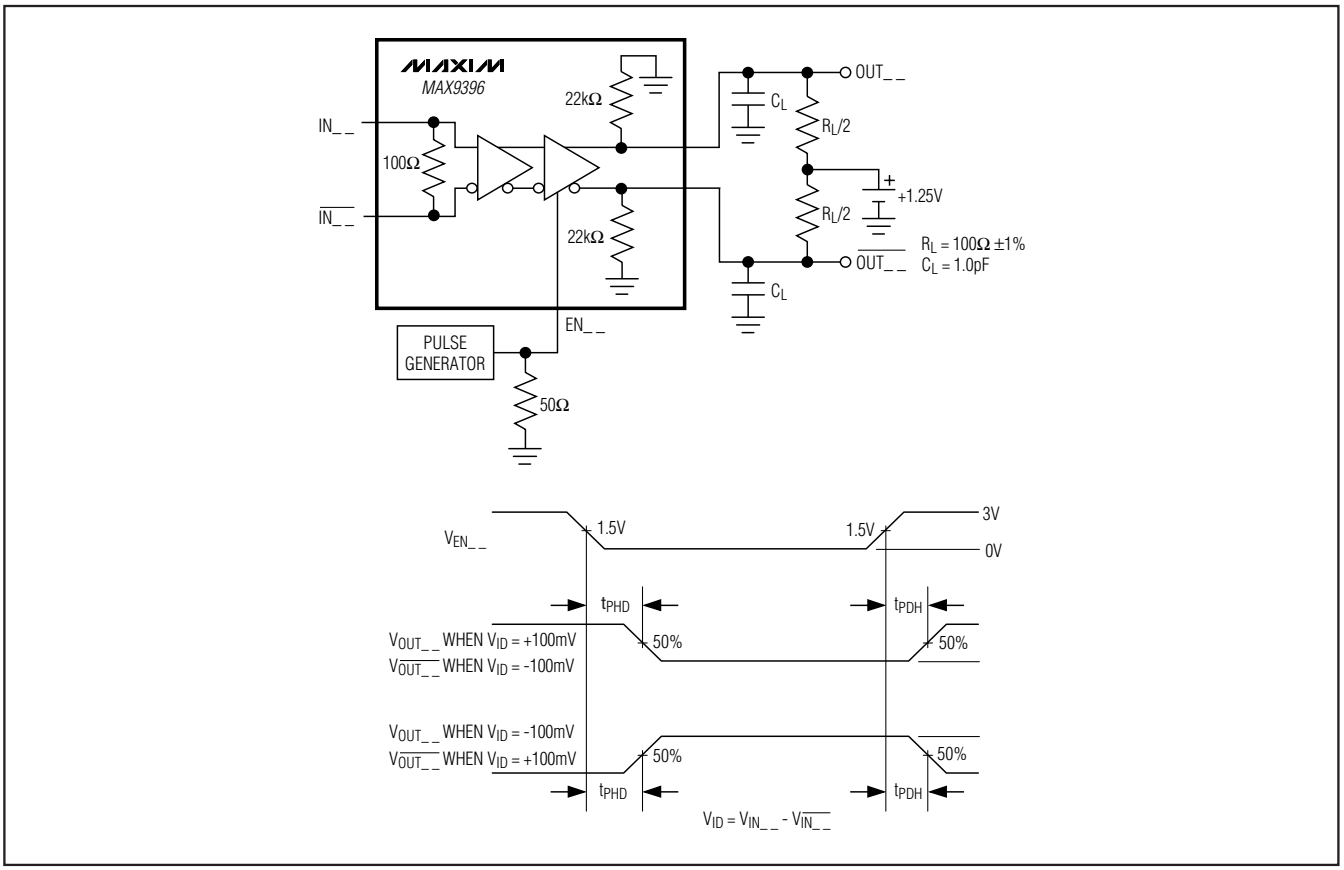


Figure 4. Output Active-to-Disable and Disable-to-Active Test Circuit and Timing Diagram

Table 1. Input Select Truth Table

LOGIC INPUTS			DIFFERENTIAL OUTPUTS	
LB_SELA	LB_SELB	BSEL	OUTA_ / $\overline{OUTA\_}$	OUTB / $\overline{OUTB}$
0	0	0	INA selected	INB0 selected
0	0	1	INA selected	INB1 selected
0	1	X	INA selected	INA selected
1	0	0	INB0 selected	INB0 selected
1	0	1	INB1 selected	INB1 selected
1	1	0	INB0 selected	INA selected
1	1	1	INB1 selected	INA selected

X = Don't care.

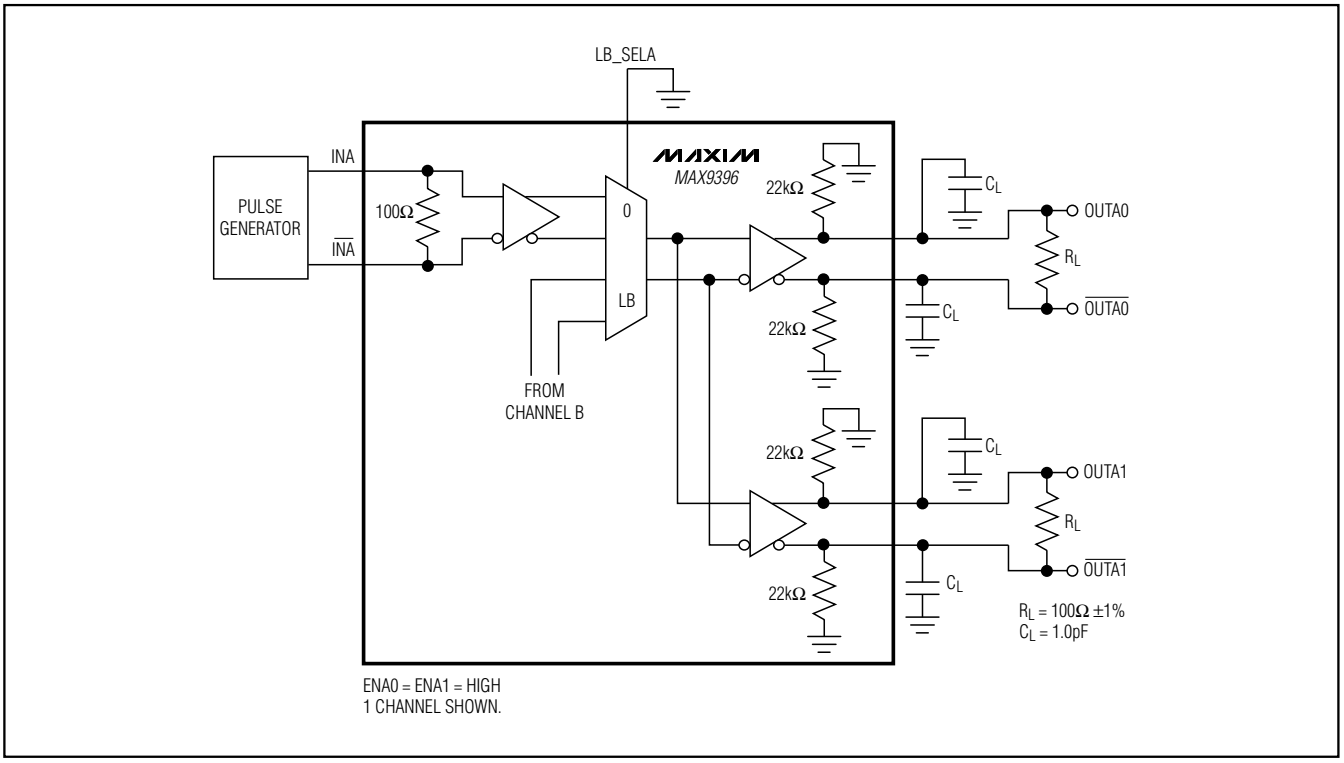


Figure 5. Output Transition Time, Propagation Delay, and Output Channel-to-Channel Skew Test Circuit

PCB Layout

Use a four-layer PCB providing separate signal, power, and ground planes for high-speed signaling applications. Bypass V_{CC} to GND as close as possible to the device. Install termination resistors as close as possible to the receiver inputs. Match the electrical length of the differential traces to minimize signal skew.

Table 2. Loopback Select Truth Table

LB_SEL_	OUT_ _
GND or open	Normal inputs selected.
V_{CC}	Loopback inputs selected.

2:1 Multiplexer and 1:2 Demultiplexer with Loopback

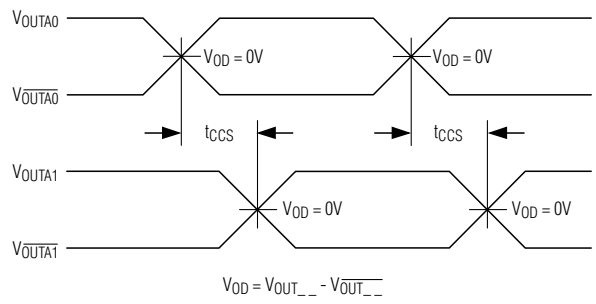
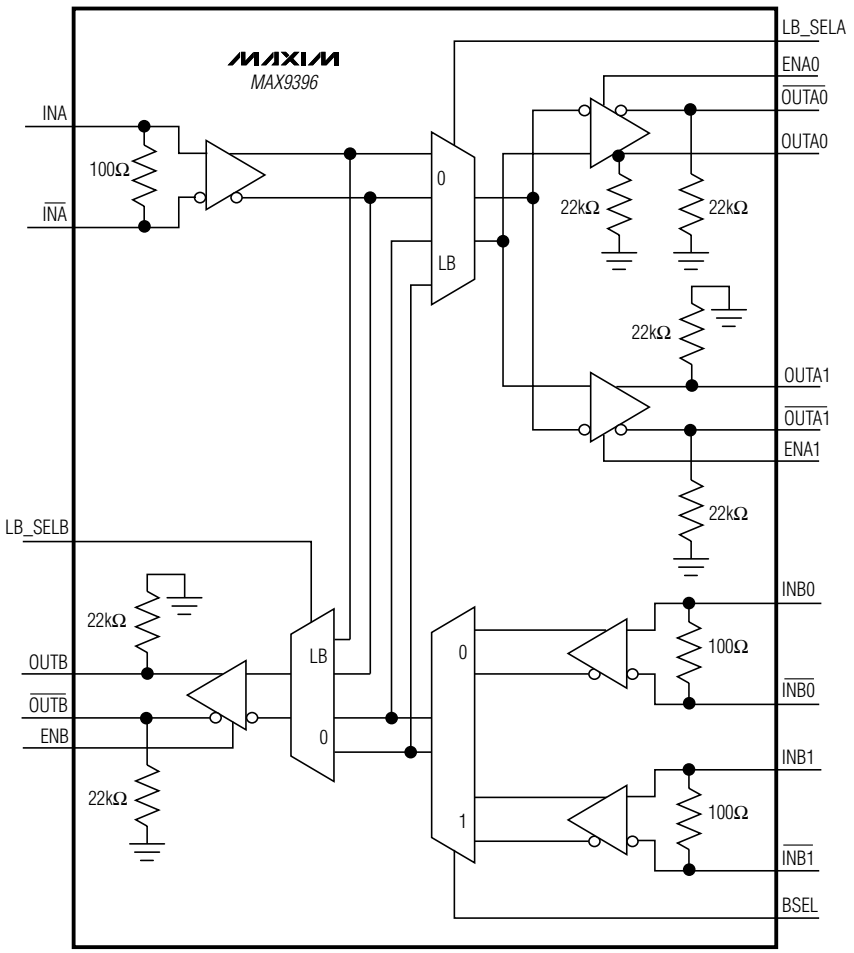


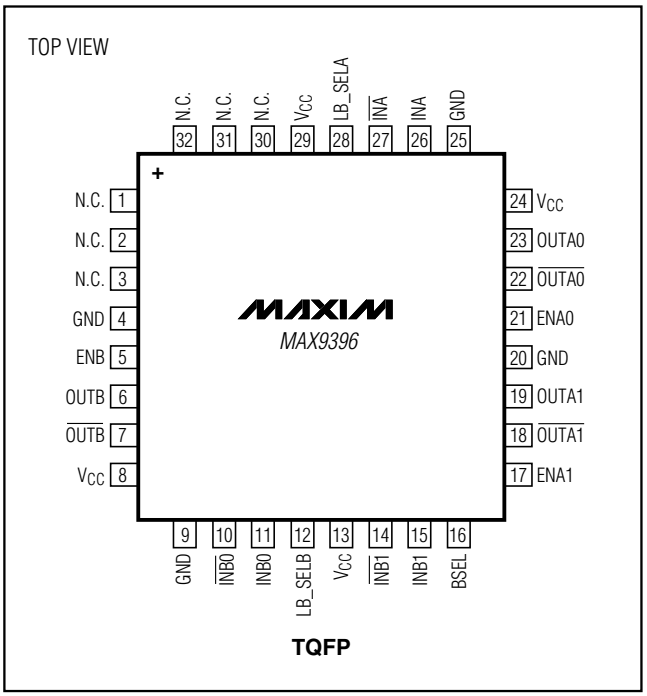
Figure 6. Output Channel-to-Channel Skew

Functional Diagram



2:1 Multiplexer and 1:2 Demultiplexer with Loopback

Pin Configuration



Chip Information

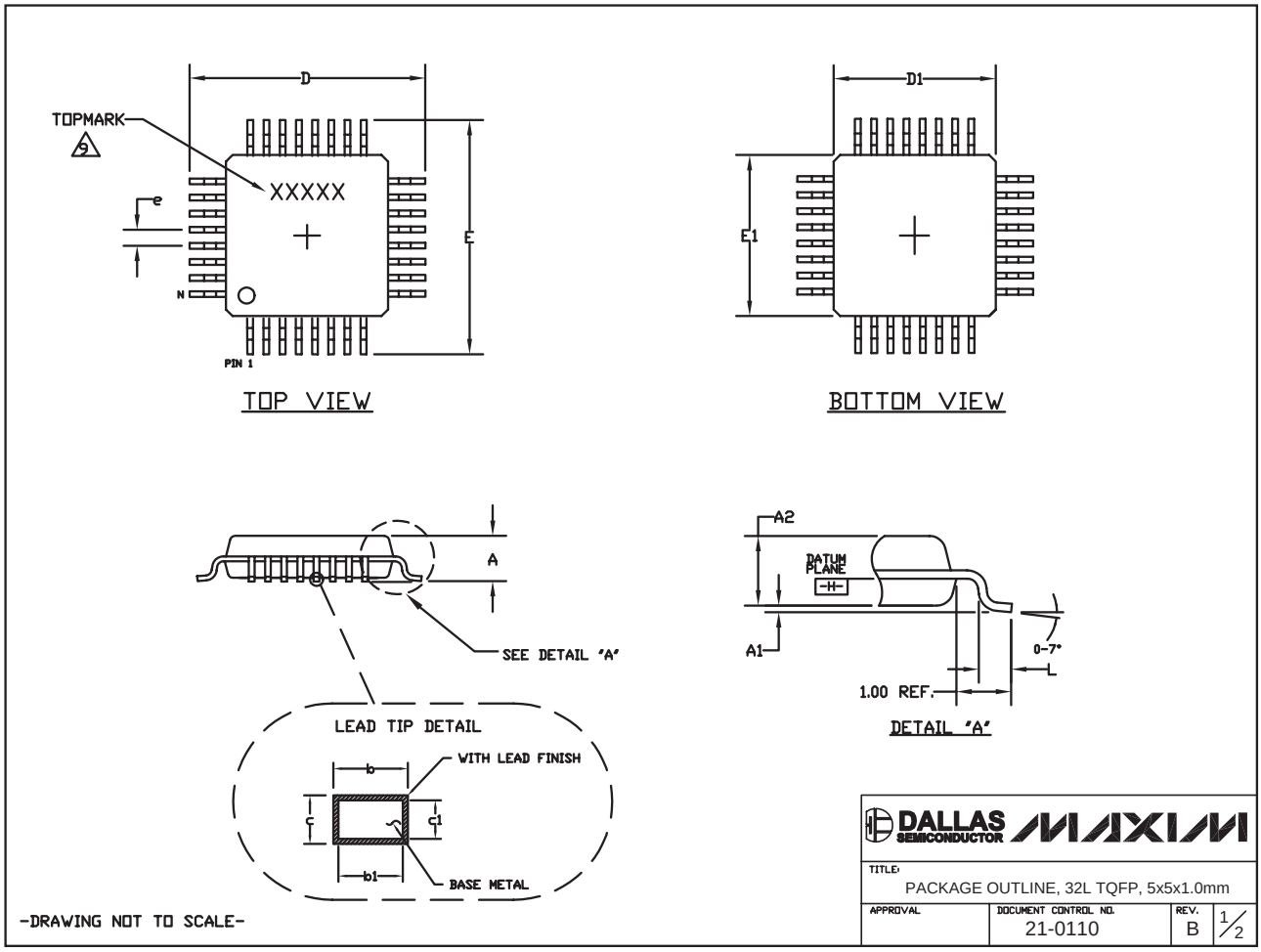
PROCESS: BiCMOS

2:1 Multiplexer and 1:2 Demultiplexer with Loopback

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32L TQFP, 5x5x01.0.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. TOPMARK SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

	JEDEC VARIATIONS DIMENSIONS IN MILLIMETERS	
	AAA	
	5x5x1.0 MM	
	MIN.	MAX.
A		1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	6.80	7.20
D_1	4.80	5.20
E	6.80	7.20
E_1	4.80	5.20
L	0.45	0.75
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 32L TQFP, 5x5x1.0mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0110	B	2/2