19-2245; Rev 0; 10/01

EVALUATION KIT AVAILABLE

Quad ECL/PECL Differential Buffers/Receivers

General Description

The MAX9401/MAX9404 are extremely fast and low-skew quad ECL/PECL differential buffers/receivers for data and clock signals. The four channels can be operated synchronously with an external clock, or in asynchronous mode, determined by the state of the SEL input. An enable input provides the ability to force all the outputs to a differential low state.

The MAX9401 has high-impedance (open) input and the MAX9404 has an integrated 100Ω differential input termination, which reduces external component count. Both devices have double amplitude swing open emitter outputs suitable for driving long cables. The MAX9401/MAX9404 operate over a V_{CC} - V_{EE} = +3.0V to +5.5V supply range, and are specified for operation from -40°C to +85°C. These devices are offered in space-saving 32-pin 5mm x 5mm QFN exposed-paddle (EP) and TQFP packages.

Applications

Data and Clock Driver and Buffer

Central Office Backplane Clock Distribution

DSLAM Backplane

Base Station

ATE

Functional Diagram appears at end of data sheet.

Features

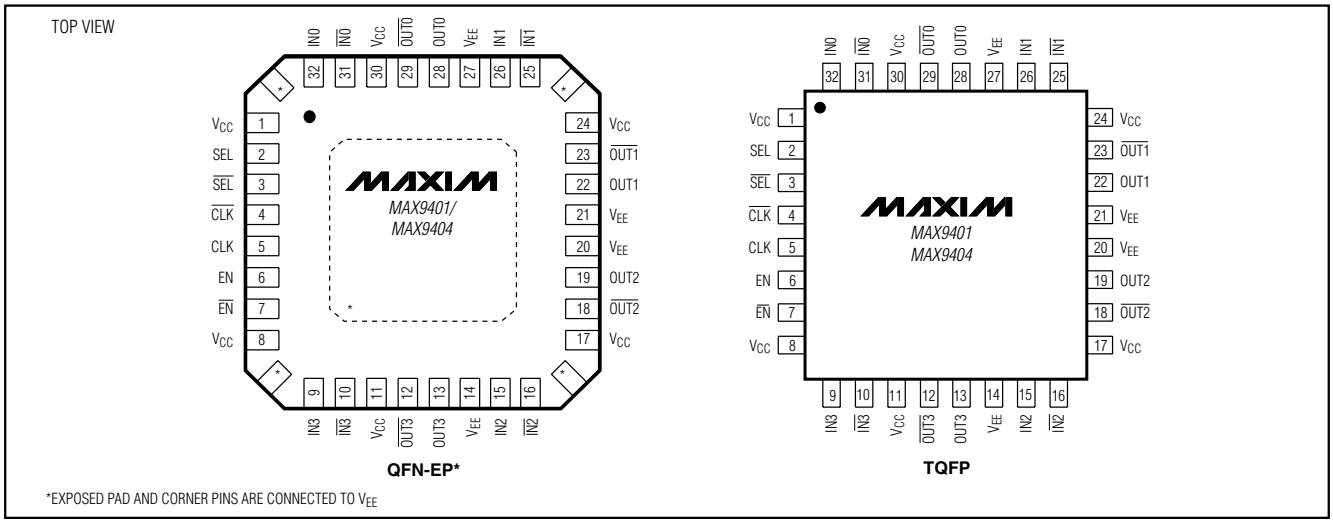
- **Differential Double-Swing ECL/PECL Outputs**
- **Input Compatible with LVECL/LVPECL**
- **Guaranteed 900mV Differential Output at 3.0GHz Clock Rate**
- **365ps Propagation Delay in Asynchronous Mode**
- **10ps Channel-to-Channel Skew in Synchronous Mode**
- **Integrated 100Ω Input Terminations (MAX9404)**
- **Compatible +3.3V/+5.0V Nominal Supplies**
- **Selectable Synchronous/Asynchronous Operation**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INPUT IMPEDANCE
MAX9401EGJ*	-40°C to +85°C	32 QFN-EP** (5mm x 5mm)	Open
MAX9401EHJ	-40°C to +85°C	32 TQFP (5mm x 5mm)	Open
MAX9404EGJ*	-40°C to +85°C	32 QFN-EP** (5mm x 5mm)	100Ω
MAX9404EHJ	-40°C to +85°C	32 TQFP (5mm x 5mm)	100Ω

**Future product—contact factory for availability.*
***EP = Exposed paddle*

Pin Configurations



Quad ECL/PECL Differential Buffers/Receivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to V_{EE} .....-0.3V to +6.0V
All Other Pins to V_{EE}.....-0.3V to (V_{CC} + 0.3V)
Differential Input Voltage…….....±3.0V
Continuous Output Current.....70mA
Surge Output Current…. 100mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin 5mm x 5mm TQFP (derate 9.5mW/°C above +70°C).....761mW
32-Pin 5mm x 5mm QFN-EP (derate 21.3mW/°C above +70°C).....1.7W
Junction-to-Ambient Thermal Resistance in Still Air
32-Pin TQFP.....+105°C/W
32-Pin QFN-EP…. .....+47°C/W
Junction-to-Ambient Thermal Resistance with 500LFPM Airflow
32-Pin TQFP.....+73°C/W
Junction-to-Case Thermal Resistance
32-Pin TQFP.....+25°C/W
32-Pin QFN-EP… .....+2°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (Inputs and Outputs).....>1.25kV
Soldering Temperature (10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +3.0V to +5.5V, outputs terminated with 50Ω ±1% to V_{CC} - 3.3V, inputs are driven, unless otherwise noted. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 0.9V, V_{ILD} = V_{CC} - 1.7V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUTS (IN_, $\overline{IN\_}$, CLK, $\overline{CLK}$, EN, $\overline{EN}$, SEL, $\overline{SEL}$)							
Differential Input High Voltage	V_{IHD}	Figure 3		V_{EE} + 2.0		V_{CC}	V
Differential Input Low Voltage	V_{ILD}	Figure 3		V_{EE}		V_{CC} - 0.2	V
Differential Input Voltage	V_{ID}	Figure 3		0.2		3.0	V
Input Current	I_{IH}, I_{IL}	MAX9401	EN, $\overline{EN}$, SEL, $\overline{SEL}$, IN_, $\overline{IN\_}$, CLK, or $\overline{CLK}$ = V_{IHD} or V_{ILD}	-10		25	µA
		MAX9404	EN, $\overline{EN}$, SEL, $\overline{SEL}$, CLK, or $\overline{CLK}$ = V_{IHD} or V_{ILD}	-10		25	
IN to $\overline{IN}$ Differential Input Resistance	R_{IN}	MAX9404		86		114	Ω
OUTPUTS (OUT_, $\overline{OUT\_}$)							
Differential Output Voltage	V_{OH} - V_{OL}	Figure 3		1.2	1.4		V
Output Common-Mode Voltage	V_{OCM}	Figure 3		V_{CC} - 1.8		V_{CC} - 1.4	V
POWER SUPPLY							
Supply Current	I_{EE}	(Note 4)			84	118	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +3.0V to +5.5V, outputs terminated with 50Ω ±1% to V_{CC} - 3.3V, outputs are enabled, input transition time = 125ps (20% to 80%), f_{CLK} = 3.0GHz, f_{IN} = 1.5GHz, V_{IHD} = V_{EE} +2.0V to V_{CC}, V_{ILD} = V_{EE} to V_{CC} - 0.2V, V_{IHD} - V_{ILD} = 0.2 to 3.0V, unless otherwise noted. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 0.9V, V_{ILD} = V_{CC} - 1.7V, T_A = +25°C, unless otherwise noted.) (Notes 1, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN to OUT Differential Propagation Delay	t_{PLH1}, t_{PHL1}	SEL = high, Figure 4	300	365	550	ps
CLK to OUT Differential Propagation Delay	t_{PLH2}, t_{PHL2}	SEL = low, Figure 5	580	620	758	ps
IN to OUT Channel-to-Channel Skew	t_{SKD1}	SEL = high (Note 6)		15	55	ps
CLK to OUT Channel-to-Channel Skew	t_{SKD2}	SEL = low (Note 6)		10	40	ps
Maximum Clock Frequency	$f_{CLK(MAX)}$	V_{OH} - V_{OL} ≥ 900mV, SEL = low	3.0			GHz
Maximum Data Frequency	$f_{IN(MAX)}$	SEL = high, V_{OH} - V_{OL} ≥ 900mV	1.5			GHz
Added Random Jitter (Note 7)	t_{RJ}	SEL = low, f_{IN} = 1.5GHz, f_{CLK} = 3.0GHz, clock		1.4	2.5	ps (RMS)
		SEL = high, f_{IN} = 1.5GHz		0.9	2.7	
Added Deterministic Jitter (Note 7)	t_{DJ}	SEL = low, f_{CLK} = 3.0GHz, IN_ = 1.5Gbps, 2^{23}-1 PRBS pattern		20	30	ps_{p-p}
		SEL = high, IN_ = 1.5Gbps, 2^{23}-1 PRBS pattern		36	55	
IN to CLK Setup Time	t_S	Figure 5	80			ps
CLK to IN Hold Time	t_H	Figure 5	80			ps
Output Rise Time	t_R	Figure 4		116	145	ps
Output Fall Time	t_F	Figure 4		115	145	ps
Propagation Delay Temperature Coefficient	$\Delta t_{PD}/\Delta T$				1	ps/°C

Note 1: Measurements are made with the device in thermal equilibrium.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to V_{EE} except V_{ID} and V_{OD}.

Note 3: DC parameters are production tested at T_A = +25°C. DC limits are guaranteed by design and characterization over the full operating range.

Note 4: Outputs are open. Inputs driven high or low.

Note 5: Guaranteed by design and characterization. Limits are set to ±6 sigma.

Note 6: Measured between outputs of the same part at the signal crossing points for a same-edge transition.

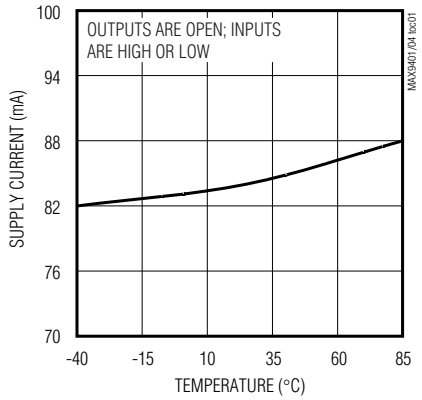
Note 7: Device jitter added to the input signal.

Quad ECL/PECL Differential Buffers/Receivers

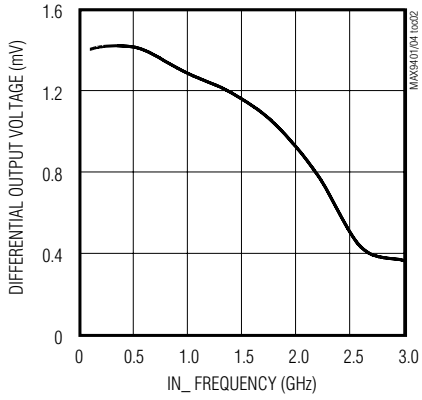
Typical Operating Characteristics

(Outputs terminated with 50Ω to V_{CC} - 3.3V, V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 0.9V, V_{ILD} = V_{CC} - 1.7V, output is enabled, SEL = high, $\overline{SEL}$ = low, input transition time = 125ps (20% to 80%), f_{CLK} = 3.0GHz, f_{IN} = 1.5GHz, T_A = +25°C, unless otherwise noted.)

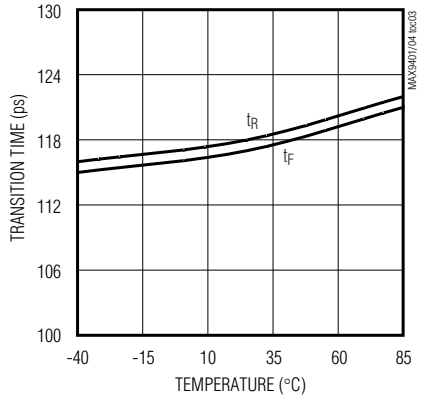
SUPPLY CURRENT vs. TEMPERATURE



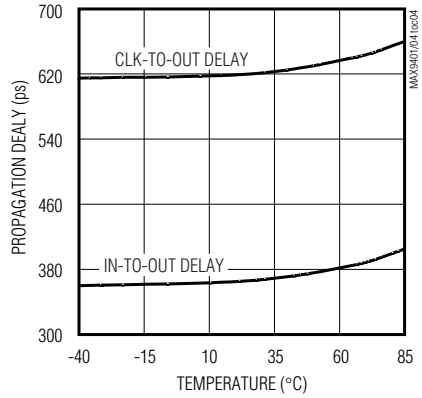
DIFFERENTIAL OUTPUT VOLTAGE (V_{OH} - V_{OL}) vs. IN_ FREQUENCY



TRANSITION TIME vs. TEMPERATURE



PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 8, 11, 17, 24, 30	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	SEL	Noninverting Differential Select Input. Setting SEL = high and $\overline{SEL}$ = low (differential high) enables all four channels to operate asynchronously. Setting SEL = low and $\overline{SEL}$ = high (differential low) enables all four channels to operate in synchronized mode.
3	$\overline{SEL}$	Inverting Differential Select Input
4	$\overline{CLK}$	Inverting Differential Clock Input. A rising edge on CLK (and falling on $\overline{CLK}$) transfers data from the inputs to the outputs when SEL = low.
5	CLK	Noninverting Differential Clock Input

Pin Description (continued)

PIN	NAME	FUNCTION
6	EN	Noninverting Differential Output Enable Input. Setting EN = high and $\overline{EN}$ = low (differential high) enables the outputs. Setting EN = low and $\overline{EN}$ = high (differential low) sets the outputs to logic low.
7	$\overline{EN}$	Inverting Differential Output Enable Input
9	IN3	Noninverting Differential Input 3
10	$\overline{IN3}$	Inverting Differential Input 3
12	$\overline{OUT3}$	Inverting Differential Output 3
13	OUT3	Noninverting Differential Output 3
14, 20, 21, 27	V_{EE}	Negative Supply Voltage
15	IN2	Noninverting Differential Input 2
16	$\overline{IN2}$	Inverting Differential Input 2
18	$\overline{OUT2}$	Inverting Differential Output 2
19	OUT2	Noninverting Differential Output 2
22	OUT1	Noninverting Differential Output 1
23	$\overline{OUT1}$	Inverting Differential Output 1
25	$\overline{IN1}$	Inverting Differential Input 1
26	IN1	Noninverting Differential Input 1
28	OUT0	Noninverting Differential Output 0
29	$\overline{OUT0}$	Inverting Differential Output 0
31	$\overline{IN0}$	Inverting Differential Input 0
32	IN0	Noninverting Differential Input 0
—	EP*	Exposed Paddle. EP is electrically connected to V_{EE}. Solder EP to PC board.

**QFN-EP package only.*

Detailed Description

The MAX9401/MAX9404 are extremely fast, low-skew quad ECL/PECL buffers/receivers designed for high-speed data and clock driver applications. These devices feature ultra-low propagation delay of 365ps and channel-to-channel skew of 15ps in asynchronous mode with 84mA supply current, making them ideal for driving long cables and double termination applications (*Functional Diagram*).

The four channels can be operated synchronously with an external clock, or in asynchronous mode, determined by the state of the SEL input. An enable input provides the ability to force all the outputs to a differential low state.

Data Input Termination

Figure 1 shows the input and output configuration of the MAX9401/MAX9404. The MAX9401 has high-impedance inputs and requires external termination. The MAX9404 has integrated 100Ω differential input termination resistors across each of the four inputs (IN_ to $\overline{IN}$_), reducing external component count.

Outputs

The MAX9401/MAX9404 have double-swing open-emitter outputs as shown in Figure 1. The double-amplitude swing outputs can drive double-terminated links or long

Quad ECL/PECL Differential Buffers/Receivers

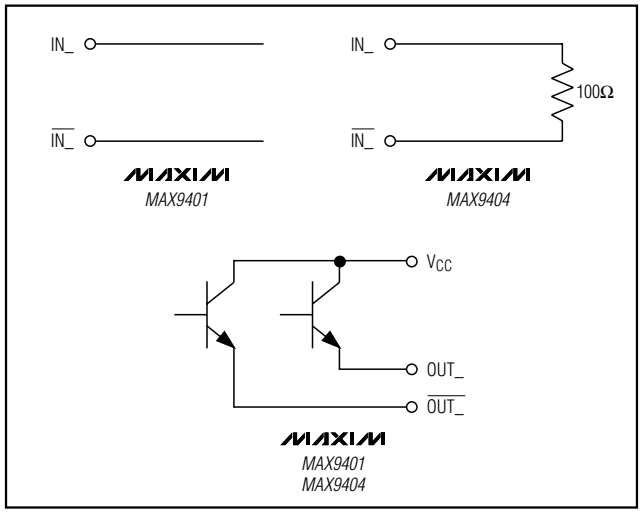


Figure 1. MAX9401/MAX9404 Input and Output Configurations

cables. External termination is required. See the *Output Termination* section.

Enable

Setting EN = high and $\overline{EN}$ = low enables the outputs. Setting EN = low and $\overline{EN}$ = high forces the outputs to a differential low when disabled. All changes on CLK, SEL, and IN_ are ignored.

Asynchronous Operation

Setting SEL = high and $\overline{SEL}$ = low enables four channels to operate independently as a buffer/receiver (CLK is ignored). In asynchronous mode, the CLK signal should be set to either logic low or high state to minimize noise coupling.

Synchronous Operation

Setting SEL = low and $\overline{SEL}$ = high enables all four channels to operate in synchronous mode. In this mode, buffered inputs are clocked into flip-flops simultaneously on every rising edge of the differential clock input (CLK and $\overline{CLK}$).

Differential Signal Input Limit

The maximum differential input signal magnitude is 3.0V.

Supply Voltages

For interfacing to differential PECL signals, the V_{CC} range is from +3.0V to +5.5V (with V_{EE} grounded). For interfacing to differential ECL, the V_{EE} range is -3.0V to -5.5V (with V_{CC} grounded). Output levels are referenced to V_{CC} and are considered PECL or ECL, depending on the level of the V_{CC} supply.

Applications Information

Input Bias

Unused inputs should be biased to avoid noise coupling that might cause toggling at the unused outputs. See Figure 2 for the biasing network.

Output Termination

Terminate the outputs through 50Ω to V_{CC} - 3.3V or use an equivalent Thevenin termination. Use identical terminations on each OUT for the lowest skew. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if OUT_ is used as a single-ended output, terminate both OUT_ and $\overline{OUT\_}$.

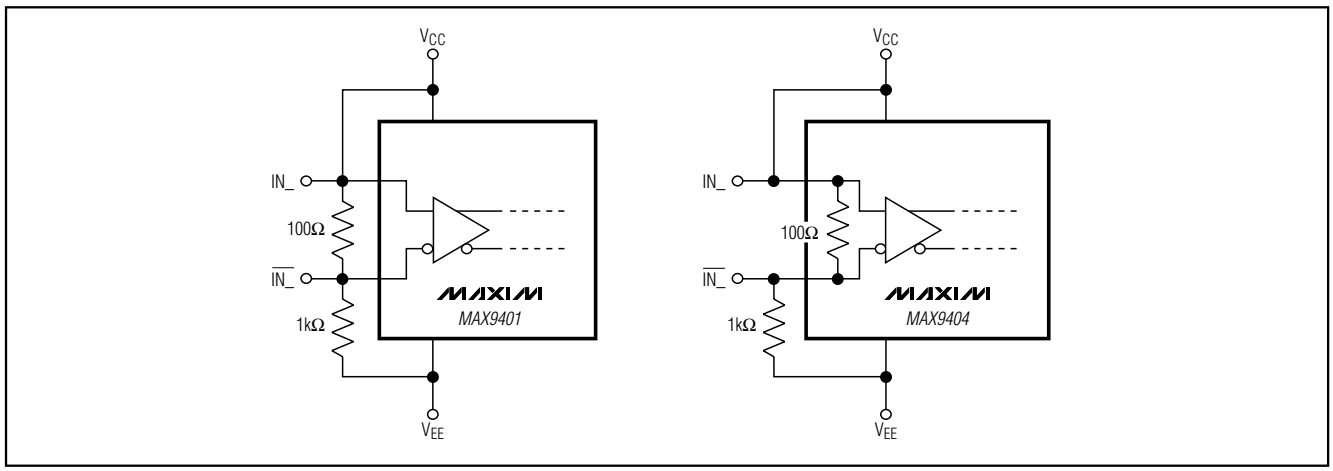


Figure 2. Input Bias Circuits for Unused Pins for MAX9401/MAX9404

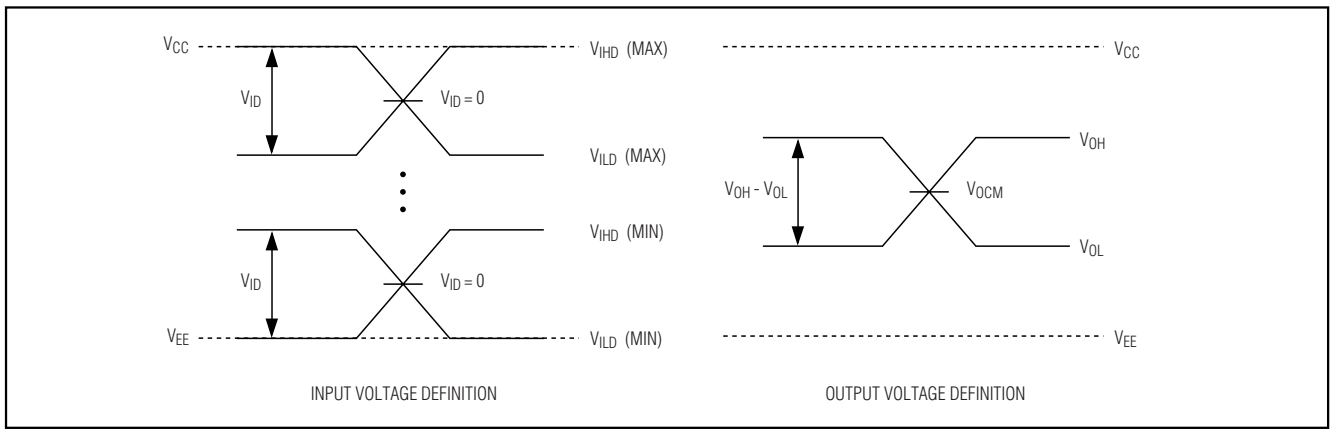


Figure 3. Input and Output Voltage Definitions

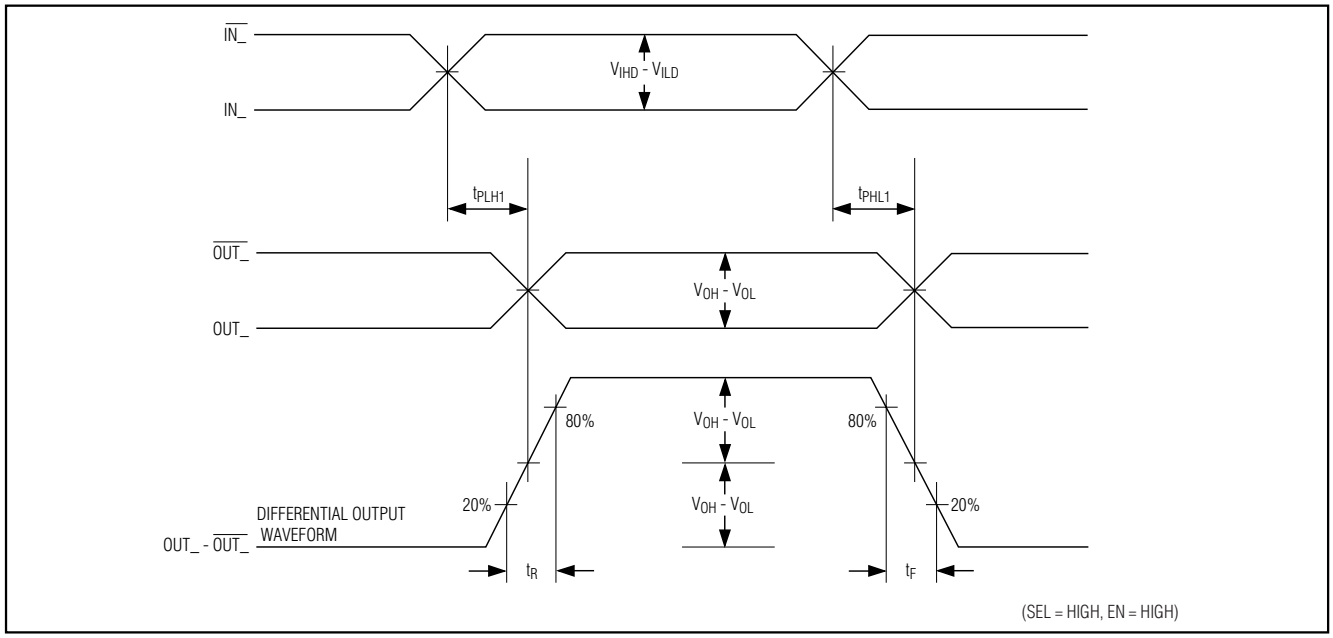


Figure 4. IN to OUT Propagation Delay Timing Diagram

Ensure that the output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings*. Under all operating conditions, the device's total thermal limits should be observed.

Power-Supply Bypassing

Adequate power-supply bypassing is necessary to maximize the performance and noise immunity. Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors as close to the device as possible, with the 0.01µF capacitor closest to the device pins. Use multiple bypass vias for connection to minimize inductance.

Circuit Board Traces

Input and output trace characteristics affect the performance of the MAX9401/MAX9404. Connect each of the inputs and outputs to a 50Ω characteristic impedance trace. Avoid discontinuities in differential impedance and maximize common-mode noise immunity by main-

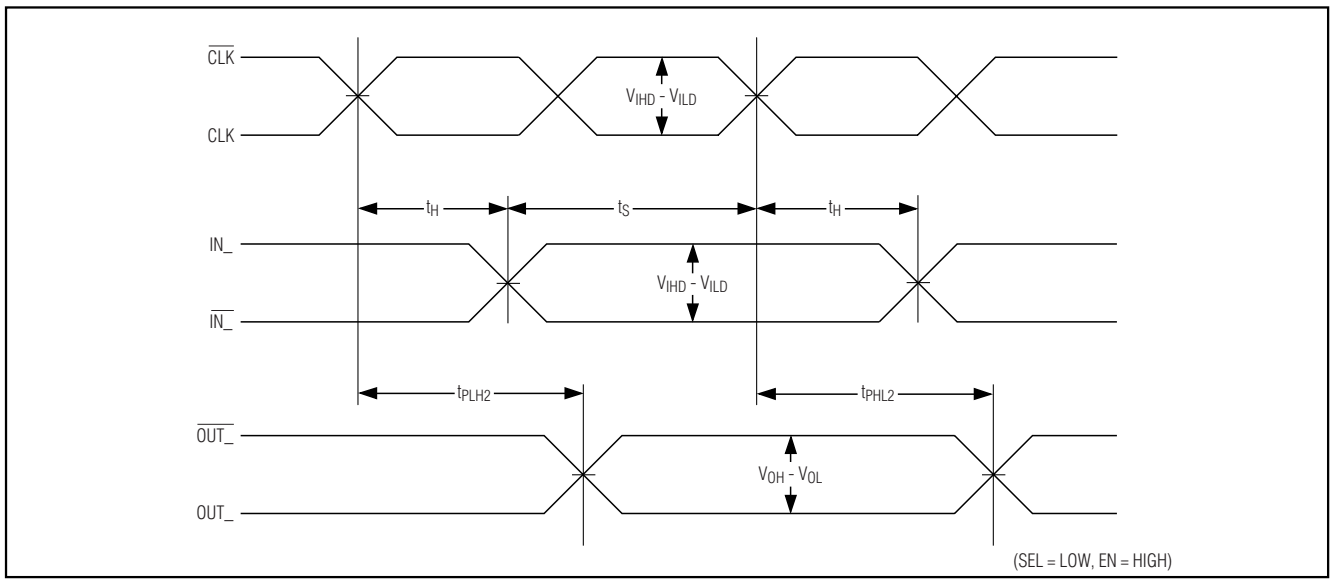


Figure 5. CLK to OUT Propagation Delay Timing Diagram

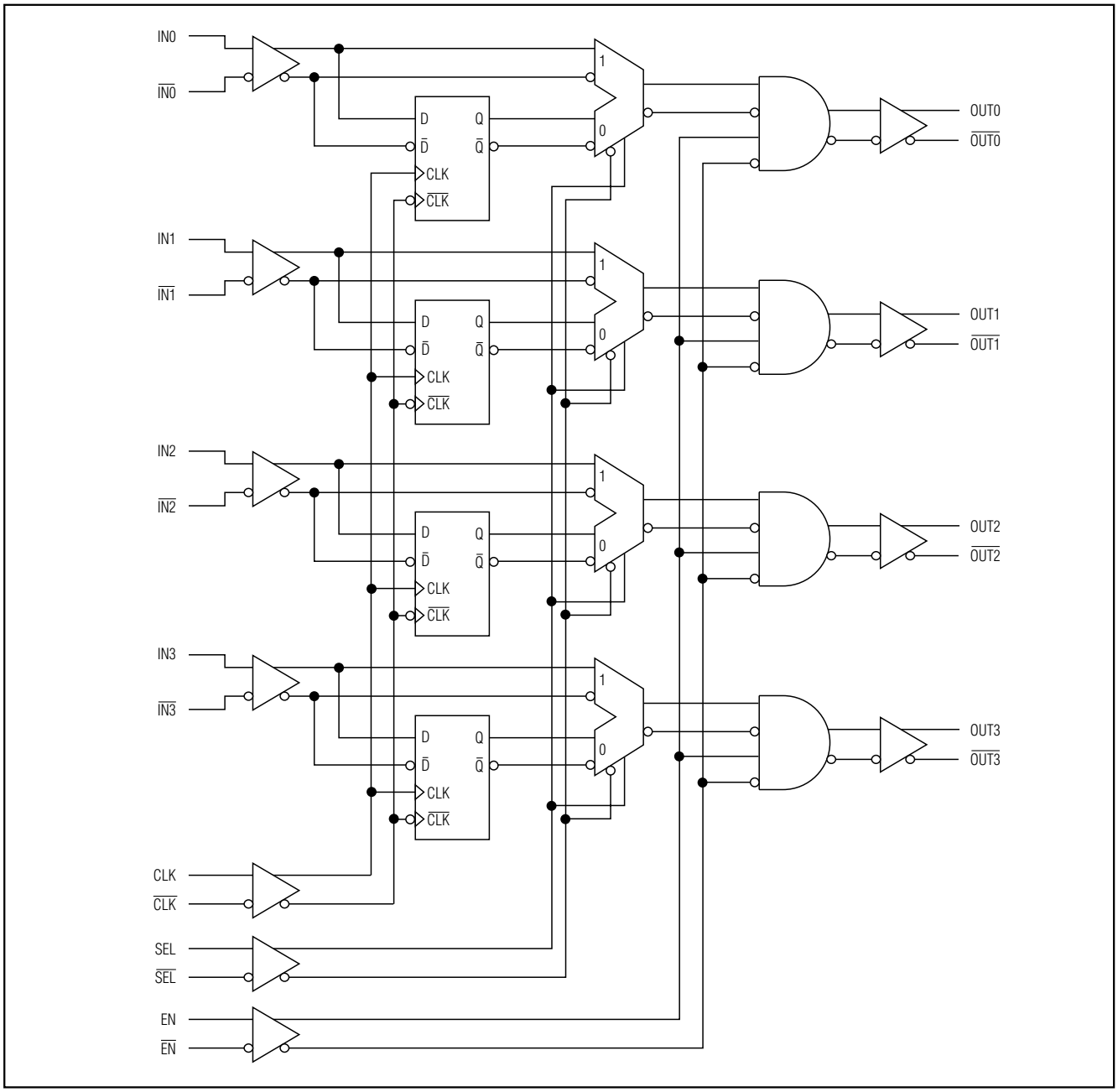
taining the distance between differential traces and avoid sharp corners. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Minimize skew by matching the electrical length of the traces.

Chip Information

TRANSISTOR COUNT: 748

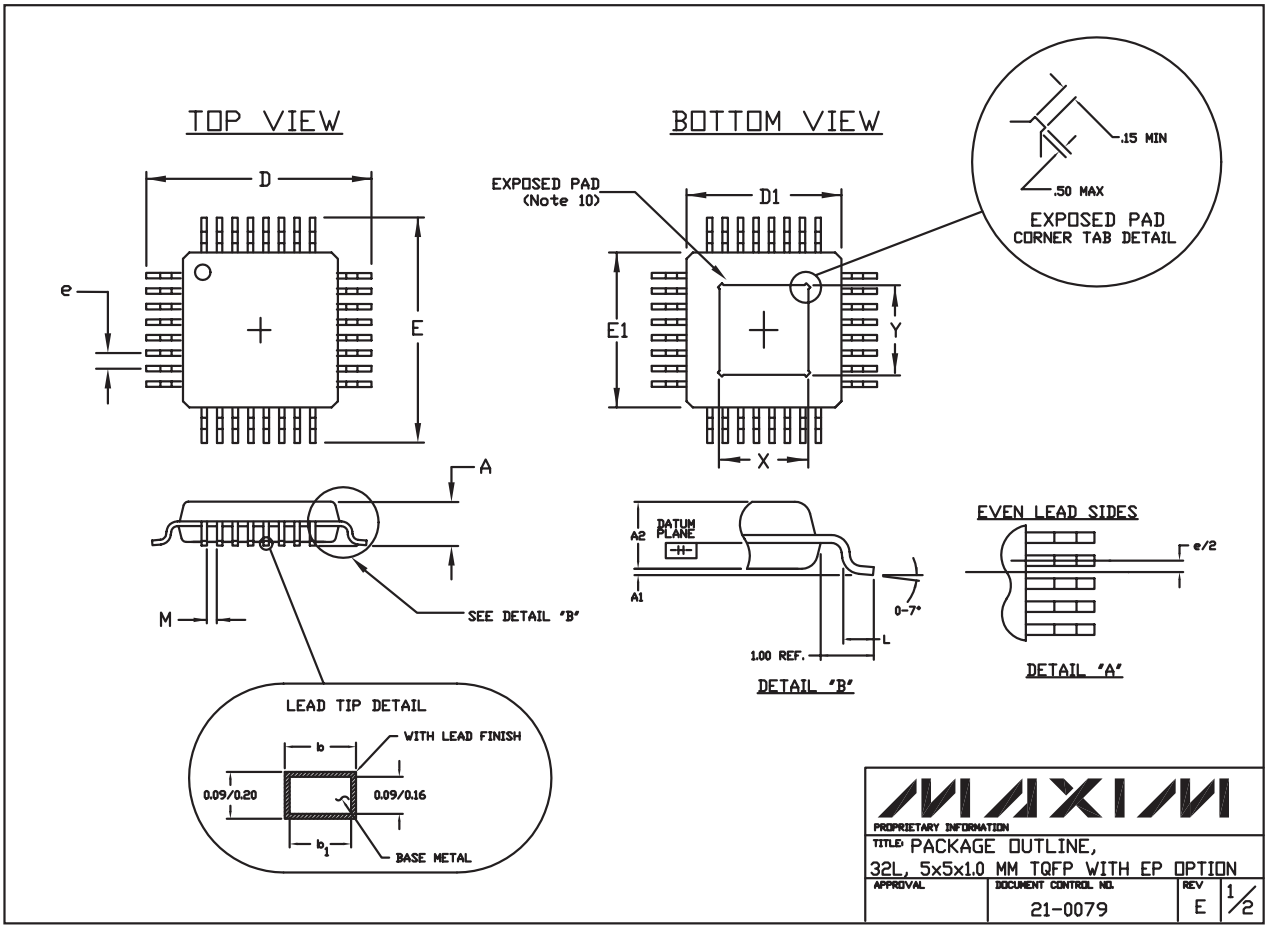
PROCESS: Bipolar

Functional Diagram



Quad ECL/PECL Differential Buffers/Receivers

Package Information



Package Information (continued)

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

	JEDEC VARIATIONS DIMENSIONS IN MILLIMETERS			
	AA		AA-EP*	
	5x5x1.0 MM		5x5x1.0 MM	
	MIN.	MAX.	MIN.	MAX.
A	~~	1.20	~~	1.20
A_1	0.05	0.15	0.05	0.15
A_2	0.95	1.05	0.95	1.05
D	7.00 BSC.		7.00 BSC.	
D_1	5.00 BSC.		5.00 BSC.	
E	7.00 BSC.		7.00 BSC.	
E_1	5.00 BSC.		5.00 BSC.	
L	0.45	0.75	0.45	0.75
M	0.15	~~	0.15	~~
N	32		32	
e	0.50 BSC.		0.50 BSC.	
b	0.17	0.27	0.17	0.27
b1	0.17	0.23	0.17	0.23
*X	N/A	N/A	2.70	3.30
*Y	N/A	N/A	2.70	3.30

* EXPOSED PAD (Note 10)

MAXIM

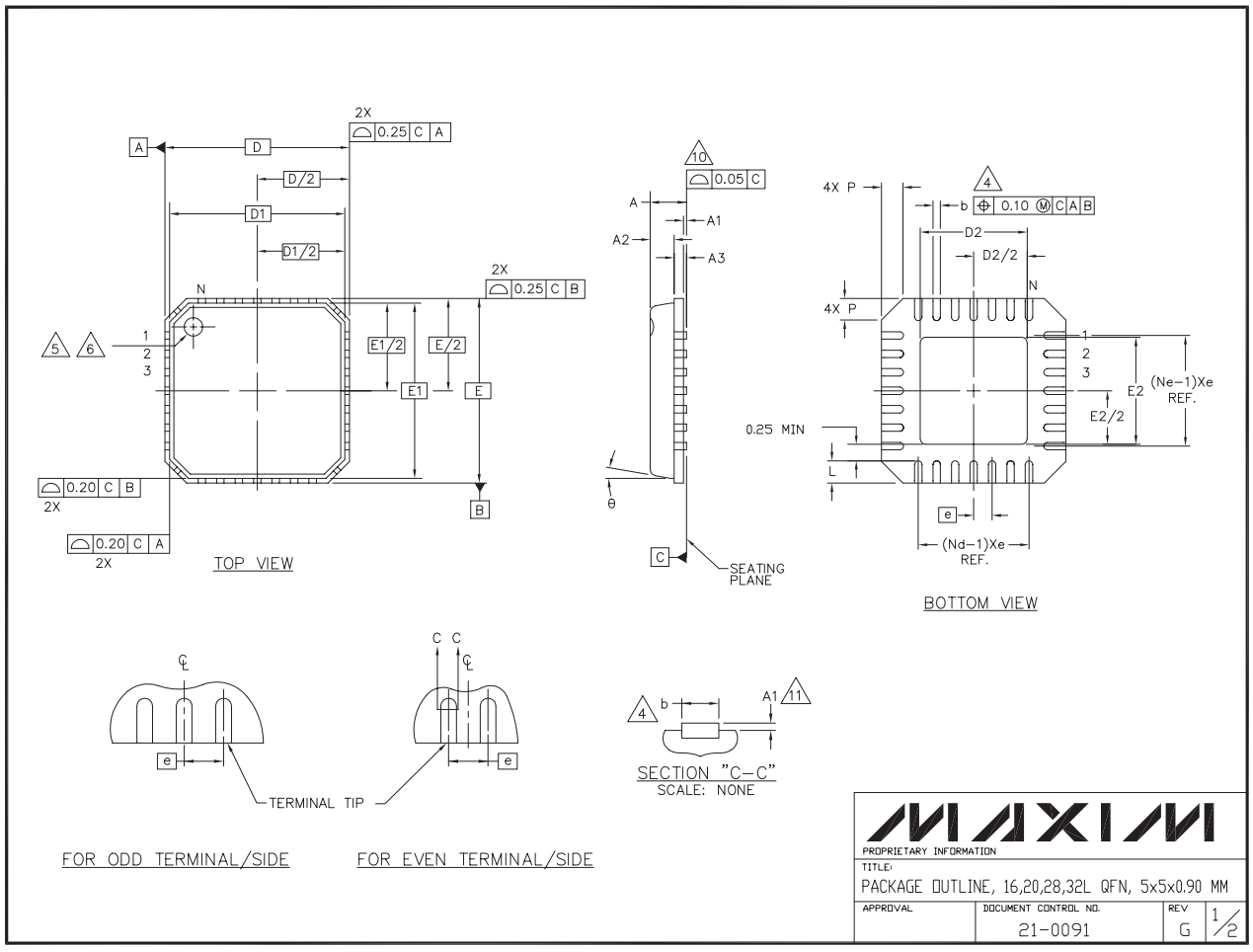
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32L, 5x5x1.0 MM TQFP WITH EP OPTION

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0079	E	2/2

Quad ECL/PECL Differential Buffers/Receivers

Package Information (continued)



Package Information (continued)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ	0°	–	12°	
P	0		0.60	
D2	1.25	–	3.25	
E2	1.25	–	3.25	

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.80 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.35	0.55	0.75	
b	0.28	0.33	0.40	4

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.35	0.55	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		28		3
Nd		7		3
Ne		7		3
L	0.35	0.55	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	G	2/2