19-3441; Rev 0; 10/04

MAXIM

Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

General Description

The MAX9960 dual-flash-pin electronics/supervoltage switch matrix replaces most of the relays and switches commonly needed to connect system resources to each of two pins in a flash memory or SOC ATE system (Figure 1). The device provides seven switches per channel to select up to four independent sources: the pin electronics (PE), two parametric measurement units (PMUs) or other Kelvin analog resources, and a flash memory programming supervoltage ($FV_{HH}\_$). The force-and-sense PMU switches are independently controlled, enabling their use to connect two non-Kelvin resources in place of each PMU or Kelvin resource. Each MAX9960 contains two complete seven-switch channels with fully independent controls.

The MAX9960 features signal path switches with wide 600MHz bandwidth, low 3Ω series resistance, and low 8pF shunt capacitance over a voltage range compatible with common pin electronics ICs. An on-chip voltage-doubling buffer with selectable 1x or 2x gain generates the flash supervoltage, allowing a 6.5V DAC reference input to generate up to a maximum of 13V for flash-memory programming levels.

When switching from the $FV_{HH}\_$ to PE_ or from PE_ to $FV_{HH}\_$, the device-under-test (DUT_) voltage behaves monotonically. Switching transitions between the PE_ and $FV_{HH}\_$ inputs are typically less than 350ns.

The MAX9960 operates over a commercial 0°C to +70°C temperature range, and is available in the 48-pin thin QFN package (7mm x 7mm x 0.8mm) with an exposed pad on the bottom for heat removal.

Applications

Flash Memory Automatic Test Equipment

SOC Automatic Test Equipment

Features

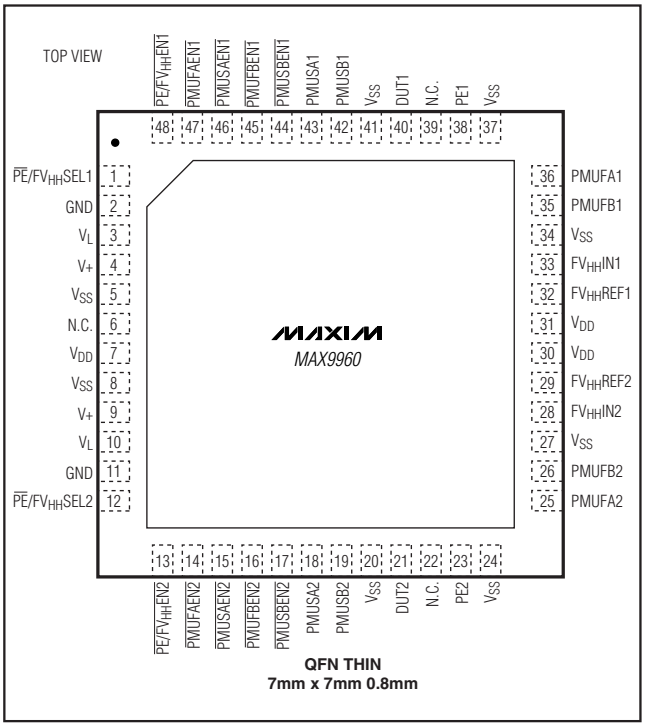
- **Dual Supervoltage Switch Arrays**
- **3Ω, 8pF, 600MHz Bandwidth Pin Electronics Paths**
- **13V Flash Programming Paths**
- **On-Chip 1x and 2x Selectable Gains**
- **2 Kelvin PMU Paths**
- **Fast Switching: 350ns (typ)**
- **Monotonic Slew Rate When Switching Between PE_ and FVHH_**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE*	PKG CODE
MAX9960BCTM	0°C to +70°C	48 Thin QFN-EP** (7mm x 7mm x 0.8mm)	T4877-6

**See full package information at the end of this data sheet.*
***EP = Exposed pad.*

Pin Configuration



Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +26V
V_{DD} to GND .....-0.3V to +16.5V
V_{SS} to GND .....-6.5V to +0.3V
V_L to GND .....-0.3V to +6V
V+ to V_{SS} .....+32V
Digital Inputs .....(GND - 0.3V) to (V_L + 0.3V)
$FV_{HH}IN\_$ .....(the higher of -4V and (V_{SS} - 0.3V)) to (the lower of +10V and (V_{DD} + 0.3V))
All Other Pins .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Continuous Current, PE_ .....±120mA
Continuous Current, PMUS_ _ .....±10mA
Continuous Current, PMUFA_ + PMUFB_ + (FVHH_ Path) .....±45mA
Peak Current (100ns), PE_ .....±300mA
Peak Current (100ns), PMUS__ .....±20mA
Peak Current (100ns), PMUFA_ + PMUFB_ + (FVHH_ Path) .....±70mA
Package Continuous Power Dissipation (T_A = +70°C)
48-Pin QFN-EP, on Single-Layer Board (derate 27.8mW/°C above +70°C) 2222mW
48-Pin QFN-EP, on Multilayer Board (derate 40.0mW/°C above +70°C) 3200mW
Operating Temperature Range .....0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
PE_ PATH						
On-Resistance	R_{ON}	$V_{DUT\_}$ = +2.5V, I_{SW} = -40mA to +40mA, T_A = 0°C to +30°C (Note 1)	2.5	3.0	3.5	Ω
		$V_{DUT\_}$ = +2.5V, I_{SW} = -40mA to +40mA, T_A = +30°C to +70°C (Note 1)	2.5		4.2	
On-Resistance Flatness	$R_{FLAT(ON)}$	$V_{DUT\_}$ = 0 to +5V (Note 1)	-0.6		+0.6	Ω
Ch1 to Ch2 Resistance Match	R_{MATCH}	$V_{DUT\_}$ = +2.5V, I_{SW} = -40mA to +40mA	-0.5		+0.5	Ω
Signal Voltage Range	V_{PE}		-3.5		+8.0	V
Operating DC Current Range	I_{SW}		-40		+40	mA
$FV_{HH\_}$ PATH						
On-Resistance	R_{ON}	$FV_{HH\_}$ = -1.5V to (V_{DD} - 1.5V), $I_{HH\_}$ = -10mA to +10mA (Notes 1, 2)	32		100	Ω
Operating Voltage Range	$FV_{HH\_}$		-1.5		V_{DD} - 1.5	V
Operating DC Current Range	I_{SW}		-10		+10	mA
FORCE PATHS						
On-Resistance	R_{ON}	$V_{PMUF\_\_}$ = -4.25V to +14.5V, $I_{PMUF\_\_}$ = -25mA to +25mA (Note 1)			70	Ω
Operating Voltage Range	V_{PMUF}		-4.25		+14.5	V
Operating DC Current Range	I_{SW}		-25		+25	mA
SENSE PATHS						
On-Resistance	R_{ON}	$V_{PMUS\_\_}$ = -4.25V to +14.5V, $I_{PMUS\_\_}$ = -1mA to +1mA (Note 1)			1250	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{PMUS}		-4.25		+14.5	V
Operating DC Current Range	I_{SW}		-1		+1	mA
FV_{HH}_ BUFFERS						
DC Output Current	I_{ODC}	FV_{HH} = -1.5V to (V_{DD} - 1.5V)	10			mA
Current Limit	I_{LIM}	DUT_ sourcing current	+15		+25	mA
		DUT_ sinking current	-25		-15	
Operating Voltage Range	FV_{HH}	FV_{HH}REF_ = 0 (Note 2)	-1.5		V_{DD} - 1.5V	V
Linearity Error	$L_{ER}\_FV_{HH}$	FV_{HH}REF_ = 0; no load; relative to 2-point line between $V_{DUT\_}$ = 0 and +13V; measured at $V_{DUT\_}$ = +3.25V, +6.5V, and +9.75V	-2		+2	mV
Gain	GFV_{HH}	FV_{HH}REF_ = 0, no load, $V_{DUT\_}$ = 0 to +13V (Note 3)	1.98	2.00	2.02	V/V
Output Offset	$V_{OS}\_FV_{HH}$	FV_{HH}REF_ = 0, $V_{DUT\_}$ = +12V, no load	-50		+50	mV
Output Offset Temperature Coefficient	T_{C_VOS}	$V_{DUT\_}$ = 0 to +13V, FV_{HH}REF_ = 0, T_{CASE} = +30°C to +50°C		±0.2		mV/°C
Input Bias Current	IFV_{HH}	FV_{HH}IN_ = -1.5V to +7.5V, FV_{HH}REF_ = open	-25		+25	µA
Gain Resistor Ground	FV_{HHREF}	(Note 4)	-1.5		+0.5	V
Gain Resistor Current	I_{VHHREF}	Measured with FV_{HH}IN_ = +5V, FV_{HH}REF_ = 0		0.4		mA
LEAKAGE (Notes 5, 6)						
DUT_ Leakage, Disabled	I_{LEAK_OFF}	Switches S1, S2, S6, S7 open; $V_{DUT\_}$ = -4.25V to +14.5V	-1		+1	nA
PE_ Leakage	I_{LEAK_PE}	S1 closed; S2, S6, S7 open; $V_{DUT\_}$ = -3.5V to +8V	-1		+1	nA
PMUA_ Path Leakage, Enabled	$I_{LEAK\_PMUA\_ON}$	S2, S4, S6 closed; S1, S3, S5, S7 open; $V_{DUT\_}$ = -4.25V to +14.5V	-1		+1	nA
PMUB_ Path Leakage, Enabled	$I_{LEAK\_PMUB\_ON}$	S2, S5, S7 closed; S1, S3, S4, S6 open; $V_{DUT\_}$ = -4.25V to +14.5V	-1		+1	nA
PMUA_ Path Leakage, Disabled	$I_{LEAK\_PMUA\_OFF}$	S4, S6 open; $V_{PMUFA\_}$ = -4.25V to +14.5V; measured at PMUFA_ with PMUSA_ externally connected to PMUFA_	-1		+1	nA
PMUB_ Path Leakage, Disabled	$I_{LEAK\_PMUB\_OFF}$	S5, S7 open; $V_{PMUFB\_}$ = -4.25V to +14.5V; measured at PMUFB_ with PMUSB_ externally connected to PMUFB_	-1		+1	nA
DIGITAL INPUTS ($\overline{PMUF\_EN\_}$, $\overline{PMUS\_EN\_}$, $\overline{PE/FV_{HH}EN\_}$, $PE/FV_{HH}SEL\_$)						
Input High Voltage	V_{IH}		+2.3			V
Input Low Voltage	V_{IL}				+0.4	V

Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		-0.2		V_L	V
Input Current	I_{IH}, I_{IL}	V_{IN} = -0.2V to V_L	-10		+10	µA
POWER SUPPLIES						
Positive Supply	V_{DD}		14.5	15	16.0	V
Negative Supply	V_{SS}		-6.00	-5	-4.25	V
High Voltage Supply	V+	(Note 1)	23	24	25	V
Logic Supply	VL		3.0	3.3	3.6	V
Quiescent Positive Supply Current	Σ (I_{DD}, I+)	V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, $FV_{HH}IN\_$ = +6.5V, $FV_{HH}REF\_$ = 0, all digital inputs = +2.3V, no loads			10	mA
Quiescent Negative Supply Current	I_{SS}	V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, $FV_{HH}IN\_$ = +6.5V, $FV_{HH}REF\_$ = 0, all digital inputs = +2.3V, no loads			8.5	mA
Quiescent Logic Supply Current	I_{VL}	V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, $FV_{HH}IN\_$ = +6.5V, $FV_{HH}REF\_$ = 0, all digital inputs = +2.3V, no loads			2	mA
Quiescent Power Dissipation	P_{DQ}	V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, $FV_{HH}IN\_$ = +6.5V, $FV_{HH}REF\_$ = 0, all digital inputs = +2.3V, no loads			200	mW
AC CHARACTERISTICS						
SWITCHING TIMES BETWEEN PE_ AND FV_{HH}_ PATHS (Note 7) (Figure 3)						
Switch PE_ to FV_{HH}_	t_{ON_FVHH}	+5V to +7V transition		275	425	ns
		0 to +13V transition		350	500	
FV_{HH}_ Settling Time	t_{S_FVHH}	Settling to within larger of 1% step voltage or 50mV of final value		500		ns
Switch FV_{HH}_ to PE_	t_{ON_PE}			300	425	ns
PE_ Settling Time	t_{S_PE}	Settling to within larger of 1% step voltage or 50mV of final value		500		ns
PE_ TO FV_{HH}_ Overshoot/Undershoot				±100		mV
PE_ to FV_{HH}_ Preshoot				±150		mV
Minimum Switching Slew Rate	SR_{MIN}	Over 20% to 80% region		±10		V/µs
SWITCHING TIMES, SAME PATH (Note 8) (Figure 2)						
PE_ Switch On-Time	t_{ON_1}	$V_{PE\_}$ = +5V from 47Ω source		150		ns
FV_{HH}_ Switch On-Time	$t_{ON\_2,3}$	$FV_{HH}IN\_$ = +2.5V, $FV_{HH}REF\_$ = 0		350		ns

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMUF_ _ Switch On-Time	$t_{ON\_2,4}$ $t_{ON\_2,5}$	$V_{PMUF\_\_}$ = +5V		150		ns
PMUS_ _ Switch On-Time	t_{ON_6} t_{ON_7}	$V_{PMUS\_\_}$ = +5V		300		ns
PE_, FV_{HH}_, PMUF_ _, PMUS_ _ Switch Off-Times	t_{OFF}			700		ns
CAPACITANCE AND BANDWIDTH (Note 5)						
Capacitance, All Paths Disconnected	C_{DUT_OFF}	All switches disconnected, for frequencies greater than 2MHz (Note 9)		20		pF
Capacitance, PE_ Path Connected (Note 9)	C_{DUT_PE}	Switch S1 closed, all others open, for frequencies greater than 2MHz		8		pF
		Switch S1 closed, all others open, for frequencies less than 1kHz		50		
Unit-to-Unit Variation, PE_ Path Connected	ΔC_{DUT_PE}	Switch S1 closed, all others open, for frequencies greater than 2MHz (Note 9)		±2		pF
Capacitance, PMUFA_ and PMUSA_ Path Connected	C_{DUT_PMUA}	S2, S4, and S6 closed; all others open (Note 9)		35		pF
Capacitance, PMUFB_ and PMUSB_ Path Connected	C_{DUT_PMUB}	S2, S5, and S7 closed; all others open (Note 9)		35		pF
Capacitance, PMUFA_ Path Disconnected	C_{PMUFA_OFF}	S4 open, measured at PMUFA_ (Note 9)		10		pF
Capacitance, PMUFB_ Path Disconnected	C_{PMUFB_OFF}	S5 open, measured at PMUFB_ (Note 9)		10		pF
Capacitance, PMUSA_ Path Connected	C_{PMUSA_ON}	S6 closed, all others open, measured at PMUSA_ (Note 9)		10		pF
Capacitance, PMUSB_ Path Connected	C_{PMUSB_ON}	S7 closed, all others open, measured at PMUSB_ (Note 9)		10		pF
Capacitance, PMUSA_ Path Disconnected	C_{PMUSA_OFF}	S6 open, measured at PMUSA_ (Note 9)		5		pF
Capacitance, PMUSB_ Path Disconnected	C_{PMUSB_OFF}	S7 open, measured at PMUSB_ (Note 9)		5		pF
PE_ Signal Bandwidth	f_{3DB}	Only PE_ path enabled (Note 10)		600		MHz
FV_{HH}_ BUFFER						
Slew Rate	$SRFV_{HH}$	FV_{HH}REF_ = 0, (gain = 2), FV_{HH}IN_ stepped from 0 to +5V and +5V to 0		±5		V/µs
Settling	t_S	$C_{DUT\_}$ = 200pF to within 0.1% of step voltage, after FV_{HH}IN_ changes		25		µs
		$C_{DUT\_}$ = 4000pF to within 0.1% of step voltage, after FV_{HH}IN_ changes (Note 11)		50		

Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

Note 1: V+ should be at least 8V above V_{DD} to guarantee specified path resistance values.

Note 2: When the FV_{HH}_ buffer is configured for a gain of +1 (FV_{HH}REF_ open), the output voltage range is limited to -1.5V to +7.5V.

Note 3: FV_{HH}_ buffer gain is typically +1, when FV_{HH}REF_ is open.

Note 4: FV_{HH}REF_ is tested by repeating the FV_{HH}_ path resistance tests over the variation of FV_{HH}REF_. For each value of FV_{HH}REF_, FV_{HH}IN_ is adjusted to FV_{HH}IN_ = (FV_{HH}_ + FV_{HH}REF_) / 2.

Note 5: All measurements taken at DUT_, except where noted.

Note 6: These specifications are guaranteed by design and characterization. In addition, these specifications will be production tested with min/max test limits of ±10nA.

Note 7: Voltage source driving PE_ has 47Ω source resistance. PE_ = 0 to +5.0V, FV_{HH}_ = +7 to +13V. Measured from 50% point of input logic to 90% of analog swing.

Note 8: All unused switches open, unless otherwise noted. Measured from 50% point of input logic to 90% of analog swing.

Note 9: Unless otherwise noted, measured at DUT_. No external connections to any of the switched analog pins—PE_, DUT_, PMUFA_, PMUFB_, PMUSA_, or PMUSB_—except as needed to make measurement.

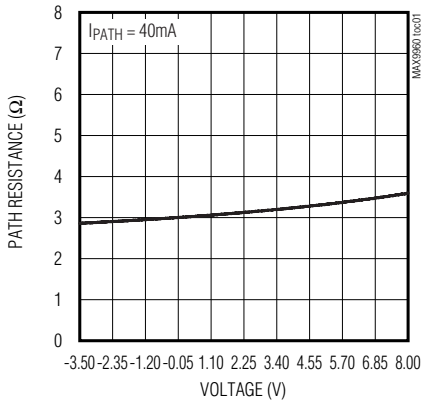
Note 10: $Z_{DUT\_}$ = 50Ω; equivalent bandwidth calculated from measured DUT_ rise and fall time with PE_ stimulated by a 3V step with 1ns 10% to 90% rise/fall time.

Note 11: The maximum load for FV_{HH} buffer is 4000pF.

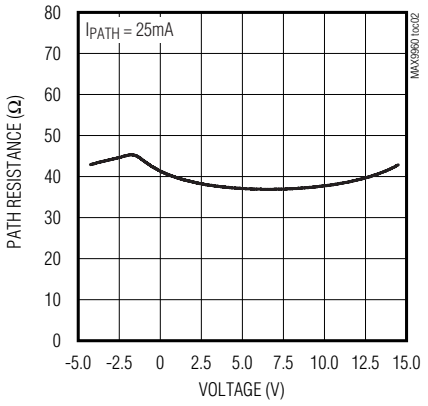
Typical Operating Characteristics

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

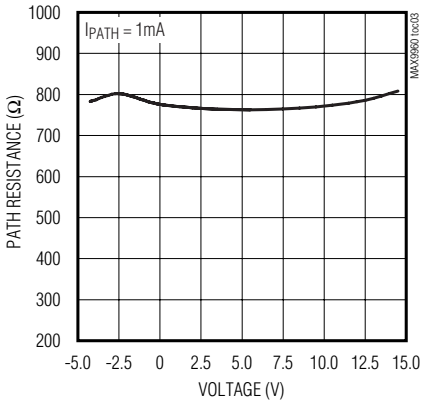
PE PATH RESISTANCE vs. VOLTAGE



FORCE PATH RESISTANCE vs. VOLTAGE



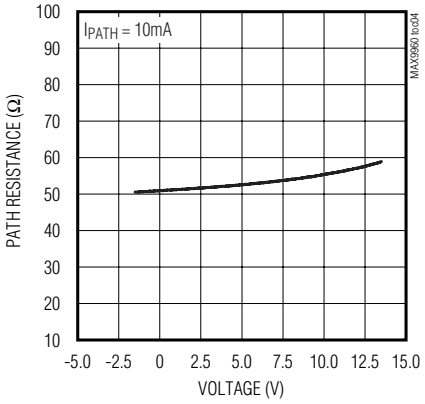
SENSE PATH RESISTANCE vs. VOLTAGE



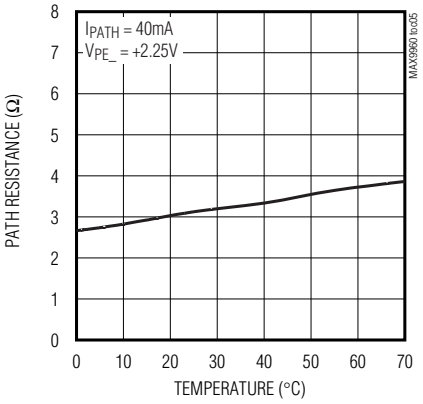
Typical Operating Characteristics (continued)

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

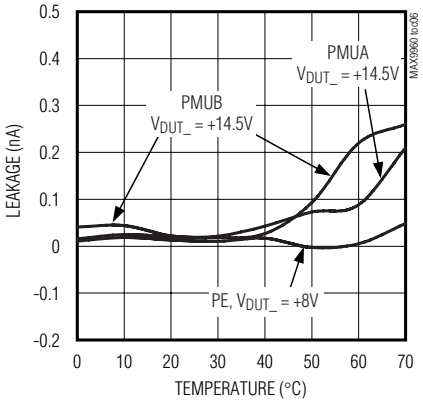
FV_{HH}_ PATH RESISTANCE vs. VOLTAGE



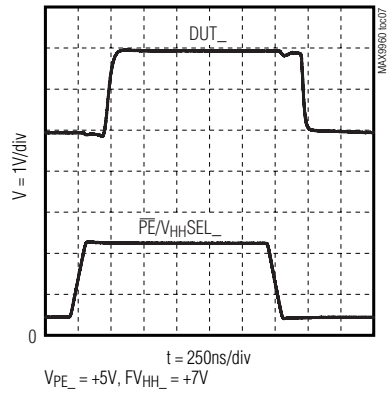
PE PATH RESISTANCE vs. TEMPERATURE



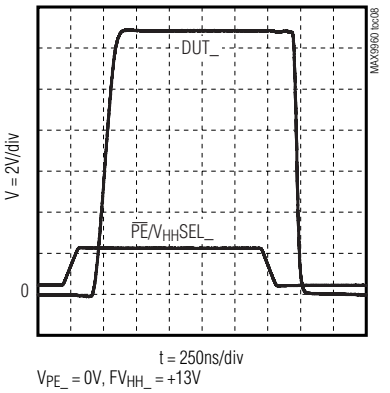
LEAKAGE CURRENT vs. TEMPERATURE



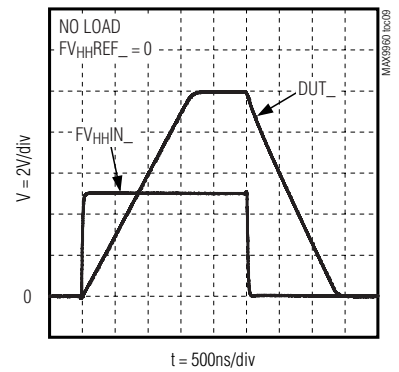
PE_ TO FV_{HH}_ TRANSITIONS



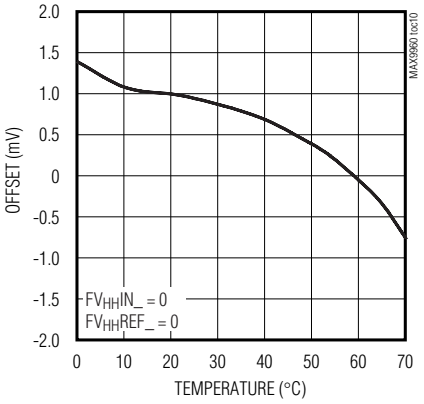
PE_ TO FV_{HH}_ TRANSITIONS



FV_{HH}_ SLEW



FV_{HH} BUFFER OUTPUT OFFSET vs. TEMPERATURE



Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

Pin Description

PIN	NAME	FUNCTION
1	$\overline{PE}$/FV_{HH}SEL1	PE1 or FV_{HH}1 Select. Selects either PE1 or FV_{HH}1 to be connected to DUT1. Force low to select PE1, force high to select FV_{HH}1.
2, 11	GND	Ground
3, 10	V_L	Logic Power Supply. Nominally 3.3V.
4, 9	V+	Analog Positive Gate-Drive Power Supply. Nominally 24V.
5, 8, 20, 24, 27, 34, 37, 41	V_{SS}	Analog Negative Power Supply. Nominally -5V.
6, 22, 39	N.C.	No Connection. Make no connection to this pin.
7, 30, 31	V_{DD}	Analog Positive Power Supply. Nominally 15V.
12	$\overline{PE}$/FV_{HH}SEL2	PE2 or FV_{HH}2 Select. Selects either PE2 or FV_{HH}2 to be connected to DUT2. Force low to select PE2, force high to select FV_{HH}2.
13	$\overline{PE}$/FV_{HH}EN2	PE2 and FV_{HH}2 Enable. Enables PE2 and FV_{HH}2 to be connected to DUT2, as determined by $\overline{PE}$/FV_{HH}SEL2. Force low to enable signal path, force high to disable the signal path.
14	$\overline{PMUFAEN2}$	PMUFA2 Enable. Controls the connection of PMUFA2 to DUT2. Force low to connect PMUFA2 to DUT2, force high to disconnect PMUFA2 from DUT2.
15	$\overline{PMUSAEN2}$	PMUSA2 Enable. Controls the connection of PMUSA2 to DUT2. Force low to connect PMUSA2 to DUT2, force high to disconnect PMUSA2 from DUT2.
16	$\overline{PMUFBEN2}$	PMUFB2 Enable. Controls the connection of PMUFB2 to DUT2. Force low to connect PMUFB2 to DUT2, force high to disconnect PMUFB2 from DUT2.
17	$\overline{PMUSBEN2}$	PMUSB2 Enable. Controls the connection of PMUSB2 to DUT2. Force low to connect PMUSB2 to DUT2, force high to disconnect PMUSB2 from DUT2.
18	PMUSA2	Sense A Analog Output for Channel 2. Kelvin feedback output for the channel 2 force A path.
19	PMUSB2	Sense B Analog Output for Channel 2. Kelvin feedback output for the channel 2 force B path.
21	DUT2	Analog I/O for Channel 2. Connects to the DUT.
23	PE2	Analog I/O for Channel 2. Connects to the pin electronics I/O.
25	PMUFA2	Analog Input Force A for Channel 2. Connects to an external DC resource such as a PMU.
26	PMUFB2	Analog Input Force B for Channel 2. Connects to an external DC resource such as a PMU.
28	FV_{HH}IN2	Analog Supervoltage Input for Channel 2. The voltage applied to FV_{HH}IN2 is amplified as determined by FV_{HH}REF2 (see the *Functional Block Diagram*).
29	FV_{HH}REF2	Analog Gain-Setting Input for Channel 2. Sets the gain of the FV_{HH}2 buffer.
32	FV_{HH}REF1	Analog Gain-Setting Input for Channel 1. Sets the gain of the FV_{HH}1 buffer.
33	FV_{HH}IN1	Analog Supervoltage Input for Channel 1. The voltage applied to FV_{HH}IN1 is amplified as determined by FV_{HH}REF1 (see the *Functional Block Diagram*).
35	PMUFB1	Analog Input Force B for Channel 1. Connects to an external DC resource such as a PMU.
36	PMUFA1	Analog Input Force A for Channel 1. Connects to an external DC resource such as a PMU.
38	PE1	Analog I/O for Channel 1. Connects to the pin electronics I/O.
40	DUT1	Analog I/O for Channel 1. Connects to the DUT.
42	PMUSB1	Sense B Analog Output for Channel 1. Kelvin feedback output for the channel 1 force B path.
43	PMUSA1	Sense A Analog Output for Channel 1. Kelvin feedback output for the channel 1 force A path.

Pin Description (continued)

PIN	NAME	FUNCTION
44	$\overline{\text{PMUSBEN1}}$	PMUSB1 Enable. Controls the connection of PMUSB1 to DUT1. Force low to connect PMUSB1 to DUT1, force high to disconnect PMUSB1 from DUT1.
45	$\overline{\text{PMUFBEN1}}$	PMUFB1 Enable. Controls the connection of PMUFB1 to DUT1. Force low to connect PMUFB1 to DUT1, force high to disconnect PMUFB1 from DUT1.
46	$\overline{\text{PMUSAEN1}}$	PMUSA1 Enable. Controls the connection of PMUSA1 to DUT1. Force low to connect PMUSA1 to DUT1, force high to disconnect PMUSA1 from DUT1.
47	$\overline{\text{PMUFAEN1}}$	PMUFA1 Enable. Controls the connection of PMUFA1 to DUT1. Force low to connect PMUFA1 to DUT1, force high to disconnect PMUFA1 from DUT1.
48	$\overline{\text{PE}}/\overline{\text{FV}_{\text{HH}}\text{EN1}}$	PE1 and $FV_{HH}1$ Enable. Enables PE1 and $FV_{HH}1$ to be connected to DUT1, as determined by $\overline{\text{PE}}/\overline{\text{FV}_{\text{HH}}\text{SEL1}}$. Force low to enable signal path, force high to disable the signal path.
—	EP	Exposed Pad for Heat Removal. Internally biased to V_{SS}. Connect to V_{SS} or leave floating.

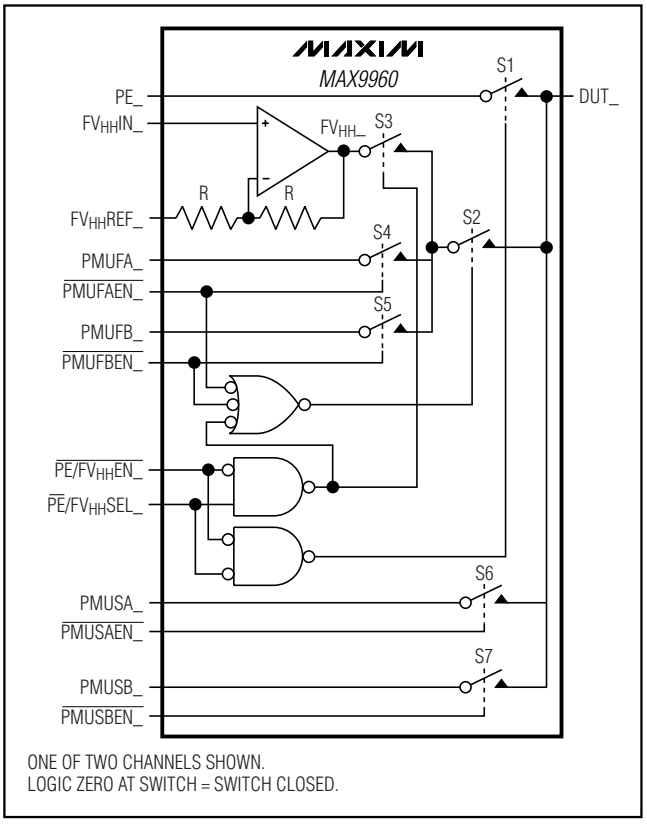


Figure 1. Functional Block Diagram

Detailed Description

The MAX9960 is a dual analog switch matrix featuring two Kelvin PMU paths, a PE path, and a flash programming supervoltage circuit that allows testing of flash memory using standard PE devices. It makes possible, without the use of relays, a fully functional pin with both AC and DC capabilities.

The signal path switches feature 600MHz bandwidth, 3Ω series resistance, and 8pF shunt capacitance over a voltage range compatible with common pin-electronics ICs. The voltage-doubling buffer, with selectable 1x or 2x gain, generates the 13V flash memory programming level from a 6.5V input. Configure the switches using digital inputs $\overline{\text{PMUFAEN\_}}$, $\overline{\text{PMUSAEN\_}}$, $\overline{\text{PMUFBEN\_}}$, $\overline{\text{PMUSBEN\_}}$, $\overline{\text{PE}}/\overline{\text{FV}_{\text{HH}}\text{EN\_}}$, and $\overline{\text{PE}}/\text{FV}_{\text{HH}}\text{SEL\_}$ as indicated in Tables 1 and 2.

The switching speed between PE_ and FV_{HH}_ paths is less than 350ns typical (Figure 3), and during switching, DUT_ behaves monotonically.

FV_{HH} Buffer Load Capacitance

The maximum load capacitance for the FV_{HH} buffer is 4000pF. While this amount of load capacitance is not expected during normal operation, an application may call for the buffer to be connected to a highly capacitive PMU path occasionally for calibration purposes. No damage to the MAX9960 will result as a consequence of this condition.

Supervoltage FV_{HH} Buffer Gain

The FV_{HH} buffer gain can be selected using FV_{HH}REF_. If FV_{HH}REF_ is grounded, the gain of the buffer is +2. If FV_{HH}REF_ is left floating, the buffer gain is +1.

Dual-Flash-Pin Electronics/Supervoltage Switch Matrix

Table 1. Switch Control, All Possible Combinations

$\overline{PMUFAEN\_}$	$\overline{PMUFBEN\_}$	$\overline{PMUSAEN\_}$	$\overline{PMUSBEN\_}$	$\overline{PE/FV_{HH}EN\_}$	$\overline{PE/FV_{HH}SEL\_}$	DUT_
0	X	X	X	X	X	PMUFA_ path connected
X	0	X	X	X	X	PMUFB_ path connected
X	X	0	X	X	X	PMUSA_ path connected
X	X	X	0	X	X	PMUSB_ path connected
X	X	X	X	0	1	FV_{HH}_ path connected
X	X	X	X	0	0	PE_ path connected
All other combinations						Every path is disconnected

Table 2. Switch Control, Use Cases

$\overline{PMUFAEN\_}$	$\overline{PMUFBEN\_}$	$\overline{PMUSAEN\_}$	$\overline{PMUSBEN\_}$	$\overline{PE/FV_{HH}EN\_}$	$\overline{PE/FV_{HH}SEL\_}$	DUT_
1	1	1	1	0	0	PE_
1	1	1	1	0	1	FV_{HH}_
0	1	0	1	1	X	PMUFA_ + PMUSA_
1	0	1	0	1	X	PMUFB_ + PMUSB_
0	1	0	1	0	0	PE_ + PMUFA_ + PMUSA_
1	0	1	0	0	0	PE_ + PMUFB_ + PMUSB_
0	1	0	1	0	1	FV_{HH}_ + PMUFA_ + PMUSA_
1	0	1	0	0	1	FV_{HH}_ + PMUFB_ + PMUSB_
0	0	0	0	0	0	PE_ + PMUFA_ + PMUSA_ + PMUFB_ + PMUSB_

Power-Supply Considerations

The MAX9960 requires four power-supply voltages, typically V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, and V_L = +3.3V. Use a 0.1µF bypass capacitor close to each supply pin, and provide bulk bypassing where power enters the circuit board. The MAX9960 does not require any special power-up sequencing.

Chip Information

TRANSISTOR COUNT: 2020

PROCESS: BiCMOS

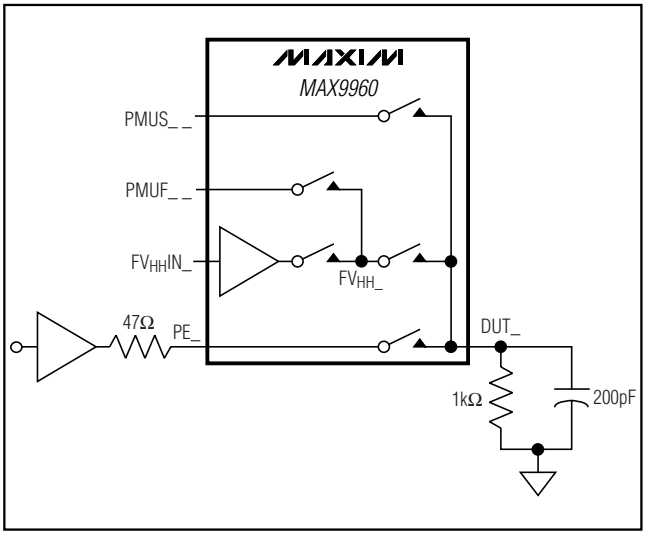


Figure 2. Switching Time Test Circuit

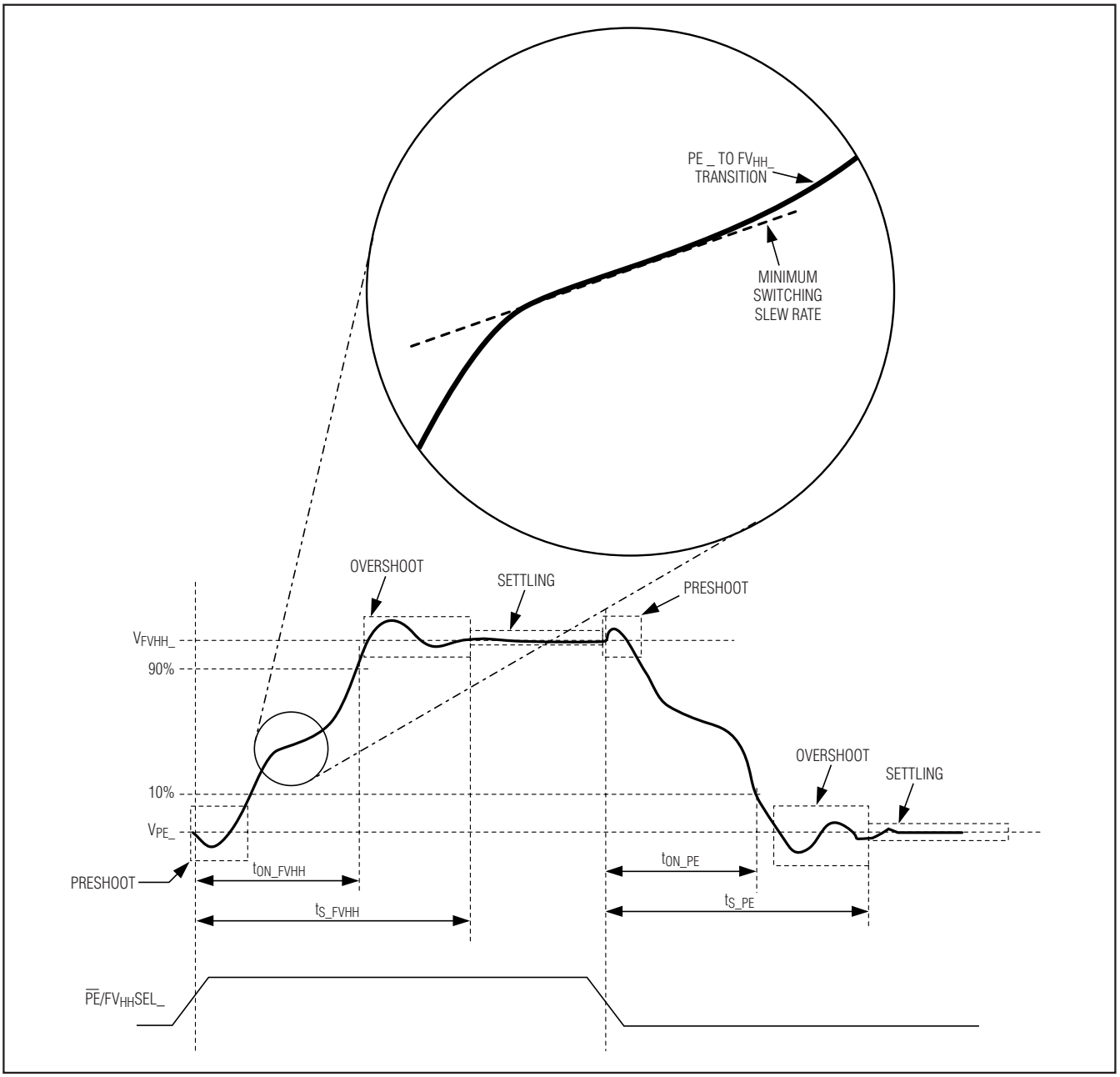


Figure 3. PE_ - $FV_{HH\_}$ and $FV_{HH\_}$ - PE_ Transition and Settling Timing

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.