MAXQ2000
Low-Power LCD Microcontroller

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REVISION A2 ERRATA

The errata listed below describe situations where MAXQ2000 revision A2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to MAXQ2000 revision A2 components. Revision A2 components are branded on the topside of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another MAXQ2000 die revision, visit our website at **www.maxim-ic.com/errata**.

1. REAL-TIME CLOCK ACCURACY DOES NOT MEET SPECIFICATION

Description:
The real-time clock is affected by port-pin activity resulting in a net gain or loss (less likely) of time.

Work Around:
Avoid high-speed switching on all I/O when using the real-time clock.

2. TXD PIN DOES NOT RESUME I/O CHARACTERISTICS FOLLOWING MODE 0 TRANSMISSION

Description:
Following a mode 0 serial port transmission, that serial port's TXD pin remains in its alternate function state and does not return to the I/O state, as implied in the user's guide. This means that the pin will remain in logic 1 (the inactive serial transmission) state, and that the pin cannot be cleared by software. This condition affects both serial ports.

Work Around:
The circuitry that holds the serial ports TXD pin in its alternate function state can be cleared by writing any value to the corresponding Serial Port Control register. On the following cycle, the pin will return to its I/O state.

3. 1-Wire PRESENCE DETECT FLAG CAN CLEAR UNEXPECTEDLY

Description:
The 1-Wire presence detect flag in 1-Wire Interrupt Flag register (OWA = 010b) can fail to be set if a software read of the bit occurs in the same cycle as internal hardware attempts to set it. This could result in the device failing to assert the corresponding interrupt and not recognizing a device on the 1-Wire bus.

Work Around:
The application software can simulate the presence detect feature by delaying 1ms after assertion of the 1-Wire reset, and the checking the state of the presence detect result bit in the 1-Wire Interrupt Flag register (OWA = 010b).

4. 1-Wire TRANSMIT BUFFER AND SHIFT REGISTER EMPTY FLAGS AUTO CLEAR WHEN READ

Description:
The 1-Wire transmit buffer and shift register empty flags in the 1-Wire Interrupt Flag register (OWA = 010b) automatically clear when the register is read. This is not indicated in the documentation. Future revisions of the device will be corrected to match the documentation and hold the register contents after being read.

Work Around:
Modify the application software to make a temporary copy of the register contents if the value needs to be accessed more than one time.

5. RTC TIME-OF-DAY AND SUBSECOND ALARM FLAGS MAY NOT CLEAR UNDER CERTAIN CIRCUMSTANCES

Description:
Either the time-of-day or the subsecond alarm flag may fail to clear properly by the application software, generating another interrupt on the next timer tick of the 32kHz clock.

Work Around:
On servicing a time-of-day or subsecond alarm interrupt, poll the RTC ready bit active, followed by polling it inactive before clearing the associated flag.

6. RTC ALARMS WILL NOT CAUSE DEVICE TO EXIT STOP MODE

Description:
Activation of the RTC alarm interrupt in stop mode causes the device to enter an invalid state.

Work Around:
Do not use the RTC alarm interrupt to exit stop mode.

7. WRITES TO THE RTC COUNT REGISTERS CAN FAIL UNDER CERTAIN CIRCUMSTANCES

Description:
Writes to the RTC count registers can fail if the write happens on the same cycle as the 32kHz clock is updating the internal counters.

Work Around:
When software needs to update the RTC count registers, poll the RTC subsecond register, RTSS, until the LSb changes. At that point, the 32kHz clock will have just updated the internal counters and there will be no danger of a collision when writing to the count registers. Update the RTC count registers immediately. This erratum has little effect on the application software, as count register updates are done infrequently.

8. SUCCESS RATE OF FLASH MEMORY WORD PROGRAMMING DEPENDENT ON BYTE VALUE

Description:
Word values with more than approximately three-quarters of their bits in the logic 0 state may fail to program correctly. The failure is location independent. The failure is exacerbated by low operating frequency.

Work Around:
After execution of the flash memory programming, read back the word or use the utility ROM verify routine to confirm the value was programmed correctly.