SSC050-01

Two-Wire Serial Backplane Controller

Data Sheet

Revision 4.0
November 10, 2004

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Contents

REVISION HISTORY

Revision	Date	Section	Change
1.01	11/4/03	All	Initial Revision
1.0	11/10/04		Updated
4.0	11/10/04		Data Manual migrated to Data Sheet status

Chapter 1 Introduction

The SSC050-01 is a I/O-intensive peripheral device which is intended to be a portion of a cost effective FC-AL, SCSI, SAS or SATA enclosure management solution. The device contains an address programmable two wire serial interface, a block of control and status registers, I/O port control logic, specialized port bypass control logic and a clock generation block. Along with an external crystal, the device can be configured to support up to 40 bits of general purpose I/O or 16 bits of general purpose I/O, 16 bits of port bypass control (8 pairs supporting 8 drives), 4 fan speed monitoring inputs and 4 pulse width modulated outputs.

The SSC050-01 is capable of supporting various combinations of individual PBC/CRU/SDU functions as well as integrated solutions. The control register portion of the device allows the user to individually program each I/O pin as an input, output or open source/drain output. Additional control features include selectable flash rates for direct LED drive, input edge detection for interrupt generation, fan speed monitoring and pulse width modulated outputs. The addressing capability of the SSC050-01 includes three pins, which are used for device addressing, as well as one pin, which can be used to select two device type identifiers. Sixteen devices can be used in a single two-wire serial interface system.

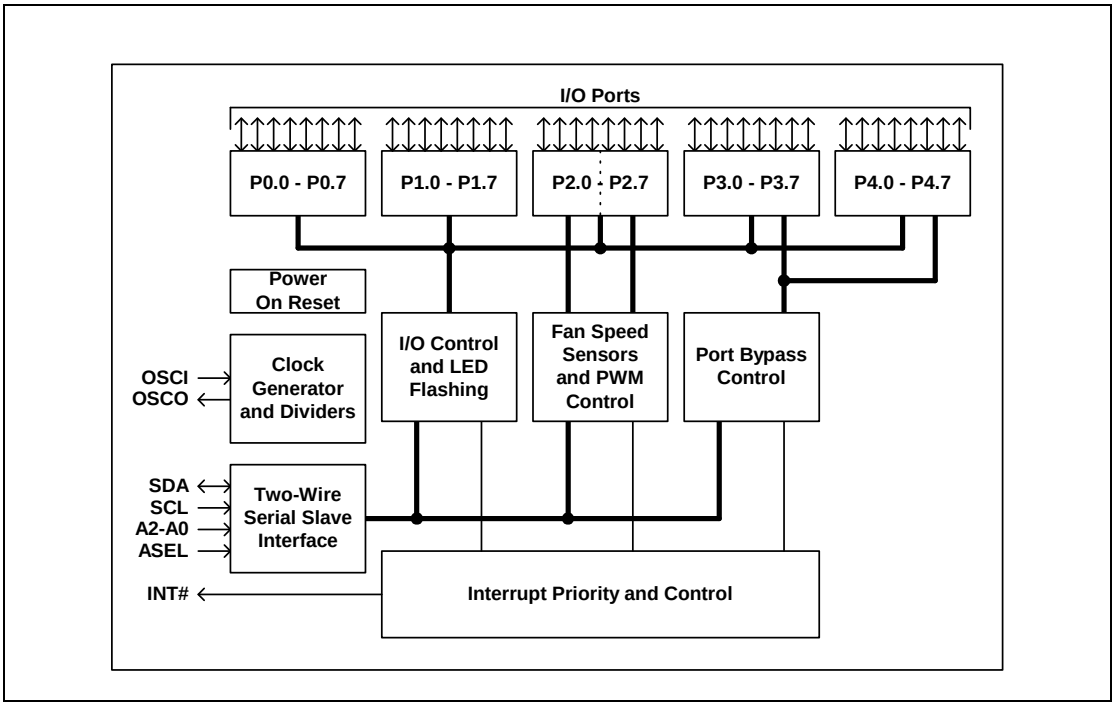

Figure 1-1. Chip Block Diagram

FEATURE SUMMARY

- Up to 40 bits of user-definable, bidirectional general purpose I/O
- Integrated Port Bypass, Clock Recovery and Signal Detect support for up to 8 drives
- Four programmable fan speed monitoring inputs
- 5 volt tolerant Interrupt output eliminates polling requirements
- Selectable direct LED drive flashing capability
- Pin-programmable addressing for up to 16 devices on a single serial bus
- 5 volt tolerant slave mode two wire serial interface
- 20% of package pins are power and ground
- Four programmable pulse width modulation outputs
- Enhanced fan speed monitor input filters

TYPICAL APPLICATIONS

FC-AL Drive Enclosure Configuration

- Basic port bypass configuration
  - Support for up to 128 drives
  - Backplane controller supports up to two sets of CRU/SDU functions and 8 drives
- Sixteen Backplane controllers can be simultaneously attached to the serial bus
- Four drive implementation shown - four channel PBC with two CRU/SDU functions
  - General purpose I/O lines used for drive control/status and system control/status

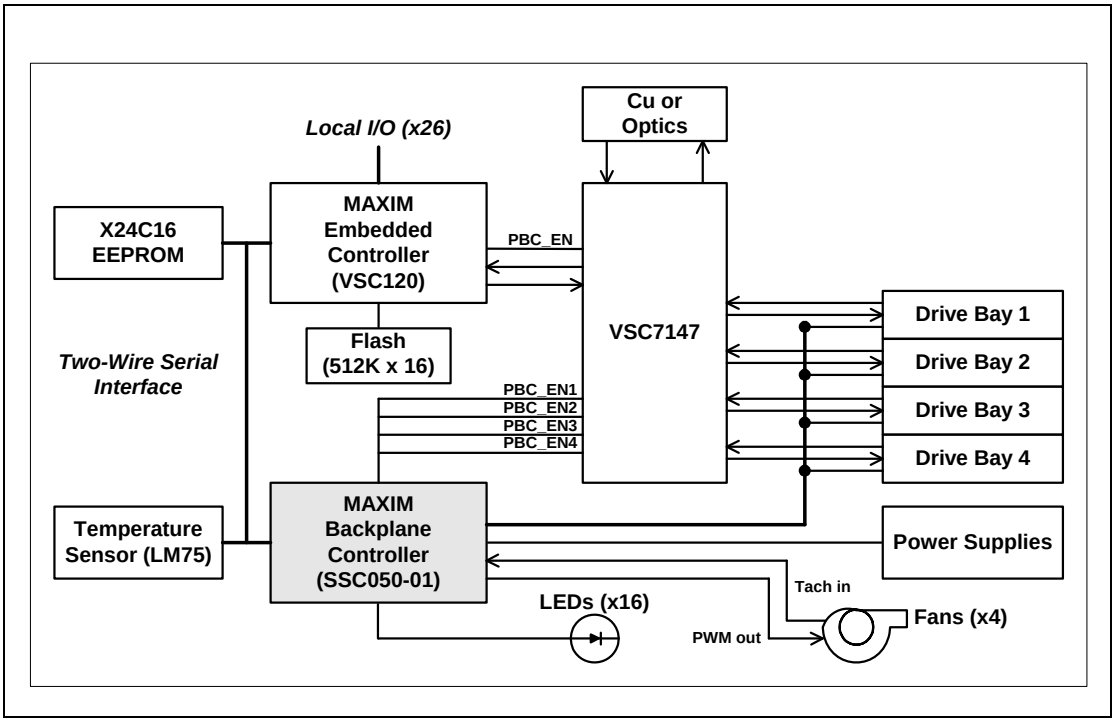

Figure 1-2. Single Loop, Single Controller with Four Drives

General Purpose I/O Configuration

- Controlled by general purpose Microcontroller with two wire serial interface
- Support for up to 640 I/O lines
  - Backplane controller supports up to 40 I/O lines
  - Sixteen backplane controllers can be simultaneously attached to the serial bus

Four backplane controller implementation shown with shared open drain interrupt

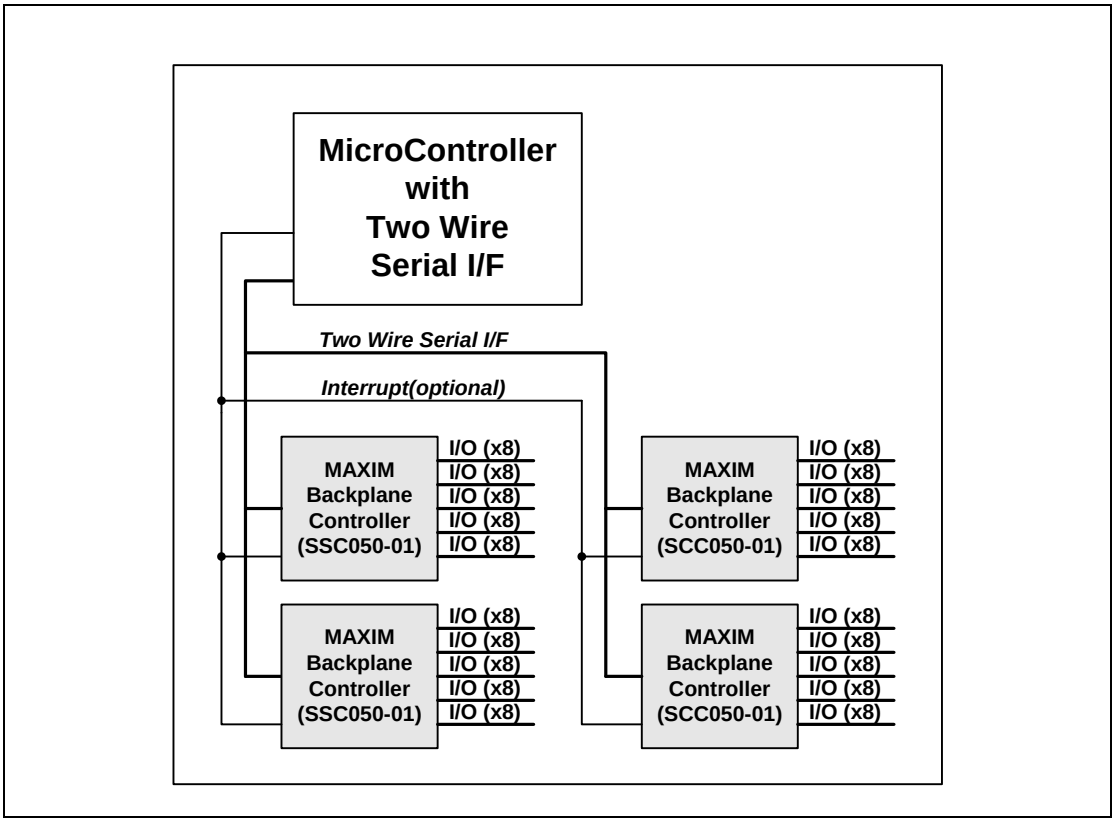

Figure 1-3. Four Backplane Controllers, 160 Bidirectional I/O Lines

Chapter 2 FUNCTIONAL DESCRIPTION

The SSC050-01 is composed of five major functional blocks; a slave mode two-wire serial interface, a block of control registers, general purpose I/O and specialized port bypass control logic, a clock generator and power-on reset control logic. The SSC050-01 fully supports a generic two-wire serial interface and is compatible with other industry standard devices which also support this interface at both 100K and 400K bits per second.

TWO-WIRE SERIAL INTERFACE

The device supports a single slave mode two-wire serial interface. All inter-chip communication to a microcontroller takes place over this bus. The interface supports a three-bit address bus, which allows the user to select one of eight possible addresses. The address bus is compared to bits three through one of the slave address byte, which is the first byte transmitted to the device after a start condition. The SSC050-01 supports two pin selectable four-bit device type identifier values, 1000b and 1100b. The address bits and the device identifier allow the use of up to 16 devices on a single two-wire serial interface. The serial interface control logic includes the slave state machine, address comparison logic, serial to parallel and parallel to serial conversion, register read/write control and filtering for the clock and data line.

A read or write transaction is determined by the least significant bit (R/W) of the first byte transferred. Write accesses require a three-byte transfer. The first byte is the slave address with the R/W bit low, the second byte contains the register address and the third byte is the write data. Read accesses require a four-byte transfer since data transfer direction can not change after receipt of the slave address byte. The first byte is the slave address with the R/W bit low, the second byte contains the register address, the third byte is a repeated slave address with the R/W bit high and the fourth byte is the read data. If the transaction is a write, the data will be latched into the appropriate register during the acknowledge of the third byte. All transactions to or from the device complete during the acknowledge of the third byte allowing the user to immediately initiate another transfer to the device. Sequential read or write transactions are allowed and are extensions of the above protocol with additional data bytes added to the end of the transaction. All sequential transactions will cause the internal address to increment by one regardless of the register address.

CONTROL REGISTERS

The SSC050-01 contains five groups of control registers. Each group supports a specific function within the device as follows; the first group is the port data registers, the second is the data direction registers, the third contains special bit control features, the fourth supports the port bypass control function and the fifth supports fan speed monitoring. Currently the device contains 78 registers to support all required functions. In normal I/O operation, each eight-bit group of I/O pins are controlled by a pair of registers, Port Data and Data Direction. The use of these pairs of registers allows each I/O line to be individually configured as an input with internal pull-up, output or open drain output with internal pull-up.

The bit control features are enabled through a separate register for each I/O pin. The Bit Control registers allow the user to independently configure each I/O pin to enable one of the special control features as well as control Port Data and Data Direction (which are shadowed copies of the standard control bits found in the Port Data and Data Direction registers). Each I/O pin which has been configured as an input can also be configured to assert the open drain interrupt pin when a rising edge, a falling edge or either edge is detected on the I/O pin. An Interrupt Status register provides the user with a binary indication of which I/O pin is the source of the current interrupt. Each I/O pin which is configured as an output can automatically generate one of seven selectable flashing rates, which are normally driven in an open drain mode. By providing all I/O control capability in a single register, the user can control the operation of the I/O on a pin-by-pin basis.

The Port Bypass registers control the operation of a selected group of I/O lines which can be dedicated to support various combinations of individual PBC/CRU/SDU functions as well as integrated solutions. Enabling port bypass control causes the normal or bit control register settings to be overridden and any further changes to the affected registers will have no effect. Each Port Bypass Control register will automatically configure the I/O lines to support a Force Bypass output and a Signal Detected input.

The Fan Speed registers control the operation of four programmable inputs which can be used to monitor signals from fans equipped with tachometer outputs. Enabling fan speed control causes the normal or bit control register settings to be overridden and any further changes to the affected registers will have no effect. Each group of three registers provides the capability to enable the function, establish a user defined RPM overflow value which indicates a failure and determine the current RPM value of the fan. The digital filters on the fan speed inputs can optionally be enabled to increase the normal 100 to 200 nanosecond filter to 400 to 500 nanoseconds.

The Pulse Width Modulation Control registers enable internal logic to provide duty cycles of 0% to 100% in 3% increments at default frequencies of 26KHz, 52KHz and 104KHz. Optionally, the PWM outputs can be programmed for three additional frequency ranges of 5.2KHz, 10.4KHz and 20.8KHz or 1.04KHz, 2.08KHz and 4.16KHz or 208Hz, 416Hz and 833Hz. These outputs can vary the speed of up to four fans through the use of external drivers and power MOSFETs or pulse width to voltage converters. They can also be used to support other pulse width modulated requirements within the system.

I/O LOGIC

Each general purpose I/O pin is controlled by a set of registers in the Control Register Block. The I/O supports a high current drive output buffer, which can be configured as a totem pole or open drain driver. The input section of the I/O supports TTL signaling and includes an internal weak pull-up device. This allows unused I/O pins to be left unconnected without high current drain issues. The port bypass control I/O pins which are shared with Port 3 and Port 4 are generated using the same buffer logic as the other ports. When enabled in port bypass control mode, internal logic overrides the existing configuration, with each I/O pin dedicated to the specific port bypass function. All I/O lines default as inputs with the weak internal pull-up enabled.

CLOCK GENERATOR

Clock generation for the device is composed of an internal oscillator, divider circuits and a distribution network. The primary clock frequency of 10.0MHz is used for filtering incoming serial interface signals and interrupt sources as well as clocking the slave state machine. Divided clocks provide the source for LED flash rate generators. Logic within the SSC050-01 synchronizes the divided clocks between devices attached to the same two-wire serial bus with no more than 200 nanoseconds of skew. Multiple devices can then be used to drive different LED's at the same frequency, providing a synchronized visible indication. The oscillator provides a stable clock source for the device and requires the use of an off chip crystal and related passive components or external clock source. There are no programmable options related to clock generation except the selection of the seven fixed LED Flashing rates. The SSC050-01 can operate at frequencies other than 10.0MHz and continue to meet both the standard mode (100KHz) and fast mode (400KHz) serial interface timings. Frequencies from 8.0MHz to 12.5MHz are allowable as long as they meet the AC timing requirements listed in section 5.3.1 of this manual. Operation of the LED flashing circuits, fan speed counters and pulse width modulated outputs will be affected by a change in base operating frequency. The user must scale the expected operating parameters by the change in frequency from a nominal 10.0MHz. As and example, operating the SSC050-01 at 8.0MHz will cause the LED flashing circuits, fan speed counters and pulse width modulated outputs to operate 25% slower than normal.

POWER-ON RESET

Power-On Reset is accomplished by the use of logic internal to the device. No external components are required. After power-on, the serial interface state machine will always return an idle state waiting for a start condition to appear on the SCL and SDA pins. A proper power-on reset sequence will clear the serial interface state machine, the clock generators, the control registers, the I/O control logic and the port bypass control logic. The divided clocks used for LED flash rate generation will also be in a known state. An external reset circuit utilizing the TEST1 and ASEL pins can be developed as an option to the internal Power-On Reset logic. Regardless of the effectiveness of either power-on reset sequence, it is highly recommended that the control registers and I/O control logic be cleared through the Soft Reset Register bit. This can be accomplished by writing a 80h to the BCT Register (FCh) followed immediately by a STOP condition. This bit is self resetting and will not require further attention.

Chapter 3 Pin Description

The SSC050-01 is packaged in a 64-pin PQFP. All pins have been placed to optimize their connection to external components. Power and ground distribution has also been optimized for core and high current I/O connections. All serial interface pins as well as the interrupt output are 5 volt tolerant. VDD and VDD2 should be connected to a 3.3 volt supply with no more than 10% tolerances.

FUNCTIONAL SIGNAL GROUPING

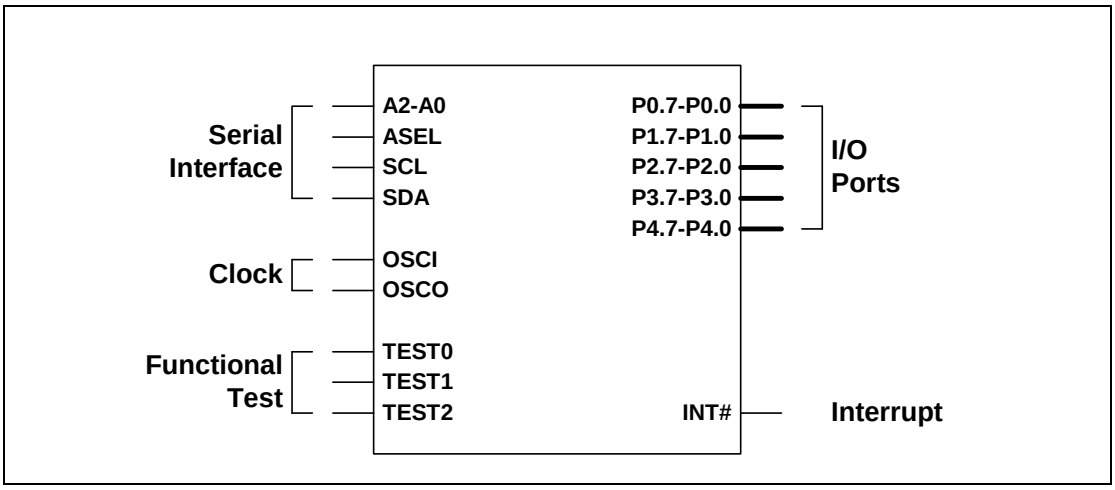

Figure 3-1. Functional Signal Grouping

PINOUT DIAGRAM

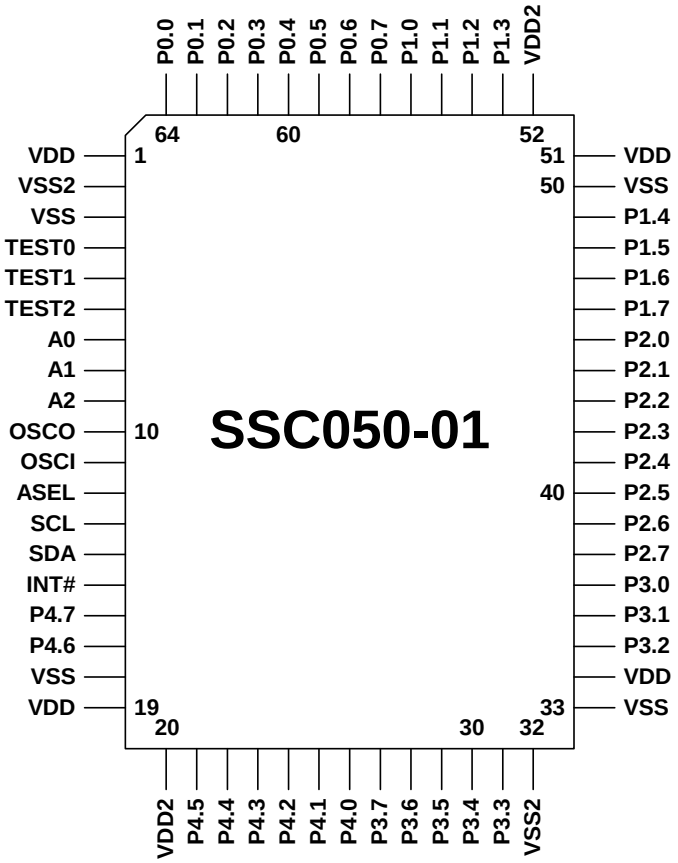

Figure 3-2. Pinout Diagram

PIN DESCRIPTION LIST

The following pin descriptions are grouped by function.

Table 3-1: Serial Interface

Pin Names	Pin No.	Type	Pin Description
A2-A0	9-7	Inputs	Address Select Bus This pin group provides the value, which will be compared to bits 3 through 1 of the serial slave address. These pins should be strapped to VDD or VSS to provide the appropriate binary value.
ASEL	12	Input	Device Type Address Select This pin provides the ability to select between two-device type address values in the serial slave address. When tied to VSS, the device type address is 1000b and when tied to VDD, the device type address is 1100b.
SCL	13	Input	Two-wire Serial Interface Clock This pin is used by the device to latch the data present on the SDA pin. This pin in conjunction with the SDA pin also determines Start and Stop conditions on the serial bus.
SDA	14	Bidirectional	Two-wire Serial Interface Data This pin is used to transfer all serial data into and out of the device. This pin in conjunction with the SCL pin also determines Start and Stop conditions on the serial bus.

Table 3-2: Clock

Pin Names	Pin No.	Type	Pin Description
OSCI	11	Input	Oscillator Input This pin is connected to one side of an external 10.0MHz crystal to produce the clock required for serial signal filtering, state machine clocking and flash rate generation. An alternate external 3.3 volt 10.0MHz clock source can be connected to this pin.
OSCO	10	Output	Oscillator Output This pin is connected to the other side of an external 10.0MHz crystal. When an alternate external clock source is used, this pin should be left unconnected.

Table 3-3: Interrupt

Pin Names	Pin No.	Type	Pin Description
INT#	15	Open-Drain Output	Interrupt This open-drain output can be used to signal the microcontroller that an event has occurred on an I/O pin which is configured as an input or that a special function event has occurred. This pin can be wire ORed with other open drain outputs to provide a single interrupt input source.

Table 3-4: I/O Ports

Pin Names	Pin No.	Type	Pin Description
P0.7-P0.0	57-64	Bidirectional	I/O Port 0 Port 0 is a dedicated eight-bit bidirectional I/O port. The user can select between an input, totem pole output or open-drain output. Additional capability to detect input edge changes and select various output flashing rates is also available.
P1.7-P1.0	46-49, 53-56	Bidirectional	I/O Port 1 Port 1 is a dedicated eight-bit bidirectional I/O port. The user can select between an input, totem pole output or open-drain output. Additional capability to detect input edge changes and select various output flashing rates is also available.
P2.7-P2.0 (Tach Inputs and PWM outputs)	38-45	Bidirectional	I/O Port 2 Port 2 is an eight-bit bidirectional I/O port. The user can select between an input, totem pole output or open-drain output. Additional capability to detect input edge changes and select various output flashing rates is also available. Through control register setup, P2.7-P2.4 can be dedicated to monitoring fans equipped with tachometer outputs. Through control register setup, P2.3-P2.0 can be dedicated to controlling fan speed utilizing pulse width modulated outputs.
P3.7-P3.0 (Bypass I/O)	27-31, 35-37	Bidirectional	I/O Port 3 Port 3 is a shared eight bit bidirectional I/O port which can be used as a general purpose I/O port or as Port Bypass control. The user can select between an input, totem pole output or open-drain output. Additional capability to detect input edge changes and select various output flashing rates is also available. Through control register setup, four two-bit portions of this port can be dedicated to the control of a combination of PBC/CRU/SDU functions. Any combination of port bypass control functions can be enabled with the remaining I/O pins used for general purpose functions.
P4.7-P4.0 (Bypass I/O)	16, 17, 21-26	Bidirectional	I/O Port 4 Port 4 is a shared eight bit bidirectional I/O port which can be used as a general purpose I/O port or as Port Bypass control. The user can select between an input, totem pole output or open-drain output. Additional capability to detect input edge changes and select various output flashing rates is also available. Through control register setup, four two-bit portions of this port can be dedicated to the control of a combination of PBC/CRU/SDU functions. Any combination of port bypass control functions can be enabled with the remaining I/O pins used for general purpose functions.

Table 3-5: Test

Pin Names	Pin No.	Type	Pin Description
TEST2- TEST0	6-4	Input	Functional Test These inputs allow the device to be placed in specific test modes for device level testing. These inputs should be connected to VSS for normal operation.

Table 3-6: Supply

Pin Names	Pin No.	Type	Pin Description
VDD	1, 19, 34, 51	Power	I/O Power These pins are the power sources for the I/O drivers of all non-analog output and bidirectional pins.
VSS	3, 18, 33, 50	Ground	I/O Ground These pins are the ground connections for the I/O drivers of all non-analog output and bidirectional pins.
VDD2	20, 52	Power	Digital Core Power These pins are the power sources for the digital core logic and receivers of all non-analog input and bidirectional pins.
VSS2	2, 32	Ground	Digital Core Ground These pins are the ground connections for the digital core logic and receivers of all non-analog input and bidirectional pins.

Chapter 4 CONTROL REGISTERS

This section contains descriptions for the device-specific control registers. All register locations are fixed within the device and are mapped for easy access as well as future enhancements.

The control register section is separated into three sub-sections; a register map, an address map and the bit level description of all registers. The register map lists all registers by operating address. The address map shows the relative layout of all control registers. All registers can be accessed at any time and no register function will interfere with the operation of the serial interface. However, changing register bits will have an immediate effect on the respective I/O lines.

REGISTER MAP

Table 4-1: Register Map

Data Memory Address	Read/Write	Label	Description
00h	R/W	GPD0	General Purpose I/O Port 0 Data Register
01h	R/W	GPD1	General Purpose I/O Port 1 Data Register
02h	R/W	GPD2	General Purpose I/O Port 2 Data Register
03h	R/W	GPD3	General Purpose I/O Port 3 Data Register
04h	R/W	GPD4	General Purpose I/O Port 4 Data Register
10h	R/W	DDP0	I/O Port 0 Data Direction Register
11h	R/W	DDP1	I/O Port 1 Data Direction Register
12h	R/W	DDP2	I/O Port 2 Data Direction Register
13h	R/W	DDP3	I/O Port 3 Data Direction Register
14h	R/W	DDP4	I/O Port 4 Data Direction Register
20h	R/W	PBC0	Port Bypass Control 0 Register
21h	R/W	PBC1	Port Bypass Control 1 Register
22h	R/W	PBC2	Port Bypass Control 2 Register
23h	R/W	PBC3	Port Bypass Control 3 Register

Table 4-1: Register Map (continued)

Data Memory Address	Read/Write	Label	Description
24h	R/W	PBC4	Port Bypass Control 4 Register
25h	R/W	PBC5	Port Bypass Control 5 Register
26h	R/W	PBC6	Port Bypass Control 6 Register
27h	R/W	PBC7	Port Bypass Control 7 Register
30h	R/W	FSC0	Fan Speed Control 0 Register
31h	R/W	FSCO0	Fan Speed Count Overflow 0 Register
32h	R	FSCC0	Fan Speed Current Count 0 Register
34h	R/W	FSC1	Fan Speed Control 1 Register
35h	R/W	FSCO1	Fan Speed Count Overflow 1 Register
36h	R	FSCC1	Fan Speed Current Count 1 Register
38h	R/W	FSC2	Fan Speed Control 2 Register
39h	R/W	FSCO2	Fan Speed Count Overflow 2 Register
3Ah	R	FSCC2	Fan Speed Current Count 2 Register
3Ch	R/W	FSC3	Fan Speed Control 3 Register
3Dh	R/W	FSCO3	Fan Speed Count Overflow 3 Register
3Eh	R	FSCC3	Fan Speed Current Count 3 Register
80h	R/W	BCP00	Bit Control Port 0 - Bit 0 Register
81h	R/W	BCP01	Bit Control Port 0 - Bit 1 Register
82h	R/W	BCP02	Bit Control Port 0 - Bit 2 Register
83h	R/W	BCP03	Bit Control Port 0 - Bit 3 Register
84h	R/W	BCP04	Bit Control Port 0 - Bit 4 Register
85h	R/W	BCP05	Bit Control Port 0 - Bit 5 Register
86h	R/W	BCP06	Bit Control Port 0 - Bit 6 Register
87h	R/W	BCP07	Bit Control Port 0 - Bit 7 Register
90h	R/W	BCP10	Bit Control Port 1 - Bit 0 Register
91h	R/W	BCP11	Bit Control Port 1 - Bit 1 Register
92h	R/W	BCP12	Bit Control Port 1 - Bit 2 Register
93h	R/W	BCP13	Bit Control Port 1 - Bit 3 Register
94h	R/W	BCP14	Bit Control Port 1 - Bit 4 Register
95h	R/W	BCP15	Bit Control Port 1 - Bit 5 Register
96h	R/W	BCP16	Bit Control Port 1 - Bit 6 Register
97h	R/W	BCP17	Bit Control Port 1 - Bit 7 Register

Table 4-1: Register Map (continued)

Data Memory Address	Read/Write	Label	Description
98h	R/W	PWMC0	Pulse Width Modulation Control 0 Register
99h	R/W	PWMC1	Pulse Width Modulation Control 1 Register
9Ah	R/W	PWMC2	Pulse Width Modulation Control 2 Register
9Bh	R/W	PWMC3	Pulse Width Modulation Control 3 Register
A0h	R/W	BCP20	Bit Control Port 2 - Bit 0 Register
A1h	R/W	BCP21	Bit Control Port 2 - Bit 1 Register
A2h	R/W	BCP22	Bit Control Port 2 - Bit 2 Register
A3h	R/W	BCP23	Bit Control Port 2 - Bit 3 Register
A4h	R/W	BCP24	Bit Control Port 2 - Bit 4 Register
A5h	R/W	BCP25	Bit Control Port 2 - Bit 5 Register
A6h	R/W	BCP26	Bit Control Port 2 - Bit 6 Register
A7h	R/W	BCP27	Bit Control Port 2 - Bit 7 Register
B0h	R/W	BCP30	Bit Control Port 3 - Bit 0 Register
B1h	R/W	BCP31	Bit Control Port 3 - Bit 1 Register
B2h	R/W	BCP32	Bit Control Port 3 - Bit 2 Register
B3h	R/W	BCP33	Bit Control Port 3 - Bit 3 Register
B4h	R/W	BCP34	Bit Control Port 3 - Bit 4 Register
B5h	R/W	BCP35	Bit Control Port 3 - Bit 5 Register
B6h	R/W	BCP36	Bit Control Port 3 - Bit 6 Register
B7h	R/W	BCP37	Bit Control Port 3 - Bit 7 Register
C0h	R/W	BCP40	Bit Control Port 4 - Bit 0 Register
C1h	R/W	BCP41	Bit Control Port 4 - Bit 1 Register
C2h	R/W	BCP42	Bit Control Port 4 - Bit 2 Register
C3h	R/W	BCP43	Bit Control Port 4 - Bit 3 Register
C4h	R/W	BCP44	Bit Control Port 4 - Bit 4 Register
C5h	R/W	BCP45	Bit Control Port 4 - Bit 5 Register
C6h	R/W	BCP46	Bit Control Port 4 - Bit 6 Register
C7h	R/W	BCP47	Bit Control Port 4 - Bit 7 Register
F8h	R/W	BCIS	Backplane Controller Interrupt Status Register
FCh	R/W	BCT	Backplane Controller Test Register
FDh	R/W	BCO	Backplane Controller Option Register
FFh	R	VER	Backplane Controller Version Register

ADDRESS MAP

Table 4-2: Address Map

11b	10b	01b	00b	Address
GPD3	GPD2	GPD1	GPD0	00h
reserved	reserved	reserved	GPD4	04h
reserved	reserved	reserved	reserved	08h
reserved	reserved	reserved	reserved	0Ch
DDP3	DDP2	DDP1	DDP0	10h
reserved	reserved	reserved	DDP4	14h
reserved	reserved	reserved	reserved	18h
reserved	reserved	reserved	reserved	1Ch
PBC3	PBC2	PBC1	PBC0	20h
PBC7	PBC6	PBC5	PBC4	24h
reserved	reserved	reserved	reserved	28h
reserved	reserved	reserved	reserved	2Ch
reserved	FSCC0	FSCO0	FSC0	30h
reserved	FSCC1	FSCO1	FSC1	34h
reserved	FSCC2	FSCO2	FSC2	38h
reserved	FSCC3	FSCO3	FSC3	3Ch
reserved	reserved	reserved	reserved	40h-7Ch
BCP03	BCP02	BCP01	BCP00	80h
BCP07	BCP06	BCP05	BCP04	84h
reserved	reserved	reserved	reserved	88h
reserved	reserved	reserved	reserved	8Ch
BCP13	BCP12	BCP11	BCP10	90h
BCP17	BCP16	BCP15	BCP14	94h
PWMC3	PWMC2	PWMC1	PWMC0	98h
reserved	reserved	reserved	reserved	9Ch
BCP23	BCP22	BCP21	BCP20	A0h
BCP27	BCP26	BCP25	BCP24	A4h
reserved	reserved	reserved	reserved	A8h
reserved	reserved	reserved	reserved	ACh
BCP33	BCP32	BCP31	BCP30	B0h

Table 4-2: Address Map (continued)

11b	10b	01b	00b	Address
BCP37	BCP36	BCP35	BCP34	B4h
reserved	reserved	reserved	reserved	B8h
reserved	reserved	reserved	reserved	BCh
BCP43	BCP42	BCP41	BCP40	C0h
BCP47	BCP46	BCP45	BCP44	C4h
reserved	reserved	reserved	reserved	C8h-F4h
reserved	reserved	reserved	BCIS	F8h
VER	reserved	BCO	BCT	FCh

CONTROL REGISTER DEFINITION

The register definition provides a bit-level description of all register bits including power-on and default values. The terms "set" and "assert" refer to bits which are programmed to a binary one. The terms "reset", "de-assert" and "clear" refer to bits which are programmed to a binary zero. Reserved bits are represented by "RES" and will always return an unknown value and should be masked. Any bits which are reserved should never be set to a binary one. These bits may be defined in future versions of the device.

00h: General Purpose I/O Port 0 Data (GPD0)

Register Name:	GPD0
Address:	00h
Reset Value:	XXXX_XXXXb
Description	General Purpose I/O Port 0 Data

7	6	5	4	3	2	1	0
General Purpose Data							

Bit(s)	Bit Label	Access	Description
7:0	GPD0.7-0	R/W	When the I/O pin has been enabled as an output, writing these bits determines the data value which will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading these register bits will represent the current voltage applied to the pin. At no time will the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors will hold the pin at a binary one. After a reset or power-on, the register bits will be set to a binary one, but the value returned from a register read will be the level applied to the pin since by default each pin is an input.

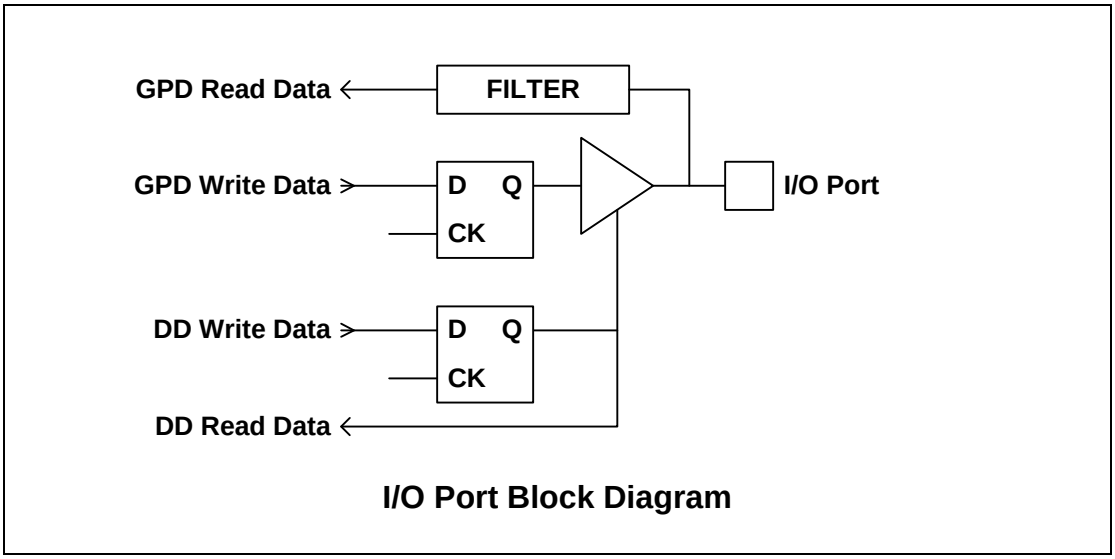

Figure 4-1. I/O Port Block Diagram

01h: General Purpose I/O Port 1 Data (GPD1)

Register Name:	GPD1
Address:	01h
Reset Value:	XXXX_XXXXb
Description	General Purpose I/O Port 1 Data

7	6	5	4	3	2	1	0
General Purpose Data							

Bit(s)	Bit Label	Access	Description
7:0	GPD0.7-0	R/W	When the I/O pin has been enabled as an output, writing these bits determines the data value which will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading these register bits will represent the current voltage applied to the pin. At no time will the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors will hold the pin at a binary one. After a reset or power-on, the register bits will be set to a binary one, but the value returned from a register read will be the level applied to the pin since by default each pin is an input.

02h: General Purpose I/O Port 2 Data (GPD2)

Register Name:	GPD2
Address:	02h
Reset Value:	XXXX_XXXXb
Description	General Purpose I/O Port 2 Data

7	6	5	4	3	2	1	0
General Purpose Data							

Bit(s)	Bit Label	Access	Description
7:0	GPD0.7-0	R/W	When the I/O pin has been enabled as an output, writing these bits determines the data value which will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading these register bits will represent the current voltage applied to the pin. At no time will the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors will hold the pin at a binary one. After a reset or power-on, the register bits will be set to a binary one, but the value returned from a register read will be the level applied to the pin since by default each pin is an input.

03h: General Purpose I/O Port 3 Data (GPD3)

Register Name:	GPD3
Address:	03h
Reset Value:	XXXX_XXXXb
Description	General Purpose I/O Port 3 Data

7	6	5	4	3	2	1	0
General Purpose Data							

Bit(s)	Bit Label	Access	Description
7:0	GPD0.7-0	R/W	When the I/O pin has been enabled as an output, writing these bits determines the data value which will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading these register bits will represent the current voltage applied to the pin. At no time will the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors will hold the pin at a binary one. After a reset or power-on, the register bits will be set to a binary one, but the value returned from a register read will be the level applied to the pin since by default each pin is an input.

04h: General Purpose I/O Port 4 Data (GPD4)

Register Name:	GPD4
Address:	04h
Reset Value:	XXXX_XXXXb
Description	General Purpose I/O Port 4 Data

7	6	5	4	3	2	1	0
General Purpose Data							

Bit(s)	Bit Label	Access	Description
7:0	GPD0.7-0	R/W	When the I/O pin has been enabled as an output, writing these bits determines the data value which will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading these register bits will represent the current voltage applied to the pin. At no time will the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors will hold the pin at a binary one. After a reset or power-on, the register bits will be set to a binary one, but the value returned from a register read will be the level applied to the pin since by default each pin is an input.

10h: I/O Port 0 Data Direction (DDP0)

Register Name:	DDP0
Address:	10h
Reset Value:	1111_1111b
Description	I/O Port 0 Data Direction

7	6	5	4	3	2	1	0
Data Direction							

Bit(s)	Bit Label	Access	Description
7:0	DDP0.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. Additionally, an open-drain or open-source function can be developed by resetting or setting the appropriate data bit and using the data direction bit as the programmed data value. After a reset or power-on, these bits will be set to a binary one, enabling the I/O as an input with weak pull-up.

11h: I/O Port 1 Data Direction (DDP1)

Register Name:	DDP1
Address:	11h
Reset Value:	1111_1111b
Description	I/O Port 1 Data Direction

7	6	5	4	3	2	1	0
Data Direction							

Bit(s)	Bit Label	Access	Description
7:0	DDP0.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. Additionally, an open-drain or open-source function can be developed by resetting or setting the appropriate data bit and using the data direction bit as the programmed data value. After a reset or power-on, these bits will be set to a binary one, enabling the I/O as an input with weak pull-up.

12h: I/O Port 2 Data Direction (DDP2)

Register Name:	DDP2
Address:	12h
Reset Value:	1111_1111b
Description	I/O Port 2 Data Direction

7	6	5	4	3	2	1	0
Data Direction							

Bit(s)	Bit Label	Access	Description
7:0	DDP0.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. Additionally, an open-drain or open-source function can be developed by resetting or setting the appropriate data bit and using the data direction bit as the programmed data value. After a reset or power-on, these bits will be set to a binary one, enabling the I/O as an input with weak pull-up.

13h: I/O Port 3 Data Direction (DDP3)

Register Name:	DDP3
Address:	13h
Reset Value:	1111_1111b
Description	I/O Port 3 Data Direction

7	6	5	4	3	2	1	0
Data Direction							

Bit(s)	Bit Label	Access	Description
7:0	DDP0.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. Additionally, an open-drain or open-source function can be developed by resetting or setting the appropriate data bit and using the data direction bit as the programmed data value. After a reset or power-on, these bits will be set to a binary one, enabling the I/O as an input with weak pull-up.

14h: I/O Port 4 Data Direction (DDP4)

Register Name:	DDP4
Address:	14h
Reset Value:	1111_1111b
Description	I/O Port 4 Data Direction

7	6	5	4	3	2	1	0
Data Direction							

Bit(s)	Bit Label	Access	Description
7:0	DDP0.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. Additionally, an open-drain or open-source function can be developed by resetting or setting the appropriate data bit and using the data direction bit as the programmed data value. After a reset or power-on, these bits will be set to a binary one, enabling the I/O as an input with weak pull-up.

20h: Port Bypass Control 0 (PBC0)

Register Name:	PBC0
Address:	20h
Reset Value:	00XX_XX1Xb
Description	Port Bypass Control 0

7	6	5	4	3	2	1	0
Port Bypass Control Enable	Signal Detected Interrupt Enable					Force Bypass	Signal Detected

Bit(s)	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P3.1 and P3.0 are automatically configured to provide a Force Bypass output pin and a Signal Detected input pin. Any other configuration which may have previously been enabled through other control registers will be overridden. When this bit is reset, the remaining bits in this register have no effect on the operation of P3.1 and P3.0.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input will be enabled to generate an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, transitions on the signal detected input will not generate an interrupt condition.
1	FB	R/W	Force Bypass This bit controls the P3.1 I/O pin which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in bypass mode. This register bit is automatically cleared when the synchronized and filtered P3.0 input is low which results in a maximum latency of 400 nanoseconds from detection of the loss of a high speed signal to the deassertion of the P3.1 output. ***NOTE:*** *Since all I/O pins on the device power-on as inputs with weak internal pull-ups, it is possible to define the default state of the force bypass function through the use of an external pull-down resistor. The default state of the I/O can be determined by reading this register since the read value of the register bits are always available through an input synchronizer and filter. Once the default state is determined, a write to the FB bit of this register with the default values as well as setting the PBCEN bit ensures that the port bypass control functions have been enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains high.*
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.0 I/O pin which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, a high speed signal has been detected by the signal detect unit. If this bit is reset, a high speed signal has not been detected by the signal detect unit.

21h: Port Bypass Control 1 (PBC1)

Register Name:	PBC1
Address:	21h
Reset Value:	00XX_XX1Xb
Description	Port Bypass Control 1

7	6	5	4	3	2	1	0
Port Bypass Control Enable	Signal Detected Interrupt Enable					Force Bypass	Signal Detected

Bit(s)	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P3.3 and P3.2 are automatically configured to provide a Force Bypass output pin and a Signal Detected input pin. Configurations for these I/O pins which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P3.3 and P3.2.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input will be enabled to generate an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, transitions on the signal detected input will not generate an interrupt condition.
1	FB	R/W	Force Bypass This bit controls the P3.3 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in bypass mode. This register bit is automatically cleared when the synchronized and filtered P3.2 input is low which results in a maximum latency of 400 nanosceonds from detection of the loss of a high speed signal to the de-assertion of the P3.1 output. ***NOTE:*** *Since all I/O pins on the device power-on as inputs with weak internal pull-ups, it is possible to define the default state of the force bypass function through the use of an external pull-down resistor. The default state of the I/O can be determined by reading this register since the read value of the register bits are always available through an input synchronizer and filter. Once the default state is determined, a write to the FB bit of this register with the default values as well as setting the PBCEN bit ensures that the port bypass control functions have been enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains high.*
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.2 I/O pin which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, a high speed signal has been detected by the signal detect unit. If this bit is reset, a high speed signal has not been detected by the signal detect unit.

22h: Port Bypass Control 2 (PBC2)

Register Name:	PBC2
Address:	22h
Reset Value:	00XX_XX1Xb
Description	Port Bypass Control 2

7	6	5	4	3	2	1	0
Port Bypass Control Enable	Signal Detected Interrupt Enable					Force Bypass	Signal Detected

Bit(s)	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P3.5 and P3.4 are automatically configured to provide a Force Bypass output pin and a Signal Detected input pin. Configurations for these I/O pins which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P3.5 and P3.4.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input will be enabled to generate an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, transitions on the signal detected input will not generate an interrupt condition.
1	FB	R/W	Force Bypass This bit controls the P3.5 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in bypass mode. This register bit is automatically cleared when the synchronized and filtered P3.4 input is low which results in a maximum latency of 400 nanosceonds from detection of the loss of a high speed signal to the de-assertion of the P3.1 output. ***NOTE:*** *Since all I/O pins on the device power-on as inputs with weak internal pull-ups, it is possible to define the default state of the force bypass function through the use of an external pull-down resistor. The default state of the I/O can be determined by reading this register since the read value of the register bits are always available through an input synchronizer and filter. Once the default state is determined, a write to the FB bit of this register with the default values as well as setting the PBCEN bit ensures that the port bypass control functions have been enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains high.*
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.4 I/O pin which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, a high speed signal has been detected by the signal detect unit. If this bit is reset, a high speed signal has not been detected by the signal detect unit.

23h: Port Bypass Control 3 (PBC3)

Register Name:	PBC3
Address:	23h
Reset Value:	00XX_XX1Xb
Description	Port Bypass Control 3

7	6	5	4	3	2	1	0
Port Bypass Control Enable	Signal Detected Interrupt Enable					Force Bypass	Signal Detected

Bit(s)	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P3.7 and P3.6 are automatically configured to provide a Force Bypass output pin and a Signal Detected input pin. Configurations for these I/O pins which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P3.7 and P3.6.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input will be enabled to generate an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, transitions on the signal detected input will not generate an interrupt condition.
1	FB	R/W	Force Bypass This bit controls the P3.7 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in bypass mode. This register bit is automatically cleared when the synchronized and filtered P3.6 input is low which results in a maximum latency of 400 nanosceonds from detection of the loss of a high speed signal to the de-assertion of the P3.1 output. ***NOTE:*** *Since all I/O pins on the device power-on as inputs with weak internal pull-ups, it is possible to define the default state of the force bypass function through the use of an external pull-down resistor. The default state of the I/O can be determined by reading this register since the read value of the register bits are always available through an input synchronizer and filter. Once the default state is determined, a write to the FB bit of this register with the default values as well as setting the PBCEN bit ensures that the port bypass control functions have been enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains high.*
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.4 I/O pin which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, a high speed signal has been detected by the signal detect unit. If this bit is reset, a high speed signal has not been detected by the signal detect unit.

24h: Port Bypass Control 4 (PBC4)

Register Name:	PBC4
Address:	24h
Reset Value:	00XX_XX1Xb
Description	Port Bypass Control 4

7	6	5	4	3	2	1	0
Port Bypass Control Enable	Signal Detected Interrupt Enable					Force Bypass	Signal Detected

Bit(s)	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P4.1 and P4.0 are automatically configured to provide a Force Bypass output pin and a Signal Detected input pin. Configurations for these I/O pins which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P4.1 and P4.0.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input will be enabled to generate an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, transitions on the signal detected input will not generate an interrupt condition.
1	FB	R/W	Force Bypass This bit controls the P4.1 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in bypass mode. This register bit is automatically cleared when the synchronized and filtered P4.0 input is low which results in a maximum latency of 400 nanosceonds from detection of the loss of a high speed signal to the de-assertion of the P3.1 output. ***NOTE:*** *Since all I/O pins on the device power-on as inputs with weak internal pull-ups, it is possible to define the default state of the force bypass function through the use of an external pull-down resistor. The default state of the I/O can be determined by reading this register since the read value of the register bits are always available through an input synchronizer and filter. Once the default state is determined, a write to the FB bit of this register with the default values as well as setting the PBCEN bit ensures that the port bypass control functions have been enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains high.*
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.4 I/O pin which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, a high speed signal has been detected by the signal detect unit. If this bit is reset, a high speed signal has not been detected by the signal detect unit.

25h: Port Bypass Control 5 (PBC5)

Register Name:	PBC5
Address:	25h
Reset Value:	00XX_XX1Xb
Description	Port Bypass Control 5

7	6	5	4	3	2	1	0
Port Bypass Control Enable	Signal Detected Interrupt Enable					Force Bypass	Signal Detected

Bit(s)	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P4.3 and P4.2 are automatically configured to provide a Force Bypass output pin and a Signal Detected input pin. Configurations for these I/O pins which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P4.3 and P4.2.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input will be enabled to generate an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, transitions on the signal detected input will not generate an interrupt condition.
1	FB	R/W	Force Bypass This bit controls the P4.3 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in bypass mode. This register bit is automatically cleared when the synchronized and filtered P4.2 input is low which results in a maximum latency of 400 nanosceonds from detection of the loss of a high speed signal to the de-assertion of the P3.1 output. ***NOTE:*** *Since all I/O pins on the device power-on as inputs with weak internal pull-ups, it is possible to define the default state of the force bypass function through the use of an external pull-down resistor. The default state of the I/O can be determined by reading this register since the read value of the register bits are always available through an input synchronizer and filter. Once the default state is determined, a write to the FB bit of this register with the default values as well as setting the PBCEN bit ensures that the port bypass control functions have been enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains high.*
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.4 I/O pin which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, a high speed signal has been detected by the signal detect unit. If this bit is reset, a high speed signal has not been detected by the signal detect unit.

26h: Port Bypass Control 6 (PBC6)

Register Name:	PBC6
Address:	26h
Reset Value:	00XX_XX1Xb
Description	Port Bypass Control 6

7	6	5	4	3	2	1	0
Port Bypass Control Enable	Signal Detected Interrupt Enable					Force Bypass	Signal Detected

Bit(s)	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P4.5 and P4.4 are automatically configured to provide a Force Bypass output pin and a Signal Detected input pin. Configurations for these I/O pins which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P4.5 and P4.4.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input will be enabled to generate an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, transitions on the signal detected input will not generate an interrupt condition.
1	FB	R/W	Force Bypass This bit controls the P4.5 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in bypass mode. This register bit is automatically cleared when the synchronized and filtered P4.4 input is low which results in a maximum latency of 400 nanosceonds from detection of the loss of a high speed signal to the de-assertion of the P3.1 output. ***NOTE:*** *Since all I/O pins on the device power-on as inputs with weak internal pull-ups, it is possible to define the default state of the force bypass function through the use of an external pull-down resistor. The default state of the I/O can be determined by reading this register since the read value of the register bits are always available through an input synchronizer and filter. Once the default state is determined, a write to the FB bit of this register with the default values as well as setting the PBCEN bit ensures that the port bypass control functions have been enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains high.*
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.4 I/O pin which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, a high speed signal has been detected by the signal detect unit. If this bit is reset, a high speed signal has not been detected by the signal detect unit.

27h: Port Bypass Control 7 (PBC7)

Register Name:	PBC7
Address:	27h
Reset Value:	00XX_XX1Xb
Description	Port Bypass Control 7

7	6	5	4	3	2	1	0
Port Bypass Control Enable	Signal Detected Interrupt Enable					Force Bypass	Signal Detected

Bit(s)	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P4.7 and P4.6 are automatically configured to provide a Force Bypass output pin and a Signal Detected input pin. Configurations for these I/O pins which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P4.7 and P4.6.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input will be enabled to generate an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, transitions on the signal detected input will not generate an interrupt condition.
1	FB	R/W	Force Bypass This bit controls the P4.7 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in bypass mode. This register bit is automatically cleared when the synchronized and filtered P4.6 input is low which results in a maximum latency of 400 nanosceonds from detection of the loss of a high speed signal to the de-assertion of the P3.1 output. ***NOTE:*** *Since all I/O pins on the device power-on as inputs with weak internal pull-ups, it is possible to define the default state of the force bypass function through the use of an external pull-down resistor. The default state of the I/O can be determined by reading this register since the read value of the register bits are always available through an input synchronizer and filter. Once the default state is determined, a write to the FB bit of this register with the default values as well as setting the PBCEN bit ensures that the port bypass control functions have been enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains high.*
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.4 I/O pin which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, a high speed signal has been detected by the signal detect unit. If this bit is reset, a high speed signal has not been detected by the signal detect unit.

30h: Fan Speed Control 0 Register (FSC0)

Register Name:	FSC0
Address:	30h
Reset Value:	00XX_XX00b
Description	Fan Speed Control 0. This register affects pin P2.4.

7	6	5	4	3	2	1	0
Fan Speed Control Enable	Fan Speed Interrupt Enable					Fan Divisor 1	Fan Divisor 0

Bit(s)	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.4 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). If the appropriate bypass bits have been set, the odd numbered fan speed input pins (P2.1, P2.3, P2.5, or P2.7) will be configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.4. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20KHz clock into an eight-bit counter. A divisor value stored in bits one and zero of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs which pulse twice per revolution. The FSCC0 register provides the user with an accurate binary fan speed count value which can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of VSS to VDD. If this input is supplied from a fan tachometer output which exceeds this range, external components will be required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.4 input will be enabled to generate an interrupt if the eight bit counter value is greater than or equal to the count overflow value loaded into the FSCO0 register. If the condition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, the fan speed monitoring logic will not generate an interrupt condition.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the eight-bit fan speed counter. Table 4-3 describes the available divisor values. The decimal count value can be calculated using the following equation: Decimal-Count-Value = (1,200,000)/(RPM X Divisor) Any nominal RPM value can be used in the above equation along with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an eight-bit counter. Typical applications may consider 60% to 70% of normal RPM a fan failure which would result in a decimal count value of 250(FAh) and 214(D6h) respectively at the above stated RPM values.

Table 4-3: Fan Divisor

FD1	FD0	Divisor	Nominal RPM	Decimal Count Value
0	0	1	8000	150(96h)
0	1	2	4000	150(96h)
1	0	4	2000	150(96h)
1	1	8	1000	150(96h)

31h: Fan Speed Count Overflow 0 (FSCO0, R/W)

Register Name:	FSCO0
Address:	31h
Reset Value:	0000_0000b
Description	Fan Speed Count Overflow 0. This register affects pin P2.4

7	6	5	4	3	2	1	0
Fan Speed Count Overflow							

Bit(s)	Bit Label	Access	Description
7	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the eight-bit fan speed counter. If the counter exceeds this value, an interrupt will be generated. This register should be loaded prior to setting the Fan Speed Control Enable (FSCEN) bit in the FSC0 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation where FF% is equal to the percentage of nominal RPM which constitutes a fan failure: Decimal-Overflow-Count-Value = (1,200,000)/(RPM X Divisor X FF%) Based on the above equation, a divisor of 8 and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic is capable of supporting a low end nominal RPM of 850. High end RPM values are basically unlimited but counter resolution will be diminished above 8000 RPM.

32h: Fan Speed Current Count 0 (FSCC0)

Register Name:	FSCC0
Address:	32h
Reset Value:	0000_0000b
Description	Fan Speed Current Count 0. This register affects pin P P2.4.

7	6	5	4	3	2	1	0
Fan Speed Current Count							

Bit(s)	Bit Label	Access	Description
7	FSCO7-0	R	These eight bits, when enabled by setting the FSCEN bit in the FSC0 register provide the user with an accurate binary fan speed count value which can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000)/(Decimal-Count-Value X Divisor) When the result of a read of this register is 00h, an accurate fan speed count value has not been generated indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or there are no tachometer pulses present. When operating in a polled mode with the FSIEN bit reset in the FSC0 register, this register will automatically update with an accurate fan speed count once per revolution of the fan. When operating in an interrupt mode with the FSIEN bit set in the FSC0 register, this register will automatically update with an accurate fan speed count once per revolution of the fan until an interrupt is generated. Once the interrupt is generated, the value will remain stable until the interrupt is cleared. When the interrupt is cleared, this register will also be cleared indicating that a valid RPM value is in the process of being generated.

34h: Fan Speed Control 1 (FSC1)

Register Name:	FSC1
Address:	34h
Reset Value:	00XX_XX00b
Description	Fan Speed Control 1. This register affects pin P2.5

7	6	5	4	3	2	1	0
Fan Speed Control Enable	Fan Speed Interrupt Enable					Fan Divisor 1	Fan Divisor 0

Bit(s)	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.5 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). If the appropriate bypass bits have been set, the odd numbered fan speed input pins (P1.1, P1.3, P1.5, P1.7, P2.1, P2.3, P2.5 or P2.7) will be configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.5. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20KHz clock into an eight-bit counter. A divisor value stored in bits one and zero of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs which pulse twice per revolution. The FSCC1 register provides the user with an accurate binary fan speed count value which can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of VSS to VDD. If this input is supplied from a fan tachometer output which exceeds this range, external components will be required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.5 input will be enabled to generate an interrupt if the eight bit counter value is greater than or equal to the count overflow value loaded into the FSCO1 register. If the condition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, the fan speed monitoring logic will not generate an interrupt condition.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the eight-bit fan speed counter. Table 4-4 describes the available divisor values: The decimal count value can be calculated using the following equation: Decimal-Count-Value = (1,200,000)/(RPM X Divisor) Any nominal RPM value can be used in the above equation along with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an eight-bit counter. Typical applications may consider 60% to 70% of normal RPM a fan failure which would result in a decimal count value of 250 (FAh) and 214 (D6h) respectively at the above stated RPM values.

Table 4-4: Fan Divisor

FD1	FD0	Divisor	Nominal RPM	Decimal Count Value
0	0	1	8000	150(96h)
0	1	2	4000	150(96h)
1	0	4	2000	150(96h)
1	1	8	1000	150(96h)

35h: Fan Speed Count Overflow 1 (FSCO1)

Register Name:	FSCO1
Address:	35h
Reset Value:	0000_0000b
Description	Fan Speed Count Overflow 1. This register affects pin P2.5

7	6	5	4	3	2	1	0
Fan Speed Count Overflow							

Bit(s)	Bit Label	Access	Description
7	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the eight-bit fan speed counter. If the counter exceeds this value, an interrupt will be generated. This register should be loaded prior to setting the Fan Speed Control Enable (FSCEN) bit in the FSC1 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation where FF% is equal to the percentage of nominal RPM which constitutes a fan failure: Decimal-Overflow-Count-Value = (1,200,000)/(RPM X Divisor X FF%) Based on the above equation, a divisor of 8 and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic is capable of supporting a low end nominal RPM of 850. High end RPM values are basically unlimited but counter resolution will be diminished above 8000 RPM.

36h: Fan Speed Current Count 1 (FSCC1)

Register Name:	FSCC1
Address:	36h
Reset Value:	0000_0000b
Description	Fan Speed Current Count 1. This register affects pin P2.5.

7	6	5	4	3	2	1	0
Fan Speed Current Count							

Bit(s)	Bit Label	Access	Description
7	FSCO7-0	R	These eight bits, when enabled by setting the FSCEN bit in the FSC1 register provide the user with an accurate binary fan speed count value which can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000)/(Decimal-Count-Value X Divisor) When the result of a read of this register is 00h, an accurate fan speed count value has not been generated indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or there are no tachometer pulses present. When operating in a polled mode with the FSIEN bit reset in the FSC1 register, this register will automatically update with an accurate fan speed count once per revolution of the fan. When operating in an interrupt mode with the FSIEN bit set in the FSC1 register, this register will automatically update with an accurate fan speed count once per revolution of the fan until an interrupt is generated. Once the interrupt is generated, the value will remain stable until the interrupt is cleared. When the interrupt is cleared, this register will also be cleared indicating that a valid RPM value is in the process of being generated.

38h: Fan Speed Control 2 (FSC2)

Register Name:	FSC2
Address:	38h
Reset Value:	00XX_XX00b
Description	Fan Speed Control 2. This register affects pin P2.6

7	6	5	4	3	2	1	0
Fan Speed Control Enable	Fan Speed Interrupt Enable					Fan Divisor 1	Fan Divisor 0

Bit(s)	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.6 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). If the appropriate bypass bits have been set, the odd numbered fan speed input pins (P1.1, P1.3, P1.5, P1.7, P2.1, P2.3, P2.5 or P2.7) will be configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.6. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20KHz clock into an eight-bit counter. A divisor value stored in bits one and zero of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs which pulse twice per revolution. The FSCC2 register provides the user with an accurate binary fan speed count value which can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of VSS to VDD. If this input is supplied from a fan tachometer output which exceeds this range, external components will be required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.6 input will be enabled to generate an interrupt if the eight bit counter value is greater than or equal to the count overflow value loaded into the FSCO0 register. If the condition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, the fan speed monitoring logic will not generate an interrupt condition.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the eight-bit fan speed counter. Table 4-5 describes the available divisor values: The decimal count value can be calculated using the following equation: Decimal-Count-Value = (1,200,000)/(RPM X Divisor) Any nominal RPM value can be used in the above equation along with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an eight-bit counter. Typical applications may consider 60% to 70% of normal RPM a fan failure which would result in a decimal count value of 250 (FAh) and 214 (D6h) respectively at the above stated RPM values.

Table 4-5: Fan Divisor

FD1	FD0	Divisor	Nominal RPM	Decimal Count Value
0	0	1	8000	150(96h)
0	1	2	4000	150(96h)
1	0	4	2000	150(96h)
1	1	8	1000	150(96h)

39h: Fan Speed Count Overflow 2 (FSCO2)

Register Name:	FSCO2
Address:	39h
Reset Value:	0000_0000b
Description	Fan Speed Count Overflow 2. This register affects pin P2.6.

7	6	5	4	3	2	1	0
Fan Speed Count Overflow							

Bit(s)	Bit Label	Access	Description
7	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the eight-bit fan speed counter. If the counter exceeds this value, an interrupt will be generated. This register should be loaded prior to setting the Fan Speed Control Enable (FSCEN) bit in the FSC2 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation where FF% is equal to the percentage of nominal RPM which constitutes a fan failure: Decimal-Overflow-Count-Value = (1,200,000)/(RPM X Divisor X FF%) Based on the above equation, a divisor of 8 and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic is capable of supporting a low end nominal RPM of 850. High end RPM values are basically unlimited but counter resolution will be diminished above 8000 RPM.

3Ah: Fan Speed Current Count 2 (FSCC2)

Register Name:	FSCC2
Address:	3Ah
Reset Value:	0000_0000b
Description	Fan Speed Current Count 2. This register affects pin P2.6.

7	6	5	4	3	2	1	0
Fan Speed Current Count							

Bit(s)	Bit Label	Access	Description
7	FSCO7-0	R/W	These eight bits, when enabled by setting the FSCEN bit in the FSC2 register provide the user with an accurate binary fan speed count value which can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000)/(Decimal-Count-Value X Divisor) When the result of a read of this register is 00h, an accurate fan speed count value has not been generated indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or there are no tachometer pulses present. When operating in a polled mode with the FSIEN bit reset in the FSC2 register, this register will automatically update with an accurate fan speed count once per revolution of the fan. When operating in an interrupt mode with the FSIEN bit set in the FSC2 register, this register will automatically update with an accurate fan speed count once per revolution of the fan until an interrupt is generated. Once the interrupt is generated, the value will remain stable until the interrupt is cleared. When the interrupt is cleared, this register will also be cleared indicating that a valid RPM value is in the process of being generated.

3Ch: Fan Speed Control 3 (FSC3)

Register Name:	FSC3
Address:	3Ch
Reset Value:	00XX_XX00b
Description	Fan Speed Control 3. This register affects pin P2.7.

7	6	5	4	3	2	1	0
Fan Speed Control Enable	Fan Speed Interrupt Enable					Fan Divisor 1	Fan Divisor 0

Bit(s)	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.7 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin which may have previously been enabled through other control registers will be overridden except for the bypass select function (bits 6 and 5 of the appropriate Bit Control Registers). If the appropriate bypass bits have been set, the odd numbered fan speed input pins (P1.1, P1.3, P1.5, P1.7, P2.1, P2.3, P2.5 or P2.7) will be configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.7. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20KHz clock into an eight-bit counter. A divisor value stored in bits one and zero of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs which pulse twice per revolution. The FSCC3 register provides the user with an accurate binary fan speed count value which can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of VSS to VDD. If this input is supplied from a fan tachometer output which exceeds this range, external components will be required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.7 input will be enabled to generate an interrupt if the eight bit counter value is greater than or equal to the count overflow value loaded into the FSCO0 register. If the condition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. When this bit is reset, the fan speed monitoring logic will not generate an interrupt condition.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the eight-bit fan speed counter. Table 4-6 describes the available divisor values: The decimal count value can be calculated using the following equation: Decimal-Count-Value = (1,200,000)/(RPM X Divisor) Any nominal RPM value can be used in the above equation along with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an eight-bit counter. Typical applications may consider 60% to 70% of normal RPM a fan failure which would result in a decimal count value of 250 (FAh) and 214 (D6h) respectively at the above stated RPM values.

Table 4-6: Fan Divisor

FD1	FD0	Divisor	Nominal RPM	Decimal Count Value
0	0	1	8000	150(96h)
0	1	2	4000	150(96h)
1	0	4	2000	150(96h)
1	1	8	1000	150(96h)

3Dh: Fan Speed Count Overflow 3 (FSCO3)

Register Name:	FSCO3
Address:	3Dh
Reset Value:	0000_0000b
Description	Fan Speed Count Overflow 3. This register affects pin P2.7.

7	6	5	4	3	2	1	0
Fan Speed Count Overflow							

Bit(s)	Bit Label	Access	Description
7	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the eight-bit fan speed counter. If the counter exceeds this value, an interrupt will be generated. This register should be loaded prior to setting the Fan Speed Control Enable (FSCEN) bit in the FSC1 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation where FF% is equal to the percentage of nominal RPM which constitutes a fan failure: Decimal-Overflow-Count-Value = (1,200,000)/(RPM X Divisor X FF%) Based on the above equation, a divisor of 8 and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic is capable of supporting a low end nominal RPM of 850. High end RPM values are basically unlimited but counter resolution will be diminished above 8000 RPM.

3Eh: Fan Speed Current Count 3 (FSCC3)

Register Name:	FSCC3
Address:	3Eh
Reset Value:	0000_0000b
Description	Fan Speed Current Count 3. This register affects pin P2.7.

7	6	5	4	3	2	1	0
Fan Speed Current Count							

Bit(s)	Bit Label	Access	Description
7	FSCO7-0	R/W	These eight bits, when enabled by setting the FSCEN bit in the FSC3 register provide the user with an accurate binary fan speed count value which can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000)/(Decimal-Count-Value X Divisor) When the result of a read of this register is 00h, an accurate fan speed count value has not been generated indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or there are no tachometer pulses present. When operating in a polled mode with the FSIEN bit reset in the FSC3 register, this register will automatically update with an accurate fan speed count once per revolution of the fan. When operating in an interrupt mode with the FSIEN bit set in the FSC3 register, this register will automatically update with an accurate fan speed count once per revolution of the fan until an interrupt is generated. Once the interrupt is generated, the value will remain stable until the interrupt is cleared. When the interrupt is cleared, this register will also be cleared indicating that a valid RPM value is in the process of being generated.

80h-87h: Bit Control Port 0 Registers (BCP00-BCP07)

Register Name:	BCP00-BCP07
Address:	80h - 87h
Reset Value:	0000_001Xb
Description	Bit Control Port 0 Registers These eight registers provide individual bit control for the Port 0 I/O pins. All register bits are identical from a control and status perspective with the only difference being the individual I/O pin controlled. The Data Direction (bit 1) and General Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths.

7	6	5	4	3	2	1	0
			Function Select			Data Direction	General Purpose Data

Bit(s)	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the DD and GPD bits, determine the function of each I/O pin. When configured as an output, these bits determine the rate at which the high current drive I/O will toggle, providing a simple mechanism for flashing LED's. The five bits allow the user to select one of seven flash rates as well as drive the LED both on and off. It is assumed that the LED is connected to VDD through an external current limiting resistor. Table 4-7 describes the possible combinations which can be used to drive an LED. When configured as an input, these bits determine the type of I/O pin edge transition which will generate an interrupt condition. Transition detectors within the device will filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. Table 4-8 describes the available input edge combinations. ***NOTE:*** *When configuring an I/O pin from an output to an input with interrupt enabled, it is suggested that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition which occurs as a result of the data direction change which may rely on the weak internal pull-up will not generate an unexpected interrupt.*
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. Additionally, an open-drain or open-source function can be developed by resetting or setting the appropriate data bit and using the data direction bit as the programmed data value. After a reset or power-on, this bit will be set to a binary one, enabling the I/O pin as an input with weak pull-up.
0	GPD	R/W	General Purpose Data When the I/O pin has been enabled as an output, writing this bit determines the data value which will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading this register bit will represent the current voltage applied to the pin. At no time will this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor will hold the pin at a binary one. After a reset or power-on, this register bit will be set to a binary one, but the value returned from a register read will be the level applied to the pin since by default each pin is an input.

Table 4-7: LED Combinations

FS2	FS1	FS0	DD	GPD	I/O State	LED State
0	0	0	0	0	output low	LED turned on
0	0	0	0	1	output high	LED turned off
0	0	0	1	X	pulled-up input	LED turned off - default state
0	0	1	0	X	output toggling	LED flashing at 0.25Hz
0	1	0	0	X	output toggling	LED flashing at 0.33Hz
0	1	1	0	X	output toggling	LED flashing at 0.50Hz
1	0	0	0	X	output toggling	LED flashing at 1.00Hz
1	0	1	0	X	output toggling	LED flashing at 2.00Hz
1	1	0	0	X	output toggling	LED flashing at 3.08Hz
1	1	1	0	X	output toggling	LED flashing at 4.00Hz
NOTE: *The I/O is driven in an open drain mode when configured as a toggling output.*						

Table 4-8: Input Edge Combinations

FS2	FS1	FS0	DD	GPD	Interrupt Condition
0	0	0	1	X	No interrupt generated - default state
X	0	1	1	X	Interrupt generated on a rising edge
X	1	0	1	X	Interrupt generated on a falling edge
X	1	1	1	X	Interrupt generated on either edge
1	0	0	1	X	No interrupt generated

90h-97h: Bit Control Port 1 Registers (BCP10-BCP17)

Register Name:	BCP10-BCP17
Address:	90h-97h
Reset Value:	0000_001Xb
Description	Bit Control Port 1 Registers These eight registers provide individual bit control for the Port 0 I/O pins. All register bits are identical from a control and status perspective with the only difference being the individual I/O pin controlled and the presence of the bypass function. The Data Direction (bit 1) and General Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths. These eight registers function the same as the eight Bit Control Port 0 Registers, described above, except that they relate to the Port 1 I/O pins.

7	6	5	4	3	2	1	0
			Function Select			Data Direction	General Purpose Data

Bit(s)	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the DD and GPD bits, determine the function of each I/O pin. When configured as an output, these bits determine the rate at which the high current drive I/O will toggle, providing a simple mechanism for flashing LED's. The five bits allow the user to select one of seven flash rates as well as drive the LED both on and off. It is assumed that the LED is connected to VDD through an external current limiting resistor. Table 4-7 describes the possible combinations which can be used to drive an LED. When configured as an input, these bits determine the type of I/O pin edge transition which will generate an interrupt condition. Transition detectors within the device will filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. Table 4-8 describes the available input edge combinations. ***NOTE:*** *When configuring an I/O pin from an output to an input with interrupt enabled, it is suggested that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition which occurs as a result of the data direction change which may rely on the weak internal pull-up will not generate an unexpected interrupt.*
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. Additionally, an open-drain or open-source function can be developed by resetting or setting the appropriate data bit and using the data direction bit as the programmed data value. After a reset or power-on, this bit will be set to a binary one, enabling the I/O pin as an input with weak pull-up.

Bit(s)	Bit Label	Access	Description
0	GPD	R/W	General Purpose Data When the I/O pin has been enabled as an output, writing this bit determines the data value which will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading this register bit will represent the current voltage applied to the pin. At no time will this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor will hold the pin at a binary one. After a reset or power-on, this register bit will be set to a binary one, but the value returned from a register read will be the level applied to the pin since by default each pin is an input.

98h-9Bh: Pulse Width Modulation Control Registers (PWMC0-PWMC3)

Register Name:	PWMC0-PWMC3
Address:	98h-9Bh
Reset Value:	X000_0000b
Description	Pulse Width Modulation Control These four registers provide a pulse width modulated output which can optionally be made available on the P2.0 through P2.3 I/O pins. Configurations for these I/O pins which may have previously been enabled through other control registers will be overridden if either or both of the PWBF bits are set. The PWBF bits have higher priority control over the P2.0 through P2.3 I/O pins than any other mode of operation. The pulse width modulated outputs are based on a 32 step counter and provide values from a 3.125% to a 100% duty cycle in 3.125% increments.

7	6	5	4	3	2	1	0
	Pulse Width Base Frequency		Pulse Width Percentage				

Bit(s)	Bit Label	Access	Description
6:5	PWBF1-0	R/W	Pulse Width Base Frequency These two bits determine the base operating frequency of the pulse width modulated output. These frequencies are based on the input clock rate of 10.0MHz. Three additional base frequency ranges are available and are selected through bits 5 and 4 of the Backplane Controller Option Register located at address FDh. The following table describes the default base frequencies:
4:0	PWP4-0	R/W	Pulse Width Percentage These five bits determine the percentage of high time that the output pulse will contain. There are 32 steps that can be adjusted in 3.125% increments. Table 4-9 describes the available percentages:

PWBF1	PWBF0	Pulse Width Base Frequency
0	0	normal operation - control is provided through GPD1/DDP1 or BCP1
0	1	26KHz base frequency
1	0	52KHz base frequency
1	1	104KHz base frequency

Table 4-9: Pulse Width Percentages

PWP4	PWP3	PWP2	PWP1	PWP0	Pulse Width Percentage
0	0	0	0	0	3.125% on/high time
0	0	0	0	1	6.25% on/high time
0	0	0	1	0	9.375% on/high time

Table 4-9: Pulse Width Percentages

PWP4	PWP3	PWP2	PWP1	PWP0	Pulse Width Percentage
0	0	0	1	1	12.5% on/high time
0	0	1	0	0	15.625% on/high time
0	0	1	0	1	18.75% on/high time
0	0	1	1	0	21.875% on/high time
0	0	1	1	1	25.0% on/high time
0	1	0	0	0	28.125% on/high time
0	1	0	0	1	31.25% on/high time
0	1	0	1	0	34.375% on/high time
0	1	0	1	1	37.5% on/high time
0	1	1	0	0	40.625% on/high time
0	1	1	0	1	43.75% on/high time
0	1	1	1	0	46.875% on/high time
0	1	1	1	1	50.0% on/high time
1	0	0	0	0	53.125% on/high time
1	0	0	0	1	56.25% on/high time
1	0	0	1	0	59.375% on/high time
1	0	0	1	1	62.5% on/high time
1	0	1	0	0	65.625% on/high time
1	0	1	0	1	68.75% on/high time
1	0	1	1	0	71.875% on/high time
1	0	1	1	1	75.0% on/high time
1	1	0	0	0	78.125% on/high time
1	1	0	0	1	81.25% on/high time
1	1	0	1	0	84.375% on/high time
1	1	0	1	1	87.5% on/high time
1	1	1	0	0	90.625% on/high time
1	1	1	0	1	93.75% on/high time
1	1	1	1	0	96.875% on/high time
1	1	1	1	1	100% on/high time

A0h-A7h: Bit Control Port 2 Registers (BCP20-BCP27)

Register Name:	BCP20-BCP27
Address:	A0h-A7h
Reset Value:	0000_001Xb
Description	Bit Control Port 2 Registers These eight registers provide individual bit control for the Port 0 I/O pins. All register bits are identical from a control and status perspective with the only difference being the individual I/O pin controlled and the presence of the bypass function. The Data Direction (bit 1) and General Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths. These eight registers function the same as the eight Bit Control Port 0 Registers, described above, except that they relate to the Port 2 I/O pins.

7	6	5	4	3	2	1	0
			Function Select			Data Direction	General Purpose Data

Bit(s)	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the DD and GPD bits, determine the function of each I/O pin. When configured as an output, these bits determine the rate at which the high current drive I/O will toggle, providing a simple mechanism for flashing LED's. The five bits allow the user to select one of seven flash rates as well as drive the LED both on and off. It is assumed that the LED is connected to VDD through an external current limiting resistor. Table 4-7 describes the possible combinations which can be used to drive an LED. When configured as an input, these bits determine the type of I/O pin edge transition which will generate an interrupt condition. Transition detectors within the device will filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. Table 4-8 describes the available input edge combinations. ***NOTE:*** *When configuring an I/O pin from an output to an input with interrupt enabled, it is suggested that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition which occurs as a result of the data direction change which may rely on the weak internal pull-up will not generate an unexpected interrupt.*
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. Additionally, an open-drain or open-source function can be developed by resetting or setting the appropriate data bit and using the data direction bit as the programmed data value. After a reset or power-on, this bit will be set to a binary one, enabling the I/O pin as an input with weak pull-up.

Bit(s)	Bit Label	Access	Description
0	GPD	R/W	General Purpose Data When the I/O pin has been enabled as an output, writing this bit determines the data value which will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading this register bit will represent the current voltage applied to the pin. At no time will this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor will hold the pin at a binary one. After a reset or power-on, this register bit will be set to a binary one, but the value returned from a register read will be the level applied to the pin since by default each pin is an input.

B0h-B7h: Bit Control Port 3 Registers (BCP30-BCP37)

Register Name:	BCP30-BCP37
Address:	B0h-B7h
Reset Value:	0000_001Xb
Description	Bit Control Port 3 Registers These eight registers provide individual bit control for the Port 0 I/O pins. All register bits are identical from a control and status perspective with the only difference being the individual I/O pin controlled and the presence of the bypass function. The Data Direction (bit 1) and General Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths. These eight registers function the same as the eight Bit Control Port 0 Registers, described above, except that they relate to the Port 3 I/O pins. In addition, the control of the individual I/O pins assigned to these registers can be overridden by the PBC0, PBC1, PBC2 and PBC3 registers when port bypass control is required.

7	6	5	4	3	2	1	0
			Function Select			Data Direction	General Purpose Data

Bit(s)	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the DD and GPD bits, determine the function of each I/O pin. When configured as an output, these bits determine the rate at which the high current drive I/O will toggle, providing a simple mechanism for flashing LED's. The five bits allow the user to select one of seven flash rates as well as drive the LED both on and off. It is assumed that the LED is connected to VDD through an external current limiting resistor. Table 4-7 describes the possible combinations which can be used to drive an LED. When configured as an input, these bits determine the type of I/O pin edge transition which will generate an interrupt condition. Transition detectors within the device will filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. Table 4-8 describes the available input edge combinations. ***NOTE:*** *When configuring an I/O pin from an output to an input with interrupt enabled, it is suggested that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition which occurs as a result of the data direction change which may rely on the weak internal pull-up will not generate an unexpected interrupt.*
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. Additionally, an open-drain or open-source function can be developed by resetting or setting the appropriate data bit and using the data direction bit as the programmed data value. After a reset or power-on, this bit will be set to a binary one, enabling the I/O pin as an input with weak pull-up.

Bit(s)	Bit Label	Access	Description
0	GPD	R/W	General Purpose Data When the I/O pin has been enabled as an output, writing this bit determines the data value which will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading this register bit will represent the current voltage applied to the pin. At no time will this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor will hold the pin at a binary one. After a reset or power-on, this register bit will be set to a binary one, but the value returned from a register read will be the level applied to the pin since by default each pin is an input.

C0h-C7h: Bit Control Port 4 Registers (BCP40-BCP47)

Register Name:	BCP40-BCP47
Address:	C0h-C7h
Reset Value:	0000_001Xb
Description	Bit Control Port 11 Registers These eight registers provide individual bit control for the Port 0 I/O pins. All register bits are identical from a control and status perspective with the only difference being the individual I/O pin controlled and the presence of the bypass function. The Data Direction (bit 1) and General Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths. These eight registers function the same as the eight Bit Control Port 0 Registers, described above, except that they relate to the Port 4 I/O pins. In addition, the control of the individual I/O pins assigned to these registers can be overridden by the PBC4, PBC5, PBC6 and PBC7 registers when port bypass control is required.

7	6	5	4	3	2	1	0
			Function Select			Data Direction	General Purpose Data

Bit(s)	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the DD and GPD bits, determine the function of each I/O pin. When configured as an output, these bits determine the rate at which the high current drive I/O will toggle, providing a simple mechanism for flashing LED's. The five bits allow the user to select one of seven flash rates as well as drive the LED both on and off. It is assumed that the LED is connected to VDD through an external current limiting resistor. Table 4-7 describes the possible combinations which can be used to drive an LED. When configured as an input, these bits determine the type of I/O pin edge transition which will generate an interrupt condition. Transition detectors within the device will filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin will assert and a binary value equal to the address of this register will appear in the BCIS register. Table 4-8 describes the available input edge combinations. ***NOTE:*** *When configuring an I/O pin from an output to an input with interrupt enabled, it is suggested that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition which occurs as a result of the data direction change which may rely on the weak internal pull-up will not generate an unexpected interrupt.*
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. Additionally, an open-drain or open-source function can be developed by resetting or setting the appropriate data bit and using the data direction bit as the programmed data value. After a reset or power-on, this bit will be set to a binary one, enabling the I/O pin as an input with weak pull-up.

Bit(s)	Bit Label	Access	Description
0	GPD	R/W	General Purpose Data When the I/O pin has been enabled as an output, writing this bit determines the data value which will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading this register bit will represent the current voltage applied to the pin. At no time will this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor will hold the pin at a binary one. After a reset or power-on, this register bit will be set to a binary one, but the value returned from a register read will be the level applied to the pin since by default each pin is an input.

F8h: Backplane Controller Interrupt Status (BCIS)

Register Name:	BCIS
Address:	F8h
Reset Value:	0000_0000b
Description	Backplane Controller Interrupt Status Register

7	6	5	4	3	2	1	0
Interrupt Active							

Bit(s)	Bit Label	Access	Description
7:0	IA7-0	R	Interrupt Active These eight bits determine the currently active interrupt source which has been enabled through the Port Bypass Control registers, the Fan Speed Control registers or the Bit Control registers. The address of the Port Bypass Control registers, the address of the Bit Control registers or the address of the Fan Speed Control registers will be generated as an indicator of the currently active interrupt source. If multiple interrupt sources are active, the value generated will be prioritized from the lowest binary value to the highest binary value. To clear the current interrupt and deassert the INT# pin, a value of FFh must be written to this register. If a higher binary value/lower priority interrupt source is still active, the new value will be generated and the INT# pin will re-assert.

FCh: Backplane Controller Test (BCT)

Register Name:	BCT
Address:	FCh
Reset Value:	0XXX_X000b
Description	Backplane Controller Interrupt Status Register

7	6	5	4	3	2	1	0
Soft Reset					Fan Speed Bypass	Flash Rate Bypass	Serial Interface Filter Bypass

Bit(s)	Bit Label	Access	Description
7	SRST	R/W	Soft Reset Setting this bit resets the device at the end of the current serial transfer. All I/O's, control registers, clock dividers and the slave state machine are reset by this bit. This bit is self resetting and writes of a zero to this bit will have no effect on the current state of the device.
2	FSB	R/W	Fan Speed Bypass Setting this bit causes the main clock divider for the fan speed monitors to be bypassed. Bypassing the main clock divider causes the fan speed counters to operate 500 times faster than normal. When reset or after power-on, the normal clock divider will be activated. This bit should not be set during normal operation.
1	FRB	R/W	Flash Rate Bypass Setting this bit causes the main clock divider for the flash rate generators to be bypassed. Bypassing the main clock divider causes the expected flash rates to be 125,000 times faster than normal. When reset or after power-on, the normal clock divider will be activated. This bit should not be set during normal operation.
0	SIFB	R/W	Serial Interface Filter Bypass Setting this bit causes the digital filters on the SCL and SDA pins to be bypassed. Bypassing the filters allows the serial transfer speed to be increased for test purposes. When reset or after power-on, normal filtering will be activated. This bit should not be set during normal operation.

FDh: Backplane Controller Option (BCO)

Register Name:	BCO
Address:	FDh
Reset Value:	X000_XXXXb
Description	Backplane Controller Interrupt Status Register

7	6	5	4	3	2	1	0
	Tach Filter Extend	Pulse Width Modulation Divider Select					

Bit(s)	Bit Label	Access	Description
6	TFE	R/W	Tach Filter Extend Setting this bit causes the input filters on P1.0 through P2.7 to be extended from a two stage voting circuit to a five stage voting circuit. Additional noise immunity of approximately 300 nanoseconds will be achieved. This bit enables the filter extension logic on all tach inputs and is independent of the tach control logic. The extended filters on P1.0 through P2.7 can be used in other applications with noisy signaling that require an enhanced input filter. After a reset or power-on, this register bit will be cleared to a zero, enabling normal input filter operation.
5:4	PDS1-0	R/W	Pulse Width Modulation Divider Select These two bits determine the divider that is used for the pulse width modulation circuits. The base frequency range of all pulse width modulation circuits are controlled by these bits. Each pulse width modulation circuit can be programmed to select one of the three available frequencies within the range. After a reset or power-on, these register bits will be cleared to a zero. The following table describes the available frequency ranges:

Table 4-10: Pulse Width Modulation Frequencies

PDS1	PDS0	Pulse Width Modulation Frequency Range
0	0	26KHz, 52KHz or 104KHz (divide by 3)
0	1	5.2KHz, 10.4KHz or 20.8KHz (divide by 15)
1	0	1.04KHz, 2.08KHz or 4.16KHz (divide by 75)
1	1	208Hz, 416Hz, 833Hz (divide by 375)

FFh: Backplane Controller Version (VER)

Register Name:	VER
Address:	FFh
Reset Value:	0001_0001b
Description	Backplane Controller Version Register

7	6	5	4	3	2	1	0
Version							

Bit(s)	Bit Label	Access	Description
7:0	VER7-0	R/W	Version These bits define the current version of the Backplane Controller. If revisions are required, these bits will change to reflect the latest version of the device. In general, changes to bits 3 through 0 will reflect a minor revision and changes to bits 7 through 4 will reflect a major revision or different device type. Firmware should check this register to determine the current capabilities of the device. ***NOTE:*** *The SSC050-01 and SSC050 currently utilize the same binary value in the Version Register. However, the device type can be determined by performing the following register write and read before configuring the device for normal operation. Write a 15h to the Pulse Width Modulation Control Register at location 98h. Read this register and check the result, if the register reads back 15h, the device is a SSC050-01, if the register reads back 00h, the device is a SSC050.*

Chapter 5 Electrical Characteristics

MAXIMUM RATINGS

Table 5-1: Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
DC Supply Voltage	Vdd	-0.3 to +3.9	V
LVTTL Input Voltage	Vin	-1.0 to VDD+0.3	V
5 Volt Compatible Input Voltage	Vin	-1.0 to +6.5	V
DC Input Current	Iin	±10	uA
Storage Temperature Range	Tstg	-40 to +125	°C
Latchup Current	Ilp	±150	mA

DC CHARACTERISTICS

Table 5-2: Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vdd	3.00	3.60	V
Supply Current	Idd		50	mA
Operating Ambient Temperature Range	TA	-40	+85	°C

Table 5-3: General Purpose I/O Ports, P4, P3, P2, P1, P0

Parameter	Symbol	Condition	Min	Max	Unit
Output High Voltage	Voh	Ioh=12mA	2.4	Vdd	V
Output Low Voltage	Vol	Iol=12mA	Vss	0.4	V
Input High Voltage	Vih		2.0	5.5	V
Input Low Voltage	Vil		Vss-0.5	0.8	V
Schmitt Threshold - Positive	Vt+			2.0	V
Schmitt Threshold - Negative	Vt-		0.8		V
Schmitt Hysteresis	Vh		0.4		V
Input Current with Pull-up	Iin	Vin=Vss	-25	-125	uA
Three State Output Leakage (Device Test Mode)	Ioz		-10	+10	uA

Table 5-4: Two-wire Serial Interface, SDA

Parameter	Symbol	Condition	Min	Max	Unit
Output Low Voltage	Vol	Iol=4mA	Vss	0.4	V
Input High Voltage	Vih		2.0	5.5	V
Input Low Voltage	Vil		Vss-0.5	0.8	V
Schmitt Threshold - Positive	Vt+			2.0	V
Schmitt Threshold - Negative	Vt-		0.8		V
Schmitt Hysteresis	Vh		0.4		V
Input Current	Iin	Vin=Vdd/Vss	-10	+10	uA
Three State Output Leakage	Ioz		-10	+10	uA

Table 5-5: Two-wire Serial Interface, SCL

Parameter	Symbol	Condition	Min	Max	Unit
Input High Voltage	Vih		2.0	5.5	V
Input Low Voltage	Vil		Vss-0.5	0.8	V
Schmitt Threshold - Positive	Vt+			2.0	V
Schmitt Threshold - Negative	Vt-		0.8		V
Schmitt Hysteresis	Vh		0.4		V
Input Current	Iin	Vin=Vdd/Vss	-10	+10	uA

Table 5-6: Address Inputs, A2, A1, A0, ASEL

Parameter	Symbol	Condition	Min	Max	Unit
Input High Voltage	Vih		2.0	5.5	V
Input Low Voltage	Vil		Vss-0.5	0.8	V
Schmitt Threshold - Positive	Vt+			2.0	V
Schmitt Threshold - Negative	Vt-		0.8		V
Schmitt Hysteresis	Vh		0.4		V
Input Current	Iin	Vin=Vdd/Vss	-10	+10	uA

Table 5-7: Interrupt Output, INT#

Parameter	Symbol	Condition	Min	Max	Unit
Output Low Voltage	Vol	Iol=4mA	Vss	0.4	V

Table 5-8: Test Inputs: TEST0, TEST1, TEST2

Parameter	Symbol	Condition	Min	Max	Unit
Input High Voltage	Vih		2.0	5.5	V
Input Low Voltage	Vil		Vss-0.5	0.8	V
Schmitt Threshold - Positive	Vt+			2.0	V
Schmitt Threshold - Negative	Vt-		0.8		V
Schmitt Hysteresis	Vh		0.4		V
Input Current	Iin	Vin=Vdd/Vss	-10	+10	uA

Table 5-9: Oscillator/Clock Input, OSCI

Parameter	Symbol	Condition	Min	Max	Unit
Input High Voltage	Vih		Vdd/2	Vdd+0.3	V
Input Low Voltage	Vil		Vss-0.5	Vdd/2	V
Switching Threshold	Vt			Vdd/2	V
Input Current	Iin	Vin=Vdd/Vss	-10	+10	uA

Table 5-10: Oscillator Output, OSCO

Parameter	Symbol	Condition	Min	Max	Unit
Output High Voltage	Voh	Ioh=4mA	Vdd-0.3	Vdd	V
Output Low Voltage	Vol	Iol=4mA	Vss	Vss+0.3	V

AC CHARACTERISTICS

External Clock Timing

Table 5-11: Low Frequency Operation

Parameter	Symbol	Condition	Min	Max	Unit
Nominal Frequency	F		9.5	10.5	MHz
Frequency Range	F		8.0	12.5	MHz
Clock Cycle Time	t1		80	125	ns
Clock Low Time	t2		32	75	ns
Clock High Time	t3		32	75	ns
Clock Slew Rate	t4		1		V/ns

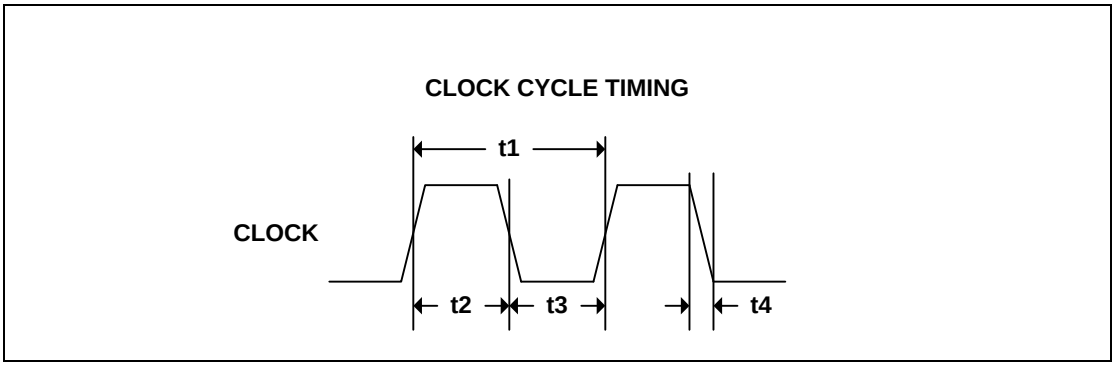

Figure 5-1. Clock Cycle Timing

Table 5-12: Two-Wire Serial Interface Timing

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL Clock Frequency	fscl	0	100	0	400	KHz
Bus Free Time	tbuf	4.7		1.3		us
Hold Time - Start Condition	thd:sta	4.0		0.6		us
SCL Low Time	tlow	4.7		1.3		us
SCL High Time	thigh	4.0		0.6		us
Setup Time - Start Condition	tsu:sta	4.7		0.6		us
Hold Time - Data	thd:dat	0		0	0.9	us
Setup Time - Data	tsu:dat	250		100		ns
Setup Time - Stop Condition	tsu:sto	4.0		0.6		us

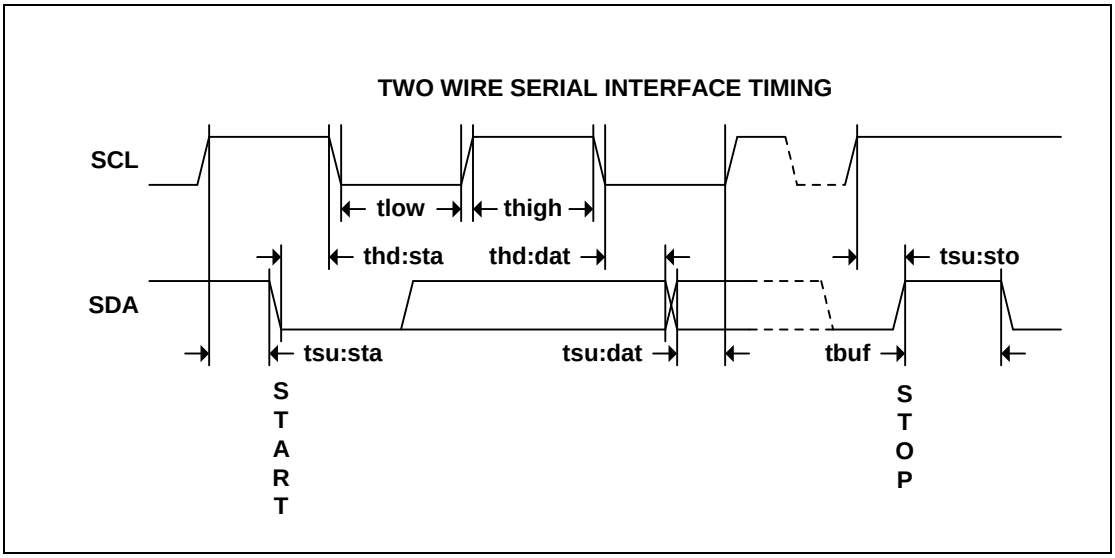

Figure 5-2.

Two-wire Serial Interface Operation

The following diagrams illustrate the two-wire serial interface read and write capabilities of the SSC050-01. All operations can be performed in any order.

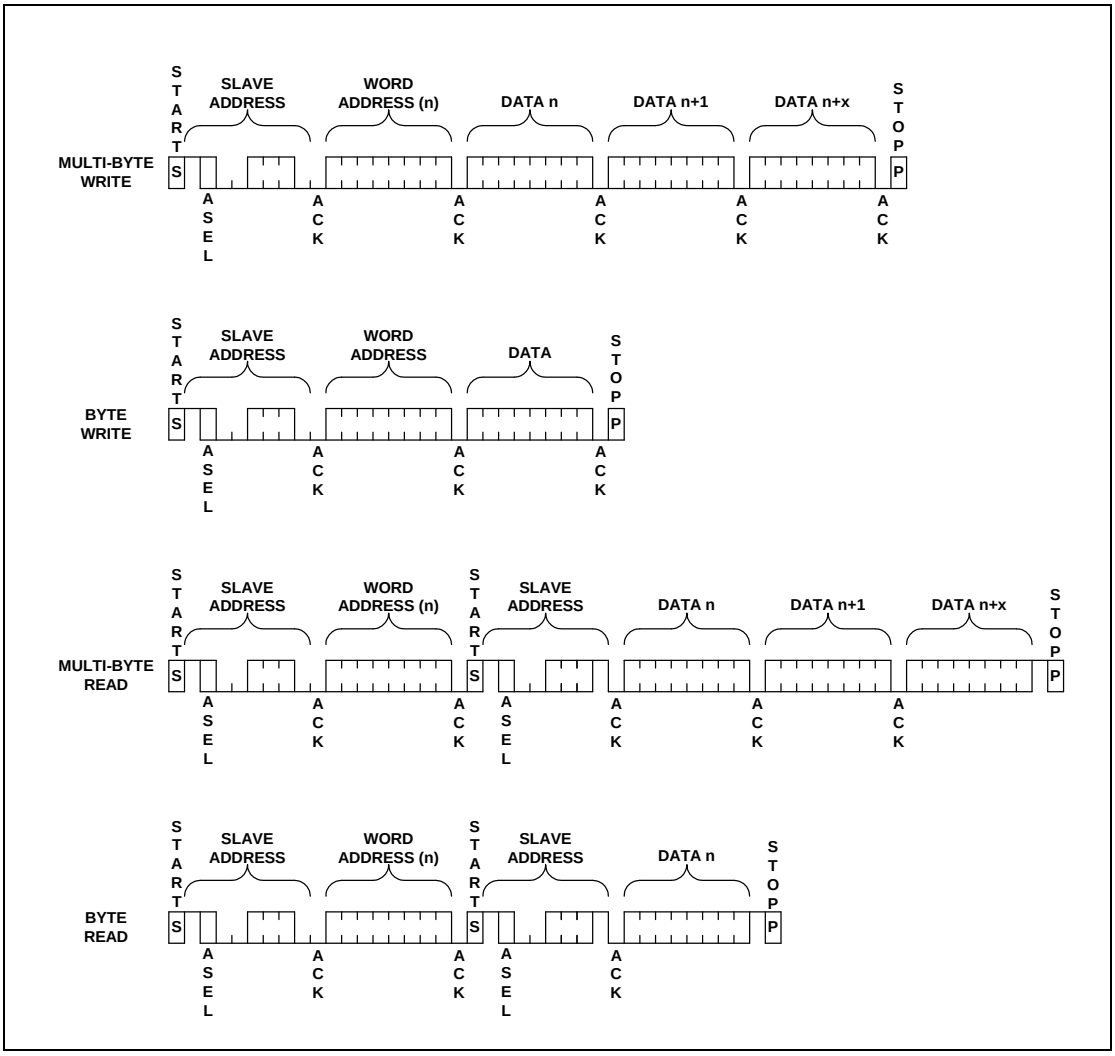

Figure 5-3. Two-Wire Serial Interface Operation

Oscillator Requirements

The SSC050-01 can use an external 3.3 volt 8.0MHz to 12.5MHz clock source connected to the OSCI pin with CKSEL2 tied to VSS. An external 3.3 volt 32.0MHz to 50.0MHz clock source can be connected to the OSCI pin with CKSEL2 tied to VDD and CKSEL1 tied to VSS. An external 3.3 volt 48.0MHz to 75.0MHz clock source can be connected to the OSCI pin with CKSEL2 tied to VDD and CKSEL1 tied to VDD. Alternatively, an 8.0MHz to 12.5MHz crystal and several passive components

may be used. The following diagrams illustrate the two options available when using a crystal. The passive components shown will function properly for all crystal frequencies. Option 1 requires fewer external components due to the high input capacitance of the OSCI pin and results in a stable configuration. Option 2 represents a classic approach with a higher level of stability.

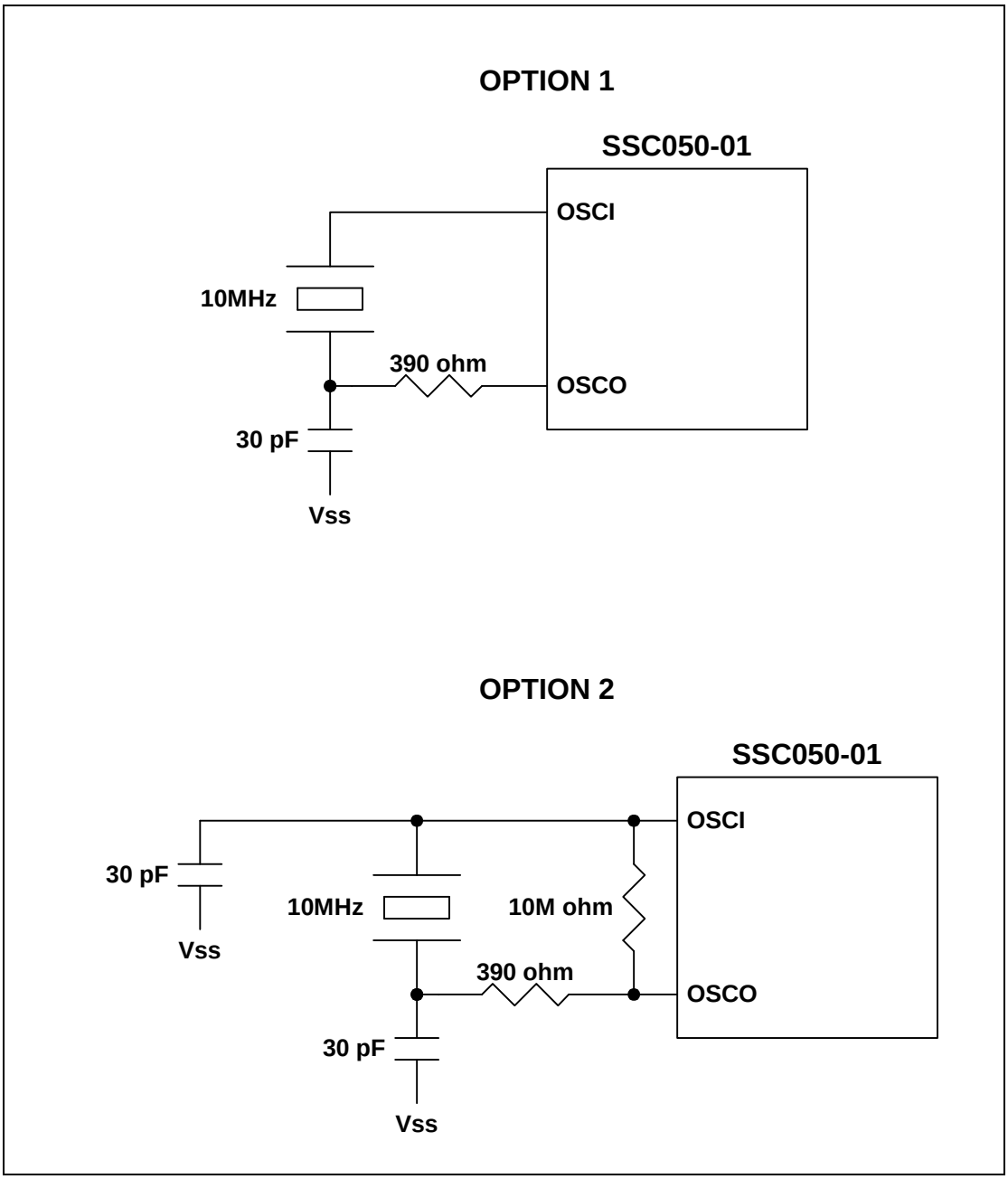

Figure 5-4. Oscillator Options

External Reset Circuit

The SSC050-01 supports an internal Power-On Reset circuit that eliminates the need for an external reset source. However, the device does support a mechanism that allows the use of an external reset for those applications where a system reset is available and required. The following diagrams show the external connections required. The external reset source must be active high and does not need to be synchronous to the clock source of the SSC050-01. TEST0 and TEST2 must remain at a low level during the reset sequence. The minimum external reset pulse width is 50 nanoseconds. Two-wire serial transactions to the SSC050-01 must not commence until a minimum of 500 nanoseconds after the deassertion of the external reset pulse. Option 1 should be used when ASEL is normally held low (the device type identifier value is 1000b). Option 2 should be used when ASEL is normally held high (the device type identifier value is 1100b).

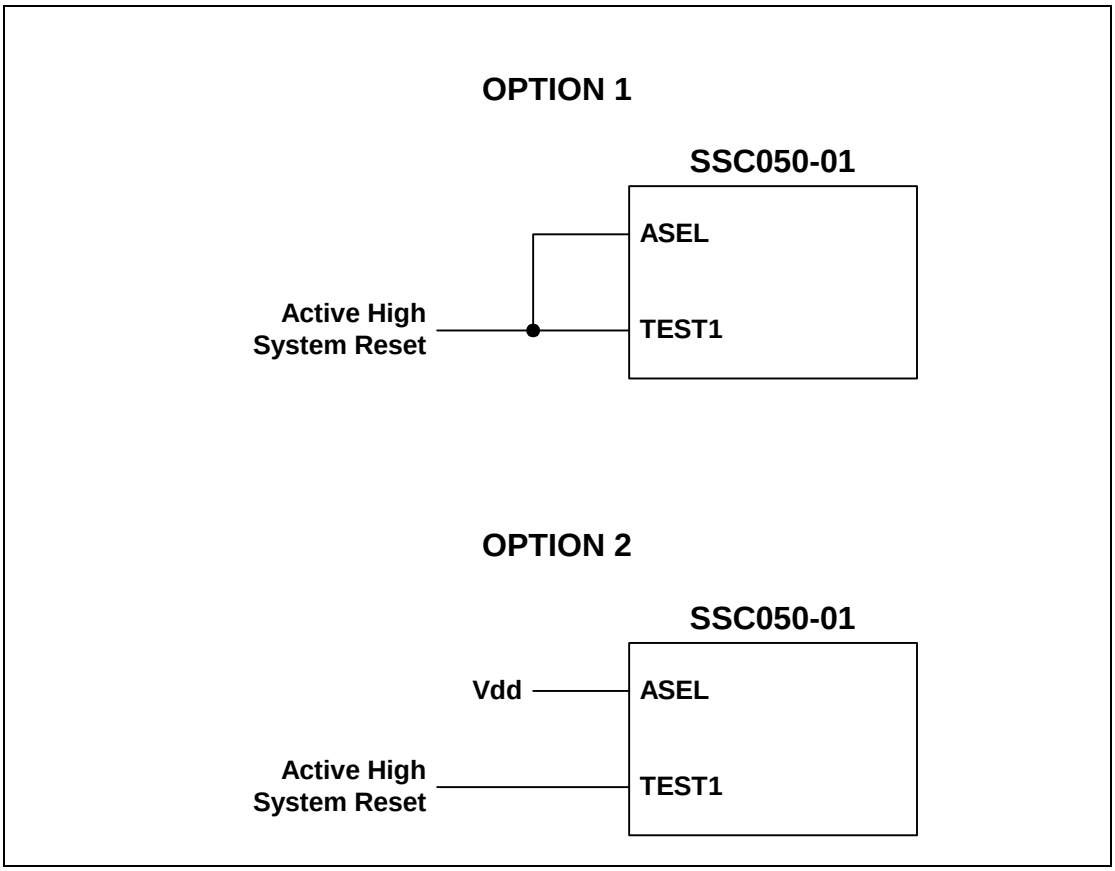

Figure 5-5. External Reset Circuit Options

Optional External Tach Filter

The fan tach inputs of the SSC050-01 utilize schmitt trigger input buffers and are also internally digitally filtered. However, excessive external noise on a tach input can result in inaccurate fan speed current count values. The use of an external low pass filter along with the use of the extended tach filter mode (Tach Filter Extend, bit 6 of register FDh) of the SSC050-01 will eliminate inaccurate current count values. The following circuit provides excellent noise rejection at all possible RPM ranges supported by the SSC050-01.

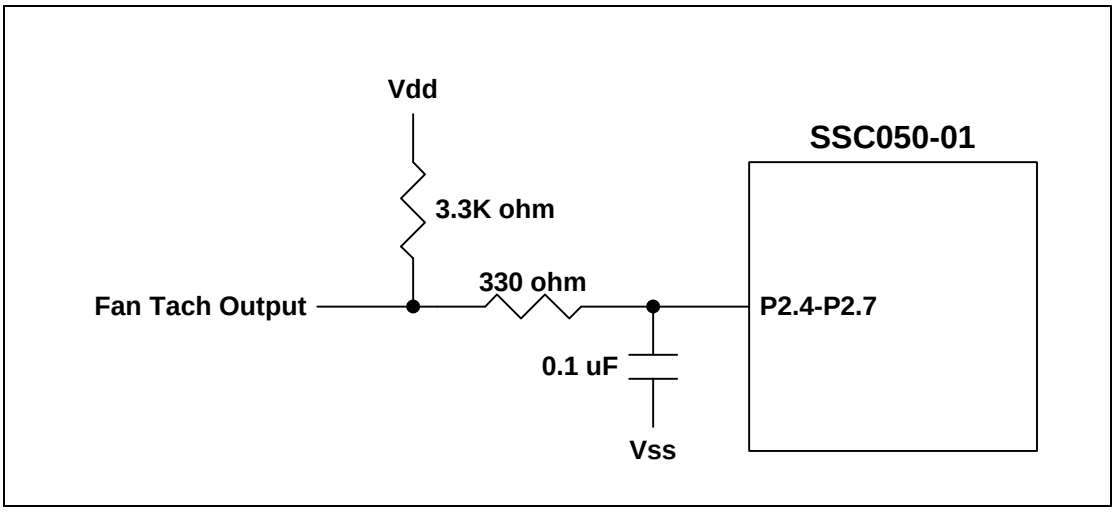

Figure 5-6. Optional External Tach Filter

Chapter 6 MECHANICAL DRAWING

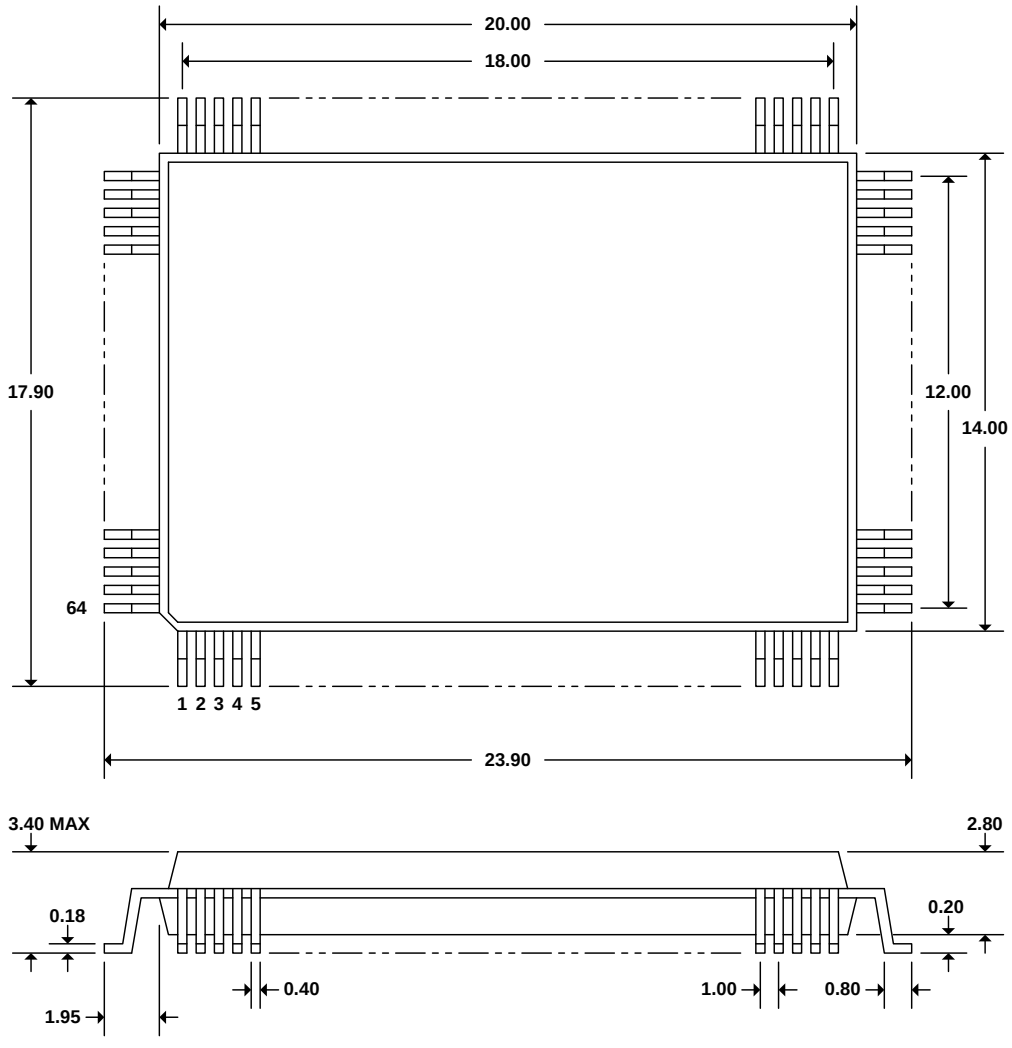

Figure 6-1. Mechanical Drawing

Chapter 7 ORDERING INFORMATION

The SSC050-01 device is available in two package types. L2A050-01 is a 64-pin plastic quad flat pack (PQFP). The device is also available in a lead(Pb)-free package, VSC050XKM-01.

Lead(Pb)-free products from Maxim comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

SSC050-01 Two-Wire Serial Backplane Controller

Part Number	Description
L2A050-01	64-pin PQFP
VSC050XKM-01	Lead(Pb)-free 64-pin PQFP