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Crimzon® ZLR32300

Z8® Low-Voltage ROM MCU with Infrared Timers

Product Specification

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Revision History

Each instance in the Revision History table reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page Number
April 2009	13	Changed to Maxim product	All
February 2008	12	Updated the Ordering Information section.	92
January 2008	11	Updated the Ordering Information section.	92
August 2007	10	Updated the Disclaimer section and implemented style guide.	All
February 2007	09	Updated Low-Voltage Detection Register—LVD(D)0CH.	60
May 2006	08	Added Pin 22 to SMR Block input, Figure 32.	54
December 2005	07	Updated section clock and Input/output port.	50, 14

Table of Contents

Architectural Overview

Maxim's Crimzon® ZLR32300 is an ROM-based member of the MCU family of infrared microcontrollers. With 237 B of general-purpose RAM and 4 KB to 32 KB of ROM, CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output (I/O) bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon ZLR32300 architecture (see Figure 1 on page 4) is based on Maxim's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8® offers a flexible
I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and
battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations:

1. Program Memory
2. Register File
3. Expanded Register File

The register file is composed of 256 bytes of RAM. It includes four I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon ZLR32300 offers a new intelligent counter/timer architecture with 8-bit and
16-bit counter/timers (see Figure 2 on page 5). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

Note: All signals with an overline, "$\overline{\ }$", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 1.

Table 1. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Development Features

Table 2 lists the features of Crimzon ZLR32300 family.

Table 2. Crimzon ZLR32300 Family Features

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Crimzon ZLR32300	4, 8, 16, 24, 32	237	32, 24 or 16	2.0–3.6 V
*General purpose				

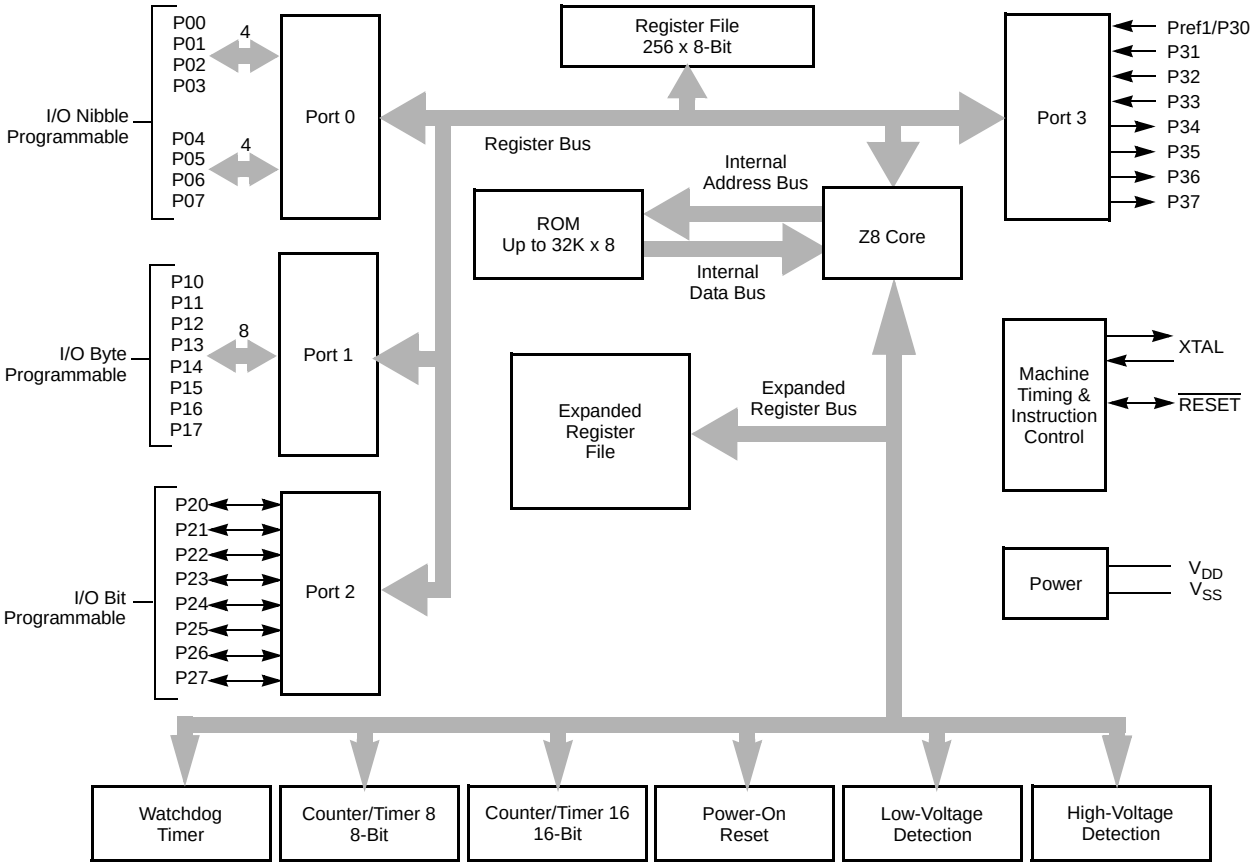
The development features of Crimzon ZLR32300 include:

- Low power consumption–5 mW (typical)
- Three standby modes:
  - STOP—1.4 µA (typical)
  - HALT—0.5 mA (typical)
  - Low voltage
- Special architecture to automate generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low-voltage detection and high-voltage detection Flags
- Programmable Watchdog Timer/Power-on reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity

- Mask selectable pull-up transistors on ports 0, 1, 2, 3
- ROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors
  - Port 1: 0–3 pull-up transistors
  - Port 1: 4–7 pull-up transistors
  - Port 2: 0–7 pull-up transistors
  - Port 3: 0–3 pull-up transistors
  - WDT enabled at POR

Functional Block Diagram

Figure 1 displays the ZLR32300 MCU functional block diagram.



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

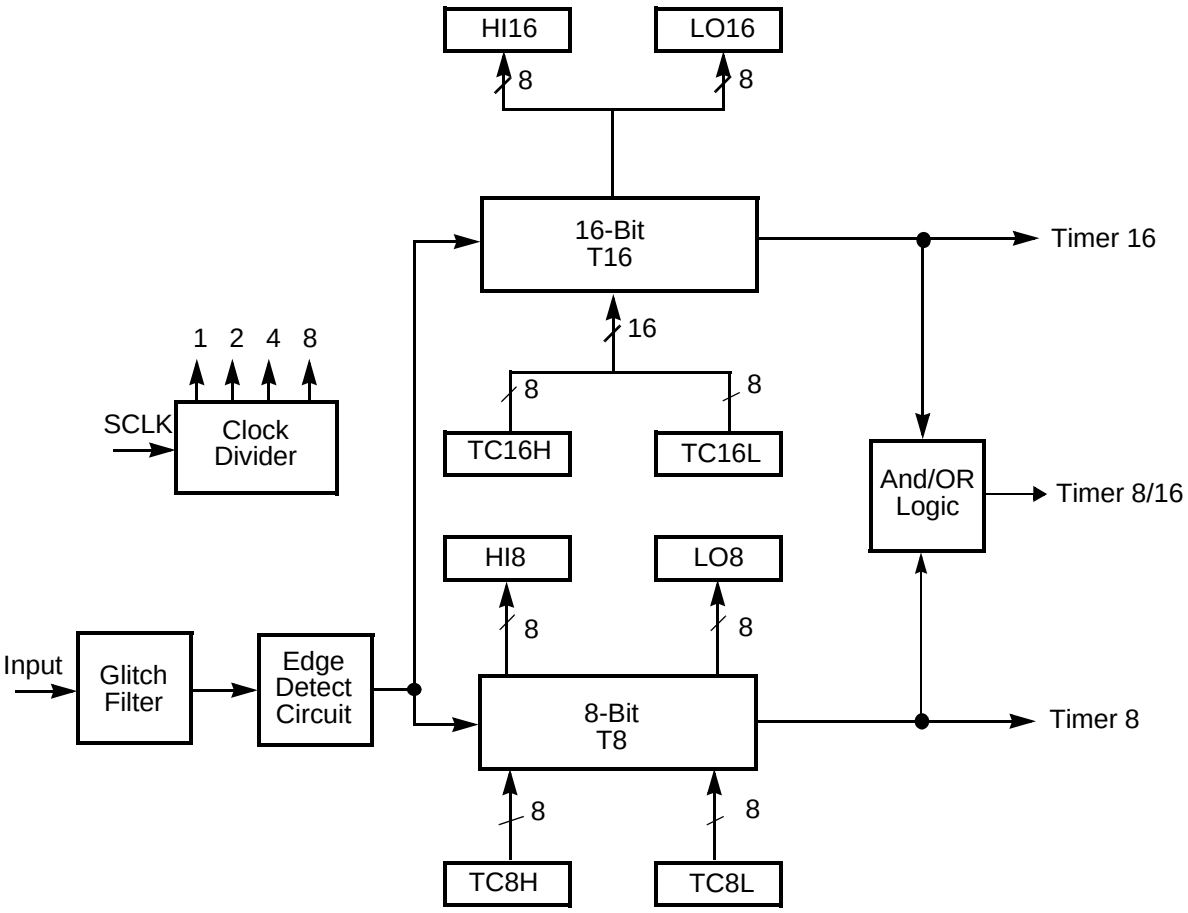


Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is displayed in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP is displayed in Figure 4 on page 7 and described in Table 4 on page 7. The pin configurations for the 48-pin SSOP versions are displayed in Figure 5 on page 8 and described in Table 5 on page 8.

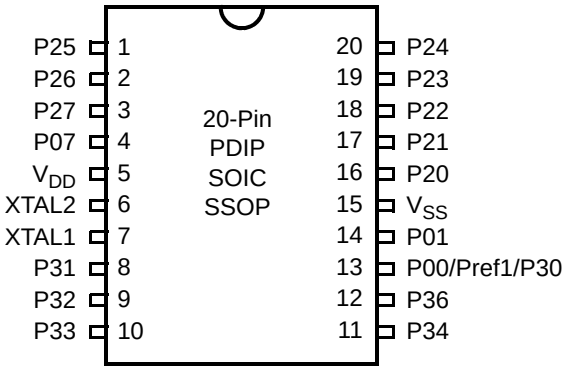


Figure 3. 20-Pin PDIP/SOIC/SSOP Pin Configuration

Table 3. 20-Pin PDIP/SOIC/SSOP Pin Identification

Pin No	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V_{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V_{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

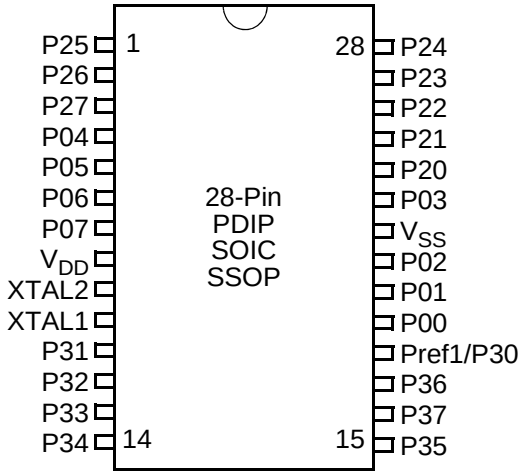


Figure 4. 28-Pin PDIP/SOIC/SSOP Pin Configuration

Table 4. 28-Pin PDIP/SOIC/SSOP Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V_{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V_{CC} if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V_{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

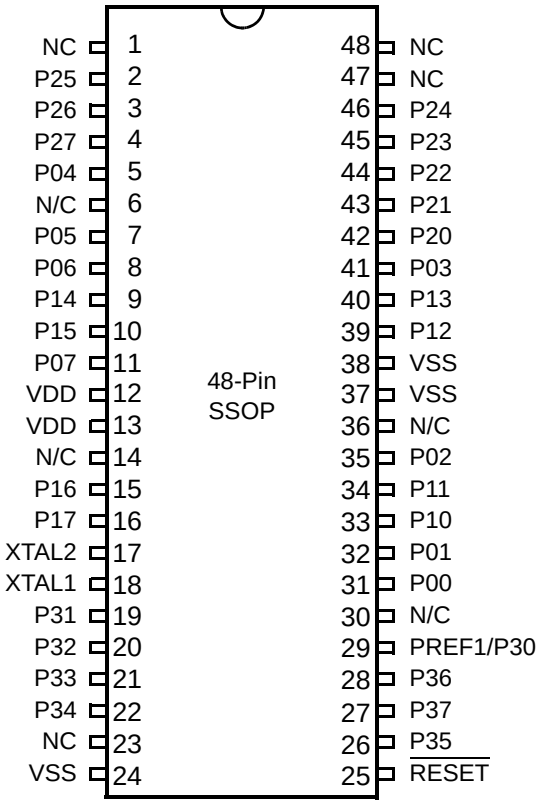


Figure 5. 48-Pin SSOP Pin Configuration

Table 5. 48-Pin Configuration

48-Pin SSOP No	Symbol
31	P00
32	P01
35	P02
41	P03
5	P04
7	P05
8	P06
11	P07
33	P10
34	P11

Table 5. 48-Pin Configuration (Continued)

48-Pin SSOP No	Symbol
39	P12
40	P13
9	P14
10	P15
15	P16
16	P17
42	P20
43	P21
44	P22
45	P23
46	P24
2	P25
3	P26
4	P27
19	P31
20	P32
21	P33
22	P34
26	P35
28	P36
27	P37
23	NC
47	NC
1	NC
25	RESET
18	XTAL1
17	XTAL2
12, 13	V_{DD}
24, 37, 38	V_{SS}
29	Pref1/P30
48	NC
6	NC

Table 5. 48-Pin Configuration (Continued)

48-Pin SSOP No	Symbol
14	NC
30	NC
36	NC

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator, to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant, crystal or ceramic resonant to the on-chip oscillator output.

Input/Output Ports

Caution: The CMOS input buffer for each Port 0, 1, or 2 pin is always connected to the pin, even when the pin is configured as an output. If the pin is configured as an open-drain output and no external signal is applied, a High output state can cause the CMOS input buffer to float. This might lead to excessive leakage current of more than 100 µA. To prevent this leakage, connect the pin to an external signal with a defined logic level or ensure its output state is Low, especially during STOP mode.

Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

Port 0, 1, and 2 have input and output capability. The input logic is always present no matter whether the port is configured as input or output. When doing a READ instruction, the MCU reads the actual value at the input logic but not from the output buffer. In addition, the instructions of OR, AND, and XOR have the Read-Modify-Write sequence. The MCU first reads the port, and then modifies the value and load back to the port.

Precaution must be taken if the port is configured as open-drain output or if the port is driving any circuit that makes the voltage different from the desired output logic. For example, pins P00–P07 are not connected to anything else. If it is configured as open-drain output with output logic as

ONE, it is a floating port and reads back as ZERO. The following instruction sets P00-P07 all LOW.

```
AND P0,#%F0
```

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

Note: The Port 0 direction is reset to be input following an Stop Mode Recovery.

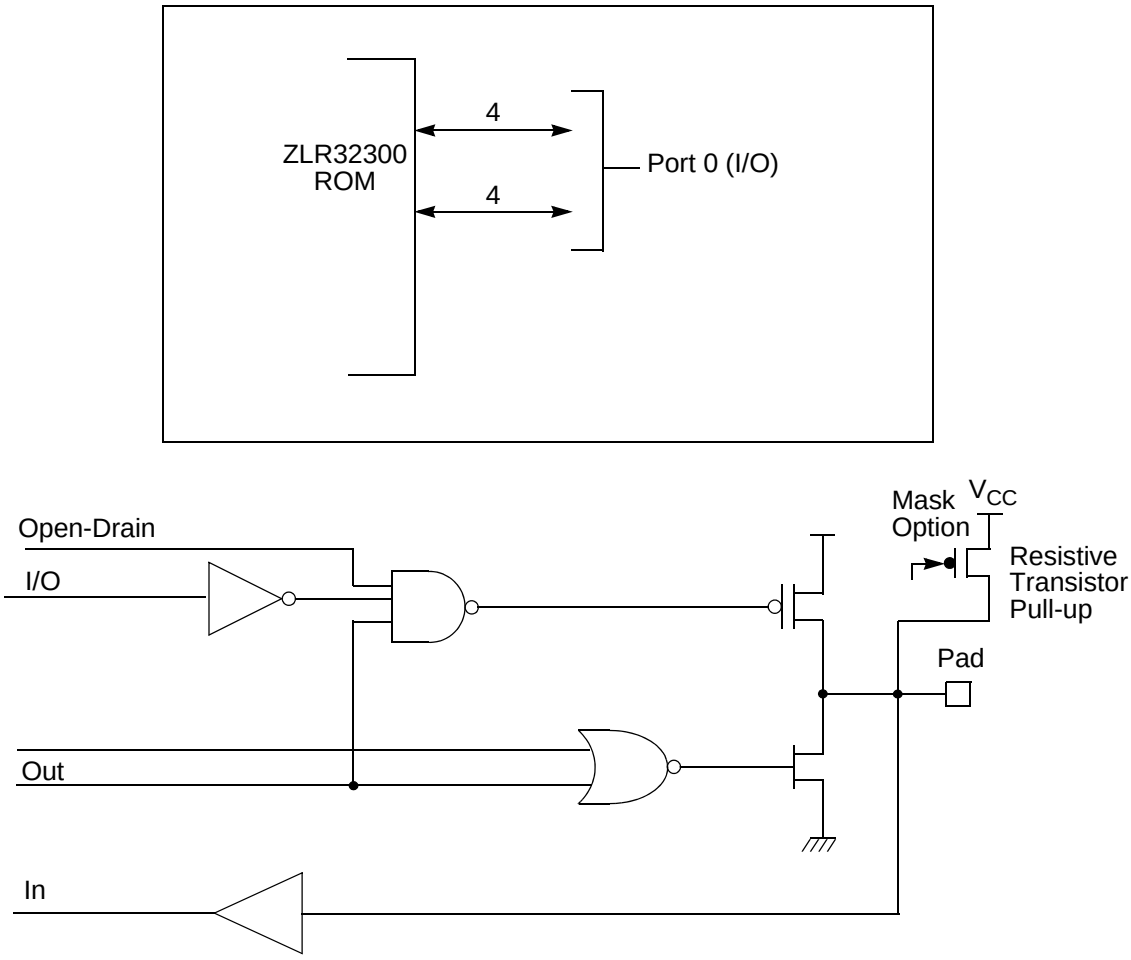


Figure 6. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 7) can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

Note: The Port 1 direction is reset to be input following an SMR.

In 20- and 28-pin packages, Port 1 is reserved. A write to this register will have no effect and will always read FF.

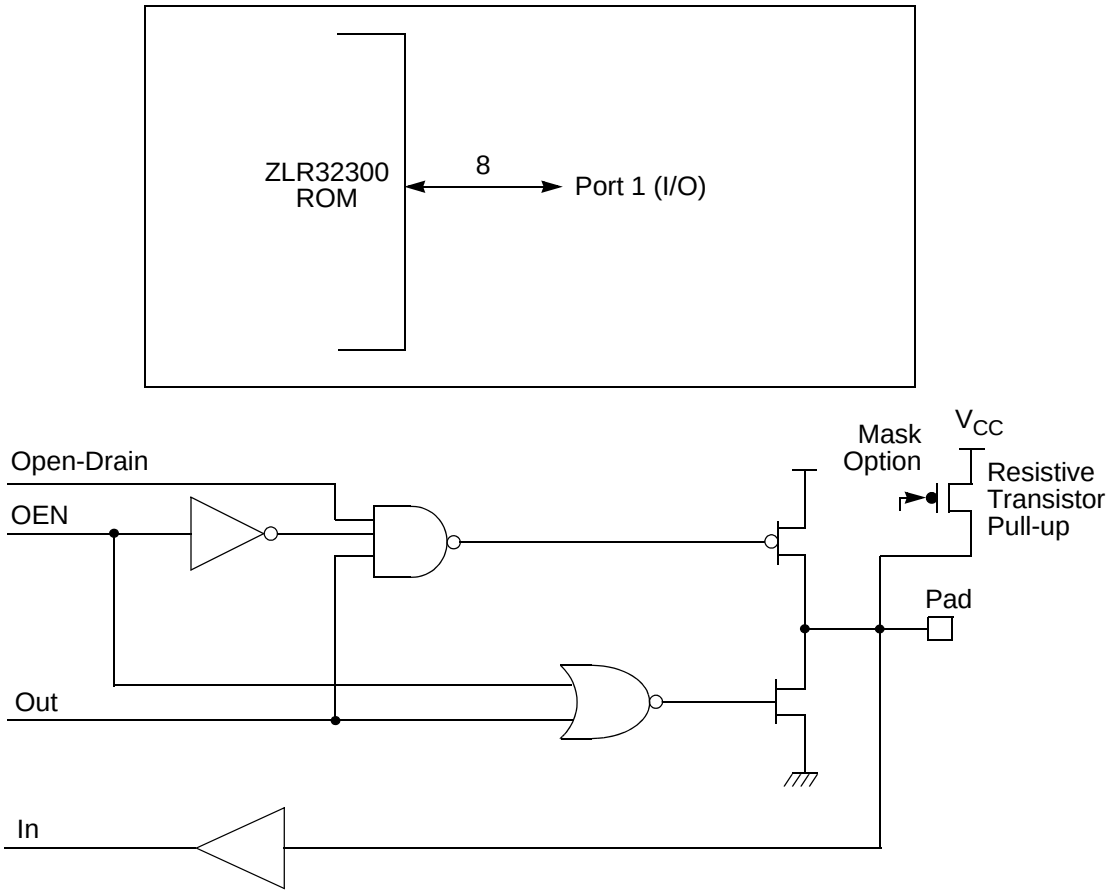


Figure 7. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 8 on page 15). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in DEMODULATION mode.

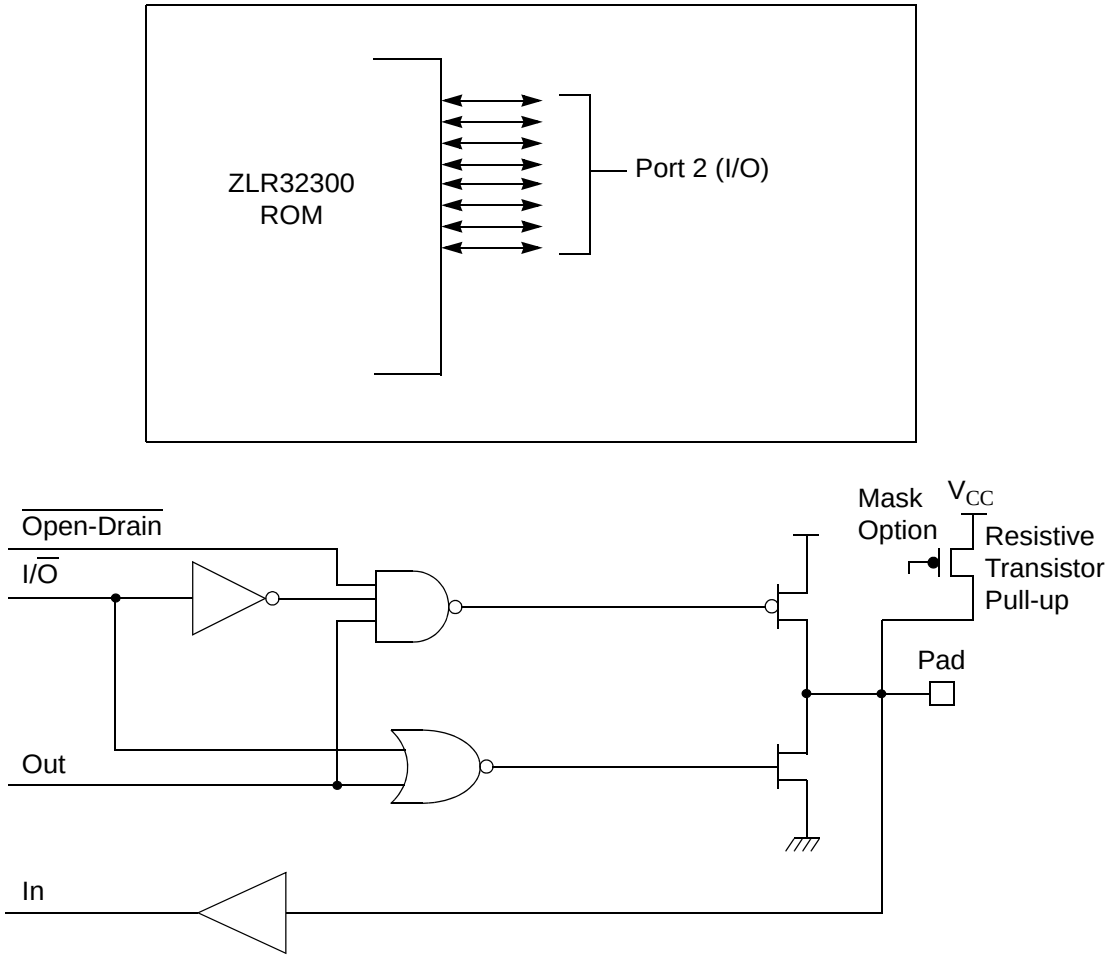


Figure 8. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 9 on page 16). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

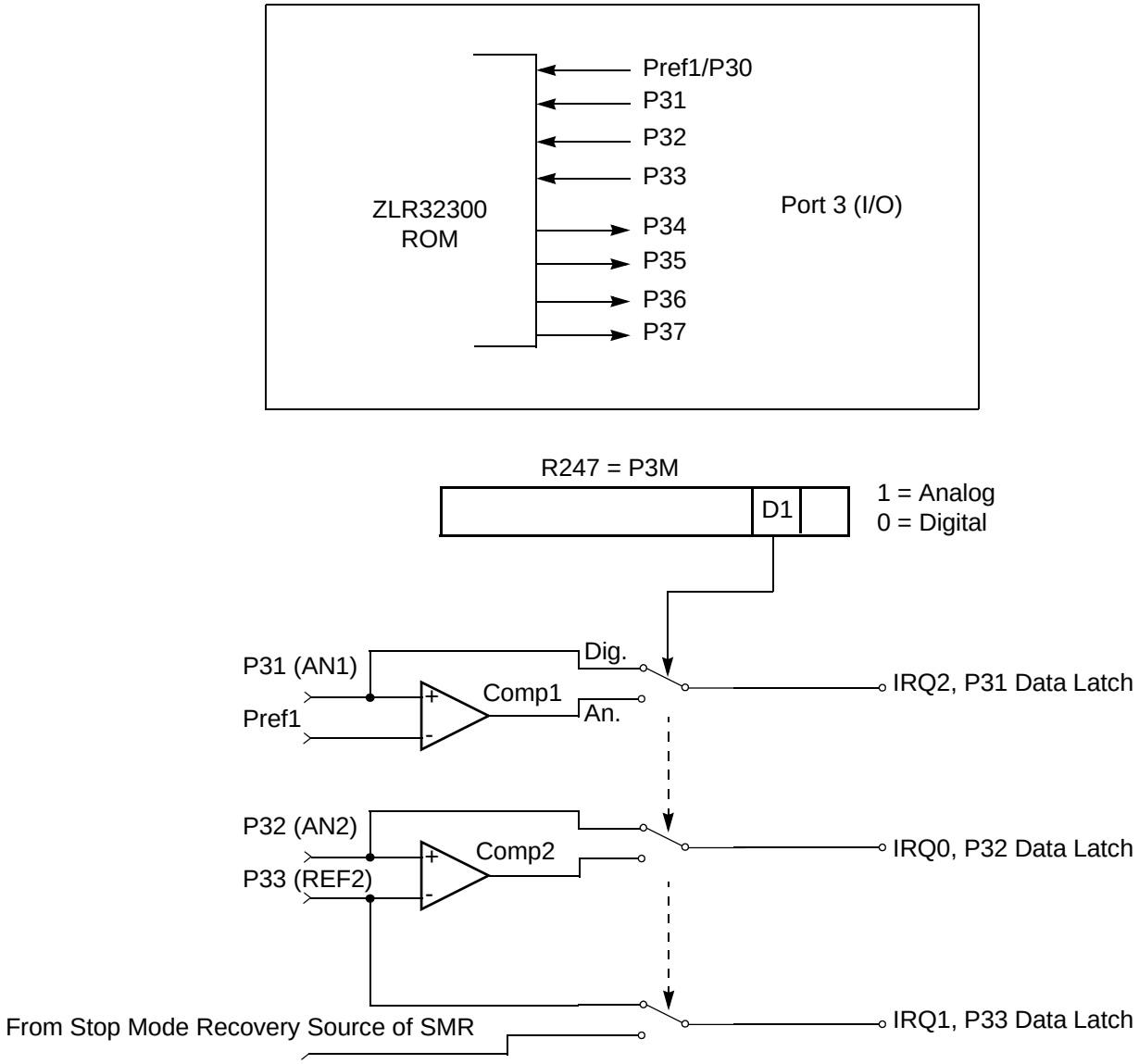


Figure 9. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The Analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see T8 and T16 Common Func-

tions—CTR1(0D)01h on page 30). Other edge detect and IRQ modes are described in Table 6.

Note: Comparators are powered down by entering STOP mode. For P31–P33 to be used in a SMR source, these inputs must be placed into DIGITAL mode.

Table 6. Port 3 Pin Function Summary

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 10 on page 18). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

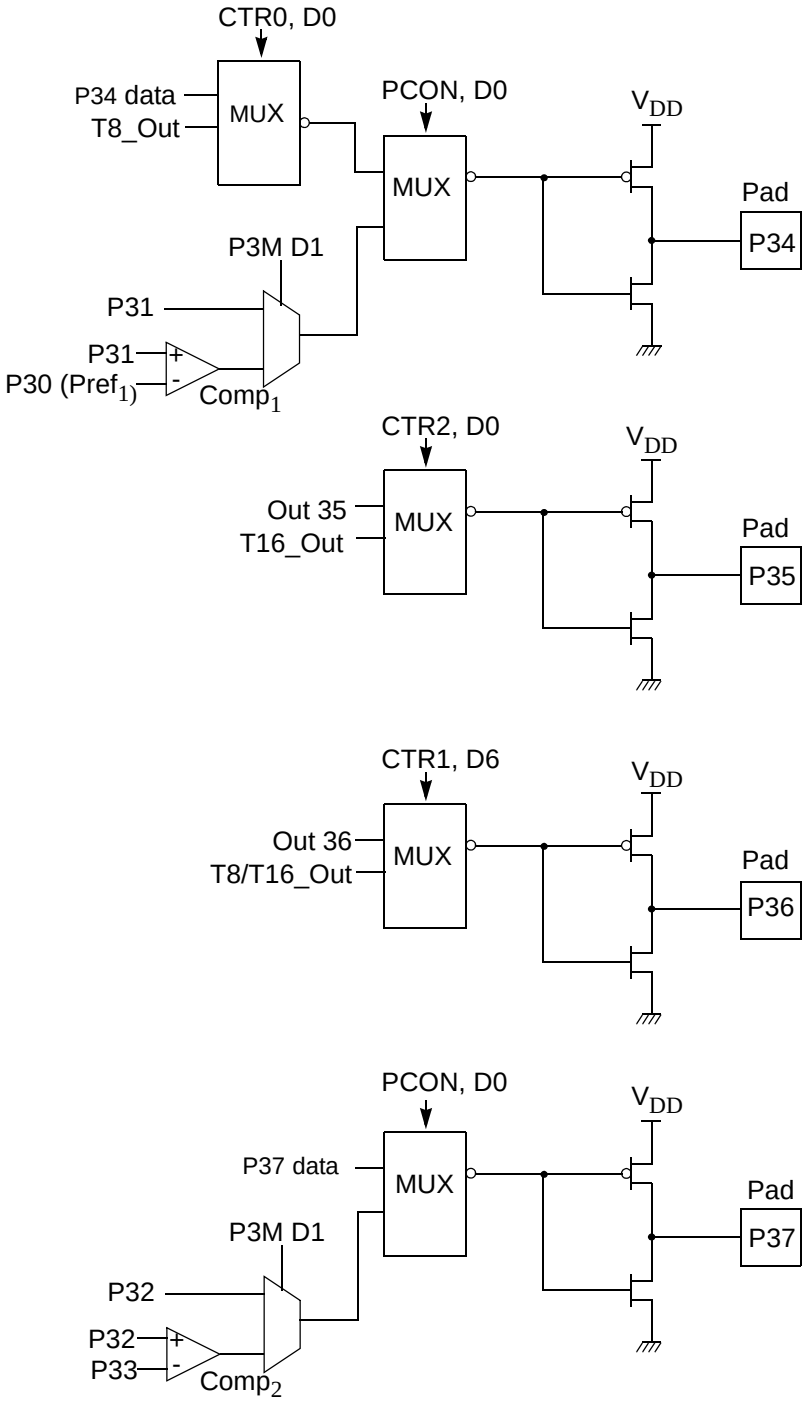


Figure 10. Port 3 Counter/Timer Output Configuration

Comparator Inputs

In ANALOG mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as displayed in Figure 9 on page 16. In DIGITAL mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

Note: Comparators are powered down by entering STOP mode. For P31–P33 to be used in a SMR source, these inputs must be placed into DIGITAL mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

$\overline{\text{RESET}}$ (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watchdog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watchdog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the ZLR32300 asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The ZLR32300 does not assert the $\overline{\text{RESET}}$ pin when under VBO.

Note: The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8® functionality in consumer and battery-operated applications.

Program Memory

This device addresses 32 KB of ROM memory. The first 12 bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts (see Figure 11on page 21).

RAM

This device features 256 B of RAM.

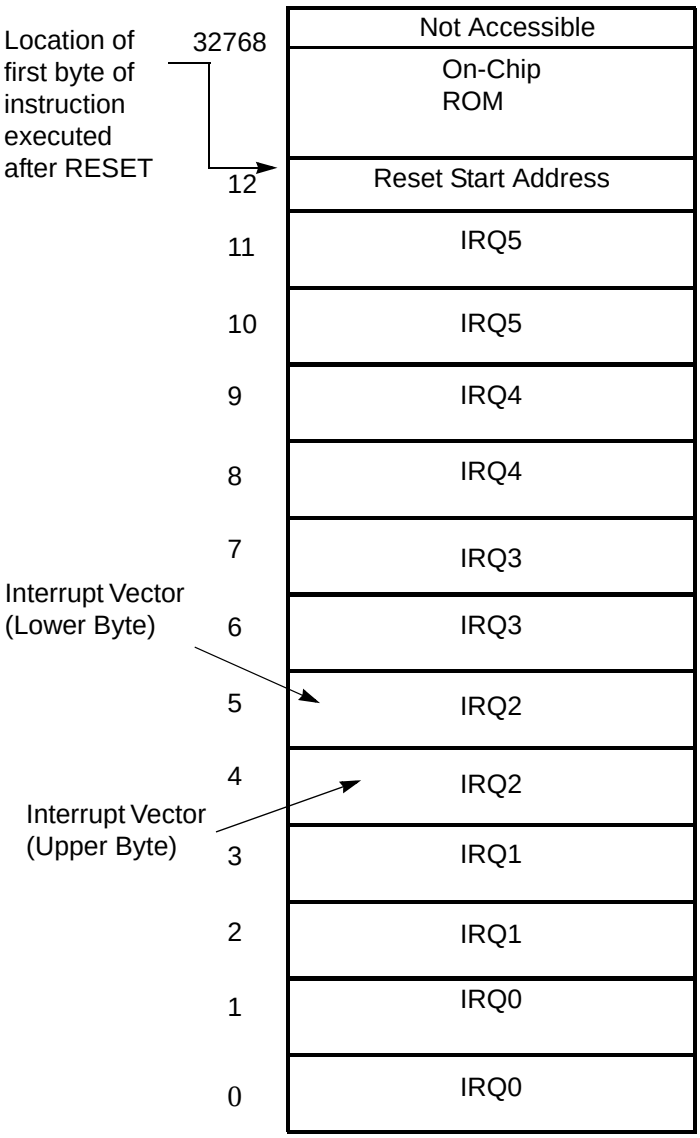


Figure 11.Program Memory Map (32 K ROM)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the

ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: An expanded register bank is also referred to as an expanded register group (see Figure 12 on page 23).

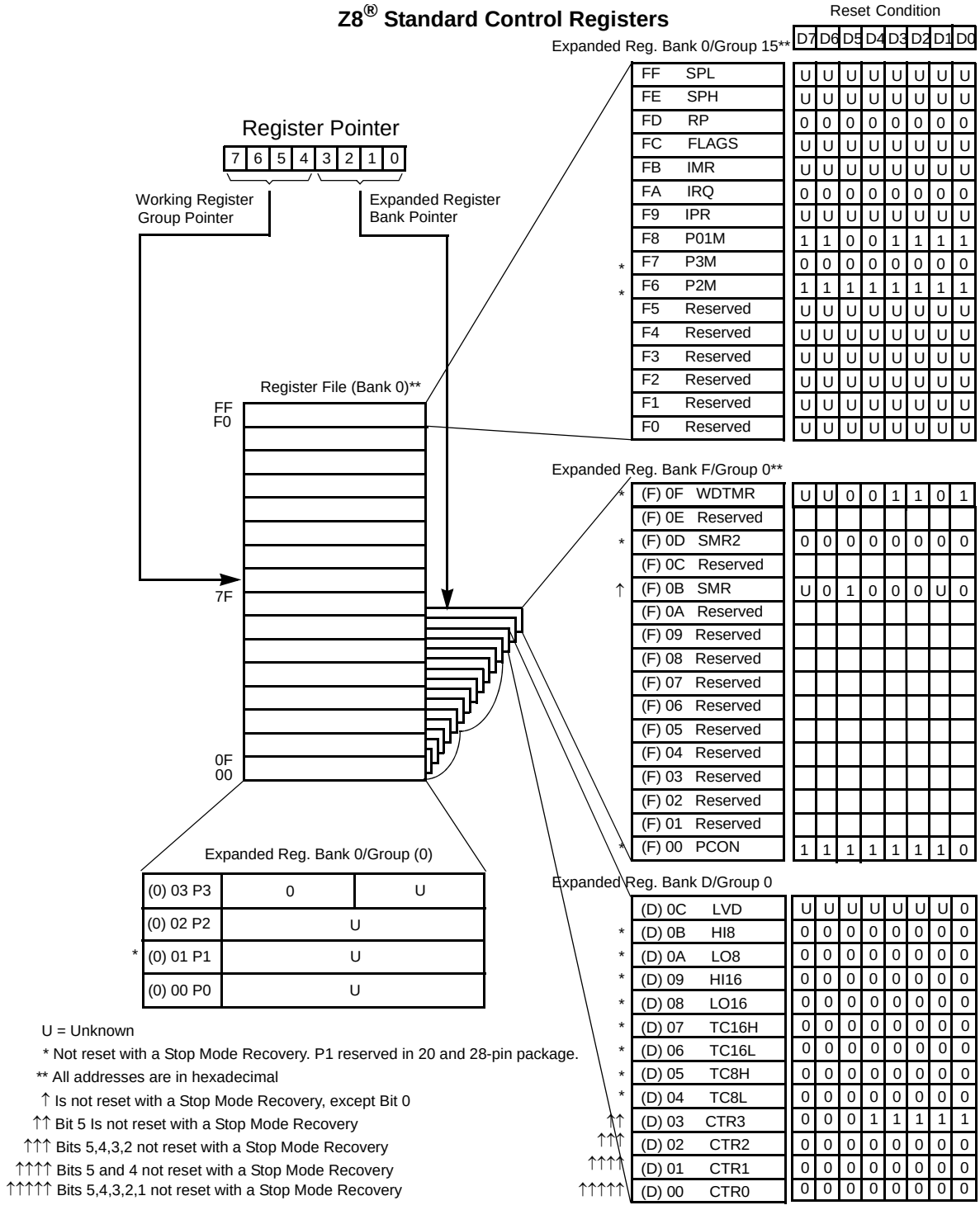


Figure 12. Expanded Register File Architecture

The upper nibble of the register pointer (see Figure 13) selects which working register group of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Crimzon ZLR32300 family, banks 0, F, and D are implemented. A `0h` in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from `1h` to `Fh` exchanges the lower 16 registers to an expanded register bank.

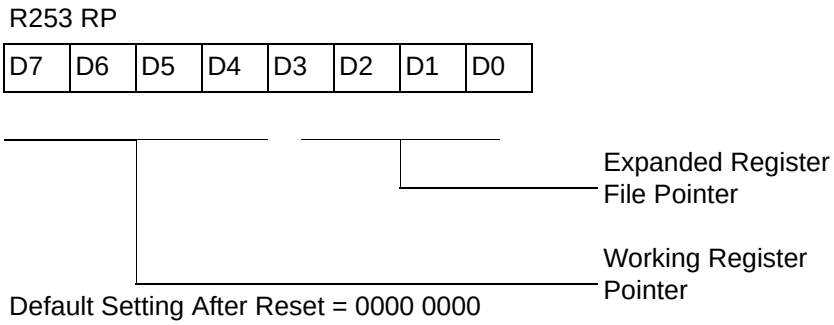


Figure 13. Register Pointer

Example: Crimzon ZLR32300 (see Figure 12 on page 23).

R253 RP = 00h
R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0Dh
R0 = CTR0
R1 = CTR1
R2 = CTR2
R3 = CTR3

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```
LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      R0,#xx                  ; load CTR0
LD                      1, #xx                  ; load CTR1
```

```
LD                      R1, 2                   ; CTR2→CTR1

LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      RP, #7Dh                ; Select
expanded register bank D and working            ; register
group 7 of bank 0 for access.
LD                      71h, 2
; CTR2→register 71h
LD                      R1, 2
; CTR2→register 71h
```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 7 on page 28) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (see Figure 14 on page 26). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

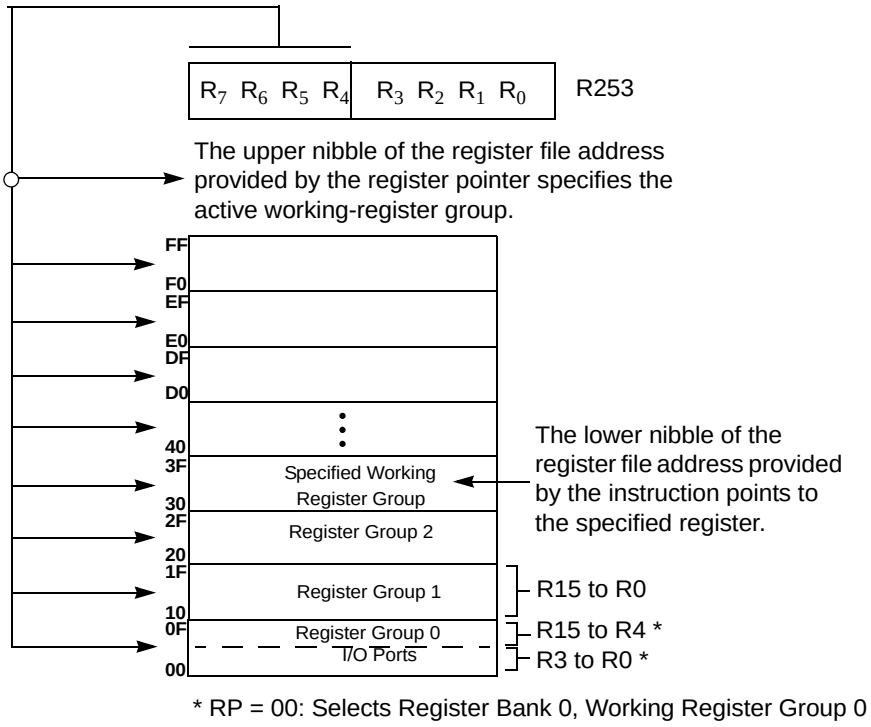


Figure 14. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data—No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	[7:0]	R/W	Captured Data—No Effect

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data—No Effect

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data—No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 7 lists and briefly describes the fields for this register.

Table 7. CTR0(D)00H Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R/W	0* 1 0 1	Counter Disabled Counter Enabled Stop Counter Enable Counter
Single/Modulo-N	-6-------	R/W	0* 1	Modulo-N Single Pass
Time_Out	--5------	R/W	0** 1 0 1	No Counter Time-Out Counter Time-Out Occurred No Effect Reset Flag to 0
T8 _Clock	---43---	R/W	0 0** 0 1 1 0 1 1	SCLK SCLK/2 SCLK/4 SCLK/8
Capture_INT_Mask	-----2--	R/W	0** 1	Disable Data Capture Interrupt Enable Data Capture Interrupt
Counter_INT_Mask	------1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	-------0	R/W	0* 1	P34 as Port Output T8 Output on P34

*Indicates the value upon Power-on reset.
**Indicates the value upon Power-on reset. Not reset with a Stop Mode Recovery.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.

Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

Note: Ensure to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (DEMODULATION mode) when using the OR or AND commands. These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

T8 Clock

These bits define the frequency of the input signal to T8.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in DEMODULATION mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01h

This register controls the functions in common with the T8 and T16.

Table 8 lists and briefly describes the fields for this register.

Table 8. CTR1(0D)01H T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	TRANSMIT mode
			1	DEMODULATION mode
P36_Out/ Demodulator_Input	-6------	R/W		TRANSMIT mode
			0*	Port Output
			1	T8/T16 Output
				DEMODULATION mode
			0*	P31
			1	P20
T8/T16_Logic/ Edge _Detect	--54----	R/W		TRANSMIT mode
			00**	AND
			01	OR
			10	NOR
			11	NAND
				DEMODULATION mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

Table 8. CTR1(0D)01H T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Transmit_Submode/ Glitch_Filter	----32--	R/W		TRANSMIT mode
			00	Normal Operation
			01	PING-PONG mode
			10	T16_Out = 0
			11	T16_Out = 1
				DEMODULATION mode
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/ Rising Edge	------1-			TRANSMIT mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				DEMODULATION mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/ Falling_Edge	-------0			TRANSMIT mode
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				DEMODULATION mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

*Default at Power-On Reset.
**Default at Power-On Reset. Not reset with a Stop Mode Recovery.

Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

P36_Out/Demodulator_Input

In TRANSMIT mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

T8/T16_Logic/Edge _Detect

In TRANSMIT mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In TRANSMIT mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to 'NORMAL OPERATION mode' terminates the 'PING-PONG mode' operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In TRANSMIT mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In TRANSMIT mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 must be written to this location.

Note: Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 9 on page 33 lists and briefly describes the fields for this register.

Table 9. CTR2(D)02H: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6------	R/W		TRANSMIT mode
			0*	Modulo-N
			1	Single Pass
				DEMODULATION mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0**	No Counter Timeout
			1	Counter Timeout Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	---43---	R/W	00**	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0**	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0*	Disable Timeout Int.
			1	Enable Timeout Int.
P35_Out	-------0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.

In DEMODULATION mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 DEMODULATION mode on page 42.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03H

Table 10 lists and briefly describes the fields for this register. This register allows the T_8 and T_{16} counters to be synchronized.

Table 10. CTR3 (D)03H: T8/T16 Control Register

Field	Bit Position		Value	Description
T_{16} Enable	7-------	R	0**	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T_8 Enable	-6------	R	0**	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0*	Disable Sync Mode
			1	Enable Sync Mode

Table 10. CTR3 (D)03H: T8/T16 Control Register (Continued)

Field	Bit Position		Value	Description
Reserved	---43210	R W	1 x	Always reads 11111 No Effect

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 15).

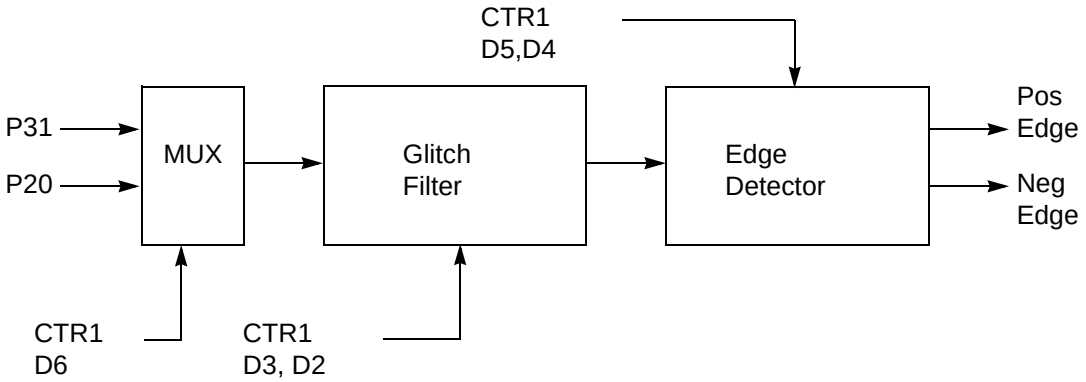


Figure 15.Glitch Filter Circuitry

T8 TRANSMIT Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0 (see Figure 16 on page 36).

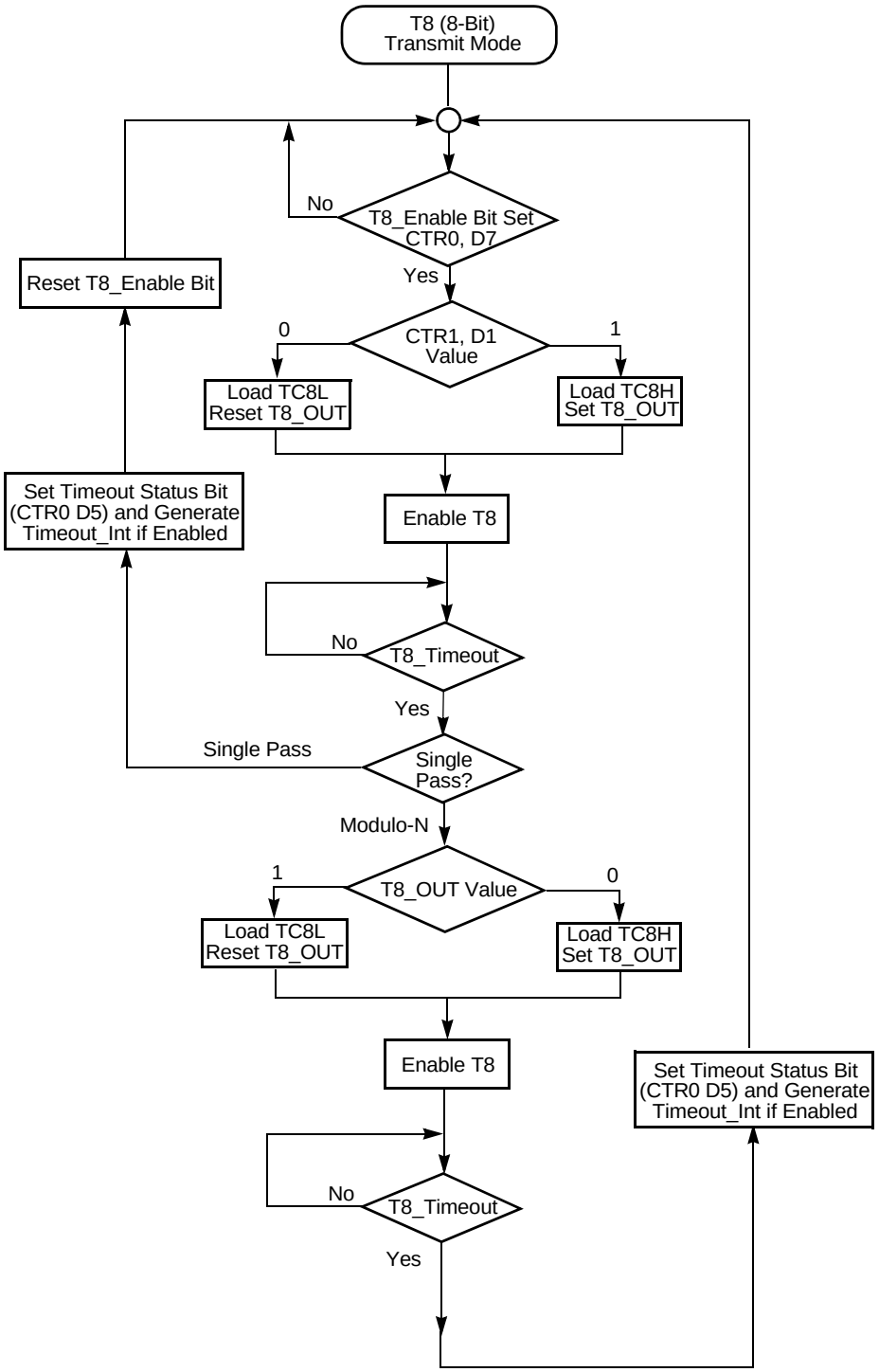


Figure 16.TRANSMIT Mode Flowchart

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In MODULO-N mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 17.

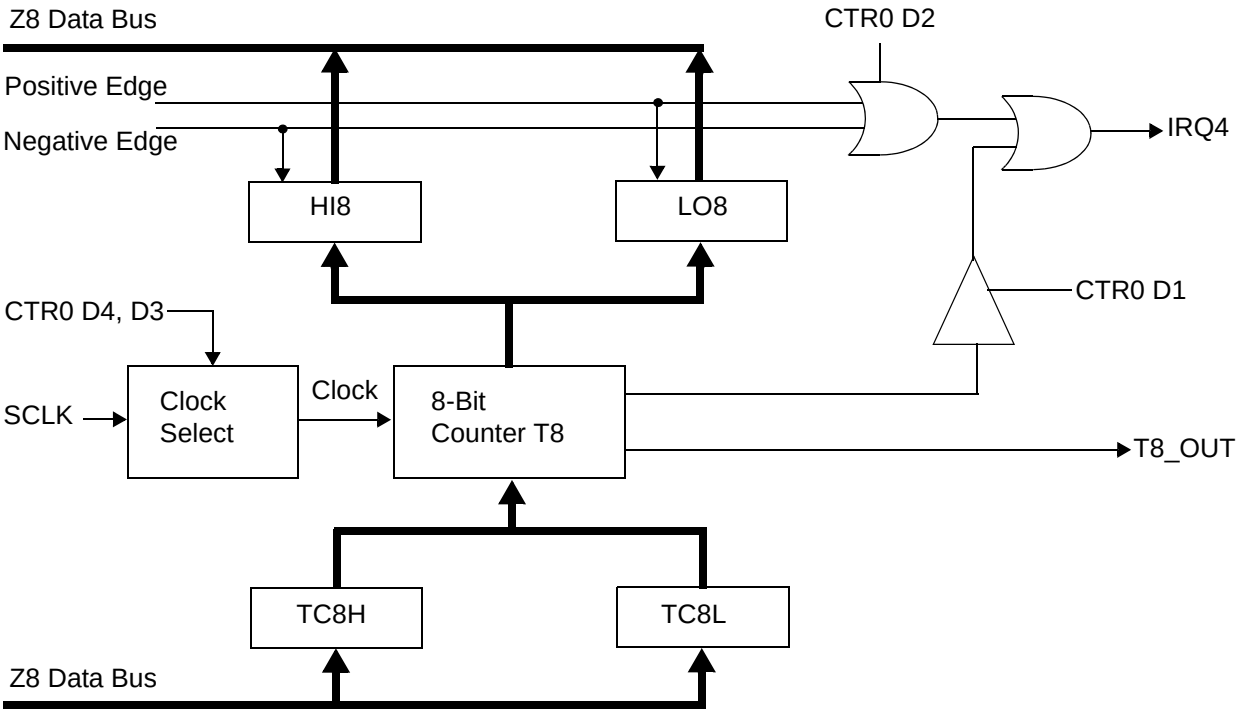


Figure 17.8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer.

An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.

Note: The letter H denotes hexadecimal values.

Transition from 0 to FFH is not a timeout condition.

Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 18 and Figure 19.

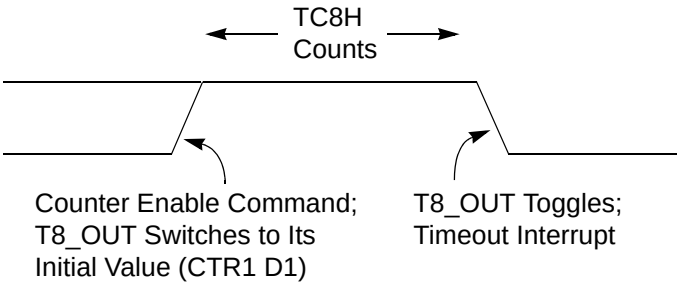


Figure 18. T8_OUT in SINGLE-PASS Mode

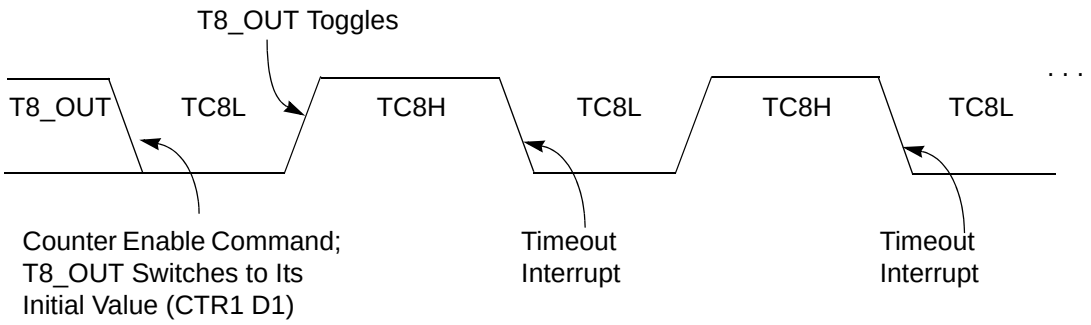


Figure 19. T8_OUT in MODULO-N Mode

T8 DEMODULATION Mode

You must program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 20 and Figure 21).

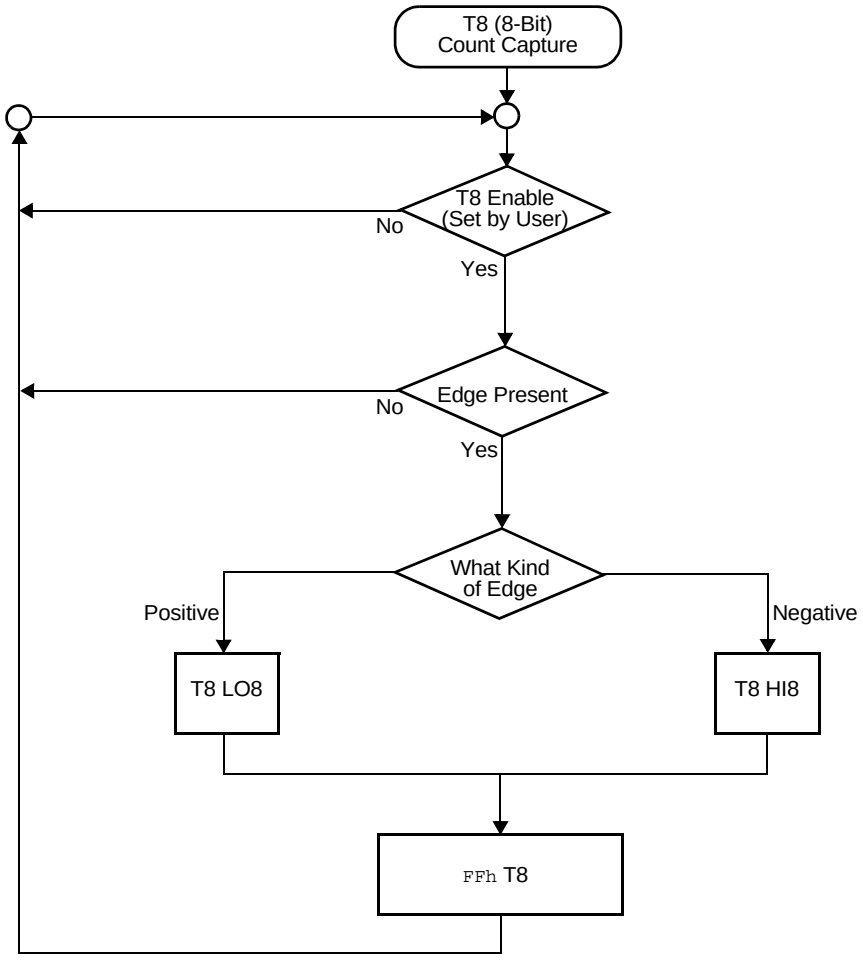


Figure 20.DEMODULATION Mode Count Capture Flowchart

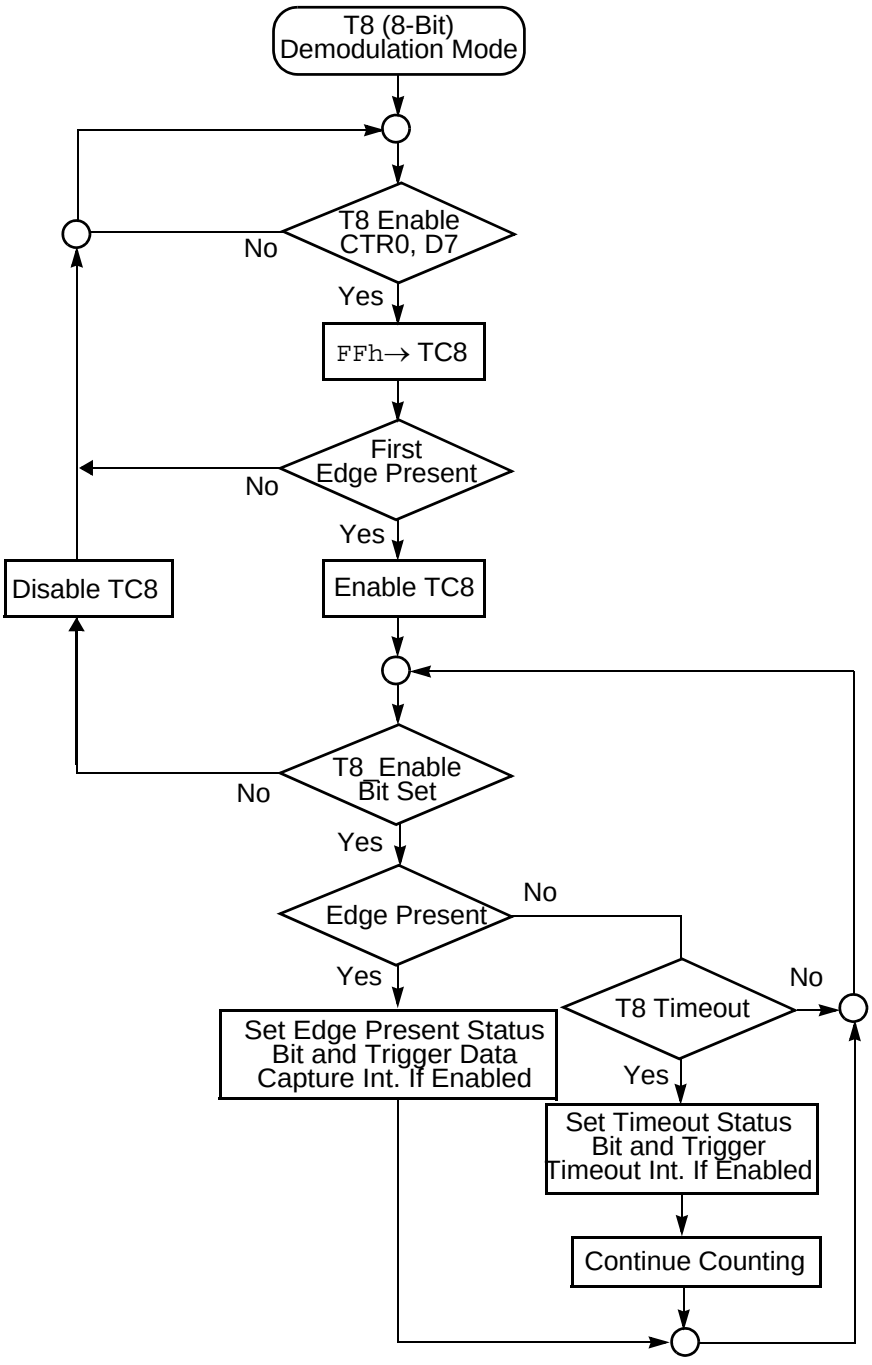


Figure 21. DEMODULATION Mode Flowchart

T16 TRANSMIT Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set (see Figure 22).

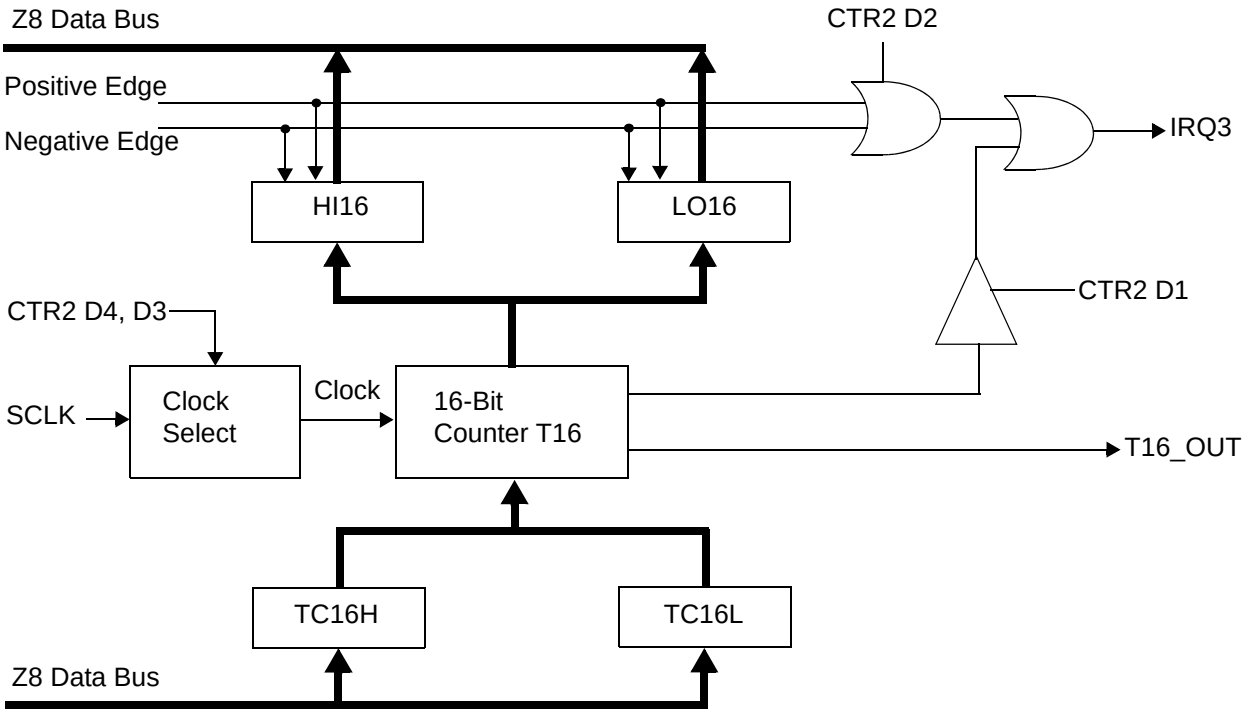


Figure 22.16-Bit Counter/Timer Circuits

Note: Global interrupts override this function as described in Interrupts on page 45.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 23 on page 42). If it is in MODULO-N mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 24 on page 42).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

Caution: Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFEH. Transition from 0 to FFFFH is not a timeout condition.

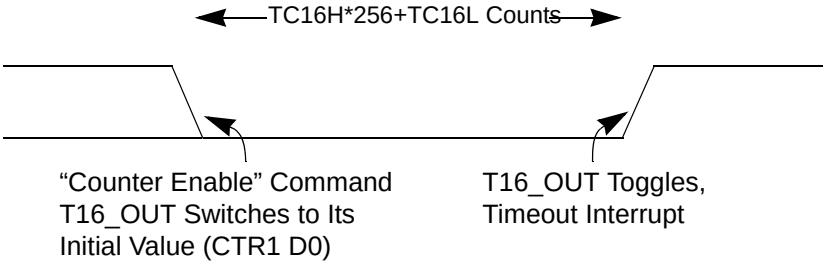


Figure 23.T16_OUT in SINGLE-PASS Mode

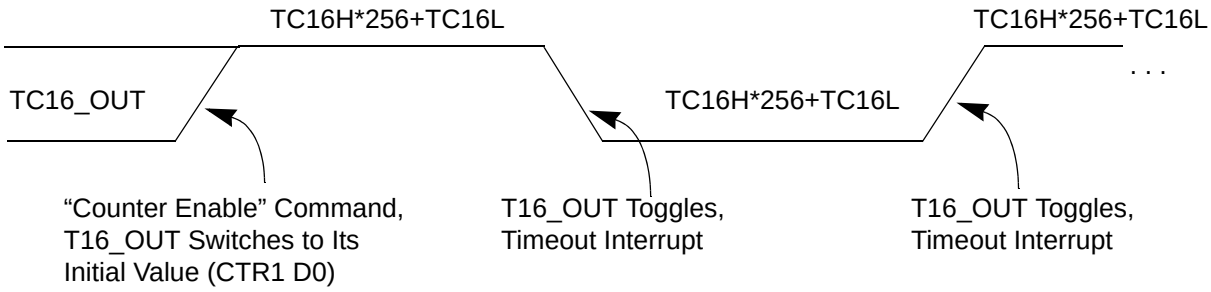


Figure 24.T16_OUT in Modulo-N Mode

T16 DEMODULATION Mode

You must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFH. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

PING-PONG Mode

This operation mode is only valid in TRANSMIT mode. T8 and T16 must be programmed in SINGLE-PASS mode (CTR0, D6; CTR2, D6), and PING-PONG mode must be programmed in CTR1, D3; D2. You can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 25.

Note: Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable

the counter/timers and reset the Status Flags before instituting this operation.

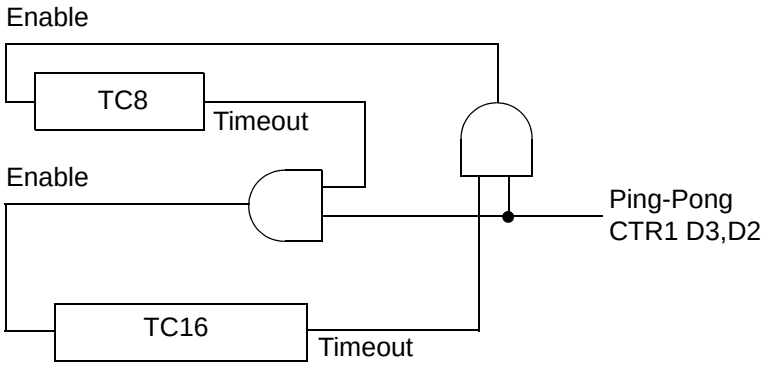


Figure 25.PING-PONG Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into SINGLE-PASS mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the PING-PONG mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 26.

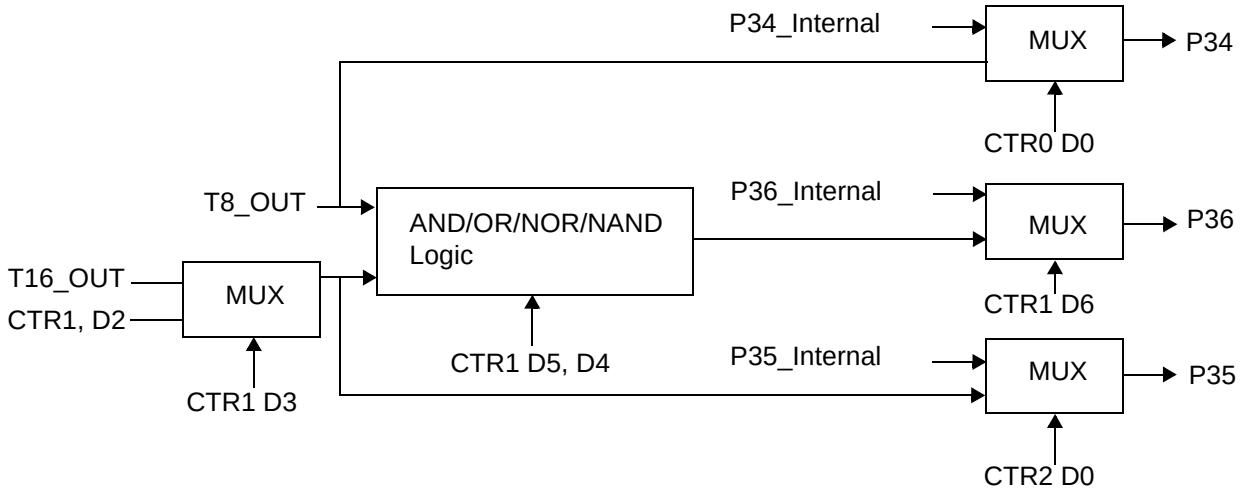


Figure 26.Output Circuit

The initial value of T8 or T16 must not be 1. If you stop the timer and restart the timer, reload the initial value to avoid an unknown previous value.

During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Timer Output

The output logic for the timers is displayed in Figure 26 on page 44. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of TI6-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

Interrupts

The Crimzon ZLR32300 features six different interrupts (see Table 11on page 47). The interrupts are maskable and prioritized (see Figure 27 on page 46). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (see Table 11 on page 47) and one for Low-Voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). In DIGITAL mode, Pin P33 is the source. In ANALOG mode the output of the Stop Mode Recovery source logic is used as the source for the interrupt. See Figure 32 on page 54.

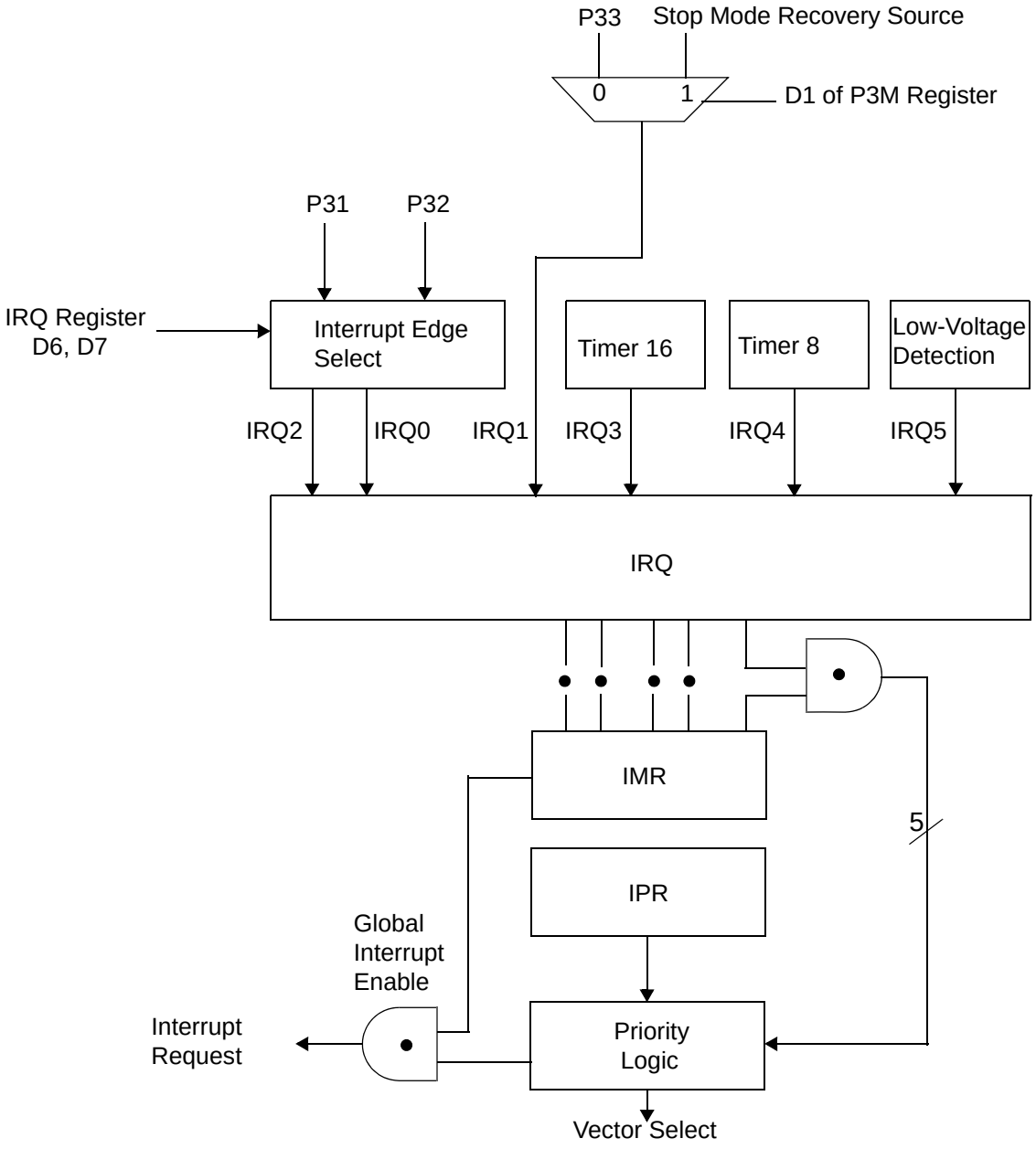


Figure 27. Interrupt Block Diagram

Table 11. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T_{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the Program Memory vector location reserved for that interrupt. All Crimzon ZLR32300 interrupts are vectored through locations in the Program Memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. You can program these interrupts. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 12.

Table 12.IRQ Register

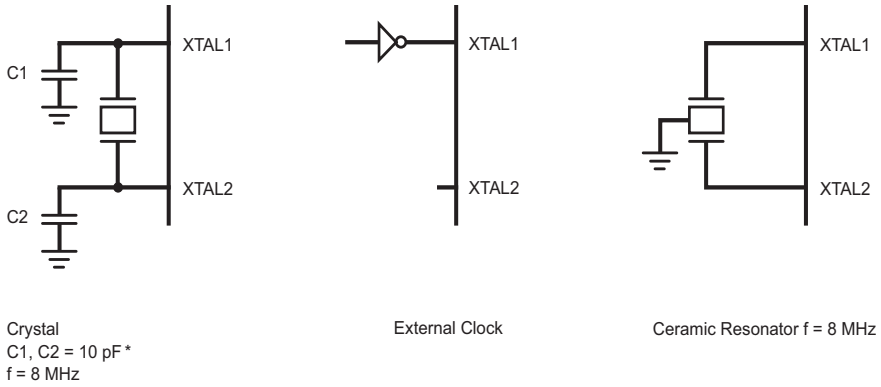
IRQ		Interrupt Edge	
D7	**D6**	**IRQ2 (P31)**	**IRQ0 (P32)**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Note: F = Falling Edge; R = Rising Edge

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω. The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors from each pin to ground. The typical capacitor value is 10 pF for 8 MHz. Also check with the crystal supplier for the optimum capacitance.



*Note: preliminary value.

Figure 28.Oscillator Configuration

Maxim's IR MCU supports crystal, resonator, and oscillator. Most resonators have a frequency tolerance of less than ±0.5%, which is enough for remote control application. Resonator has a very fast startup time, which is around few hundred microseconds. Most crystals have a frequency tolerance of less than 50 ppm (±0.005%). However, crystal needs longer startup time than the resonator. The large loading capacitance slows down the oscillation startup time. Maxim® suggests not to use more than 10 pF loading capacitor for the crystal. If the stray capacitance of the PCB or the crystal is high, the loading capacitance C1 and C2 must be reduced further to ensure stable oscillation before the T_{POR} (Power-On Reset time is typically 5–6 ms, see Table 20 on page 85).

For Stop Mode Recovery operation, bit 5 of SMR register allows you to select the Stop Mode Recovery delay, which is the T_{POR}. If Stop Mode Recovery delay is not selected, the MCU executes instruction immediately after it wakes up from the

STOP mode. If resonator or crystal is used as a clock source then Stop Mode Recovery delay has to be selected (bit 5 of SMR = 1).

For resonator and crystal oscillator, the oscillation ground must go directly to the ground pin of the microcontroller. The oscillation ground must use the shortest distance from the microcontroller ground pin and it must be isolated from other connections.

Power Management

Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-on reset timer function. The POR time allows V_{DD} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop Mode Register determines whether the POR timer is bypassed after Stop Mode Recovery (typical for external clock).

HALT Mode

This instruction turns OFF the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after HALT mode.

STOP Mode

This instruction turns OFF the internal clock and external crystal oscillation, reducing the standby current to 10 μA or less. STOP mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:

```
   FF          NOP         ; clear the pipeline
   6F          STOP        ; enter STOP mode
```

or

```
   FF          NOP         ; clear the pipeline
   7F          HALT        ; enter HALT Mode
```

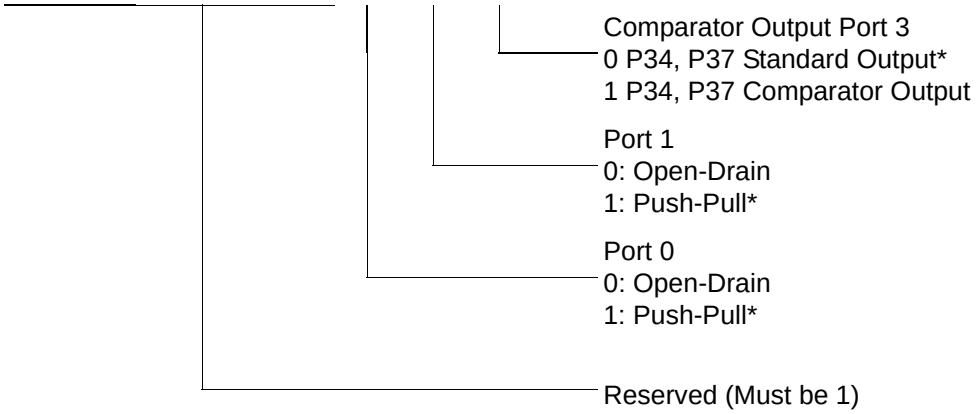
Port Configuration

Port Configuration Register

The Port Configuration (PCON) register (see Figure 29) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00h

D7	D6	D5	D4	D3	D2	D1	D0



*Default setting after reset.

Figure 29. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop Mode Recovery

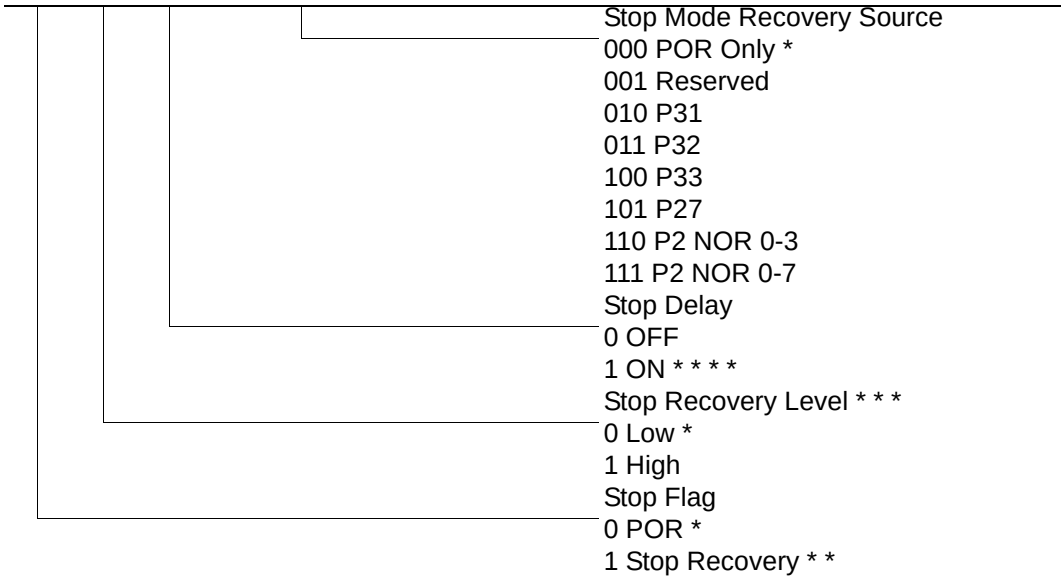
Stop Mode Recovery Register

This register selects the clock divide value and determines the mode of Stop Mode Recovery (see Figure 30). All bits are write only except bit 7, which is read only. Bit 7 is a Flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (see Figure 32 on page 54) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

SMR(0F)0Bh

D7	D6	D5	D4	D3	D2	D1	D0

SCLK/TCLK Divide-by-16
0 OFF * *
1 ON
Reserved (Must be 0)



*Default setting after reset.
* *Default setting after reset and Stop Mode Recovery.
* * *At the XOR gate input.
* * * *Default setting after reset. Recommended to be set to 1 if using a crystal or resonator clock source.

Figure 30. Stop Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (see Figure 31). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

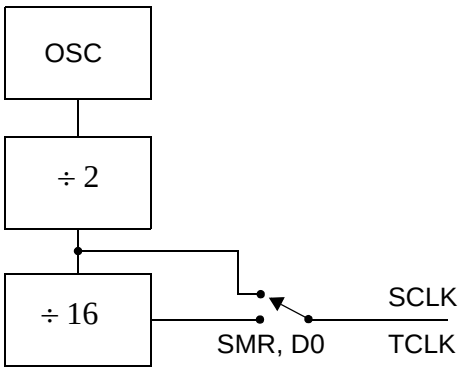


Figure 31.SCLK Circuit

Stop Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (see Figure 32 and Table 14).

Stop Mode Recovery Register 2—SMR2(F)0Dh

Table 13 lists and briefly describes the fields for this register.

Table 13. SMR2(F)0Dh:Stop Mode Recovery Register 2*

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0† 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000† 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND of P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

*Port pins configured as outputs are ignored as an SMR source.
†Indicates the value upon Power-On Reset.

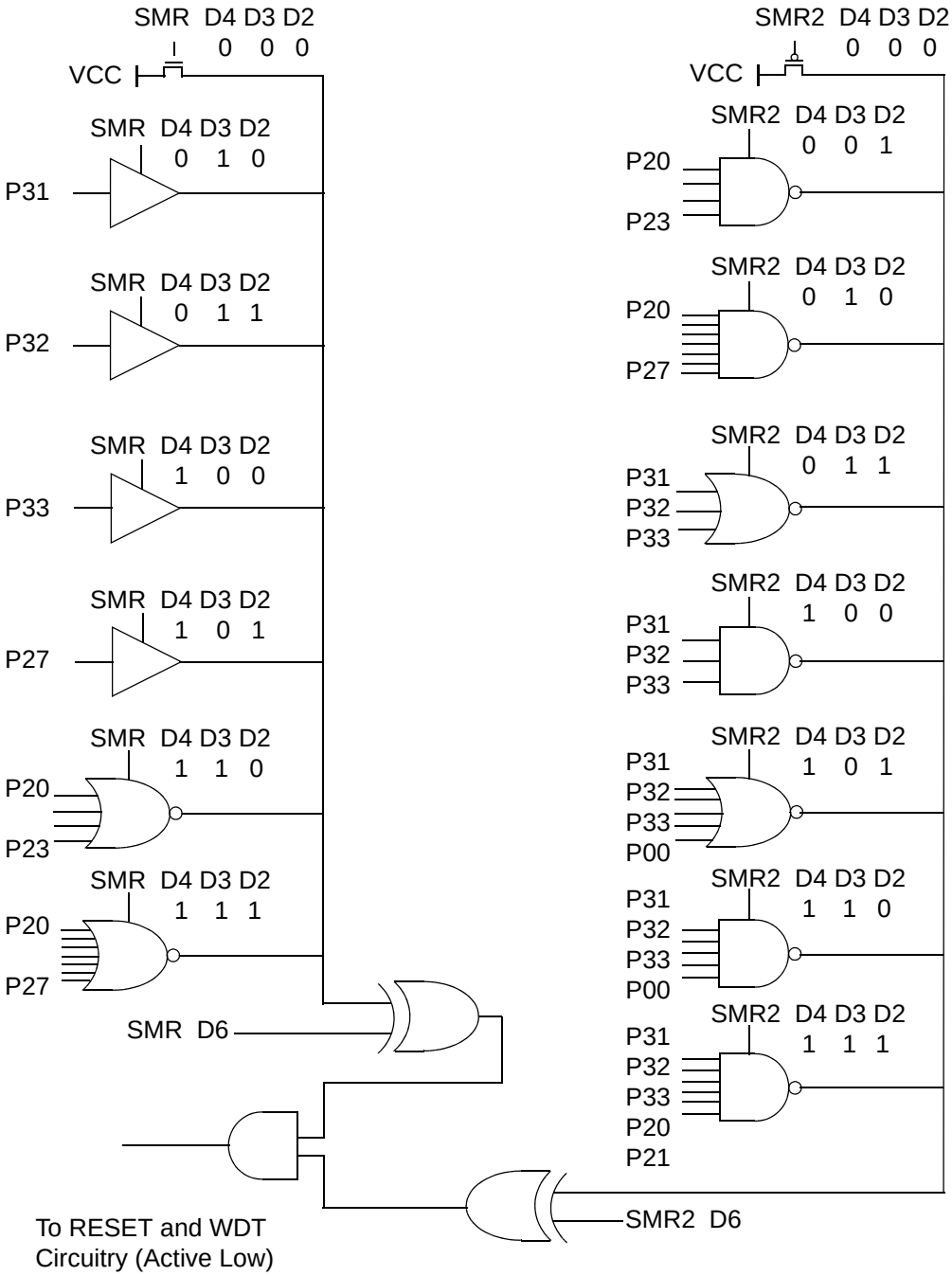


Figure 32. Stop Mode Recovery Source

Table 14. Stop Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note: Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. See SMR2 register on page 56 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the ‘fast’ wake up is selected, the Stop Mode Recovery source must be kept active for at least 10 TpC.

Note: This bit must be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Crimzon ZLR32300 from STOP mode. A 0 indicates Low level recovery. The default is 0 on POR.

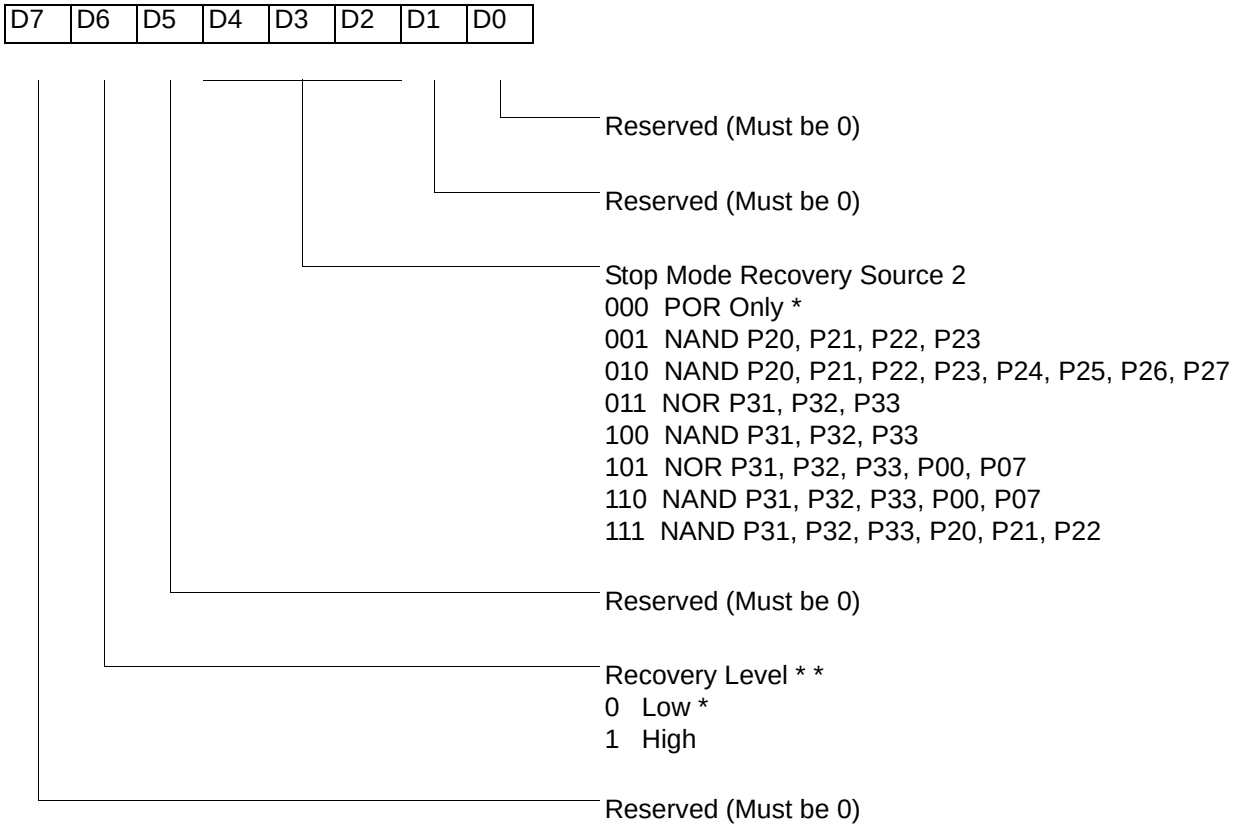
Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from STOP mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery.

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (see Figure 33).

SMR2(0F)Dh



Note: If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset.
**At the XOR gate input.

Figure 33. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

Note: Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an

output, the remaining SMR pins (P23–P21) form the NAND equation.

Watchdog Timer Mode

Watchdog Timer Mode Register (WDTMR)

The Watchdog Timer is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) Flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (see Figure 34). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-on reset, Watchdog Reset, or a Stop Mode Recovery (see Figure 33 on page 56). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as displayed in Figure 34.

WDTMR(0F)0Fh

D7	D6	D5	D4	D3	D2	D1	D0

WDT TAP INT RC OSC
00 10 ms min.
01* 20 ms min.
10 40 ms min.
11 160 ms min.

WDT During HALT
0 OFF
1 ON *

WDT During Stop
0 OFF
1 ON *

Reserved (Must be 0)

*Default setting after reset.

Figure 34. Watchdog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

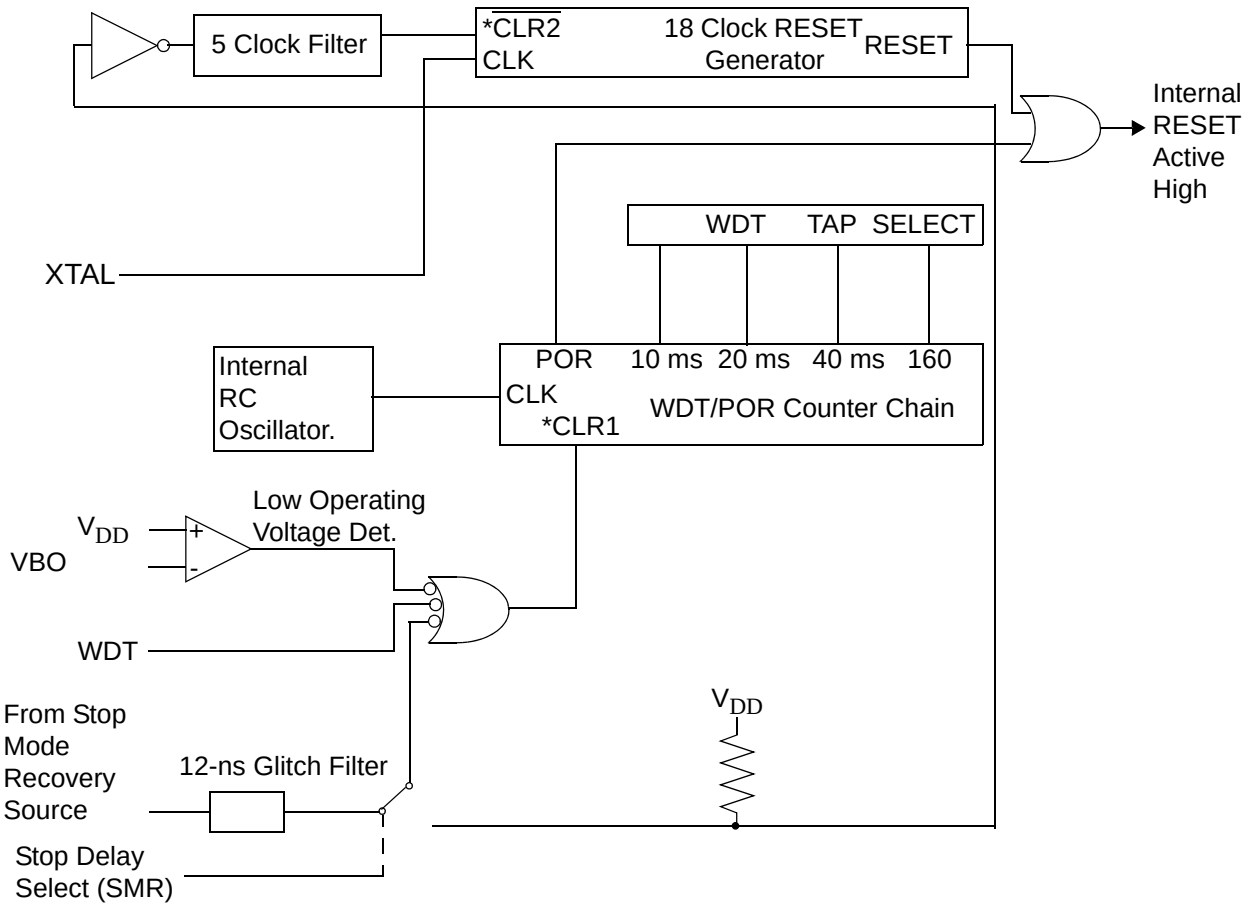
This bit selects the WDT time period. It is configured as indicated in Table 15.

Table 15. Watchdog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	10 ms min.
0	1	20 ms min.
1	0	40 ms min.
1	1	160 ms min.

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1. See Figure 35.



* CLR1 and $\overline{\text{CLR2}}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High input translation.

Figure 35. Resets and WDT

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during Stop. The default is 1.

ROM Selectable Options

There are seven ROM Selectable Options to choose from based on ROM code requirements. These are listed in Table 16.

Table 16. ROM Selectable Options

Port 00–03 Pull-Ups	ON/OFF
Port 04–07 Pull-Ups	ON/OFF
Port 10–13 Pull-Ups	ON/OFF
Port 14–17 Pull-Ups	ON/OFF
Port 20–27 Pull-Ups	ON/OFF
Port 3 Pull-Ups	ON/OFF
Watchdog Timer at Power-On Reset	ON/OFF

Voltage Brownout/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.

Low-Voltage Detection

Low-Voltage Detection Register—LVD(D)0CH

Note: Voltage detection does not work at STOP mode.

Field	Bit Position			Description
LVD	76543---			Reserved No Effect
	-----2--	R	1 0*	HVD Flag set HVD Flag reset
	------1-	R	1 0*	LVD Flag set LVD Flag reset
	-------0	R/W	1 0*	Enable VD Disable VD

*Default after POR.

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD Flag.

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0Ch at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The voltage detection is enabled when bit 0 of LVD register is set. Once voltage detection is enabled, the V_{CC} level is monitored in real time. The Flags in the LVD register valid 20 µs after voltage detection is enabled. The HVD Flag (bit 2 of the LVD register) is set only if V_{CC} is higher than $V_{HVD.}$ The LVD Flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When voltage detection is enabled, the LVD Flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a Flag only.

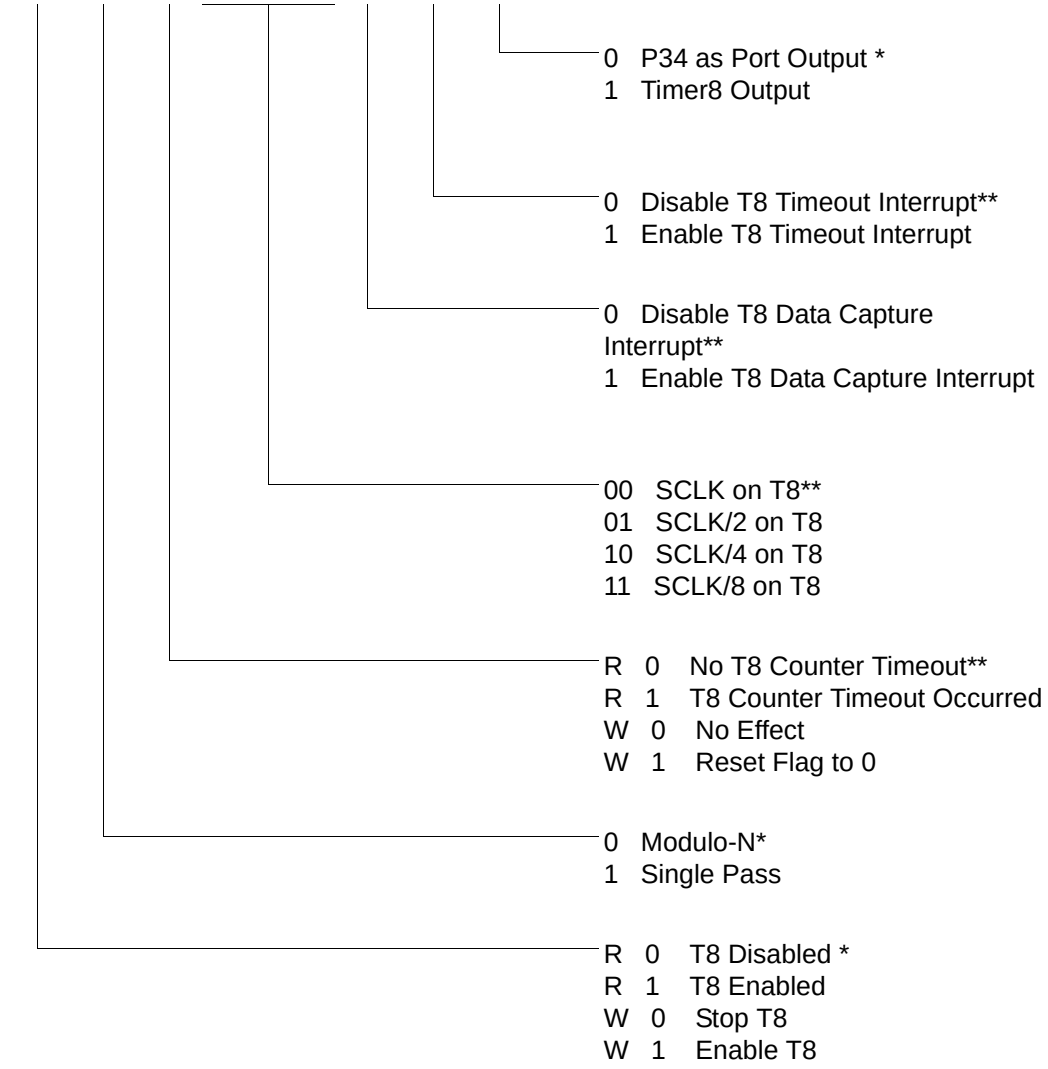
Note: If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low-battery detect threshold, enable interrupts using the Enable Interrupt (EI) instruction prior to enabling the voltage detection.

Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are displayed in Figure 36 on page 63 through Figure 40 on page 68.

CTR0(0D)00h

D7	D6	D5	D4	D3	D2	D1	D0

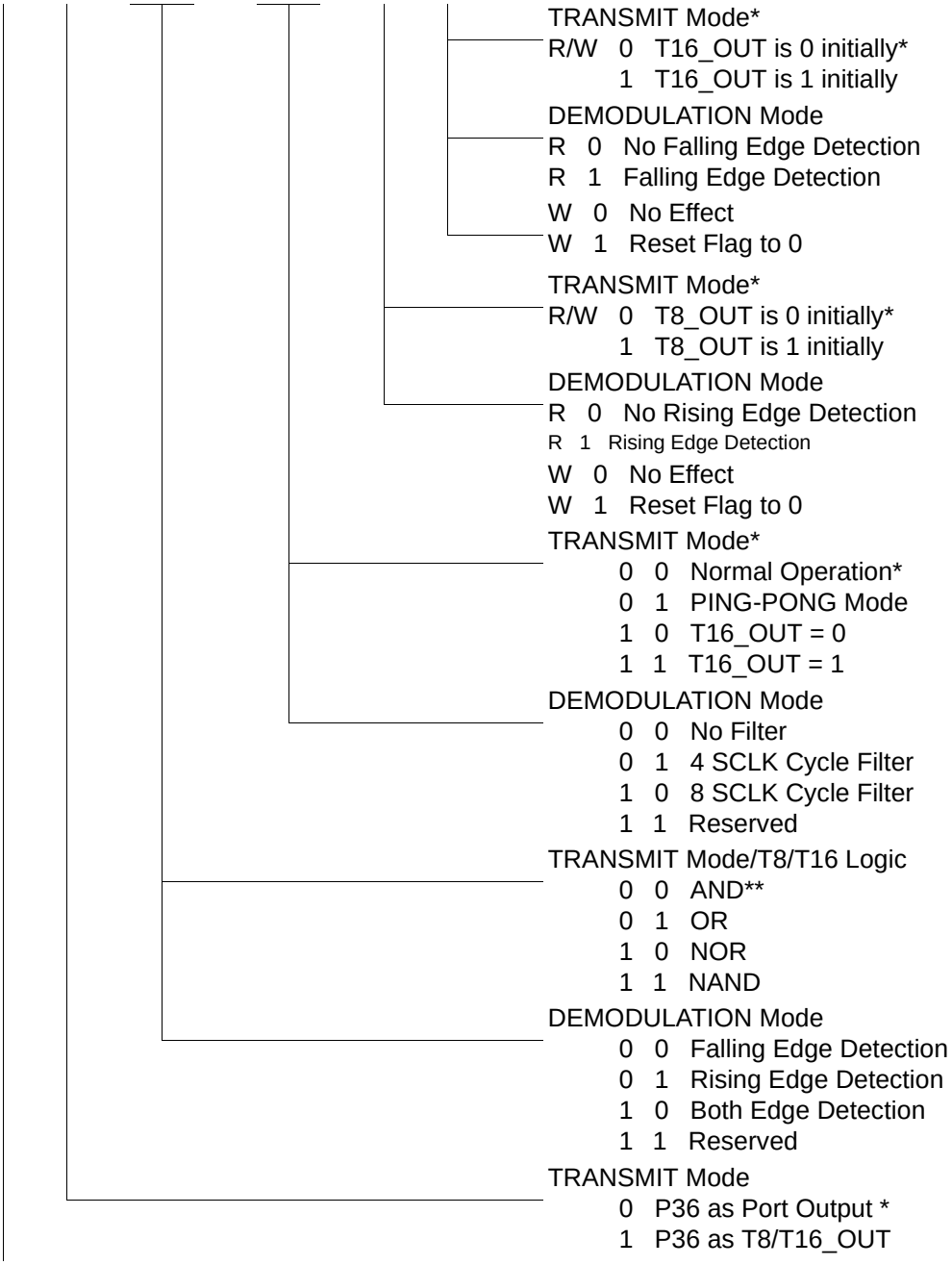


*Default setting after reset.
**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 36.TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)

CTR1(0D)01h

D7	D6	D5	D4	D3	D2	D1	D0



CTR1(0D)01h

		DEMODULATION Mode 0 P31 as Demodulator Input 1 P20 as Demodulator Input TRANSMIT/DEMODULATION Mode 0 TRANSMIT Mode * 1 DEMODULATION Mode

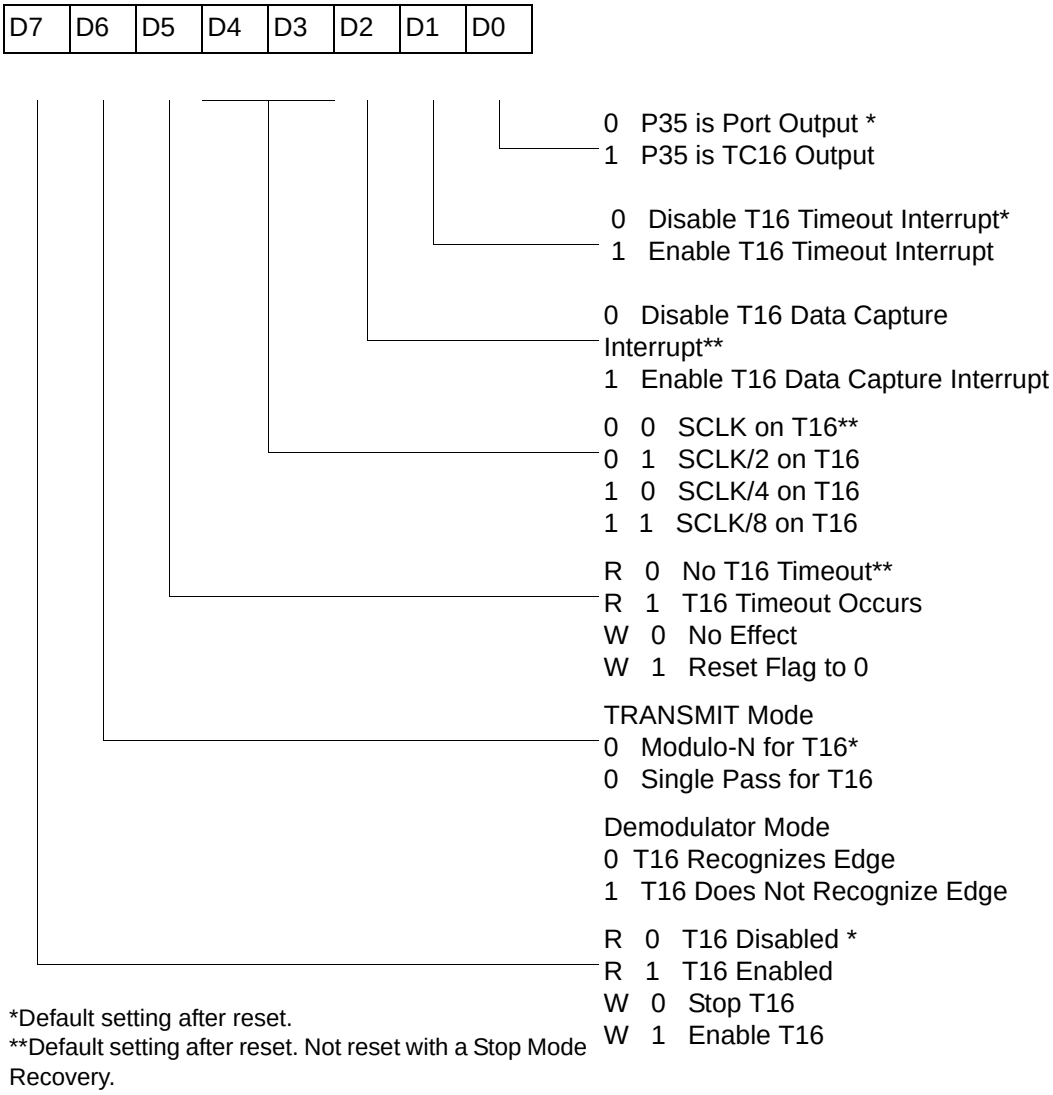
*Default setting after reset.
**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 37.T8 and T16 Common Control Functions ((0D)01H: Read/Write)

Note: Ensure differentiating the TRANSMIT mode from DEMODULATION mode. Depending on which of these two modes is operating, the CTR1 bit has different functions. Changing from one mode to another cannot be performed

without disabling the counter/timers.

CTR2(0D)02h



*Default setting after reset.
**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 38. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)

CTR3(0D)03h

D7	D6	D5	D4	D3	D2	D1	D0

Reserved
0 No Effect
1 Always reads 11111

Sync Mode
0** Disable Sync Mode
1 Enable Sync Mode

T_8 Enable
0* Counter Disabled
1 Counter Enabled
0 Stop Counter
1 Enable Counter

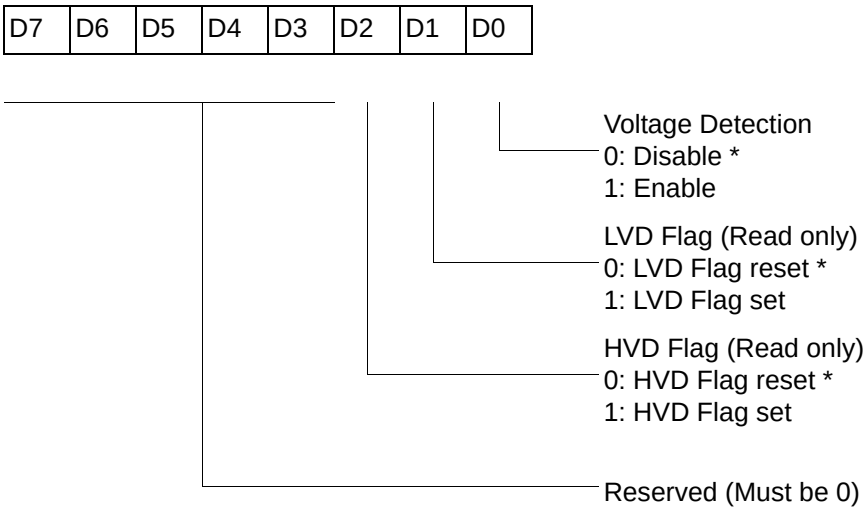
T_{16} Enable
0* Counter Disabled
1 Counter Enabled
0 Stop Counter
1 Enable Counter

*Default setting after reset.
**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 39. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

Note: If Sync Mode is enabled, the first pulse of T8 (carrier) is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.

LVD(0D)0Ch



*Default setting after reset.

Figure 40. Voltage Detection Register

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD Flag.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are displayed in Figure 41 on page 69 through Figure 54 on page 79.

PCON(0F)00h

D7	D6	D5	D4	D3	D2	D1	D0

Comparator Output Port 3
0 P34, P37 Standard Output *
1 P34, P37 Comparator Output

Port 1
0: Open-Drain
1: Push-Pull*

Port 0
0: Open-Drain
1: Push-Pull *

Reserved (Must be 1)

*Default setting after reset.

Figure 41. Port Configuration Register (PCON)(0F)00H: Write Only)

SMR(0F)0Bh

D7	D6	D5	D4	D3	D2	D1	D0

SCLK/TCLK Divide-by-16
0 OFF *
1 ON

Reserved (Must be 0)

Stop Mode Recovery Source
000 POR Only * *
001 Reserved
010 P31
011 P32
100 P33
101 P27
110 P2 NOR 0–3
111 P2 NOR 0–7

Stop Delay
0 OFF
1 ON * * * *

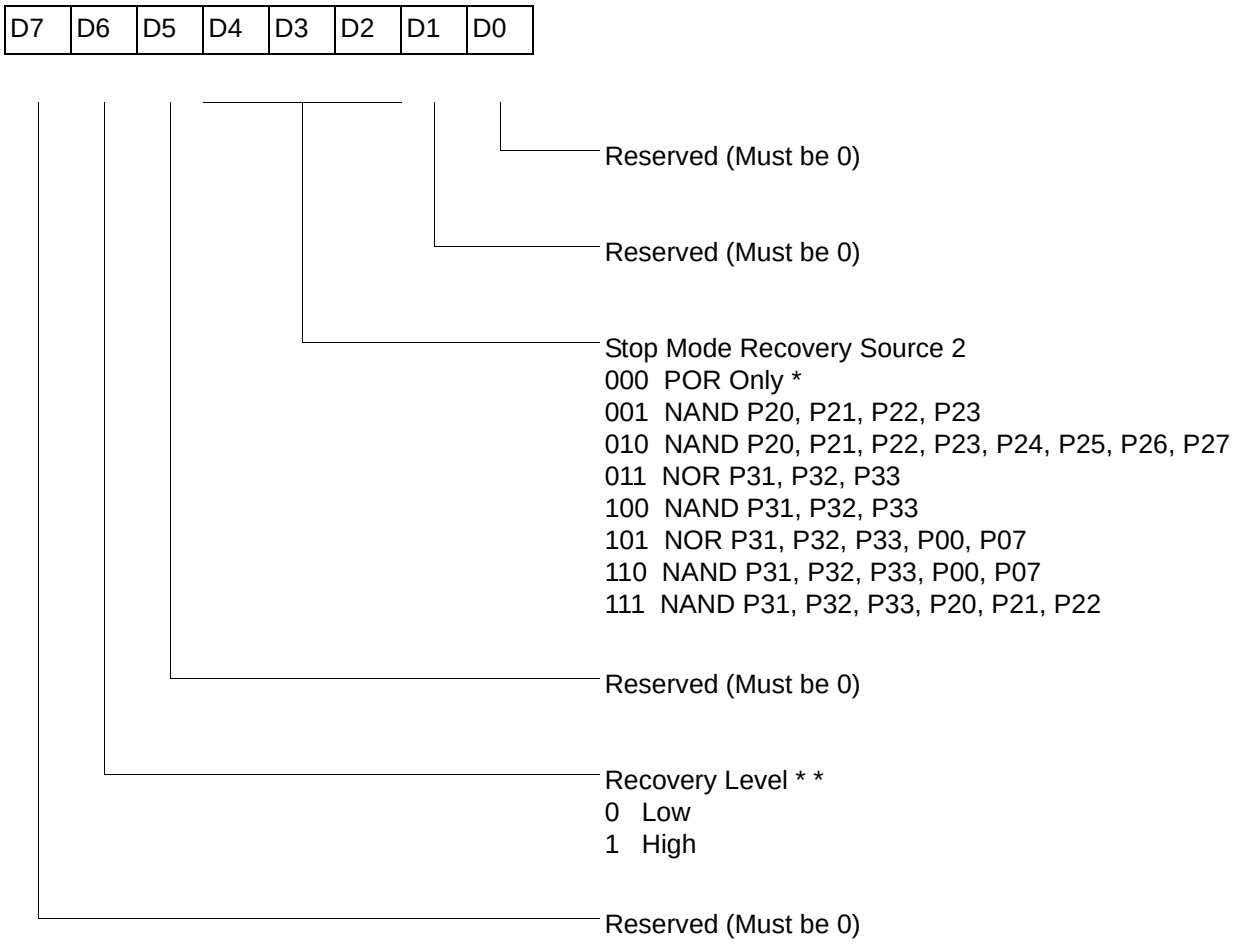
Stop Recovery Level * * *
0 Low **
1 High

Stop Flag
0 POR * * * * *
1 Stop Recovery * *

*Default setting after reset.
* *Default setting after reset and Stop Mode Recovery.
* * *At the XOR gate input.
* * * *Default setting after reset. Recommended to be set to 1 if using a crystal or resonator clock source.Not reset with Stop Mode Recovery.
* * * * *Default setting after Power-On Reset.

Figure 42. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)

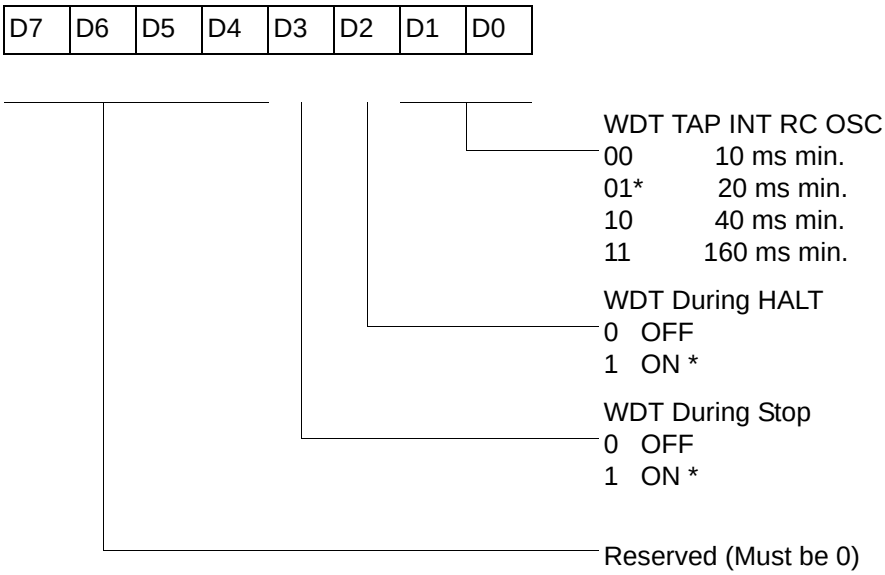
SMR2(0F)0Dh



Note: If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset. Not reset with a Stop Mode Recovery.
* *At the XOR gate input.

Figure 43. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)

WDTMR(0F)0Fh



*Default setting after reset. Not reset wit a Stop Mode Recovery.

Figure 44. Watchdog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers

The standard control registers are displayed in Figure 45 through Figure 54 on page 79.

R246P2M(F6H)

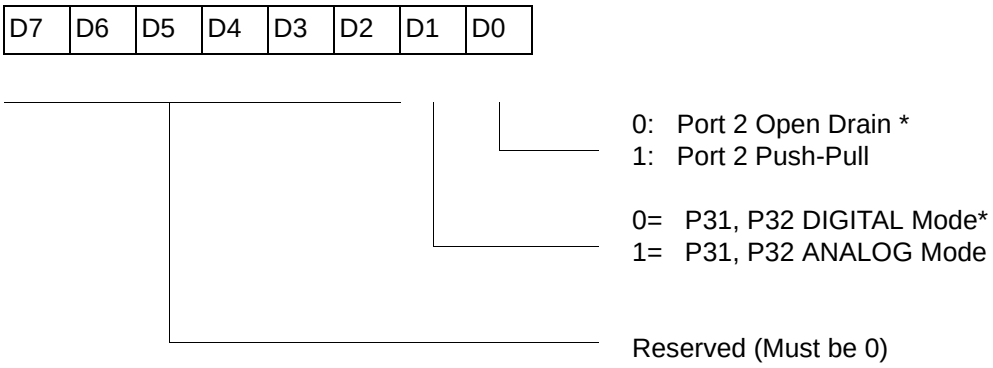
D7	D6	D5	D4	D3	D2	D1	D0

P27–P20 I/O Definition
0 Defines bit as OUTPUT
1 Defines bit as INPUT *

*Default setting after reset. Not reset wit a Stop Mode Recovery.

Figure 45. Port 2 Mode Register (F6H: Write Only)

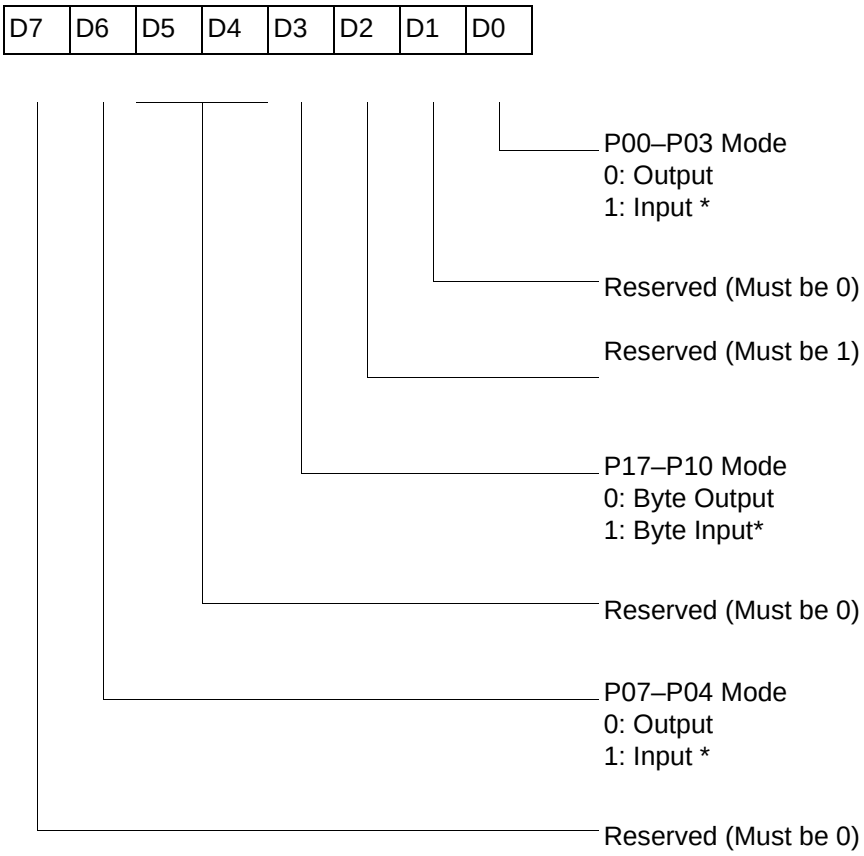
R247P3M(F7H)



*Default setting after reset. Not reset wit a Stop Mode recovery.

Figure 46. Port 3 Mode Register (F7H: Write Only)

R248 P01M(F8H)



*Default setting after reset; only P00, P01, and P07 are available on Crimzon ZLR32300 20-pin configurations.

Figure 47.Port 0 and 1 Mode Register (F8H: Write Only)

R249 IPR(F9H)

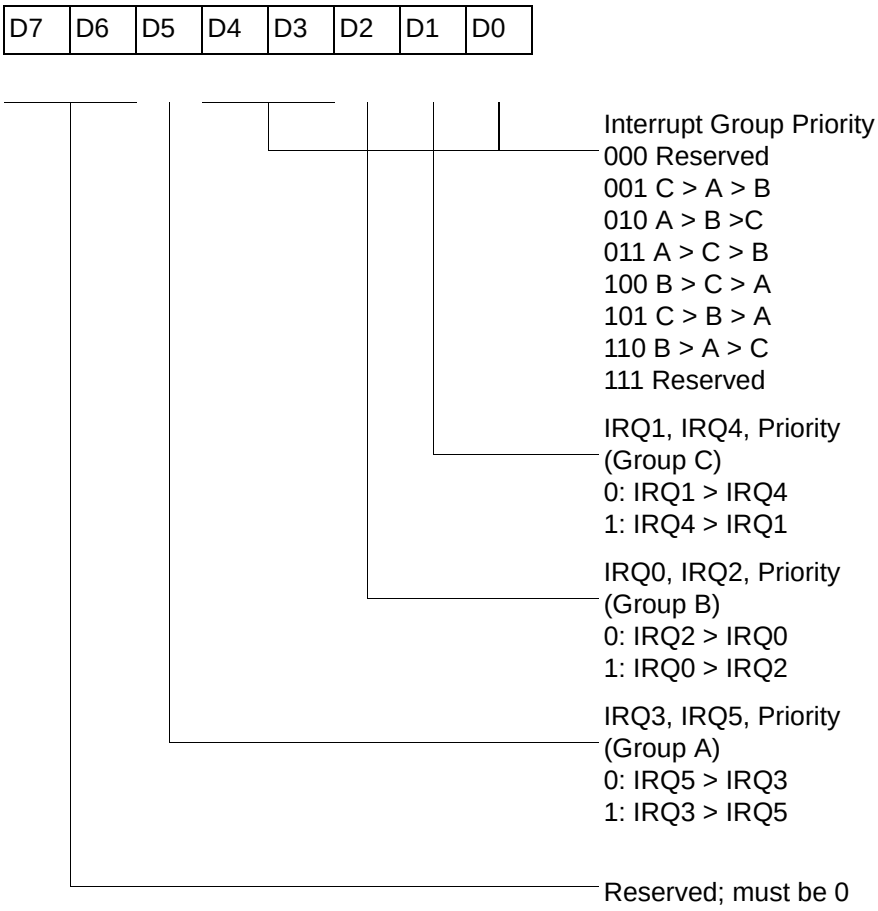


Figure 48.Interrupt Priority Register (F9H: Write Only)

R250 IRQ(FAH)

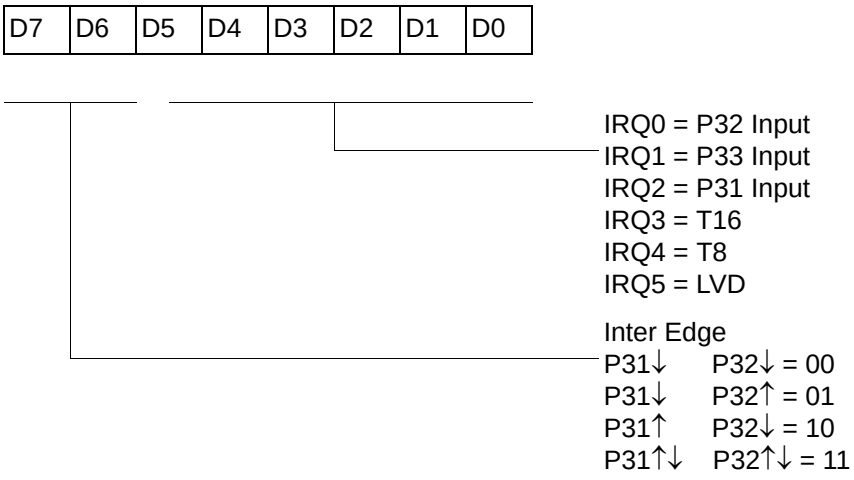
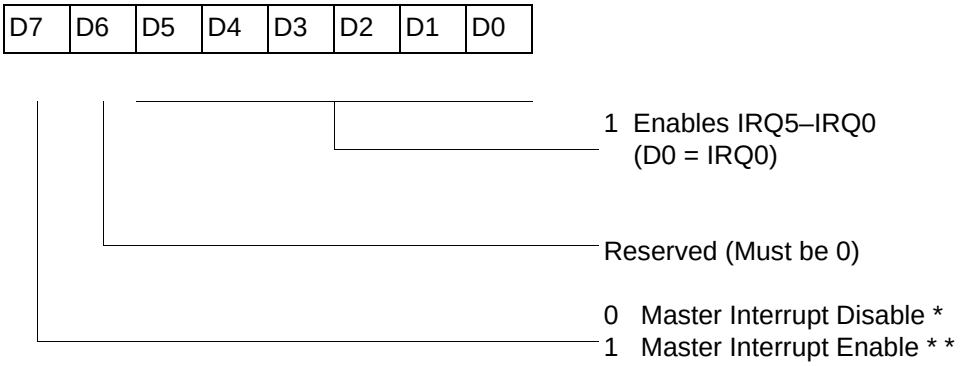


Figure 49.Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



*Default setting after reset.
* *Only by using EI, DI instruction; DI is required before changing the IMR register.

Figure 50.Interrupt Mask Register (FBH: Read/Write)

R252 Flags(FCH)

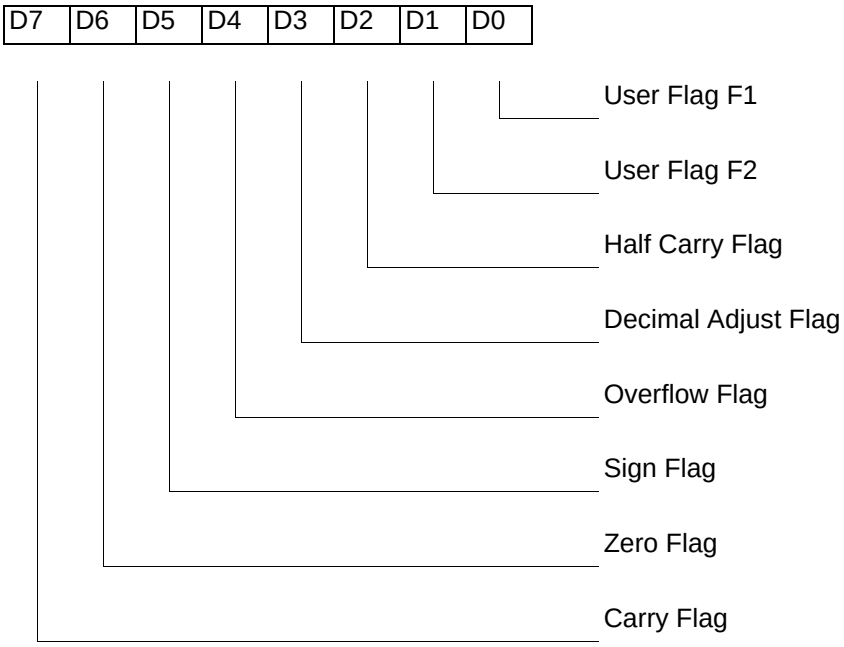
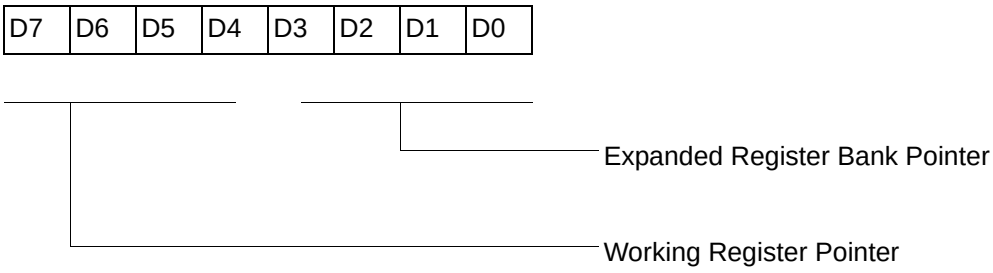


Figure 51.Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 52.Register Pointer (FDH: Read/Write)

R254 SPH(FEH)

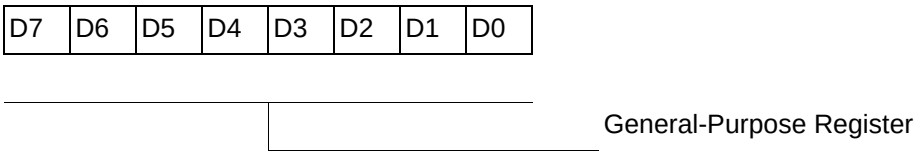


Figure 53.Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

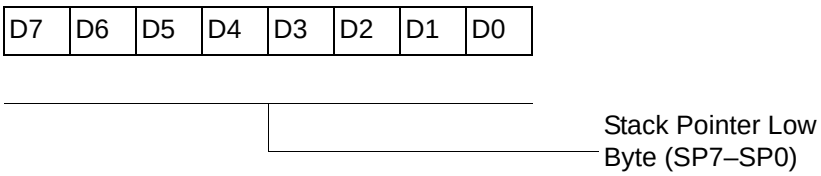


Figure 54.Stack Pointer Low (FFH: Read/Write)

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than those listed in Table 17 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 17.Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	0	+70	C	
Storage temperature	–65	+150	C	
Voltage on any pin with respect to V_{SS}	–0.3	+4.0	V	1
Voltage on V_{DD} pin with respect to V_{SS}	–0.3	+3.6	V	
Maximum current on input and/or inactive output pin	–5	+5	µA	
Maximum output current from active output pin	–25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	

[1]This voltage applies to all pins except the following: V_{DD} and $\overline{\text{RESET}}$.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 55 on page 81).

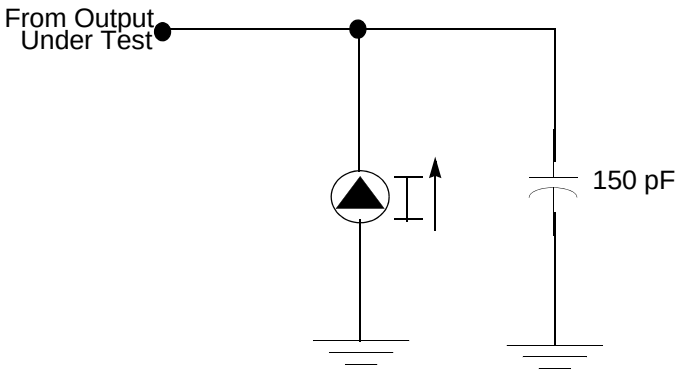


Figure 55.Test Load Diagram

Capacitance

Table 18 lists the capacitances.

Table 18.Capacitance

Parameter	Maximum
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF
Note: T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND	

DC Characteristics

Table 19.DC Characteristics

T_A= 0 °C to +70 °C								
Symbol	**Parameter**	**V_{CC}**	**Minimum**	**Typ(7)**	**Maximum**	**Units**	**Conditions**	**Notes**
V_{CC}	Supply Voltage		2.0		3.6	V	See notes 5	5
V_{CH}	Clock Input High Voltage	2.0-3.6	$0.8V_{CC}$		V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-3.6	V_{SS}–0.3		0.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-3.6	$0.7V_{CC}$		V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0-3.6	V_{SS}–0.3		0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0-3.6	V_{CC}–0.4			V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	V_{CC}–0.8			V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.0-3.6			0.4	V	I_{OL} = 4.0 mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	I_{OL} = 10 mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-3.6	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-3.6	–1		1	µA	V_{IN} = 0 V, V_{CC} Pull-ups disabled	
R_{PU}	Pull-Up Resistance		225		675	K Ω	V_{IN} = 0 V; Pullups selected by mask option	
			75		275	K Ω		
I_{OL}	Output Leakage	2.0-3.6	–1		1	µA	V_{IN} = 0 V, V_{CC}	
I_{CC}	Supply Current	2.0 3.6		1.2 2.2	3 5	mA mA	at 8.0 MHz at 8.0 MHz	1, 2 1, 2
I_{CC1}	Standby Current (HALT mode)	2.0 3.6		0.5 0.8	1.6 2.0	mA mA	V_{IN} = 0 V, V_{CC} at 8.0 MHz Same as above	1, 2, 6 1, 2, 6

Table 19.DC Characteristics (Continued)

T_A= 0 °C to +70 °C								
Symbol	**Parameter**	**V_{CC}**	**Minimum**	**Typ(7)**	**Maximum**	**Units**	**Conditions**	**Notes**
I_{CC2}	Standby Current (STOP mode)	2.0 3.6 2.0 3.6		1.5 2.1 4.7 7.4	8 10 20 30	µA µA µA µA	V_{IN} = 0 V, V_{CC} WDT is not Running Same as above V_{IN} = 0 V, V_{CC} WDT is Running Same as above	3 3 3 3
I_{LV}	Standby Current (Low Voltage)			1.0	6	µA	Measured at 1.3 V	4
V_{BO}	V_{CC} Low Voltage Protection			1.8	2.0	V	8 MHz maximum Ext. CLK Freq.	
V_{LVD}	Vcc Low Voltage Detection			2.4		V		
V_{HVD}	Vcc High Voltage Detection			2.7		V		

Notes:
1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 µF), physically close to VDD and GND if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 °C.

AC Characteristics

Figure 56 on page 84 and Table 20 on page 85 describe the AC characteristics.

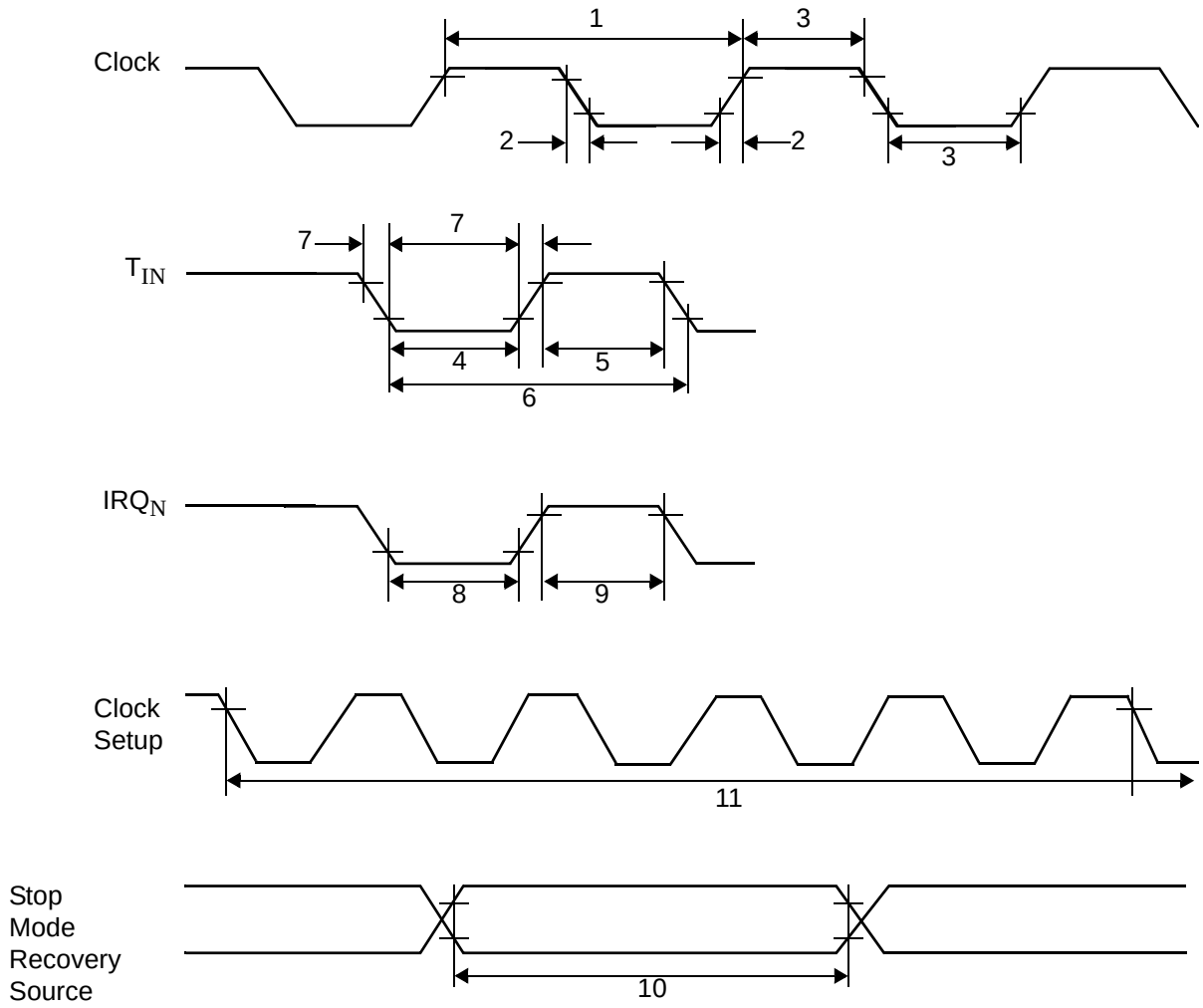


Figure 56. AC Timing Diagram

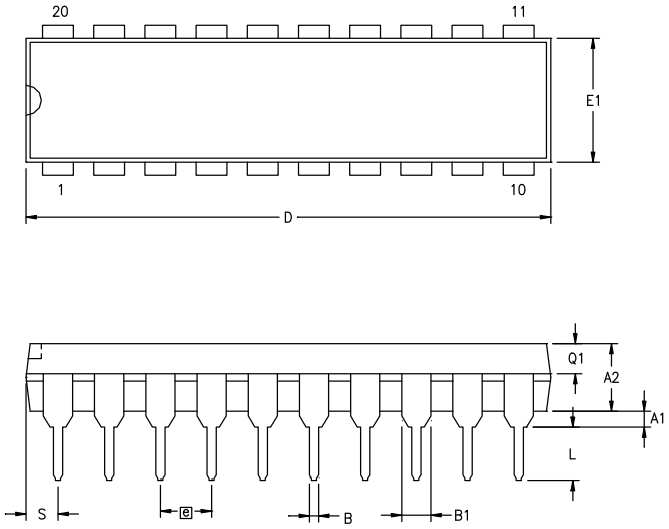
Table 20.AC Characteristics

T_A=0 °C to +70 °C 8.0 MHz								
No	**Symbol**	**Parameter**	**V_{CC}**	**Minimum**	**Maximum**	**Units**	**Notes**	**Watchdog Timer Mode Register (D1, D0)**
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0–3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1	
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–3.6	10TpC			1, 2	
10	Twsm	Stop Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4	
12	Twdt	Watchdog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	10 20 40 160		ms ms ms ms		0, 0 0, 1 1, 0 1, 1
13	T_{POR}	Power-On Reset	2.0–3.6	2.5	10	ms		

Notes:
1.Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2.Interrupt request through Port 3 (P33–P31).
3.SMR – D5 = 1.
4.SMR – D5 = 0.

Packaging

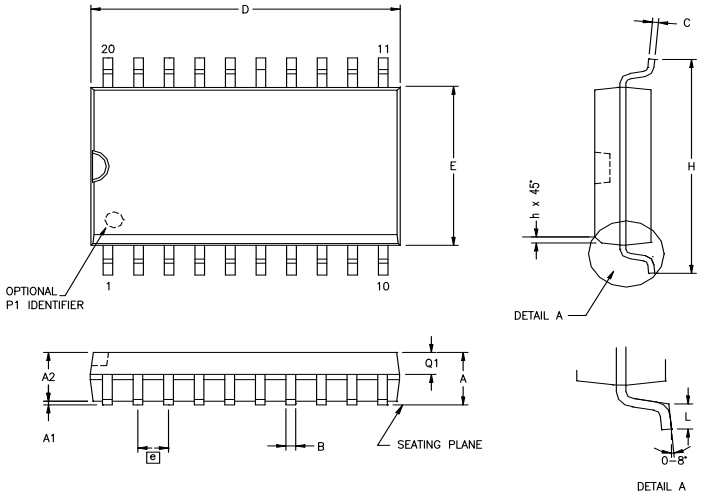
Package information for all versions of Crimzon ZLR32300 is displayed in Figure 57 through Figure 63 on page 91.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

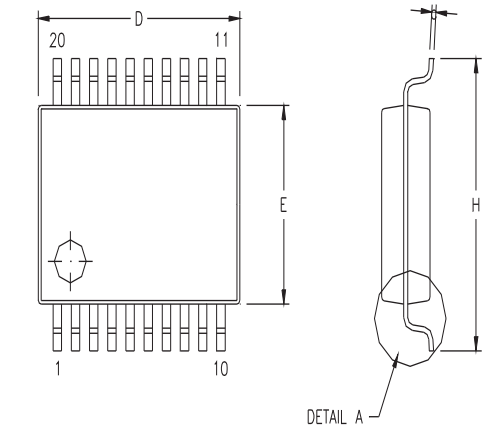
Figure 57.20-Pin PDIP Package Diagram



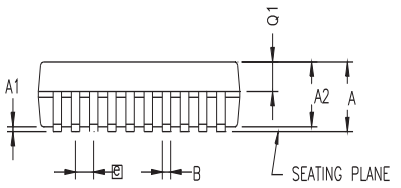
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	**.496**	.510
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

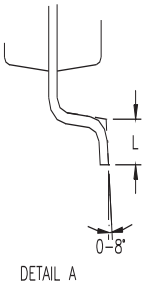
CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 58.20-Pin SOIC Package Diagram



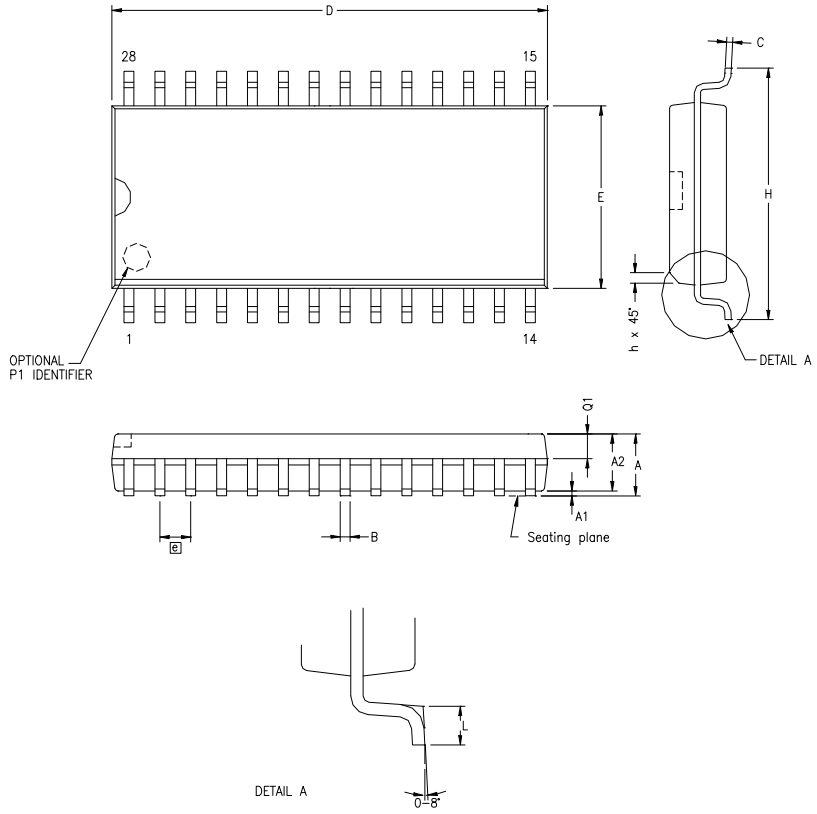
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 BSC			0.0256 BSC		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

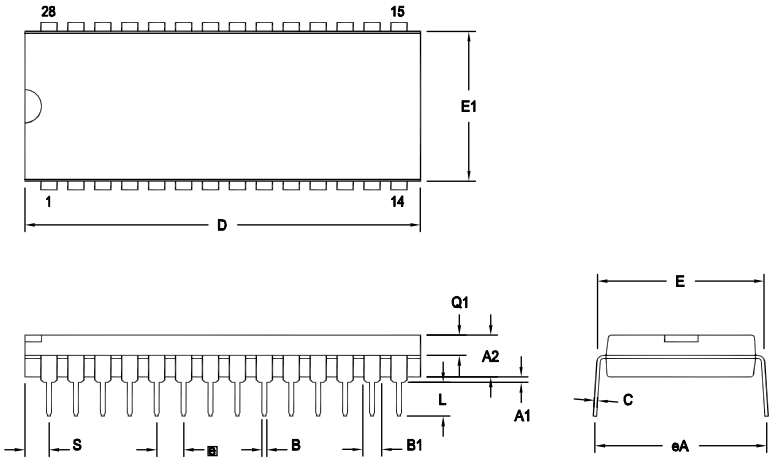
Figure 59. 20-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 60. 28-Pin SOIC Package Diagram



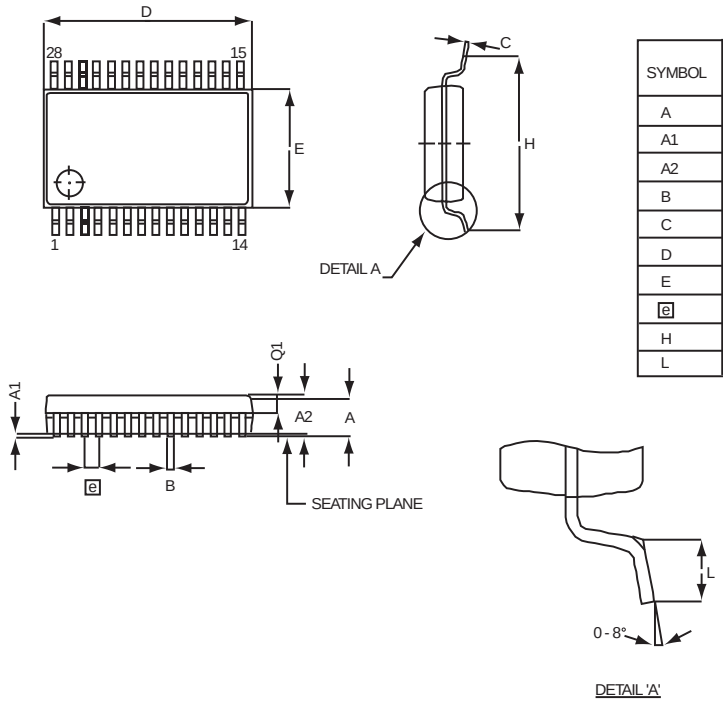
SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

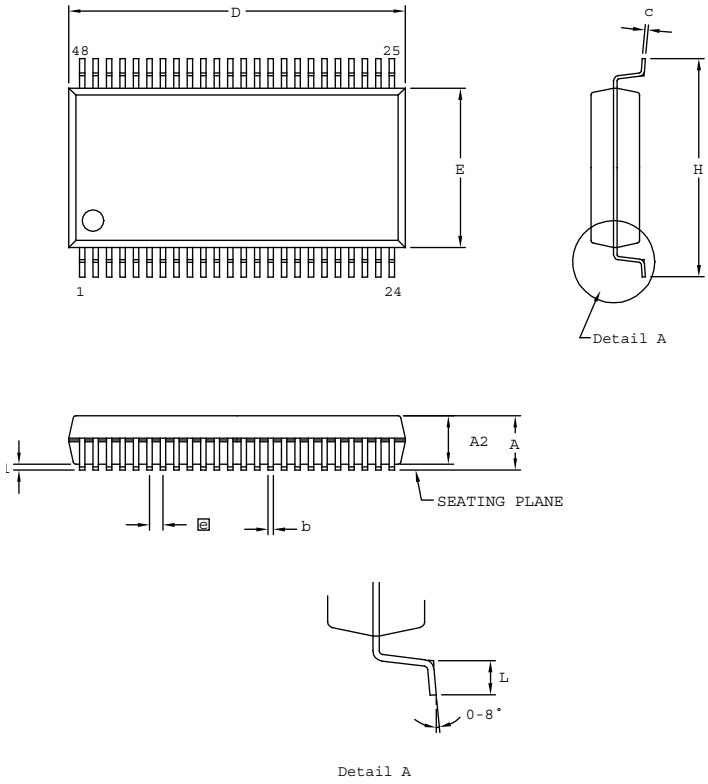
Figure 61. 28-Pin PDIP Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.86	1.99	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.78	0.066	0.068	0.070
B	0.25		0.38	0.010		0.015
C	0.09	–	0.20	0.004	0.006	0.008
D	10.07	10.20	10.33	0.397	0.402	0.407
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.63	0.75	0.95	0.025	0.030	0.037

CONTROLLING DIMENSIONS: MM
LEADS ARE COPLANAR WITHIN .004 INCHES.

Figure 62. 28-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
e	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 63. 48-Pin SSOP Package Design

Note: Contact Maxim® on the actual bonding diagram and coordinate for chip-on-board assembly.

Ordering Information

The following table provides part number, description, and memory size of Crimzon ZLR32300.

Memory Size	Part Number	Description
32 K	**ZLR32300H4832G**	48-pin SSOP 32 K ROM
	ZLR32300H2832G	28-pin SSOP 32 K ROM
	ZLR32300P2832G	28-pin PDIP 32 K ROM
	ZLR32300S2832G	28-pin SOIC 32 K ROM
	ZLR32300H2032G	20-pin SSOP 32 K ROM
	ZLR32300P2032G	20-pin PDIP 32 K ROM
	ZLR32300S2032G	20-pin SOIC 32 K ROM
24 K	**ZLR32300H4824G**	48-pin SSOP 24 K ROM
	ZLR32300H2824G	28-pin SSOP 24 K ROM
	ZLR32300P2824G	28-pin PDIP 24 K ROM
	ZLR32300S2824G	28-pin SOIC 24 K ROM
	ZLR32300H2024G	20-pin SSOP 24 K ROM
	ZLR32300P2024G	20-pin PDIP 24 K ROM
	ZLR32300S2024G	20-pin SOIC 24 K ROM
16 K	**ZLR32300H4816G**	48-pin SSOP 16 K ROM
8 K	**ZLR32300H4808G**	48-pin SSOP 8 K ROM
4 K	ZLR32300H4804G	48-pin SSOP 4 K ROM
	Development Tools	
	ZLP128ICE01ZEMG*	In-Circuit Emulator
	Note: *ZLP128ICE01ZEMG has been replaced by an improved version, ZCRMZNICE01ZEMG.	
	ZLP323ICE01ZACG	40-PDIP/48-SSOP Accessory Kit
	ZCRMZNICE01ZEMG	Crimzon In-Circuit Emulator
	ZCRMZN00100KITG	Crimzon In-Circuit Emulator Development Kit
	ZCRMZNICE01ZACG	20-Pin Accessory Kit
	ZCRMZNICE02ZACG	40/48-Pin Accessory Kit

Memory Size	Part Number	Description

Note: Contact www.maxim-ic.com for the die form.

For fast results, contact your local Maxim sales office for assistance in ordering the part desired.

Part Number Description

Maxim part numbers consist of a number of components, as displayed in Figure 64. The example part number ZLR32300H2832G is a Crimzon masked ROM product in a 28-pin SSOP package, with 32 KB of ROM and built with lead-free solder.

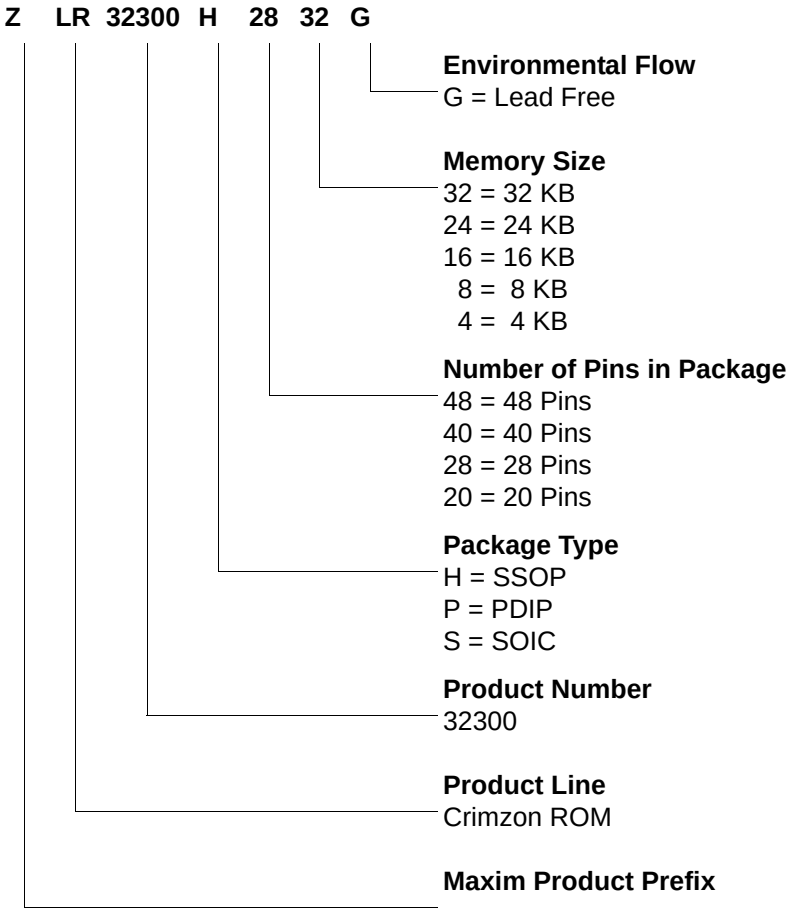


Figure 64. Part Number Description Example

Index

Numerics

A

B

C

D

E

F

G

H

I

L

M

O

P

R

S

T

V

W

X

Customer Support

For any comments, detail technical questions, or reporting problems, please visit Maxim's Technical Support at https://support.maxim-ic.com/micro.