

LEA-M8F

u-blox M8 time and frequency reference GNSS module

Hardware Integration Manual

Abstract

This document describes the hardware features and design-in aspects for the LEA-M8F time and frequency reference module. This device incorporates the u-blox M8 concurrent GNSS IC that can receive GPS, GLONASS, BeiDou and QZSS signals. It provides a low phase noise 30.72MHz system reference oscillator disciplined by GNSS, a precise and jitter-free time-pulse and features high sensitivity signal acquisition and single satellite timing with automatic hold over during signal outage.



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Document status explanation

Objective Specification	Document contains target values. Revised and supplementary data will be published later.
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This document applies to the following products:

Product name	Type number	ROM/FLASH version	PCN reference
LEA-M8F	LEA-M8F-0-00	FLASH FW2.20 FTS1.01	N/A

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1 Hardware description

1.1 Overview

The u-blox LEA-M8F module is a standalone GNSS time and frequency reference product featuring the high performance u-blox M8 positioning engine. The device provides multi-GNSS synchronization for cost-sensitive network edge equipment including Small Cell and Femto wireless base-stations. The LEA-M8F module is a fully self-contained phase and frequency reference based on GNSS, but can also be used as part of a complete timing sub-system including macro-sniff (network listen), Synchronous Ethernet and packet timing.

The LEA-M8F module includes a low-noise 30.72 MHz VCTCXO meeting the master reference requirements for LTE Small Cells and providing 100 ppb autonomous hold-over. An external TCXO or OCXO can also be measured and controlled for TD-LTE, LTE-Advanced and other applications requiring extended hold-over. External sources of synchronization are supported through time-pulse and frequency inputs and a message interface. This allows measurements from macro-sniff, Synchronous Ethernet or packet timing to be combined with measurements from GNSS.

The industry standard LEA form factor in the leadless chip carrier (LCC) package makes the LEA-M8F easy to integrate, while combining exceptional timing and frequency performance with highly flexible design and connectivity options. SMT pads allow fully automated assembly with standard pick & place and reflow-soldering equipment for cost-efficient, high-volume production enabling short time-to-market.



For product features see the *LEA-M8F Data Sheet* [1].



To determine which u-blox product best meets your needs, see the product selector tables on the u-blox website www.u-blox.com.

1.2 Architecture

Figure 1 shows a block schematic view of the module's internal organization.

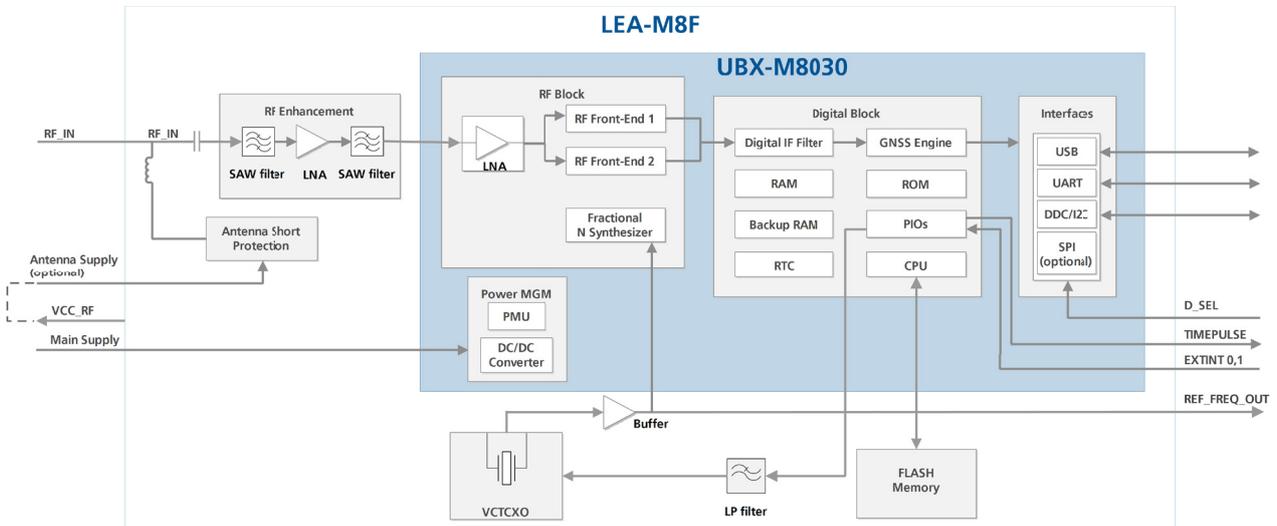


Figure 1: LEA-M8F Block Diagram

The device contains all the elements required to implement a multi-GNSS frequency and time synchronization system. It comprises a u-blox M8030 GNSS receiver, RF LNA/SAW filter and disciplined VCTCXO. A FLASH memory contains the FTS firmware and provides configuration storage.

1.3 Pin description for LEA-M8F designs

Function	PIN	No	I/O	Description	Remarks
Power	VCC	6	I	Supply Voltage	Provide a clean and stable supply.
	GND	7, 13-15, 17	I	Ground	Assure a low impedance GND connection to all GND pins of the module, preferably with a large ground.
	V_BCKP	11	I		connect to VCC . (Back-up mode not supported)
	VDDUSB	24	I	USB Power Supply	To use the USB interface connect this pin to 3.0 – 3.6 V derived from VBUS. If no USB serial port used connect to GND.
Antenna	RF_INPUT	16	I	GPS/GLONASS/BeiDou/signal input from antenna	Use a controlled impedance transmission line of 50 Ω to connect to RF_IN. Don't supply DC through this pin. Use V_ANT pin to supply power.
	VCC_RF	18	O	Output Voltage RF section	Can be used to power an external active antenna (Ω). The max power consumption of the Antenna must not exceed the datasheet specification of the module. Leave open if not used.
	V_ANT	19	I	Antenna Bias voltage	Connect to GND (or leave open) if Passive Antenna is used. If an active Antenna is used, add a 10 Ω resistor in front of V_ANT input to the Antenna Bias Voltage or VCC_RF
	Reserved	20	I		Leave open
UART	TxD1/MISO/TX ready	3	O	Serial Port 1 or SPI Data i/p	Communication interface o/p function dependent on D_SEL. It can also can be programmed as TX ready for DDC interface. Leave open if not used.
	RxD1/MOSI	4	I	Serial Port 1 or SPI Data o/p	Communication interface i/p dependent on D_SEL with internal pull-up resistor to VCC. Leave open if not used. Don't use external pull up resistor.
USB	USB_DM	25	I/O	USB I/O line	USB2.0 bidirectional communication pin. Leave open if unused. For example implementations see section 1.5.2
	USB_DP	26	I/O	USB I/O line	
System	RESET_N	10	I	Hardware Reset (Active Low)	Leave open if not used.
	TIMEPULSE/TP2/SAFEBOOT_N	28	I/O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
	FREQ_PHASE_IN0/EXTINT0	27	I	TimePulse/Frequency	General purpose frequency/phase measurement input 0, Alternate function: External Interrupt 0
	FREQ_PHASE_IN1/EXTINT1	21	I	TimePulse/Frequency	General purpose frequency/phase measurement input 1 Alternate function: External Interrupt 1
	REF_FREQ_OUT	9	I	VCTCXO o/p	Buffered output from the disciplined internal 30.72MHz VCTCXO
	SDA/CS_N	1	I/O	DDC Data Pin or SPI chip sel.	DDC Data. Leave open if not used. or SPI chip select: dependent on DSEL
	SCL/SCLK	2	I/O	DDC Clk Pin or SPI clk	DDC Clock. Leave open if not used. or SPI clock: dependent on DSEL
	SAFEBOOT_N	12	I		Test-point for service access. Leave open, do not drive low.
	D_SEL	5		Selects the interface protocol	Used to select UART+DDC or SPI Open = UART+DDC; low = SPI on pins 1,2,3,4
	SDA_DAC	22	I/O	DDC Data pin	For DAC control of external Freq Reference Only
SCL_DAC	23	O	DDC Clk pin	For DAC control of external Freq Reference Only	

Table 1: LEA-M8F Pinout

1.4 Connecting power

The u-blox LEA-M8F module has three power supply pins: **VCC**, **V_BCKP** and **VDD_USB**.

1.4.1 VCC

The **VCC** pin provides the main supply voltage. During operation, the current drawn by the module can vary by some orders of magnitude. For this reason, it is important that the supply circuitry be able to support the peak power for a short time. For specification see the *LEA-M8F Data Sheet* [1].



Use a proper GND concept with preferably low ESR decoupling capacitors at the module supply input. Do not use any resistors or coils in the power line.

1.4.2 V_BCKP

This pin must be connected to the main module supply VCC.

1.4.3 VCC_RF

The **VCC_RF** pin provides a filtered source of DC to power an active antenna or external LNA. For more information, see section 2.2.

1.5 Interfaces

The following interfaces are available for communication with a host for control and data handling.

1.5.1 UART

The LEA-M8F module includes a Universal Asynchronous Receiver Transmitter (UART) serial interface **RxD/TxD** supporting configurable baud rates. See the *LEA-M8F Data Sheet* [1] for the supported baud rates.

The signal input and output levels are 0 V to **VCC** with inverted logic. An interface based on RS232 standard levels (+/- 12 V) can be implemented using level shifters such as a Maxim MAX3232.



The interface does not support hardware handshake signals or synchronous operation.



Designs must allow access to the UART and the **SAFEBOOT_N** pin for future service, updates and reconfiguration.

1.5.2 USB

A USB 2.0 (Full Speed, 12 Mb/s) compatible interface is available for communication as a development option. The module is not designed to use the USB interface in an operational sense as the message latency cannot be guaranteed.

The **USB_DP** pin has a pull-up resistor to signal a full-speed device to the USB host. The **VDD_USB** pin requires connection to a 3 V (nom.) source to enable the USB interface. If the USB interface is not used, connect **VDD_USB** to GND.

u-blox provides Microsoft® certified USB drivers for Windows XP, Windows Vista, Windows 7 and Windows 8 operating systems. These drivers are available for down-load at our website: www.u-blox.com



The USB port is for non-operational use e.g. for evaluation or firmware down-load

1.5.2.1 USB external components

The USB interface requires some external components to comply with the USB 2.0 specification. These are shown below in Figure 2 and listed in Table 2. To comply with USB specifications, VBUS must be connected through an LDO (U1) to pin 24 (**VDD_USB**) to regulate the 5 V VBUS down to a nominal 3.3 V for the module.

The LEA-M8F module USB interface is intended to be used as a USB **self-powered** device deriving its power supply from **VCC**. However, the module power supply (**VCC**) can be turned off independently of the host VBUS supplying VDD_USB. With VDD_USB active, the USB host would receive a signal indicating that the device is present and ready to communicate. This should be avoided by disabling the LDO (U1) using the enable signal (EN) of the VCC-LDO enabled by e.g. **VCC**. Depending on the characteristics of the LDO (U1) it is recommended to add a pull-down resistor (R11) at its output to ensure **VDD_USB** is not floating if the LDO (U1) is disabled or the USB cable is disconnected i.e. VBUS is not supplied.

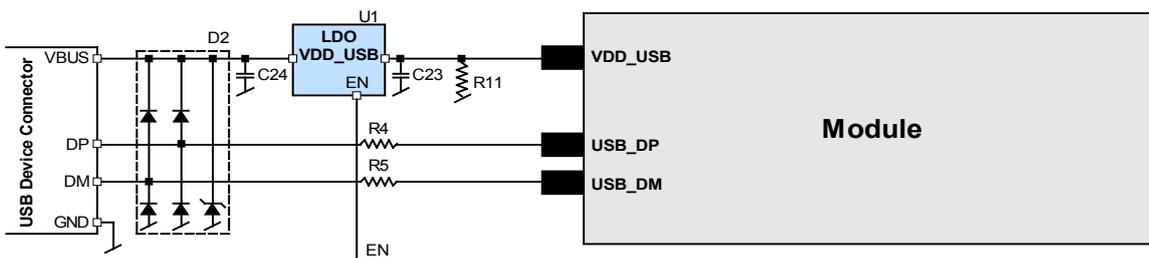


Figure 2: USB Interface

Name	Component	Function	Comments
U1	LDO	Regulates VBUS (4.4 ... 5.25 V) down to a voltage of 3.3 V.	Almost no current requirement (~1 mA) if the GNSS receiver is operated as a USB self-powered device.
C23, C24	Capacitors		Required according to the specification of LDO U1
D2	Protection diodes	Protect circuit from overvoltage / ESD when connecting.	Use low capacitance ESD protection such as ST Microelectronics USBLC6-2.
R4, R5	Serial termination resistors	Establish a full-speed driver impedance of 28...44 Ω	A value of 27 Ω is recommended.
R11	Resistor		100 kΩ is recommended for USB self-powered setup. For bus-powered setup, R11 can be ignored.

Table 2: Summary of USB external components

1.5.3 Display Data Channel (DDC)

An I²C compatible Display Data Channel (DDC) interface is available for serial communication with an external host CPU. The interface only supports slave mode operation (master mode is not supported). The DDC protocol and electrical interface are fully compatible with the Fast-Mode of the I²C industry standard. The DDC pins **SDA** and **SCL** have internal 10 kΩ pull-up resistors.

For more information about the DDC implementation, see the *u-blox M8 Receiver Description Including Protocol Specification* [2]. For bandwidth information, see the *LEA-M8F Data Sheet* [1]. For timing, parameters consult the *I²C-bus specification* [8].



The u-blox M8 DDC interface supports serial communication with u-blox cellular modules. See the specification of the applicable cellular module to confirm compatibility.

1.5.4 SPI

An SPI interface is available for communication to a host CPU, however its interface connections are shared with the UART and DDC interface pins. The SPI interface is not available in the default configuration but can be

enabled by connecting pin 5 (**D_SEL**) to ground - see 1.6.2 below. For speed and clock frequency specifications, see the *LEA-M8F Data Sheet* [1].

1.5.5 DDC interface for External DAC Control

A dedicated DDC (I2C) interface (pins **SDA_DAC**, **SCL_DAC**) is provided for implementations in which the LEA-M8F controls an external voltage controlled frequency reference via a DAC. This is set up via FTS specific configuration messages. See the *u-blox M8 Receiver Description Protocol Specification* [2] and the *u-blox M8F Applications Guide* [3] for more information. The DDC pins **SDA_DAC** and **SCL_DAC** have internal 10 k Ω pull-up resistors.

When the LEA-M8F is configured to discipline a voltage controlled oscillator via the dedicated DDC interface (**SDA_DAC**, **SCL_DAC**) a choice must be made with respect to the DAC component. The recommended types (TI or Microchip) offer 16 or 12 bit resolution respectively and should be chosen for the desired performance/cost requirements. This section shows a suggested circuitry for implementing a 16 bit TI DAC analog filter combination connected to a VCTCXO/VCOCXO. Note that 12 bit DAC may not provide sufficient resolution if used over the full circuit voltage range and hence may compromise the controlled frequency performance. Implementing a circuit using a smaller DAC voltage range and adding the output to a fixed low noise offset voltage would be beneficial.

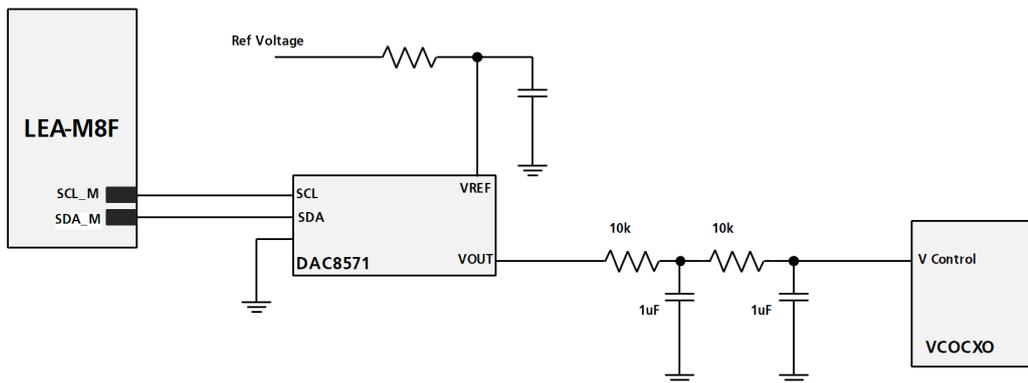


Figure 3: 16 bit DAC connection for VCOCXO control

1.6 I/O and Control Pins

1.6.1 RESET_N

RESET_N is an input-only pin with an internal pull-up resistor. The LEA-M8F performs an automatic reset function on application of the power supply but this input may also be used to re-start the device during operation if necessary. The pin must be held low for at least 10 ms to ensure **RESET_N** is detected. Leave **RESET_N** open for normal operation. The **RESET_N** input complies with the power supply VCC voltage level and can be actively driven high. Use this pin only to reset the module. Do not use **RESET_N** to turn the module on and off since the reset state increases power consumption.

1.6.2 D_SEL

The **D_SEL** pin selects the available communication interfaces available at the module pins. This allows a choice between UART+DDC or SPI control of the module, see Table 3 below. If **D_SEL** is left open both UART and DDC are available. If pulled low, a single SPI interface is available. See the *LEA-M8F Data Sheet* [1].

PIN	PIN 5 (D_SEL) = "high" (left open)	PIN 5 (D_SEL) = "Low" (connected to GND)
1	DDC SDA	SPI CS
2	DDC SCL	SPI CLK
3	UART TX	SPI MISO
4	UART RX	SPI MOSI

Table 3: D_SEL pin configuration

1.6.3 FREQ_PHASE_IN0 / EXINT0, FREQ_PHASE_IN1 / EXTINT1

These two frequency/phase inputs are provided for connecting an external source of phase (pulse stream) or frequency reference into the module. The pulse stream can be derived from a frequency reference or external synchronization source. The module will measure and report the phase or frequency offset of this input with respect to the current synchronization source and optionally steer the related oscillator to bring the externally derived pulses into alignment.

NB. These two pins have an alternate legacy function as external interrupts and are also called EXTINT0,EXTINT1 for compatibility with standard u-blox M8 functionality.

1.6.4 REF_FREQ_OUT

This pin carries a low phase noise buffered output from the module's disciplined 30.72MHz VCTCXO (CMOS buffer via on-module resistor).

1.6.5 TIMEPULSE / TP2

The timepulse signal is output from this pin. This pin is the standard u-blox M8 TP2 output, hence all timepulse settings must be made with respect to TP2 in UBX control messages.

The timepulse output pin also functions as the SAFEBOOT_N input pin at start up, initiating a special Safe Boot Mode operation from ROM if held LO during reset (for example for Flash firmware recovery). As a result, applications using the timepulse output should ensure that this pin is not held LO during start-up in normal operation. This can be achieved safely by re-buffering the timepulse output using the VDD_IO supply. This pin has an internal pull-up resistor of nominally 11 kΩ.

1.7 Device Configuration

The device configuration can be modified using UBX protocol configuration messages. Configuration settings for the FTS functionality are explored further in the accompanying Application Guide [3]. All modified settings remain effective until power-down or reset. The configuration can be saved permanently in SQI flash using the UBX-CFG-CFG message. For a full explanation of all configuration messages, refer to the *u-blox M8 Receiver Description Protocol Specification* [2].

2 Design

2.1 Layout: Footprint and paste mask

This section describes the footprint and provides recommendations for the paste mask for the u-blox M8F LCC module.

These are recommendations only and not specifications. Note that the copper and solder masks have the same size and position.

To improve the wetting of the half vias, reduce the amount of solder paste under the module and increase the volume outside of the module by defining the dimensions of the paste mask to form a T-shape (or equivalent) extending beyond the copper mask. For the stencil thickness, see section 4.2.



Consider the paste mask outline when defining the minimal distance to the next component. The exact geometry, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering) of the customer.

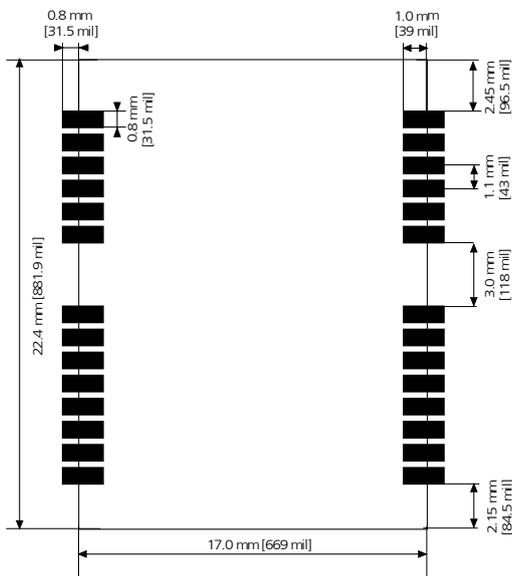


Figure 4: LEA-M8F footprint

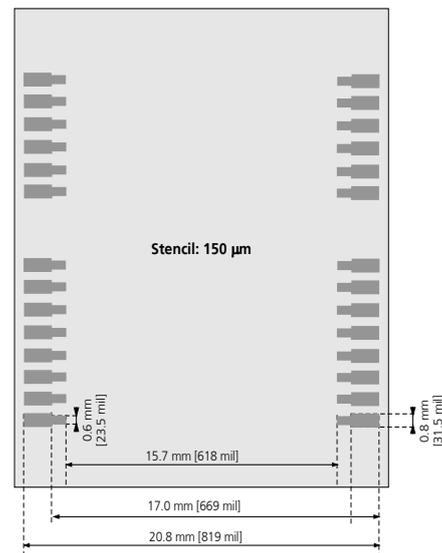


Figure 5: LEA-M8F paste mask

2.1.1 Placement

A very important factor in achieving maximum performance is the placement of the receiver on the PCB. The connection to the antenna must be as short as possible to avoid jamming into the very sensitive RF section.

Make sure that RF critical circuits are clearly separated from any other digital circuits on the system board. To achieve this, position the receiver digital part towards your digital section of the system PCB. Care must also be exercised with placing the receiver in proximity to circuitry that can emit heat. The RF part of the receiver is very sensitive to temperature and sudden changes can have an adverse impact on performance.



The RF part of the receiver is a temperature sensitive component. Avoid high temperature drift and air vents near the receiver.

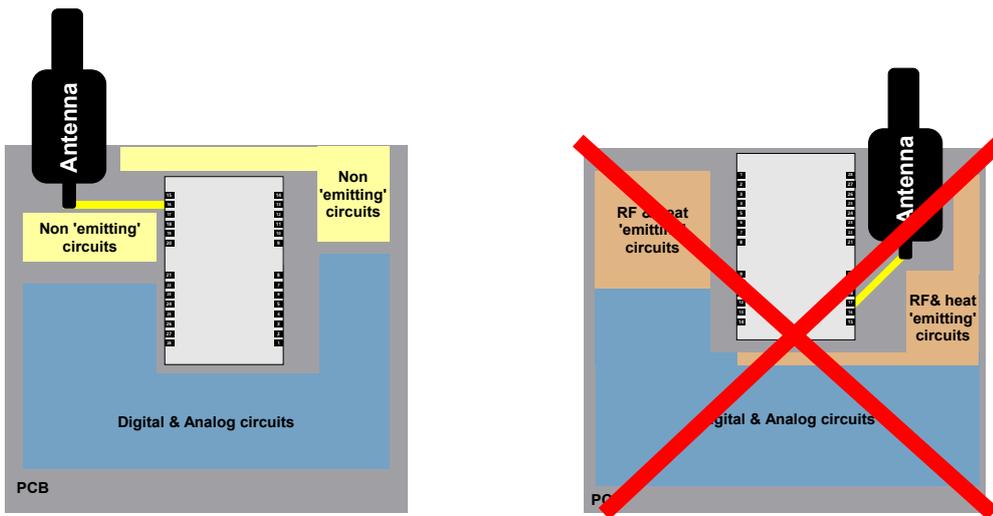


Figure 6: Placement (for exact pin orientation see *LEA-M8F Data Sheet [1]*)

2.1.2 Antenna connection and ground plane design

The LEA-M8F module can be connected to passive patch or active antennas. The RF connection is on the PCB and connects the **RF_IN** pin with the antenna feed point or the signal pin of the connector, respectively. Figure 7 illustrates connection to a typical five-pin RF connector. One can see the improved shielding for digital lines as discussed in the *GPS Antenna Application Note [5]*. Depending on the actual size of the ground area, additional vias should be placed in the outer region. In particular, the edges of the ground area should be terminated with a dense line of vias.

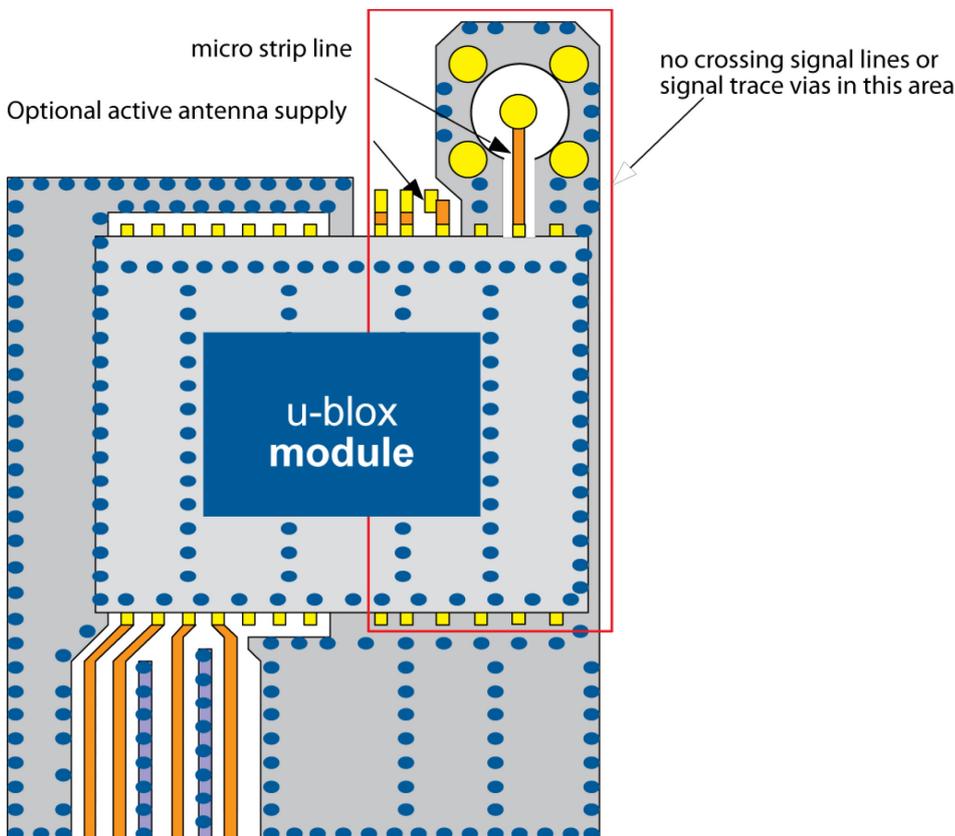


Figure 7: Recommended layout (for exact pin orientation see the *LEA-M8F data sheet [1]*)

As seen in Figure 7, an isolated ground area is created around and below the RF connection. This part of the circuit **MUST** be kept as far from potential noise sources as possible. Make certain that no signal lines cross, and that no signal trace vias appear at the PCB surface within the area of the red rectangle. The ground plane should also be free of digital supply return currents in this area. On a multi layer board, the whole layer stack below the RF connection should be kept free of digital lines. This is because even solid ground planes provide only limited isolation.

The impedance of the antenna connection has to match the $50\ \Omega$ impedance of the receiver. To achieve an impedance of $50\ \Omega$, the width W of the micro strip has to be chosen depending on the dielectric thickness H , the dielectric constant ϵ_r of the dielectric material of the PCB, and on the build-up of the PCB (see section 2.1.3). Figure 8 shows two different builds: A 2-layer PCB and a 4-layer PCB. The reference ground plane is on layer 2 in both designs. Therefore, the effective thickness of the dielectric is different.

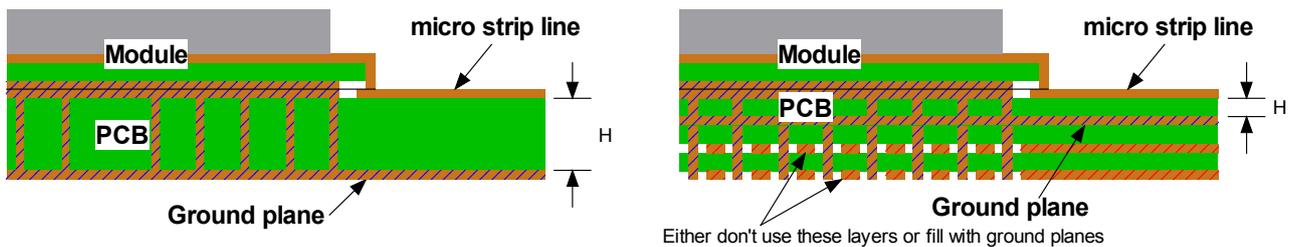


Figure 8: PCB build-up for micro strip line. Left: 2-layer PCB, right: 4-layer PCB

General design recommendations:

- The length of the micro strip line should be kept as short as possible. Lengths over 2.5 cm (1 inch) should be avoided on standard PCB material and without additional shielding.
- For multi-layer boards, the distance between micro strip line and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF connection close to digital sections of the design should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

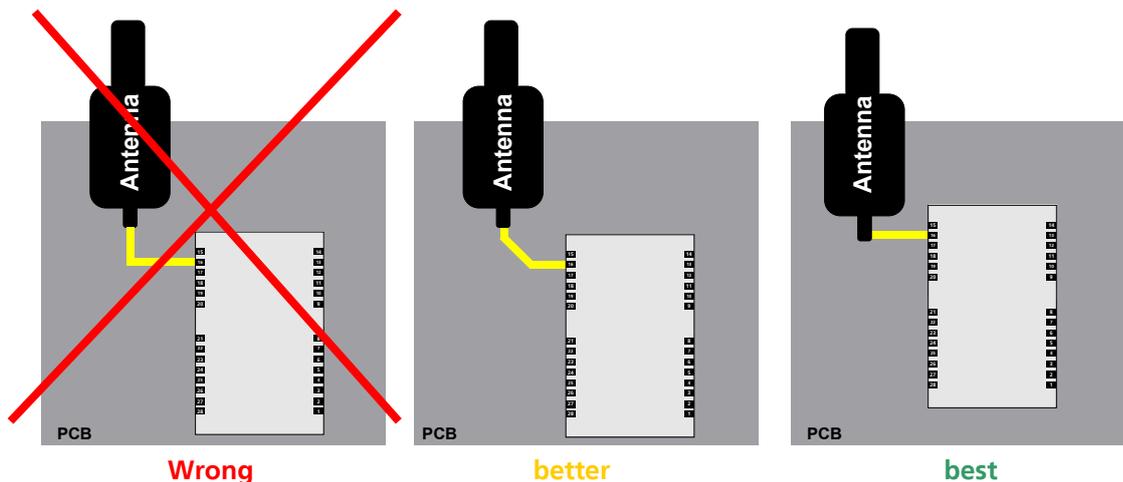


Figure 9: Recommended micro strip routing to RF pin (for exact pin orientation see *LEA-M8F Data Sheet* [1])

- Do not route the RF-connection underneath the receiver. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small (some $100\ \mu\text{m}$) and has huge tolerances (up to 100%). Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

- In order to avoid reliability hazards, the area on the PCB under the receiver should be entirely covered with solder mask. Vias should not be open. Do not route under the receiver.

2.1.3 Antenna micro strip connection

There are many ways to design wave-guides on printed circuit boards. Common to all is that calculation of the electrical parameters is not straightforward. Freeware tools like AppCAD from Avago Technologies or TXLine from Applied Wave Research, Inc. are of great help. They can be downloaded from <http://www.avagotech.com/pages/appcad> or <http://www.hp.woodshot.com/> and www.mwoffice.com.

The micro strip is the most common RF interconnect configuration for printed circuit boards. The basic configuration is shown in Figure 10 and Figure 11. As a rule of thumb, for an FR-4 material the width of the conductor is roughly double the thickness of the dielectric to achieve 50 Ω line impedance.

For the correct calculation of the micro strip impedance, not only must one consider the distance between the top and the first inner layer, but also the distance between the micro strip and the adjacent GND plane on the same layer.



Use the Coplanar Waveguide model for the calculation of the micro strip dimensions.

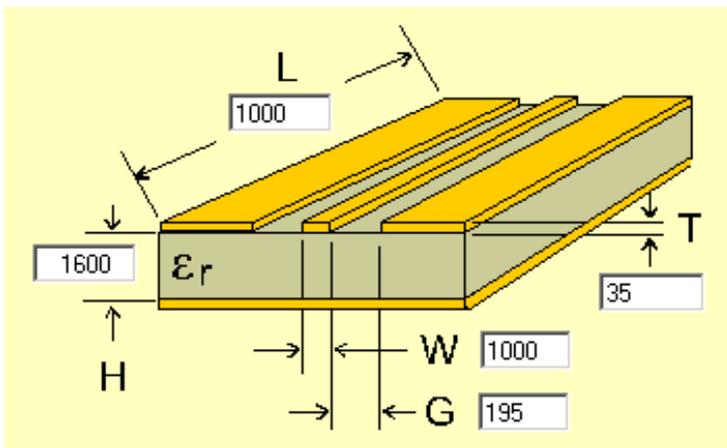


Figure 10: Micro strip on a 2-layer board (Agilent AppCAD Coplanar Waveguide)

Figure 10 shows an example of a 2-layer FR4 board with 1.6 mm thickness and a 35 μm (1 ounce) copper cladding. The thickness of the micro strip is comprised of the cladding (35 μm) plus the plated copper (typically 25 μm). Figure 11 is an example of a multi layer FR4 board with 18 μm ($\frac{1}{2}$ ounce) cladding and 180 μ dielectric between layer 1 and 2.

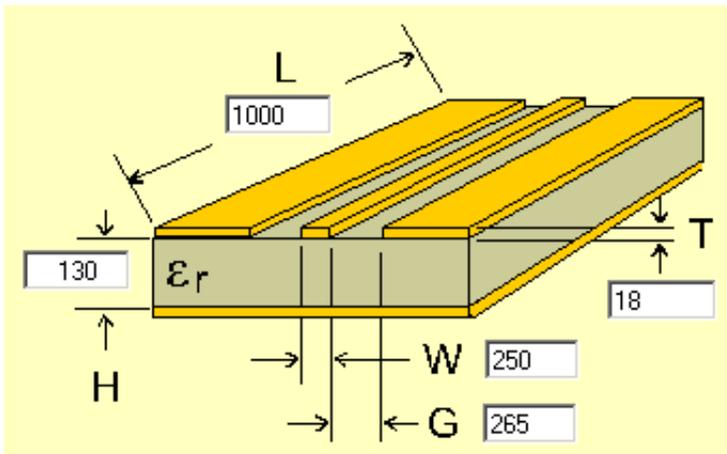


Figure 11: Micro strip on a multi layer board (Agilent AppCAD Coplanar Waveguide)

2.2 GNSS Antenna Connection

2.2.1 Passive Antenna Connection

A design using a passive antenna requires more attention to the layout of the RF section. Typically, a passive antenna is located near electronic components; therefore take care to reduce electrical noise that may interfere with the antenna performance. Passive antennas do not require a DC bias voltage and can be directly connected to the RF input pin, **RF_IN**. Sometimes, they may also need a passive matching network to match the impedance to 50 Ω .

Figure 12 shows a minimal setup for a design with a good GNSS patch antenna.

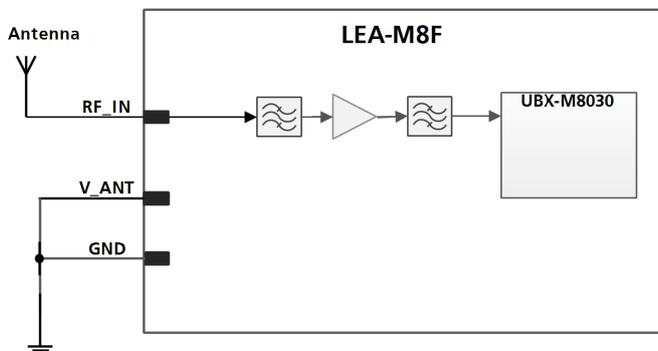


Figure 12: Module design with passive antenna (for exact pin orientation see the *LEA-M8F Data Sheet*[1])



Use an antenna that has sufficient bandwidth to receive all GNSS constellations. See the recommended types in the Appendix.

2.2.2 Active antenna connection

Active antennas have an integrated low-noise amplifier. Typically, they require an additional 5 to 20 mA that will contribute to the total GNSS system power consumption.

If the supply voltage of the u-blox M8 receiver matches the supply voltage range of the antenna (e.g. 3.0 V), use the filtered supply voltage at **VCC_RF** to supply the antenna DC power. The **V_ANT** pin provides a current limited supply connection to the **RF_IN** pin for antenna LNA biasing, see Figure 13 below.

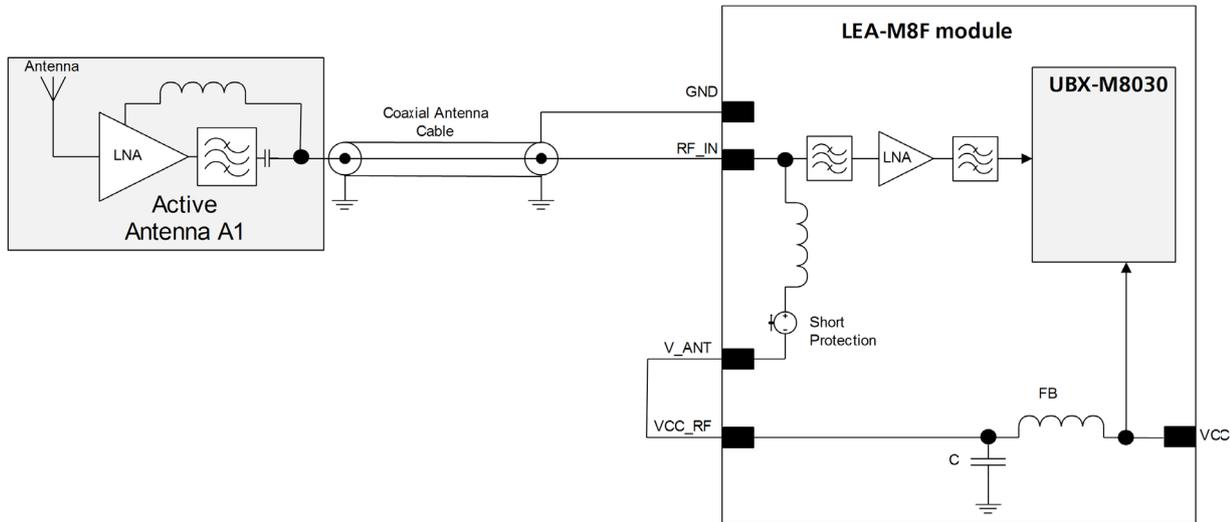


Figure 13: Active antenna design, external supply from VCC_RF (for exact pin orientation see LEA-M8F Data Sheet [1])

For powering an active antenna with an alternative voltage to the module VCC, use an external supply as shown in Figure 14.

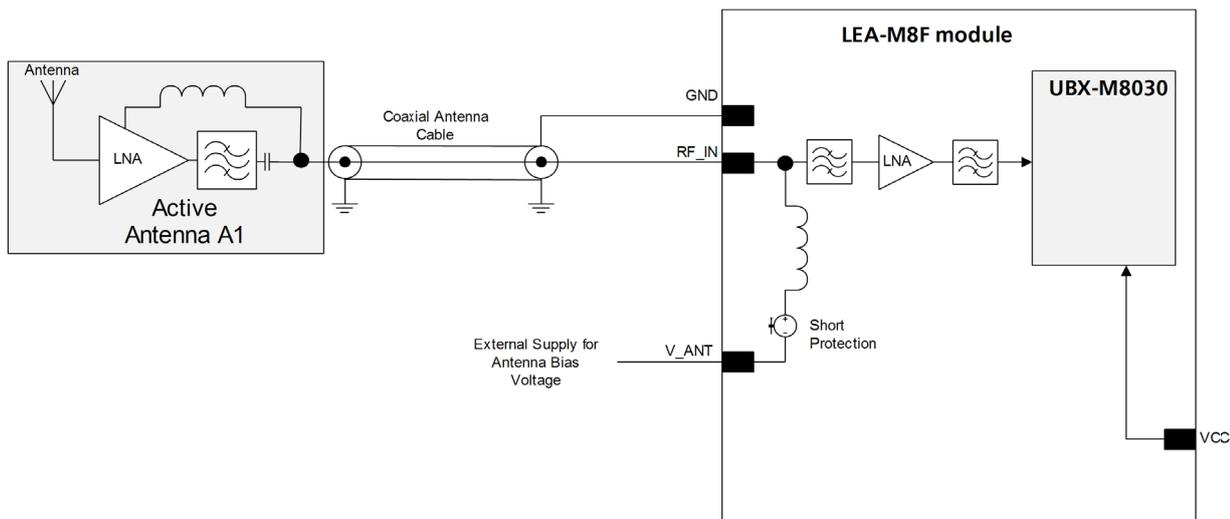


Figure 14: Active antenna design, direct external supply (for exact pin orientation see the LEA-M8F Data Sheet [1])



When the **VCC_RF** voltage does not match with the antenna supply voltage, use a filtered external supply as shown in Figure 14.

3 Migration to u-blox M8 modules

u-blox is committed to ensuring that products in the same form factor are backwards compatible over several technology generations. Utmost care has been taken to minimize impact on function and performance and to make u-blox M8 modules as compatible as possible with earlier modules.

Make sure that the RF path (antenna and filtering parameters) matches that of the GNSS constellations used.

To use BeiDou, review the bandwidth of the external RF components and the antenna. For information about power consumption, see the *LEA-M8F Data Sheet* [1].

It is highly advisable that customers consider a design review with the u-blox support team to ensure the compatibility of key functionalities.

3.1 Software migration



For an overall description of the module software operation, see the *u-blox M8 Receiver Description including Protocol Specification* [2]



For software migration details, see the *u-blox 7 to u-blox M8 Software Migration Guide* [4].

3.2 Hardware migration LEA-6T -> LEA-M8F

This section compares the functionality when a design is migrated from a LEA-6T to a LEA-M8F. Most pins are compatible however, the following items have changed:-

- A single timepulse (TP2) output
- USB interface not recommended for operational use
- No back-up battery operation supported
- Interface option serial/SPI selectable by D_SEL line
- No antenna supervisor(status) function
- Timepulse 2 replaced with output frequency signal REF_FREQ_OUT

The Timepulse output from LEA-M8F must be allowed to float during start-up and reset (see section 1.6.5)

Table 4 outlines the difference in pin connections between the two modules.

Pin No.	LEA-6T		LEA-M8F		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	SDA2	DDC Pins	SDA2/CS_N	DDC data or SPI chip select	Depends on D_SEL (pin 5) status
2	SCL2	DDC Pins	SCL2/SCLK	DDC clock or SPI clock	Depends on D_SEL (pin 5) status
3	TxD1	Serial Port 1	TxD1/MISO	UART TX or SPI MISO	Depends on D_SEL (pin 5) status
4	RxD1	Serial Port 1	RxD1/MOSI	UART RX or SPI MOSI	Depends on D_SEL (pin 5) status
5	NC	Leave open	DSEL	Interface type selection	Used to select UART+DDC or SPI only Open = UART+DDC; GND = SPI on pins 1,2,3,4
6	VCC	Supply Voltage	VCC	Supply Voltage	No difference
7	GND	Ground	GND	Ground	No difference
8	VCC_OUT	Leave open if not used.	VCC_OUT	Leave open if not used.	No difference
9	Timepulse	TimePulse2 o/p	REF_FREQ_OUT	VCTCXO o/p	Module VCTCXO signal o/p
10	RESET_N	Hardware Reset (Active Low)	RESET_N	Hardware Reset (Active Low)	
11	V_BCKP	Backup voltage supply	V_BCKP	Backup voltage supply	Back-up operation not supported - Connect to Vcc
12	SAFEBOOT_N	GND	Reserved	Leave Open	Test-point for service access
13	GND	GND	GND	GND	No difference
14	GND	GND	GND	GND	No difference
15	GND	GND	GND	GND	No difference
16	RF_IN	RF input	RF_IN	RF input	No difference
17	GND	GND	GND	GND	No Difference
18	VCC_RF	O/P Voltage for RF section	VCC_RF	O/P Voltage for RF section	No difference
19	V_ANT	Ant. Bias V	V_ANT	Ant. Bias V	No difference
20	AADET_N	Active Antenna Detect	Reserved	Leave Unconnected	No Antenna Supervision
21	NC	No Connection	FREQ_PHASE_IN1/ EXTINT1	2nd Freq/ PPS input	
22	NC	No Connection	SDA_DAC	DDC pin for Ext DAC o/p	
23	NC	No Connection	SCL_DAC	DDC pin for Ext DAC o/p	
24	VDD USB	USB Voltage Source	VDD USB	USB Voltage Source	Not supported for operational use
25	USB_DM	USB I/O Line -	USB I/O Line	USB I/O Line -	Not supported for operational use
26	USB_DP	USB I/O Line +	USB I/O Line	USB I/O Line +	Not supported for operational use
27	EXTINT0	Ext. Interrupt	FREQ_PHASE_IN0/ EXTINT0	1 st Freq/ PPS input	
28	Timepulse	Timepulse signal	Timepulse/TP2/ SAFEBOOT_N	Timepulse signal SAFEBOOT_N	Timepulse is TP2 Must float during reset (see 1.6.5)

Table 4: Pin-out comparison LEA-6T vs. LEA-M8F

4 Product handling

4.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to reels and tapes, Moisture Sensitivity levels (MSL), shipment and storage information, as well as drying for preconditioning see the *LEA-M8F Data Sheet* [1].

Population of Modules



When populating the modules, make sure that the pick and place machine is aligned to the copper pins of the module and not on the module edge.

4.2 Soldering

Soldering paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	Sn 95.5/ Ag 4/ Cu 0.5 (95.5% Tin/ 4% Silver/ 0.5% Copper)
Melting Temperature:	217 °C
Stencil Thickness:	See section 2.1

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations.



The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

Reflow soldering

A convection type-soldering oven is highly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature, and all parts will heat up evenly, regardless of material properties, thickness of components and surface color.

As a reference, see the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes", published in 2001.

Preheat phase

During the initial heating of component leads and balls, residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max. 3 °C/s. If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 - 120 s. If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 - 200 °C. If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ Reflow phase

The temperature rises above the liquidus temperature of 217°C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 217 °C liquidus temperature: 40 - 60 s
- Peak reflow temperature: 245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s



To avoid falling off, the u-blox M8 GNSS module should be placed on the topside of the motherboard during soldering.

The final soldering temperature chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

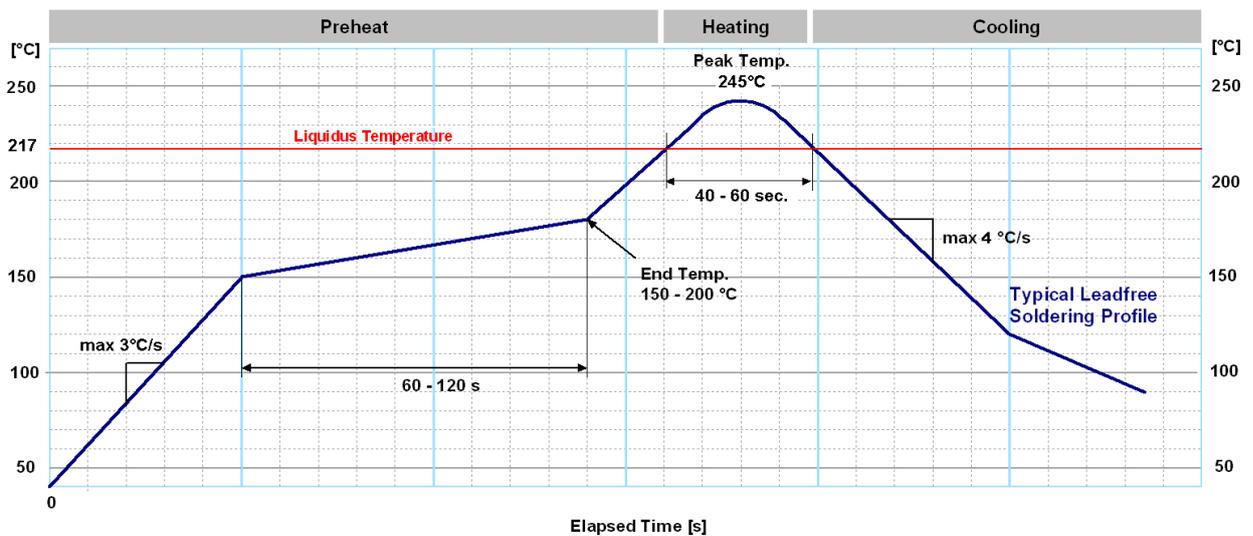


Figure 15: Recommended soldering profile



u-blox M8 modules **must not** be soldered with a damp heat process.

Optical inspection

After soldering the u-blox M8 module, consider an optical inspection step to check whether:

- The module is properly aligned and centered over the pads
- All pads are properly soldered
- No excess solder has created contacts to neighboring pads, or possibly to pad stacks and vias nearby

Cleaning

In general, cleaning the populated modules is strongly discouraged. Residues underneath the modules cannot easily be removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

The best approach is to use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

Repeated reflow soldering

Only single reflow soldering processes are recommended for boards populated with u-blox M8 modules. u-blox M8 modules should not be submitted to two reflow cycles on a board populated with components on both sides in order to avoid upside down orientation during the second reflow cycle. In this case, the module should always be placed on that side of the board, which is submitted into the last reflow cycle. The reason for this (besides others) is the risk of the module falling off due to the significantly higher weight in relation to other components.

Two reflow cycles can be considered by excluding the above described upside down scenario and taking into account the rework conditions described in Section Product handling.



Repeated reflow soldering processes and soldering the module upside down are not recommended.

Wave soldering

Base boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with u-blox M8 modules.

Hand soldering

Hand soldering is allowed. Use a soldering iron temperature setting equivalent to 350 °C and carry out the hand soldering according to the IPC recommendations / reference documents IPC7711. Place the module precisely on the pads. Start with a cross-diagonal fixture soldering (e.g. pins 1 and 15), and then continue from left to right.

Rework

The u-blox M8 module can be unsoldered from the baseboard using a hot air gun. When using a hot air gun for unsoldering the module, a maximum of one reflow cycle is allowed. In general, we do not recommend using a hot air gun because this is an uncontrolled process and might damage the module.

 **Attention: use of a hot air gun can lead to overheating and severely damage the module. Always avoid overheating the module.**

After the module is removed, clean the pads before placing and hand soldering a new module.

 **Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.**

In addition to the two reflow cycles, manual rework on particular pins by using a soldering iron is allowed. For hand soldering the recommendations in IPC 7711 should be followed. Manual rework steps on the module can be done several times.

Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products. These materials affect the HF properties of the GNSS module and it is important to prevent them from flowing into the module. The RF shields do not provide 100% protection for the module from coating liquids with low viscosity; therefore, care is required in applying the coating.



Conformal Coating of the module will void the warranty.

Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the u-blox M8 module before implementing this in the production.



Casting will void the warranty.

Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.



u-blox makes no warranty for damages to the u-blox M8 module caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

Use of ultrasonic processes

Some components on the u-blox M8 module are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the GNSS Receiver.



u-blox offers no warranty against damages to the u-blox M8 module caused by any Ultrasonic Processes.

4.3 EOS/ESD/EMI precautions

When integrating GNSS positioning modules into wireless systems, careful consideration must be given to electromagnetic and voltage susceptibility issues. Wireless systems include components that can produce Electrical Overstress (EOS) and Electro-Magnetic Interference (EMI). CMOS devices are more sensitive to such influences because their failure mechanism is defined by the applied voltage, whereas bipolar semiconductors are more susceptible to thermal overstress. The following design guidelines are provided to help in designing robust yet cost effective solutions.



To avoid overstress damage during production or in the field it is essential to observe strict EOS/ESD/EMI handling and protection measures.



To prevent overstress damage at the RF_IN of your receiver, never exceed the maximum input power (see *LEA-M8F Data Sheet 0*).

Electrostatic discharge (ESD)

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.



ESD handling precautions

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

GNSS positioning modules are sensitive to ESD and require special precautions when handling. Particular care must be exercised when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver.

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device



- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10 pF, coax cable ~50 - 80 pF/m, soldering iron, ...)
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the receiver's RF pin, make sure to use an ESD safe soldering iron (tip).



Failure to observe these precautions can result in severe damage to the GNSS module!

ESD protection measures



GNSS positioning modules are sensitive to Electrostatic Discharge (ESD). Special precautions are required when handling.



For more robust designs, employ additional ESD protection measures. Using an LNA with appropriate ESD rating can provide enhanced GNSS performance with passive antennas and increases ESD protection.

Most defects caused by ESD can be prevented by following strict ESD protection rules for production and handling. When implementing passive antenna patches or external antenna connection points, then additional ESD measures can also avoid failures in the field as shown in Figure 16.

Small passive antennas (<2 dBic and performance critical)	Passive antennas (>2 dBic or performance sufficient)	Active antennas
LNA with appropriate ESD rating		

Figure 16: ESD Precautions



Protection measure A is preferred because it offers the best GNSS performance and best level of ESD protection.

Electrical Overstress (EOS)

Electrical Overstress (EOS) usually describes situations when the maximum input power exceeds the maximum specified ratings. EOS failure can happen if RF emitters are close to a GNSS receiver or its antenna. EOS causes damage to the chip structures. If the RF_IN is damaged by EOS, it is hard to determine whether the chip structures have been damaged by ESD or EOS.

EOS protection measures



For designs with GNSS positioning modules and wireless (e.g. GSM/GPRS) transceivers in close proximity, ensure sufficient isolation between the wireless and GNSS antennas. If wireless power output causes the specified maximum power input at the GNSS RF_IN to be exceeded, employ EOS protection measures to prevent overstress damage.

For robustness, EOS protection measures as shown in Figure 17 are recommended for designs combining wireless communication transceivers (e.g. GSM, GPRS) and GNSS in the same design or in close proximity.

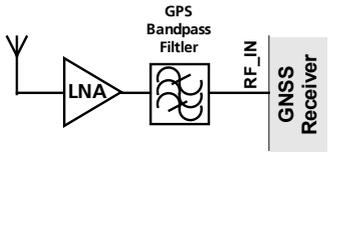
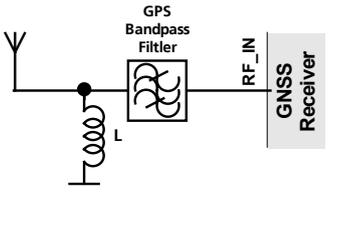
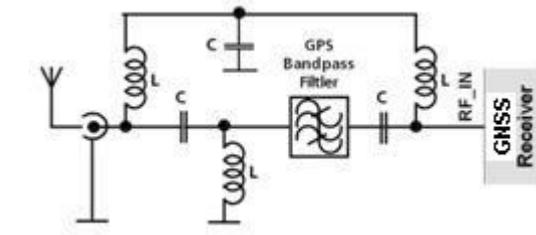
Small passive antennas (<2 dBic and performance critical)	Passive antennas (>2 dBic or performance sufficient)	Active antennas (without internal filter which need the module antenna supervisor circuits)
<p>D</p> 	<p>E</p> 	<p>F</p> 
LNA with appropriate ESD rating and maximum input power	GNSS Band pass Filter: SAW or Ceramic with low insertion loss and appropriate ESD rating	

Figure 17: EOS and ESD Precautions

Electromagnetic interference (EMI)

Electromagnetic interference (EMI) is the addition or coupling of energy originating from any RF emitting device. This can cause a spontaneous reset of the GNSS receiver or result in unstable performance. Any unshielded line or segment (>3mm) connected to the GNSS receiver can effectively act as antenna and lead to EMI disturbances or damage.

The following elements are critical regarding EMI:

- Unshielded connectors (e.g. pin rows etc.)
- Weakly shielded lines on PCB (e.g. on top or bottom layer and especially at the border of a PCB)
- Weak GND concept (e.g. small and/or long ground line connections)

EMI protection measures are recommended when RF emitting devices are near the GNSS receiver. To minimize the effect of EMI a robust grounding concept is essential. To achieve electromagnetic robustness follow the standard EMI suppression techniques.

<http://www.murata.com/products/emc/knowhow/index.html>

<http://www.murata.com/products/emc/knowhow/pdf/4to5e.pdf>

Improved EMI protection can be achieved by inserting a resistor (e.g. $R > 20 \Omega$) or better yet a ferrite bead (BLM15HD102SN1) or an inductor (LQG15HS47NJ02) into any unshielded PCB lines connected to the GNSS receiver. Place the resistor as close as possible to the GNSS receiver pin.

Example of EMI protection measures on the RX/TX line using a ferrite bead:

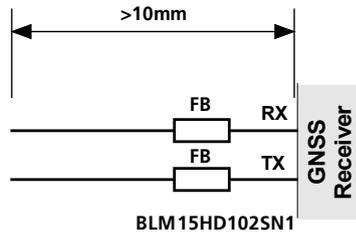


Figure 18: EMI Precautions

VCC can be protected using a feed thru capacitor. For electromagnetic compatibility (EMC) of the RF_IN pin, refer to section Soldering.

4.4 Applications with cellular modules

GSM uses power levels up to 2 W (+33 dBm). Consult the Data Sheet for the absolute maximum power input at the GNSS receiver.



See the *GPS Implementation and Aiding Features in u-blox wireless modules* [9].

Isolation between GNSS and GSM antenna

In a handheld type design, an isolation of approximately 20 dB can be reached with careful placement of the antennas. If such isolation cannot be achieved, e.g. in the case of an integrated GSM/GNSS antenna, an additional input filter is needed on the GNSS side to block the high energy emitted by the GSM transmitter. Examples of these kinds of filters would be the SAW Filters from Epcos (B9444 or B7839) or Murata.

Increasing jamming immunity

Jamming signals come from in-band and out-band frequency sources.

In-band jamming

With in-band jamming, the signal frequency is very close to the GNSS constellation frequency used, e.g. GPS frequency of 1575 MHz (see Figure 19). Such jamming signals are typically caused by harmonics from displays, micro-controller, bus systems, etc.

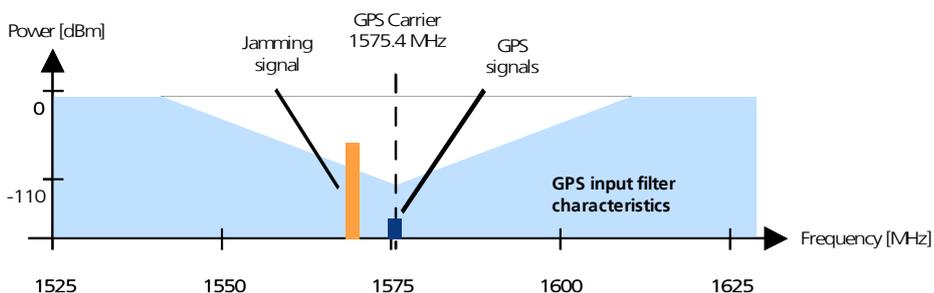


Figure 19: In-band jamming signals

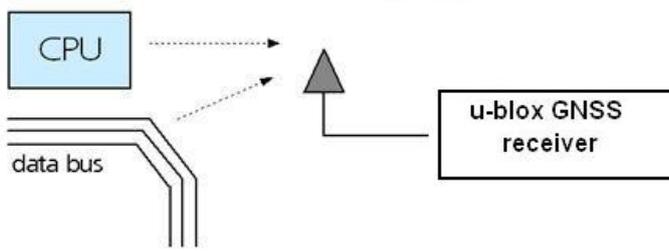


Figure 20: In-band jamming sources

Measures against in-band jamming include:

- Maintaining a good grounding concept in the design
- Shielding
- Layout optimization
- Filtering
- Placement of the GNSS antenna
- Adding a CDMA, GSM, WCDMA band pass filter before handset antenna

Out-band jamming

Out-band jamming is caused by signal frequencies that are different from the GNSS carrier (see Figure 21). The main sources are wireless communication systems such as GSM, CDMA, WCDMA, Wi-Fi, BT, etc.

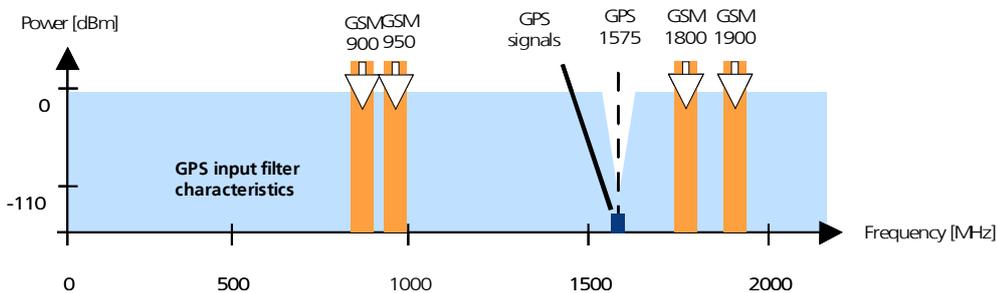


Figure 21: Out-band jamming signals

Measures against out-band jamming include maintaining a good grounding concept in the design and adding a SAW or band pass ceramic filter (as recommend in Section 4) into the antenna input line to the GNSS receiver (see Figure 22).



Figure 22: Measures against in-band jamming

Appendix

Recommended parts

Recommended parts are selected on a data sheet basis only. Other components may also be used.

	Manufacturer	Part ID	Remarks	Parameters to consider
Diode Semiconductor	ON	ESD9R3.3ST5G	Standoff Voltage>3.3 V	Low Capacitance < 0.5 pF
		ESD9L3.3ST5G	Standoff Voltage>3.3 V	Standoff Voltage > Voltage for active antenna
		ESD9L5.0ST5G	Standoff Voltage>5 V	Low Inductance
SAW	TDK/ EPCOS	B8401: B39162-B8401-P810	GPS+GLONASS	High attenuation
	TDK/ EPCOS	B3913: B39162B3913U410	GPS+GLONASS+BeiDou	For automotive application
	TDK/ EPCOS	B4310: B39162B4310P810	GPS+GLONASS	Compliant to the AEC-Q200 standard
	ReyConns	NDF9169	GPS+GLONASS	Low insertion loss, Only for mobile application
	muRata	SAFFB1G56KB0F0A	GPS+GLONASS+BeiDou	Low insertion loss, Only for mobile application
	muRata	SAFEA1G58KB0F00	GPS+GLONASS	Low insertion loss, only for mobile application
	muRata	SAFEA1G58KA0F00	GPS+GLONASS	High attenuation, only for mobile application
	muRata	SAFFB1G58KA0F0A	GPS+GLONASS	High attenuation, only for mobile application
	muRata	SAFFB1G58KB0F0A	GPS+GLONASS	Low insertion loss, Only for mobile application
	TAI-SAW	TA1573A	GPS+GLONASS	Low insertion loss
	TAI-SAW	TA1343A	GPS+GLONASS+BeiDou	Low insertion loss
TAI-SAW	TA0638A	GPS+GLONASS+BeiDou	Low insertion loss	
LNA	JRC	NJG1143UA2	LNA	Low noise figure, up to 15 dBm RF input power
DAC	TI	DAC8571	Osc. Control Voltage	No of bits (16)
	MicroChip	MCP4726	Osc. Control Voltage	No of bits (12)
Inductor	Murata	LQG15HS27NJ02	L, 27 nH	Impedance @ freq GPS > 500 Ω
Capacitor	Murata	GRM1555C1E470JZ01	C, 47 pF	DC-block
Ferrite Bead	Murata	BLM15HD102SN1	FB	High IZI @ fGSM
Feed thru Capacitor for Signal	Murata	NFL18SP157X1A3	Monolithic Type Array Type	Load Capacitance appropriate to signal rate
		NFA18SL307V1A45		
Feed thru Capacitor	Murata	NFM18PC	0603 2A	Rs < 0.5 Ω
		NFM21P....	0805 4A	
Resistor		10 Ω ± 10%, min 0.250 W	R _{bias}	
		560 Ω ± 5%	R2	
		100 kΩ ± 5%	R3, R4	

Table 5: Recommended parts

Recommended Antennas

Manufacturer	Order No.	Comments
Hirschmann (www.hirschmann-car.com)	GLONASS 9 M	GPS+GLONASS active
Taoglas (www.taoglas.com)	AA.160.301111	36*36*4 mm, 3-5 V 30 mA active
Taoglas (www.taoglas.com)	AA.161.301111	36*36*3 mm, 1.8 to 5.5 V / 10 mA at 3 V active
INPAQ (www.inpaq.com.tw)	B3G02G-S3-01-A	2.7 to 3.9 V / 10 mA active
Amotech (www.amotech.co.kr)	B35-3556920-2J2	35x35x3 mm GPS+GLONASS passive
Amotech (www.amotech.co.kr)	A25-4102920-2J3	25x25x4 mm GPS+GLONASS passive
Amotech (www.amotech.co.kr)	A18-4135920-AMT04	18x18x4 mm GPS+GLONASS passive
INPAQ (www.inpaq.com.tw)	ACM4-5036-A1-CC-S	5.2 x 3.7 x 0.7 mm GPS+GLONASS passive

Additional antenna Manufacturer: Allis Communications, 2J, Tallysman Wireless

Table 6: Recommend antenna

Related documents

- [1] LEA-M8F Data Sheet, Doc. No. UBX-14001772
- [2] u-blox M8 Receiver Description Protocol Specification, Doc. No. UBX-14002171
- [3] ublox M8F Applications Guide, Doc No. UBX-14001603
- [4] u-blox 7 to u-blox M8 Software Migration Guide, Doc. No. UBX-13003254
- [5] GPS Antenna Application Note, Docu. No. GPS-X-08014
- [6] UBX-M8030 Data Sheet, Docu. No. UBX-13001634
- [7] GPS Compendium, Docu. No. GPS-X-02007
- [8] I²C-bus specification, Version 2.1, Jan 2000,
http://www.nxp.com/acrobat_download/literature/9398/39340011_21.pdf
- [9] GPS Implementation and Aiding Features in u-blox wireless modules, Docu. No. GSM.G1-CS-09007



For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (<http://www.u-blox.com>)

Revision history

Revision	Date	Name	Status / Comments
R01	20-Mar-2014	byou	Objective Specification
R02	05-Jun-2014	smos	Advance Information; Renamed <code>FREQ_PHASE_IN</code> pins from 1, 2 to 0, 1 to match <code>EXTINT</code> pins.
R03	19-Aug-2014	amil	Early Production Information. Updated Pin12 and Pin28 information in Table 1 and section 3.2; added design recommendation in section 1.5.1; updated section 1.6.5 (<code>SAFEBOOT_N</code> pin);

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