

74ALVC08

Quad 2-input AND gate

Rev. 4 — 30 April 2021

Product data sheet

1. General description

The 74ALVC08 is a quad 2-input AND gate. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall times.

2. Features and benefits

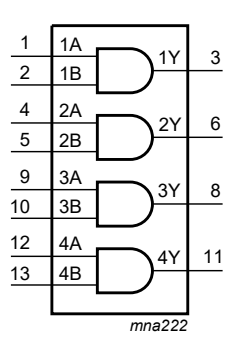
- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B (2.7 V to 3.6 V)
- ESD protection:
 - MM JESD22-A115-A exceeds 200 V
 - HBM JESD22-A114E exceeds 2000 V
- Multiple package options
- Specified from -40 °C to +85 °C

3. Ordering information

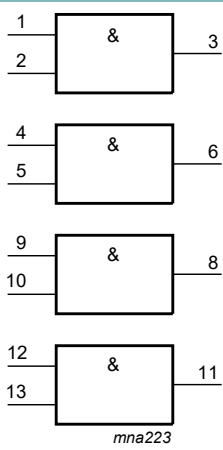
Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVC08D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ALVC08PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ALVC08BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

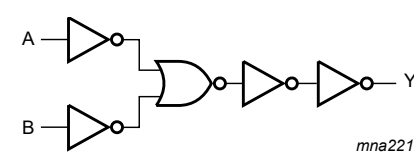
4. Functional diagram



mna222



mna223



mna221

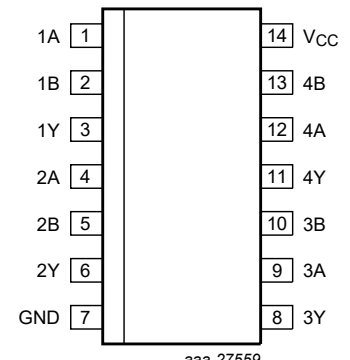
Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

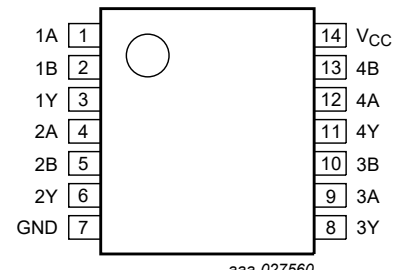
Fig. 3. Logic diagram (one gate)

5. Pinning information

5.1. Pinning



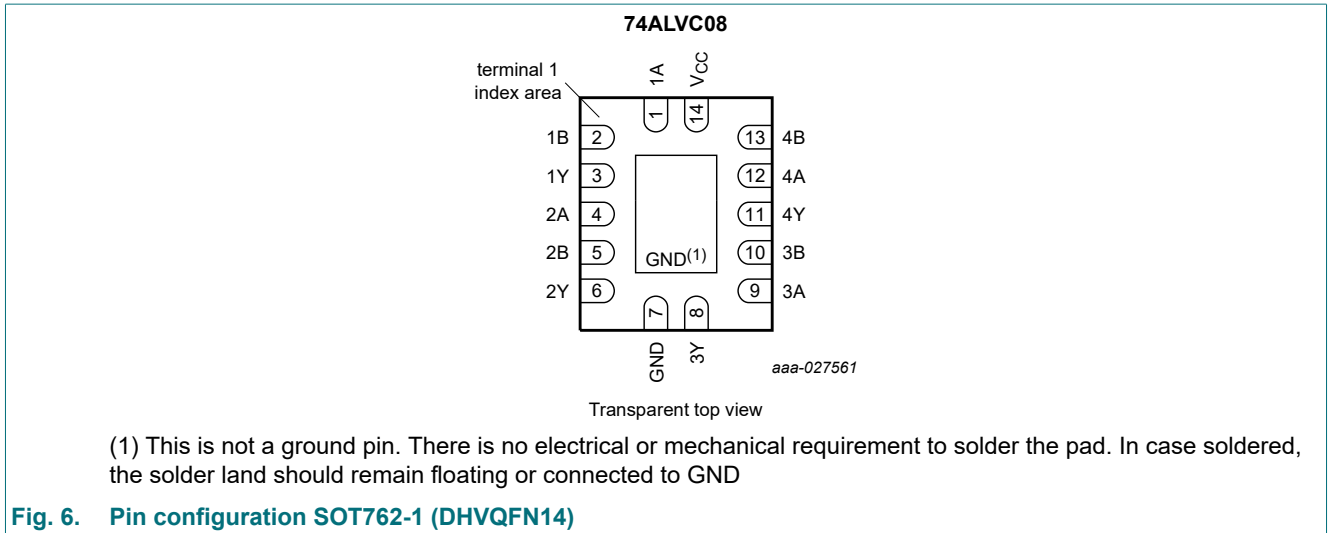
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Fig. 4. Pin configuration SOT108-1 (SO14)

Fig. 5. Pin configuration SOT402-1 (TSSOP14)



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input		Output
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage		[1] -0.5	+4.6	V
V_O	output voltage	none	[1] -0.5	$V_{CC} + 0.5$	V
		power-down mode; $V_{CC} = 0$ V	-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-	-50	mA
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	$V_{CC} = 1.65$ to 3.6 V	0	V_{CC}	V
		power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V
		I _O = -6 mA; V _{CC} = 1.65 V	1.25	1.51	-	V
		I _O = -12 mA; V _{CC} = 2.3 V	1.8	2.10	-	V
		I _O = -18 mA; V _{CC} = 2.3 V	1.7	2.01	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	2.53	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	2.76	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	V
		I _O = 6 mA; V _{CC} = 1.65 V	-	0.11	0.3	V
		I _O = 12 mA; V _{CC} = 2.3 V	-	0.17	0.4	V
		I _O = 18 mA; V _{CC} = 2.3 V	-	0.25	0.6	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	0.16	0.4	V
		I _O = 18 mA; V _{CC} = 3.0 V	-	0.23	0.4	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 3.6 V or GND	-	±0.1	±5	μA
		V _{CC} = 0 V; V _I or V _O = 3.6 V	-	±0.1	±10	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.2	20	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	750	μA
C _I	input capacitance		-	3.5	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 8.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t _{pd}	propagation delay	nA, nB to nY; see Fig. 7 [2]				
		V _{CC} = 1.65 V to 1.95 V	1.2	2.7	5.3	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	1.9	3.2	ns
		V _{CC} = 2.7 V	-	2.2	3.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	2.0	2.9	ns
C _{PD}	power dissipation capacitance	per gate; V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3]	-	24	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

Σ(C_L × V_{CC}² × f_o) = sum of the outputs

10.1. Waveforms and test circuit

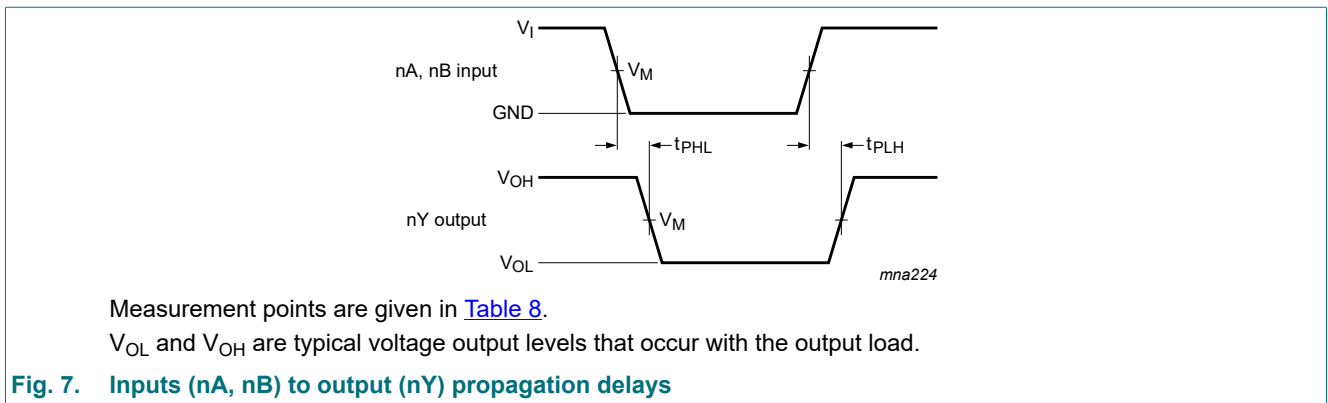
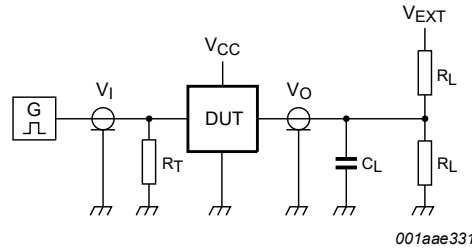
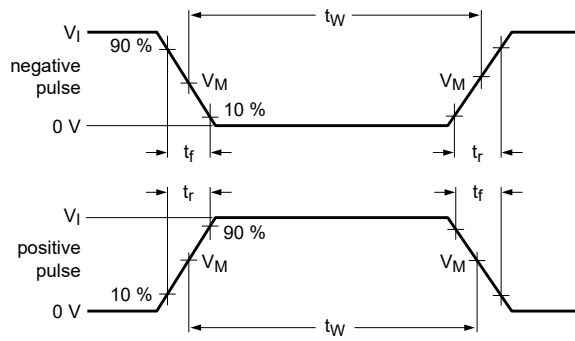


Table 8. Measurement points

Supply voltage	Input	
V _{CC}	V _I	V _M
1.65 V to 1.95 V	V _{CC}	0.5 × V _{CC}
2.3 V to 2.7 V	V _{CC}	0.5 × V _{CC}
2.7 V	2.7 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V



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Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = Test voltage for switching times.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig. 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 11. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC08 v.4	20210430	Product data sheet	-	74ALVC08 v.3
Modifications:	<ul style="list-style-type: none"> • Section 1 updated. • Section 2: Reference to JESD36 removed. • Section 7: Derating values for P_{tot} total power dissipation have been updated. 			
74ALVC08 v.3	20171005	Product data sheet	-	74ALVC08 v.2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. 			
74ALVC08 v.2	20030516	Product specification	-	74ALVC08 v.1
74ALVC08 v.1	20030204	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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