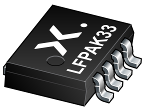



# BUK9M4R3-40H

## N-channel 40 V, 4.3 mΩ logic level MOSFET in LFPAK33

30 March 2020 Product data sheet

## 1. General description

Automotive qualified logic level N-channel MOSFET in an LFPAK33 package using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101 for use in high performance automotive applications.

## 2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Trench 9 superjunction technology:
  - Low power losses, high power density
- LFPAK copper clip package technology:
  - High robustness and reliability
  - Gull wing leads for high manufacturability and AOI
- Repetitive avalanche rated

## 3. Applications

- 12 V automotive systems
- Powertrain, chassis, body and infotainment applications
- Medium/Low power motor drive
- DC-DC systems
- LED lighting

## 4. Quick reference data

**Table 1. Quick reference data**

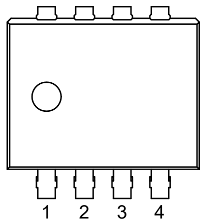
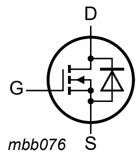
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 40 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | - | 95 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 90 | W |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 11 | | 2.4 | 3.4 | 4.3 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 4.5 V; Fig. 13; Fig. 14 | | - | 3.3 | 6.6 | nC |
| **Source-drain diode** | | | | | | | |
| $Q_r$ | recovered charge | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V | | - | 20 | - | nC |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| S | softness factor | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C; Fig. 17 | | - | 0.66 | - | |

[1] 95A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

# 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S | source |  LFPAK33 (SOT1210) |  |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | Mounting base; connected to drain | | |

# 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BUK9M4R3-40H | LFPAK33 | Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch | SOT1210 |

# 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| BUK9M4R3-40H | 94H340 |

# 8. Limiting values

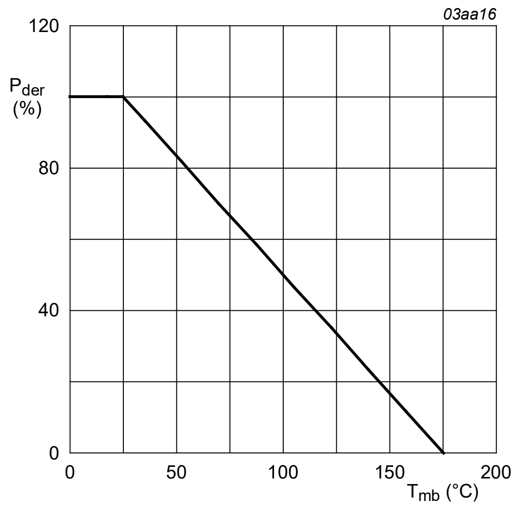
**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 40 | V |
| $V_{GS}$ | gate-source voltage | DC; $T_j$ ≤ 175 °C | | -10 | 16 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 90 | W |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | 95 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 2 | | - | 69 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 392 | A |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |

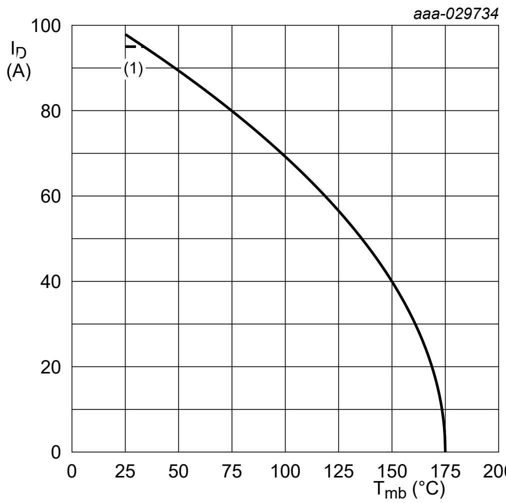
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | | - | 95 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p \leq$ 10 µs; $T_{mb}$ = 25 °C | | - | 392 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 70 A; $V_{sup} \leq$ 40 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4 | [2] [3] [4] | - | 44 | mJ |
| $I_{AS}$ | non-repetitive avalanche current | $V_{sup} \leq$ 40 V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $R_{GS}$ = 50 Ω | [4] | - | 70 | A |

[1] 95A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.
[4] Protected by 100% test.



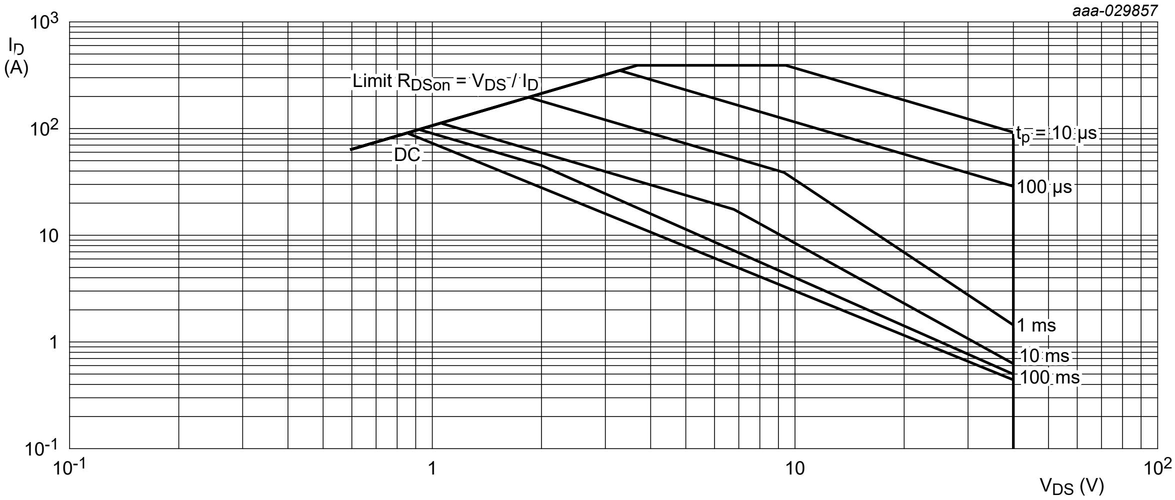

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**



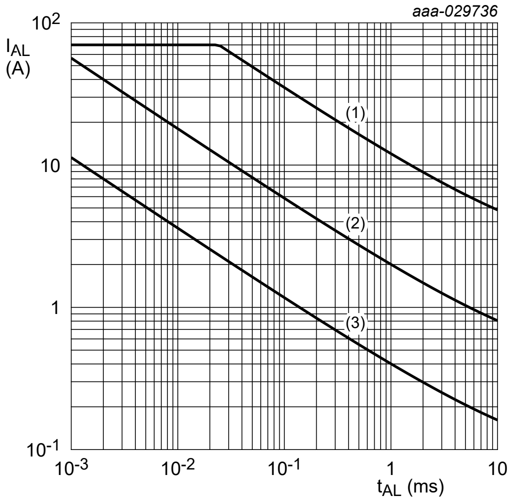

$V_{GS} \geq$ 10 V
(1) 95A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

**Fig. 2. Continuous drain current as a function of mounting base temperature**




$T_{mb} = 25$ °C; $I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**




(1) $T_{j\ (init)} = 25$ °C; (2) $T_{j\ (init)} = 150$ °C; (3) Repetitive Avalanche

**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | 1.48 | 1.67 | K/W |

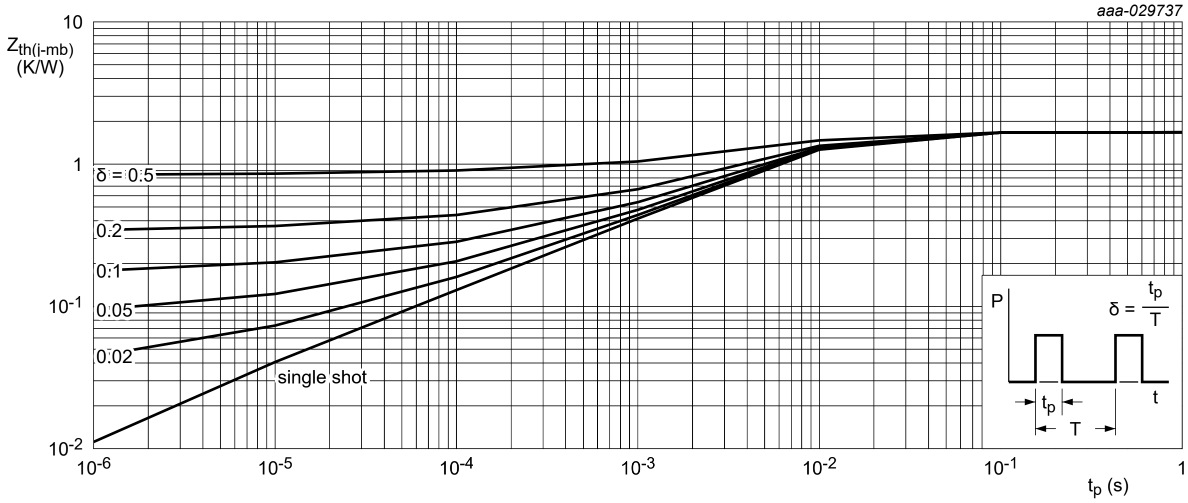


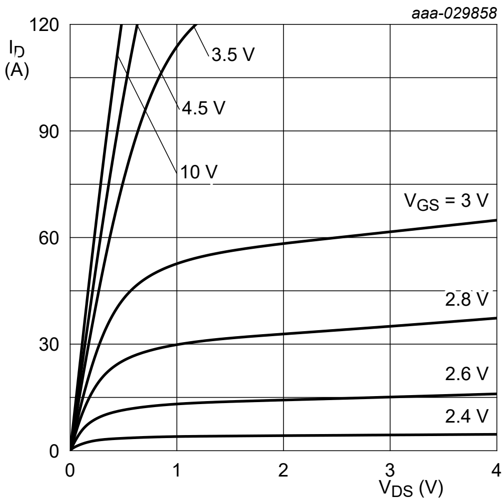

**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

# 10. Characteristics

**Table 7. Characteristics**

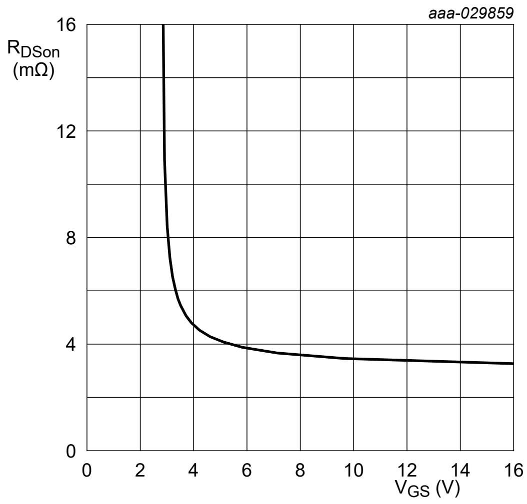
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 40 | 43 | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -40 °C | | - | 40.5 | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 36 | 40 | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C; Fig. 9; Fig. 10 | | 1.45 | 1.77 | 2.15 | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = -55 °C; Fig. 10 | | - | - | 2.6 | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 175 °C; Fig. 10 | | 0.7 | - | - | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.03 | 5 | µA |
| | | $V_{DS}$ = 16 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | 0.76 | 10 | µA |
| | | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | | - | 63 | 500 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = -10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 11 | | 2.4 | 3.4 | 4.3 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 105 °C; Fig. 12 | | 3.5 | 5.2 | 6.8 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 125 °C; Fig. 12 | | 3.9 | 5.8 | 7.5 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 175 °C; Fig. 12 | | 5 | 7.1 | 9.4 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 20 A; $T_j$ = 25 °C; Fig. 11 | | 3 | 4.4 | 5.5 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 20 A; $T_j$ = 105 °C; Fig. 12 | | 4.5 | 6.5 | 8.6 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 20 A; $T_j$ = 125 °C; Fig. 12 | | 4.9 | 7.2 | 9.6 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 20 A; $T_j$ = 175 °C; Fig. 12 | | 6.2 | 8.8 | 12 | mΩ |
| $R_G$ | gate resistance | f = 1 MHz; $T_j$ = 25 °C | | 0.3 | 0.8 | 2 | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 10 V; Fig. 13; Fig. 14 | | - | 31 | 43 | nC |
| | | $I_D$ = 25 A; $V_{DS}$ = 20 V; $V_{GS}$ = 4.5 V; Fig. 13; Fig. 14 | | - | 14 | 20 | nC |
| $Q_{GS}$ | gate-source charge | | | - | 5.6 | 8.4 | nC |
| $Q_{GD}$ | gate-drain charge | | | - | 3.3 | 6.6 | nC |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 25 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 15 | | - | 2132 | 2985 | pF |
| $C_{oss}$ | output capacitance | | | - | 491 | 687 | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 80 | 176 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 20 V; $R_L$ = 0.8 Ω; $V_{GS}$ = 4.5 V; $R_{G(ext)}$ = 5 Ω | | - | 14 | - | ns |
| $t_r$ | rise time | | | - | 16 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 15 | - | ns |
| $t_f$ | fall time | | | - | 9.3 | - | ns |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 16 | | - | 0.83 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; Fig. 17 | | - | 26 | - | ns |
| $Q_r$ | recovered charge | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V | | - | 20 | - | nC |
| S | softness factor | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C; Fig. 17 | | - | 0.66 | - | |
| | | $I_S$ = 25 A; $dI_S/dt$ = -500 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C; Fig. 17 | | - | 0.44 | - | |



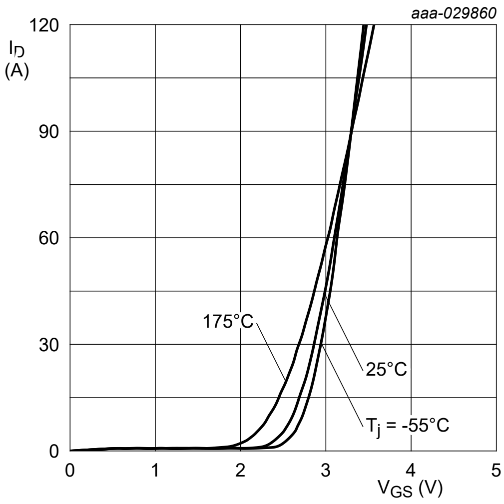

$T_j$ = 25 °C

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



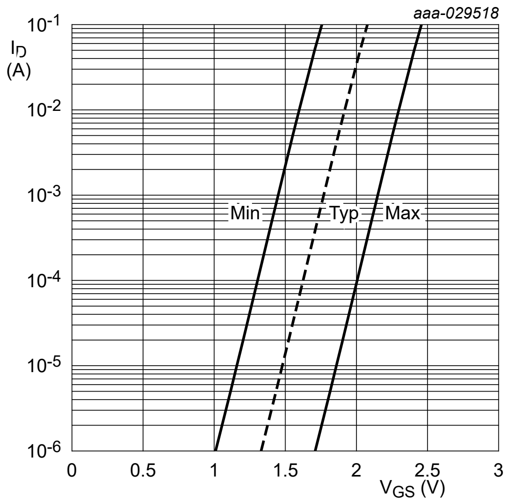

$T_j$ = 25 °C; $I_D$ = 25 A

**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**



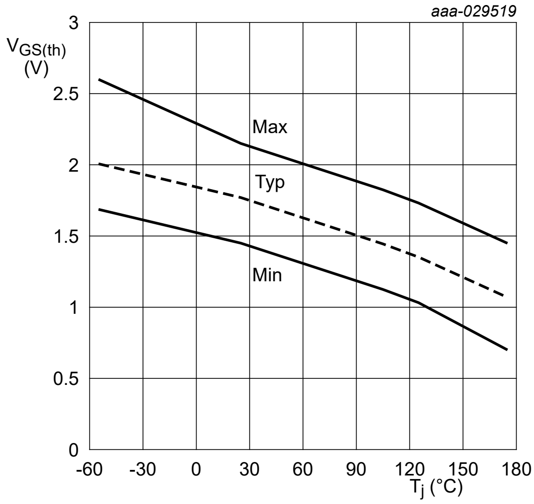

$V_{DS}$ = 8 V

**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



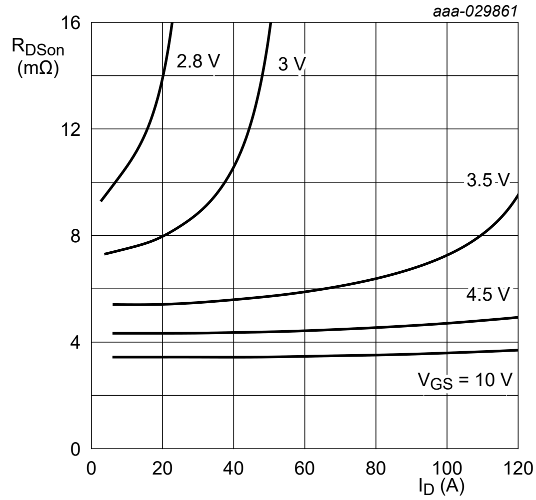

$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig. 9. Sub-threshold drain current as a function of gate-source voltage**



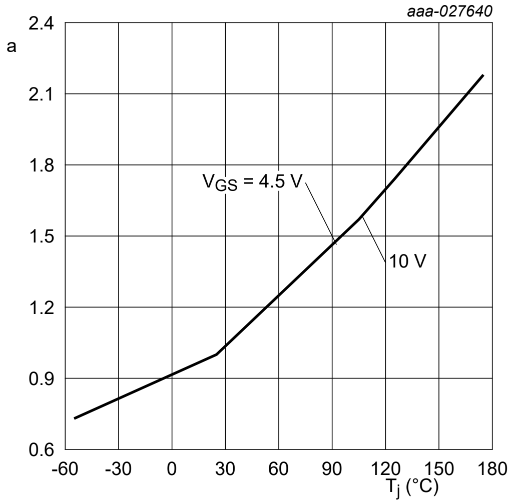

$I_D$ = 1 mA ; $V_{DS} = V_{GS}$

**Fig. 10. Gate-source threshold voltage as a function of junction temperature**



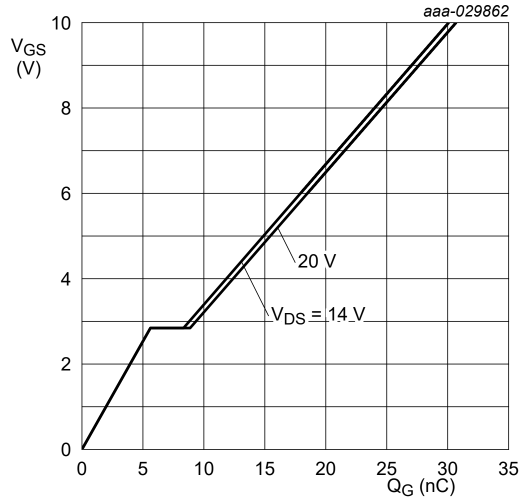

$T_j$ = 25 °C

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**




$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**




$T_j$ = 25 °C; $I_D$ = 25 A

**Fig. 13. Gate-source voltage as a function of gate charge; typical values**

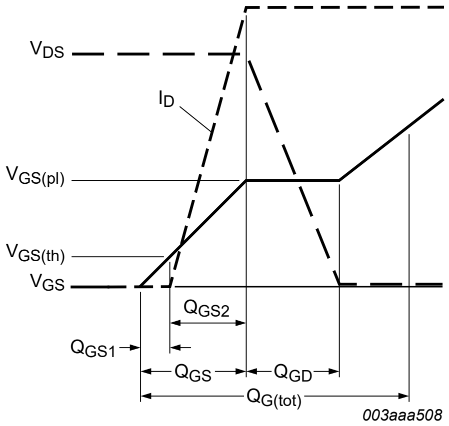
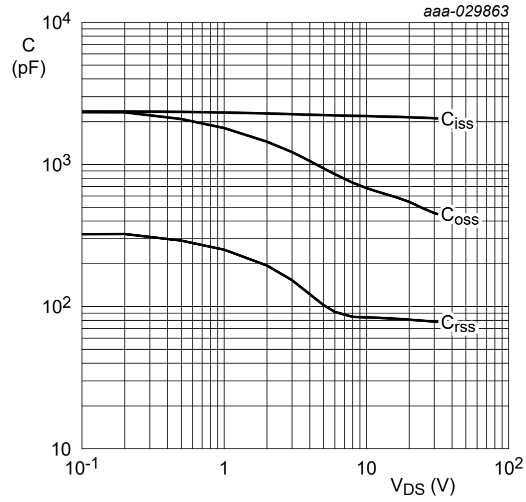
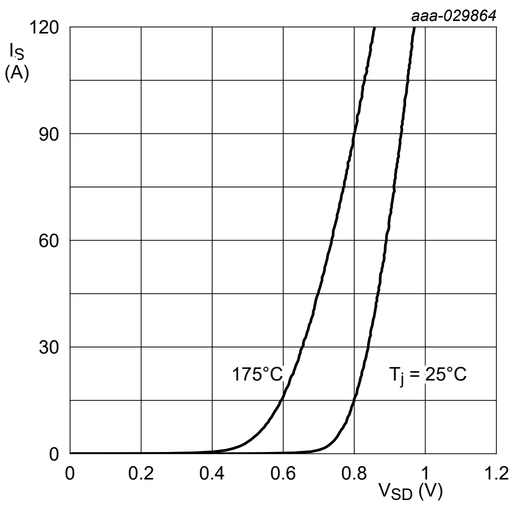



**Fig. 14. Gate charge waveform definitions**




$V_{GS}$ = 0 V; f = 1 MHz

**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**




$V_{GS}$ = 0 V

**Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

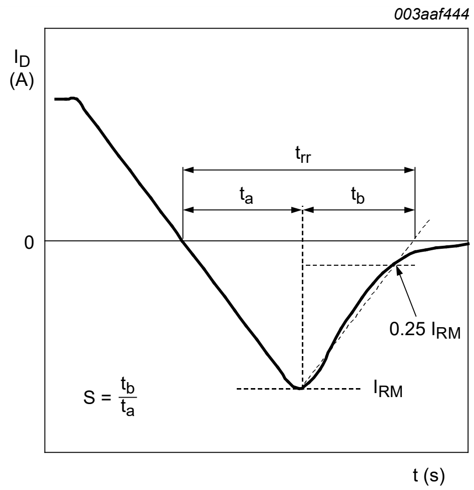
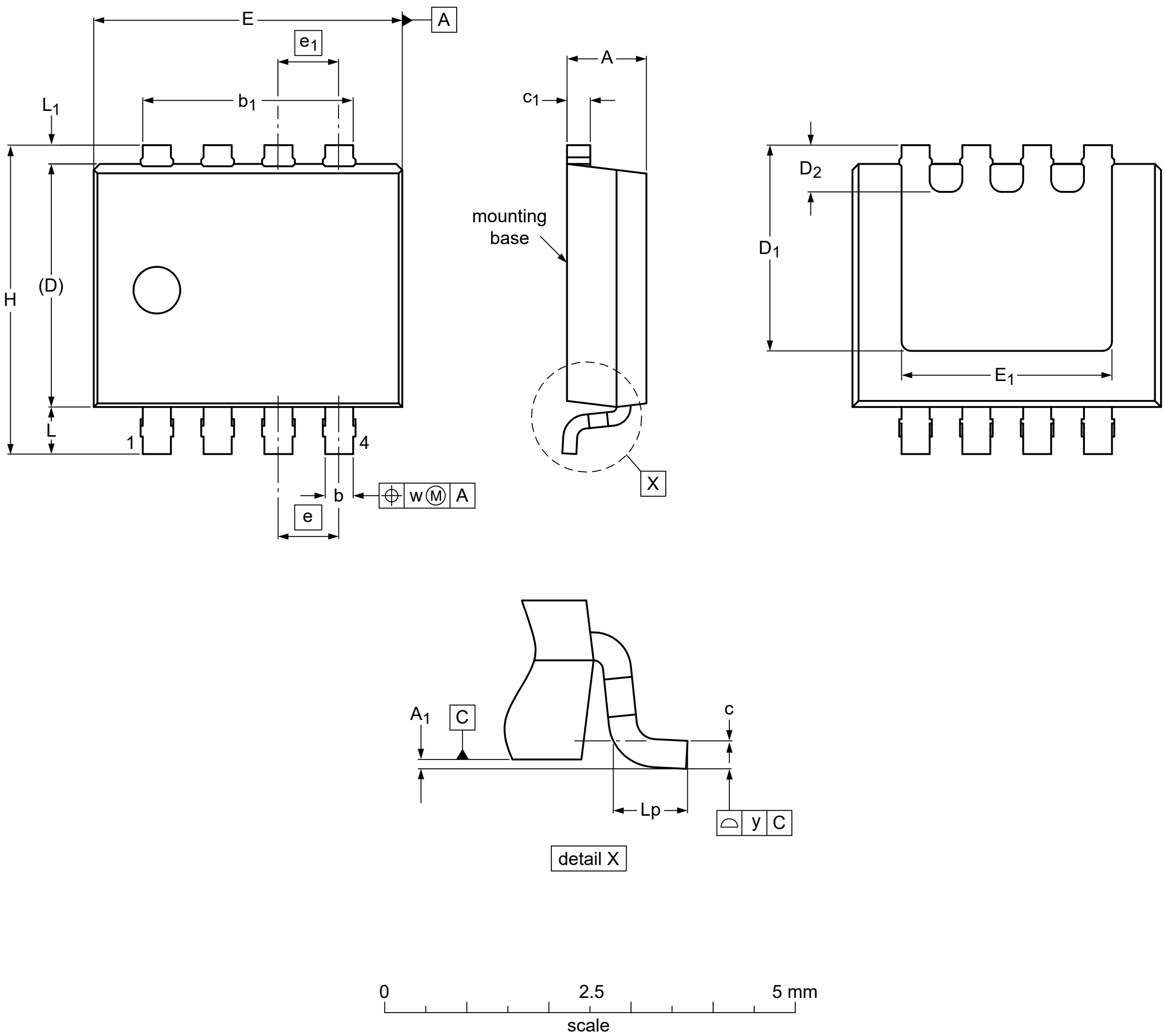



**Fig. 17. Reverse recovery timing definition**

## 11. Package outline

**Plastic single ended surface mounted package (LFPAK33); 8 leads** **SOT1210**




Dimensions

| Unit(1) | | A | $A_1$ | b(1) | $b_1$(1) | c | $c_1$ | D ref | $D_1$ | $D_2$ | E(1) | $E_1$ | e | $e_1$ | H | L | $L_1$ | $L_p$ | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 0.90 | 0.10 | 0.35 | 2.4 | 0.20 | 0.30 | | 2.35 | | 3.40 | 2.45 | | | 3.40 | 0.65 | 0.25 | 0.50 | | |
| mm | nom | | | | | | | 2.60 | | 0.50 | | | 0.65 | 0.65 | | | | | 0.20 | 0.10 |
| | min | 0.80 | 0.00 | 0.25 | 2.2 | 0.10 | 0.20 | | 1.90 | | 3.20 | 2.00 | | | 3.20 | 0.45 | 0.13 | 0.30 | | |

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

*sot1210_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1210 | | | | | | ~~14-04-25~~<br>16-08-09 |

**Fig. 18. Package outline LFPAK33 (SOT1210)**

## 12. Soldering

**Footprint information for reflow soldering of LFPAK33 package** **SOT1210**

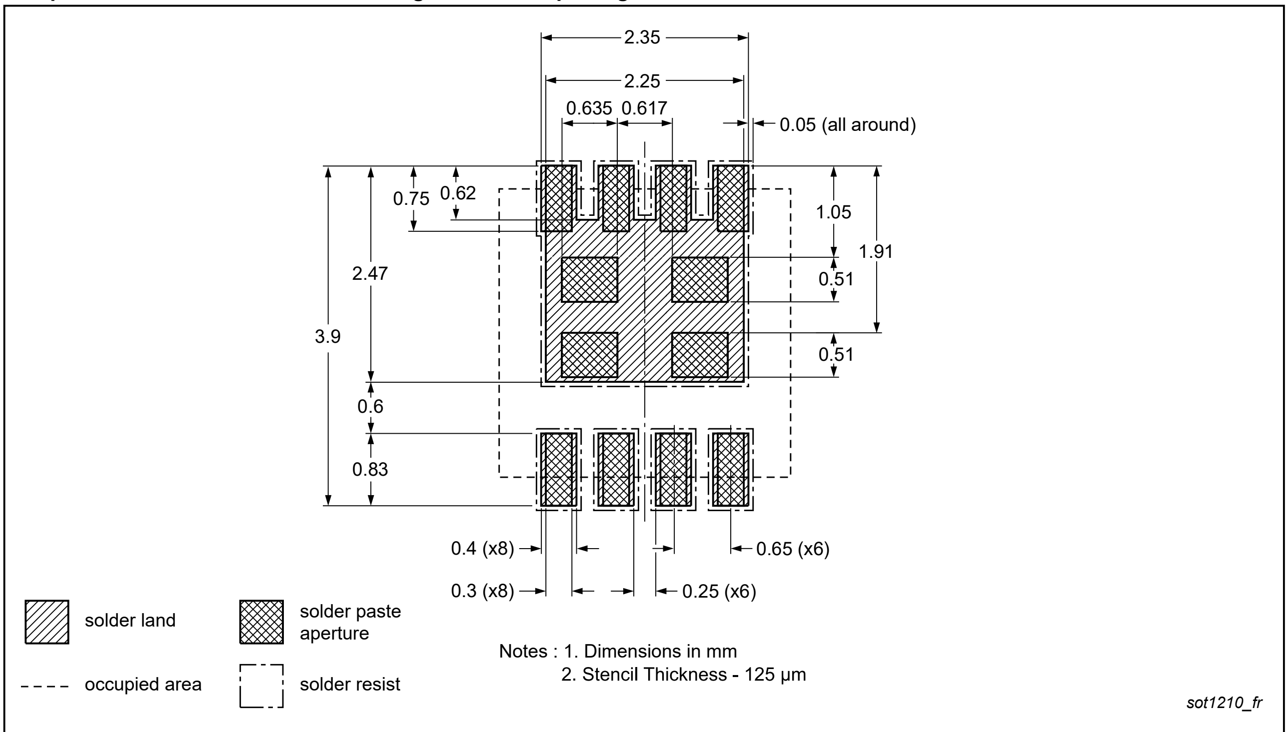



**Fig. 19. Reflow soldering footprint for LFPAK33 (SOT1210)**

# 13. Legal information

### Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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