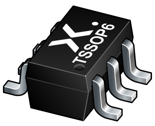

PBLS4002Y

40 V PNP loadswitch transistor

27 April 2022 Product data sheet

1. General description

PNP low V_{CEsat} transistor and NPN Resistor-Equipped Transistor (RET) in one very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Low V_{CEsat} transistor and resistor-equipped transistor in one package
- Low threshold voltage (<1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count
- AEC-Q101 qualified

3. Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1: PNP low V_{CEsat} transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	-40	V
I_{Clim}	limiting collector current			-	-	-500	mA
R_{CEsat}	collector-emitter saturation resistance	I_C = -500 mA; I_B = -50 mA; T_{amb} = 25 °C; pulsed; $t_p \leq$ 300 µs; $\delta_{factor} \leq$ 0.02		-	440	700	mΩ
TR2: NPN resistor-equipped transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	50	V
I_O	output current			-	-	100	mA
R1	bias resistor 1 (input)			3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	

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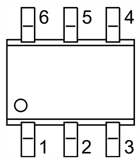
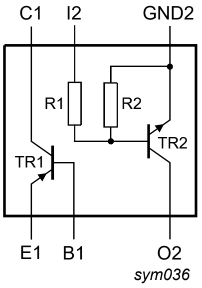
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 TSSOP6 (SOT363)	
2	B1	base TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	C1	collector TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBLS4002Y	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PBLS4002Y	S2%

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR1: PNP low V_{CEsat} transistor						
V_{CBO}	collector-base voltage	open emitter		-	-40	V
V_{CEO}	collector-emitter voltage	open base		-	-40	V
V_{EBO}	emitter-base voltage	open collector		-	-6	V
I_{Clim}	limiting collector current			-	-500	mA
I_{CM}	peak collector current	$t_p \leq$ 1 ms; single pulse		-	-1	mA
I_B	base current			-	-50	mA
I_{BM}	peak base current	single pulse; $t_p \leq$ 1 ms		-	-100	mA
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C	[1]	-	200	mW
TR2: NPN resistor-equipped transistor						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_I	input voltage	input voltage TR2 positive		-	30	V
		input voltage TR2 negative		-	-10	V
I_O	output current			-	100	mA
I_{CM}	peak collector current	$t_p \leq$ 1 ms; single pulse		-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C	[1]	-	200	mW
Per device						
P_{tot}	total power dissipation			-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	416	K/W

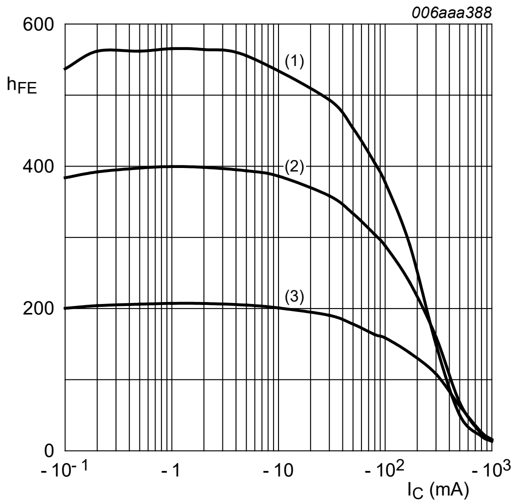
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

10. Characteristics

Table 7. Characteristics

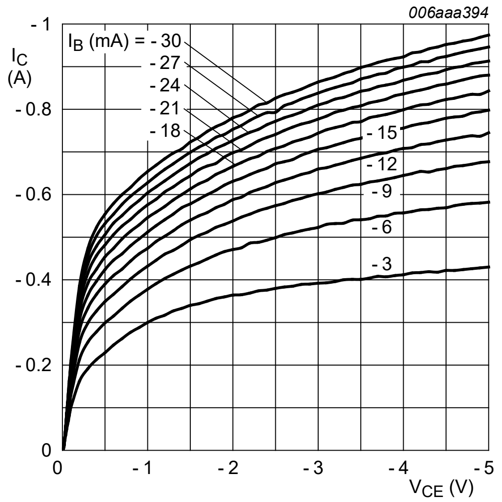
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1: PNP low V_{CEsat} transistor							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = -100 µA; I_E = 0 A; T_{amb} = 25 °C		-40	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = -10 mA; I_B = 0 A; T_{amb} = 25 °C		-40	-	-	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_C = 0 A; I_E = 100 µA; T_{amb} = 25 °C		-6	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = -40 V; I_E = 0 A; T_{amb} = 25 °C		-	-	-100	nA
		V_{CB} = -40 V; I_E = 0 A; T_{amb} = 150 °C		-	-	-50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = -5 V; I_C = 0 mA; T_{amb} = 25 °C		-	-	-100	nA
h_{FE}	DC current gain	V_{CE} = -2 V; I_C = -10 mA; pulsed; T_{amb} = 25 °C		200	-	-	
		V_{CE} = -2 V; I_C = -100 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		150	-	-	
		V_{CE} = -2 V; I_C = -500 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		40	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = -10 mA; I_B = -0.5 mA; T_{amb} = 25 °C		-	-	-50	mV
		I_C = -100 mA; I_B = -5 mA; T_{amb} = 25 °C		-	-	-130	mV
		I_C = -200 mA; I_B = -10 mA; T_{amb} = 25 °C		-	-	-200	mV
		I_C = -500 mA; I_B = -50 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02 %; T_{amb} = 25 °C		-	-	-350	mV
R_{CEsat}	collector-emitter saturation resistance	I_C = -500 mA; I_B = -50 mA; T_{amb} = 25 °C; pulsed; t_p ≤ 300 µs; $δ_{factor}$ ≤ 0.02		-	440	700	mΩ
V_{BEsat}	base-emitter saturation voltage			-	-	-1.2	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = -2 V; I_C = -100 mA; T_{amb} = 25 °C; pulsed; t_p ≤ 300 µs; $δ_{factor}$ ≤ 0.02		-	-	-1.1	V
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	10	pF
f_T	transition frequency	V_{CE} = -5 V; I_C = -100 mA; f = 100 MHz; T_{amb} = 25 °C		100	300	-	MHz
TR2: NPN resistor-equipped transistor							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A; T_{amb} = 25 °C		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 10 mA; I_B = 0 A; T_{amb} = 25 °C		50	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A; T_{amb} = 25 °C		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 50 V; I_B = 0 A; T_{amb} = 25 °C		-	-	1	µA
		V_{CE} = 50 V; I_B = 0 A; T_{amb} = 150 °C		-	-	50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	900	µA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 10 mA; T_{amb} = 25 °C		30	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; T_{amb} = 25 °C		-	-	150	mV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 µA; T_{amb} = 25 °C		-	1.1	0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 20 mA; T_{amb} = 25 °C		2.5	1.9	-	V
R1	bias resistor 1 (input)			3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	2.5	pF



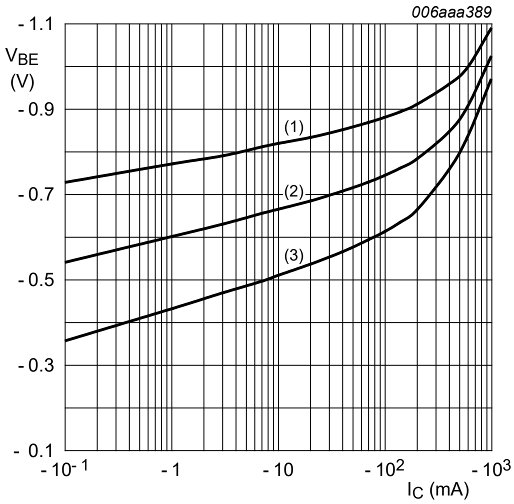
V_{CE} = −2 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 1. TR1 (PNP): DC current gain as a function of collector current; typical values



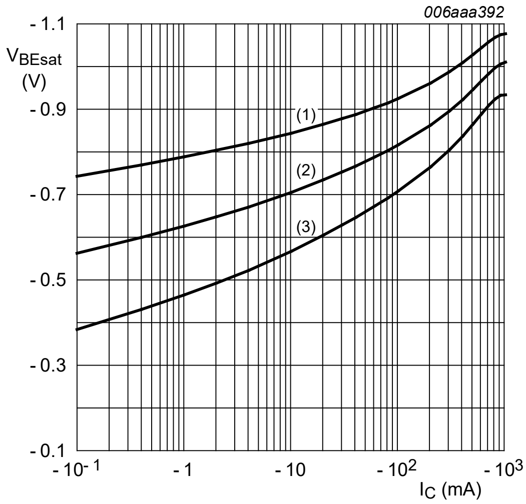
T_{amb} = 25 °C

Fig. 2. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values



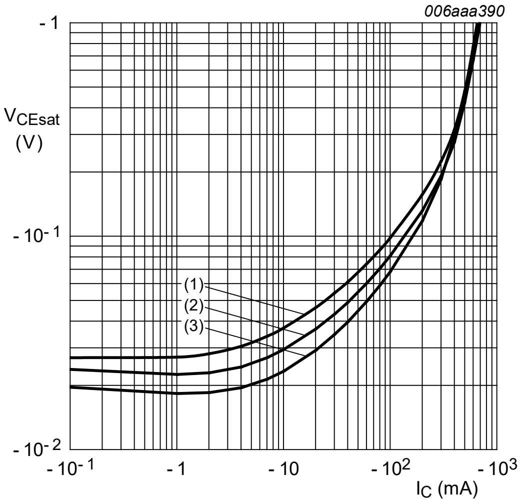
V_{CE} = −2 V
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 3. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values



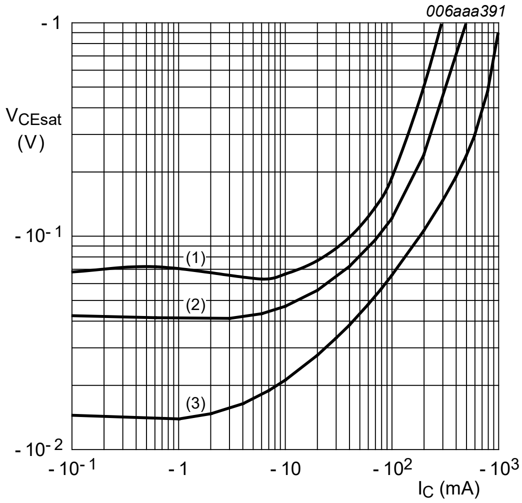
I_C/I_B = 20
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 4. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



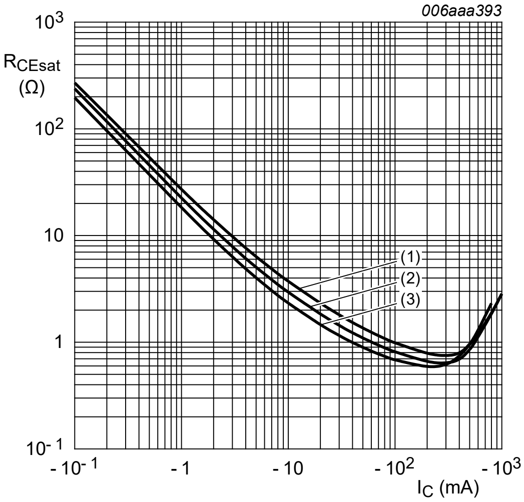
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 5. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



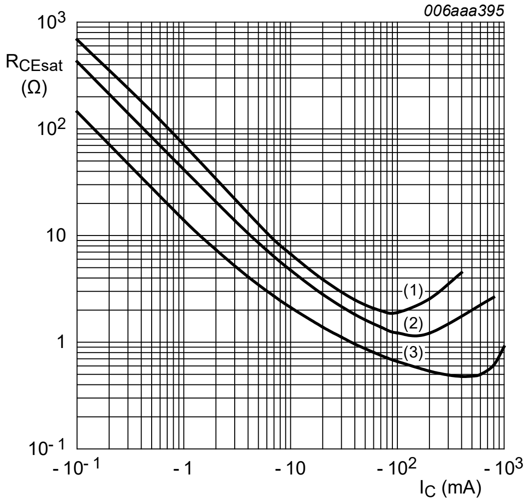
T_{amb} = 25 °C
(1) I_C/I_B = 100
(2) I_C/I_B = 50
(3) I_C/I_B = 10

Fig. 6. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



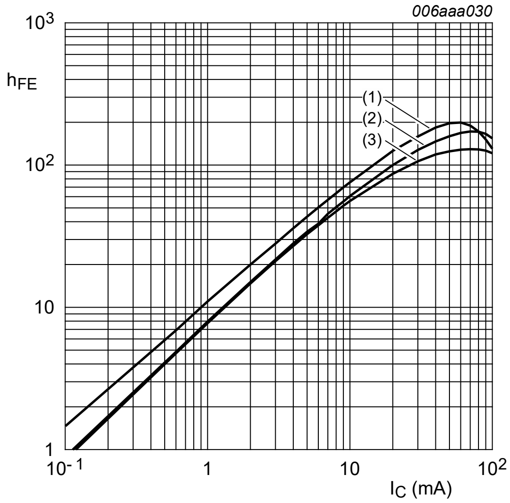
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb}= 25 °C
(3) T_{amb} = −55 °C

Fig. 7. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



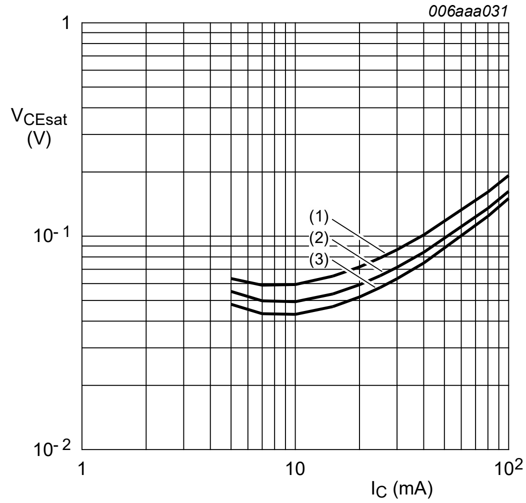
T_{amb} = 25 °C
(1) I_C/I_B = 100
(2) I_C/I_B = 50
(3) I_C/I_B = 10

Fig. 8. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



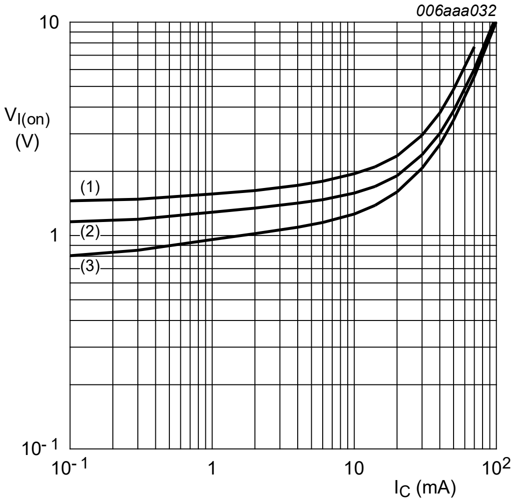
V_{CE} = 5 V
(1) T_{amb} = 150 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −40 °C

Fig. 9. TR2 (NPN): DC current gain as a function of collector current; typical values



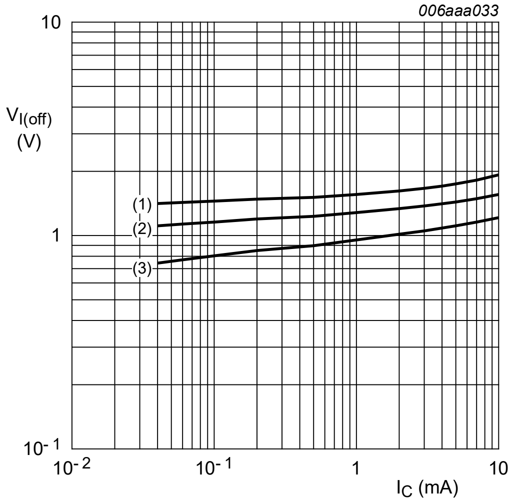
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 10. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



V_{CE} = 0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 11. TR2 (NPN): On-state input voltage as a function of collector current; typical values



V_{CE} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 12. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I_{i2}) - V(I_{i1})}{I_{i2} - I_{i1}}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_{i3})}{R1 \times I_{i3}} - 1$$

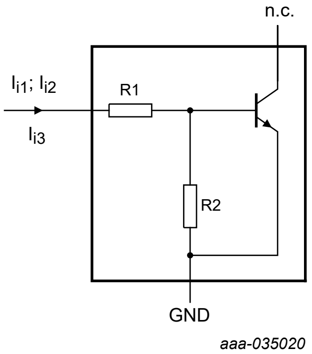


Fig. 13. TR2 (NPN): Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

R1 (kΩ)	R2 (kΩ)	Test conditions		
		I_{i1}	I_{i2}	I_{i3}
Per transistor, for the PNP with negative polarity				
4.7	4.7	750 µA	950 µA	850 µA

12. Package outline

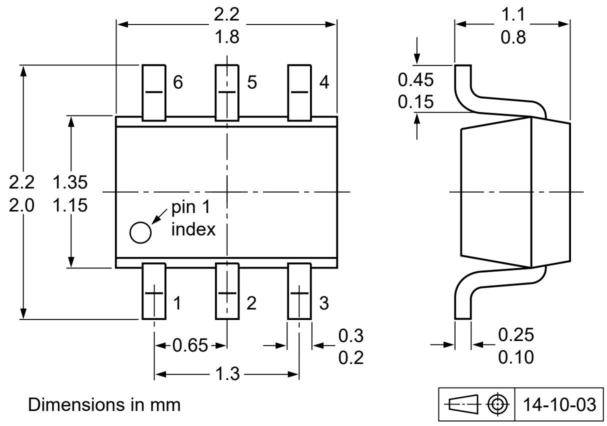


Fig. 14. Package outline TSSOP6 (SOT363)

13. Soldering

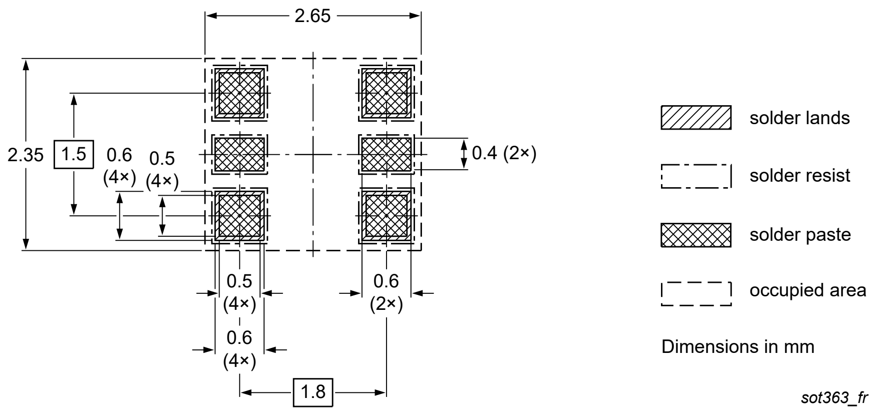


Fig. 15. Reflow soldering footprint for TSSOP6 (SOT363)

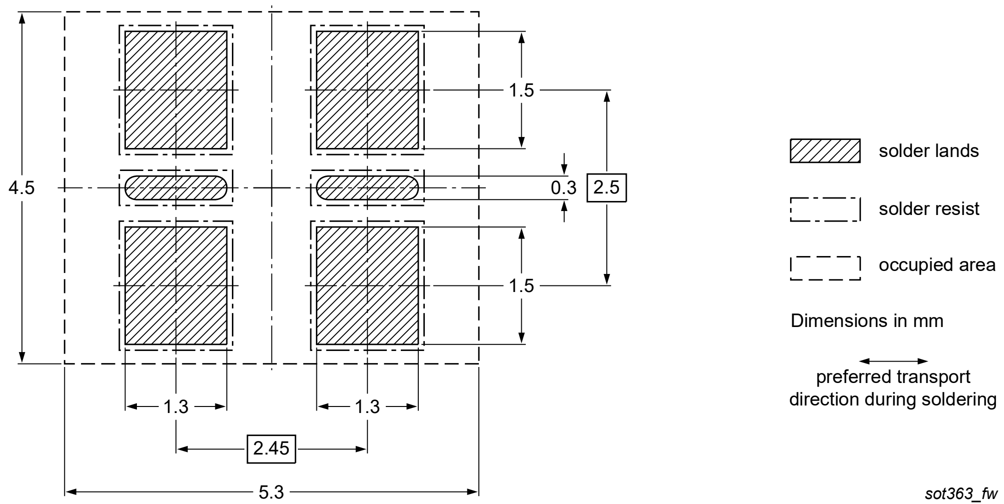


Fig. 16. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBLS4002Y v.4	20220427	Product data sheet	-	PBLS4002Y_PBLS4002V_3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Family data sheet splitted to single type data sheets. • Packing section removed.			
PBLS4002Y_PBLS4002V_3	20090212	Product data sheet	-	PBLS4002Y_PBLS4002V_2
PBLS4002Y_PBLS4002V_2	20050719	Product data sheet	-	PBLS4002Y_PBLS4002V_1
PBLS4002Y_PBLS4002V_1	20041206	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Contents

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Date of release: 27 April 2022