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Kind regards,

Team Nexperia

PESD5V0L6UAS; PESD5V0L6US

Low capacitance 6-fold ESD protection diode arrays

Rev. 03 — 18 August 2009 Product data sheet

1. Product profile

1.1 General description

Low capacitance 6-fold ESD protection diode arrays in small plastic packages designed to protect up to six transmission or data lines from the damage caused by ElectroStatic Discharge (ESD) and other transients.

Table 1. Product overview

Type number	Package	
	Name	NXP
PESD5V0L6UAS	TSSOP8	SOT505-1
PESD5V0L6US	SO8	SOT96-1

1.2 Features

- ESD protection of up to six lines
- Low diode capacitance
- Max. peak pulse power: P_{PP} = 35 W
- Low clamping voltage: $V_{(CL)R}$ = 15 V
- Ultra low leakage current: I_{RM} = 8 nA
- ESD protection of up to 20 kV
- IEC 61000-4-2, level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PP} = 2.5 A

1.3 Applications

- Computers and peripherals
- Communication systems
- Audio and video equipment
- High speed data lines
- Parallel ports

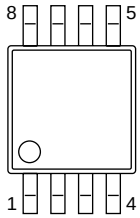
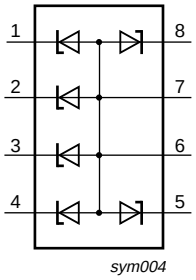
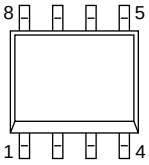
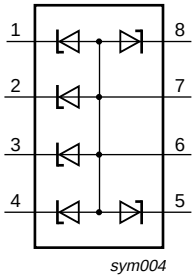
1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse stand-off voltage		-	-	5	V
C_d	diode capacitance	V_R = 0 V; f = 1 MHz	-	16	19	pF

2. Pinning information

Table 3. Discrete pinning

Pin	Description	Simplified outline	Symbol
TSSOP8			
1	cathode 1		
2	cathode 2		
3	cathode 3		
4	cathode 4		
5	cathode 5		
6	common anode		
7	common anode		
8	cathode 6		
SO8			
1	cathode 1		
2	cathode 2		
3	cathode 3		
4	cathode 4		
5	cathode 5		
6	common anode		
7	common anode		
8	cathode 6		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0L6UAS	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PESD5V0L6US	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Marking

Table 5. Marking

Type number	Marking code
PESD5V0L6UAS	5V06U
PESD5V0L6US	5V06US

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per diode						
P_{PP}	peak pulse power	8/20 µs pulse	[1][2]	-	35	W
I_{PP}	peak pulse current	8/20 µs pulse	[1][2]	-	2.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] Non-repetitive current pulse 8/20 µs exponentially decay waveform according to IEC 61000-4-5; see Figure 1.

[2] Measured from pin 1, 2, 3, 4, 5 or 8 to pin 6 or 7.

Table 7. ESD maximum ratings

Symbol	Parameter	Conditions		Min	Max	Unit
ESD	electrostatic discharge capability	IEC 61000-4-2 (contact discharge)	[1][2]	-	20	kV
		HBM MIL-STD883		-	10	kV

[1] Device stressed with ten non-repetitive ElectroStatic Discharge (ESD) pulses; see Figure 2.

[2] Measured from pin 1, 2, 3, 4, 5 or 8 to pin 6 or 7.

Table 8. ESD standards compliance

Standard	Conditions
IEC 61000-4-2, level 4 (ESD); see Figure 2	> 15 kV (air); > 8 kV (contact)
HBM MIL-STD883, class 3	> 4 kV

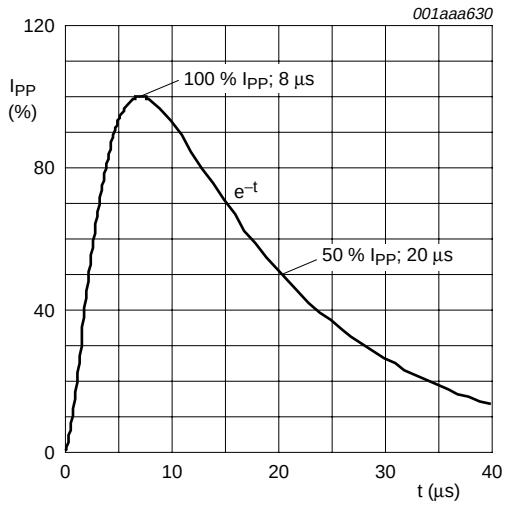


Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5

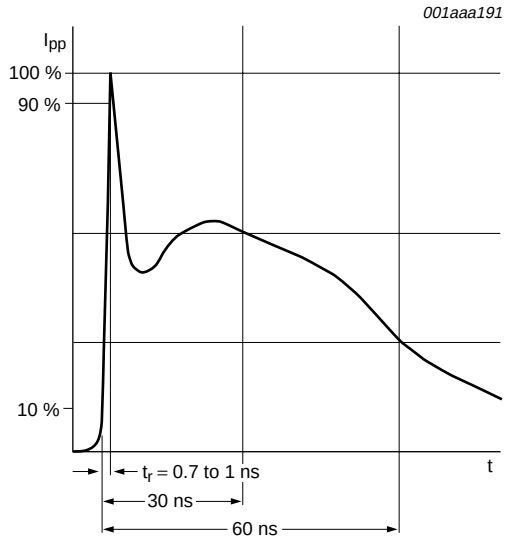


Fig 2. ElectroStatic Discharge (ESD) pulse waveform according to IEC 61000-4-2

6. Characteristics

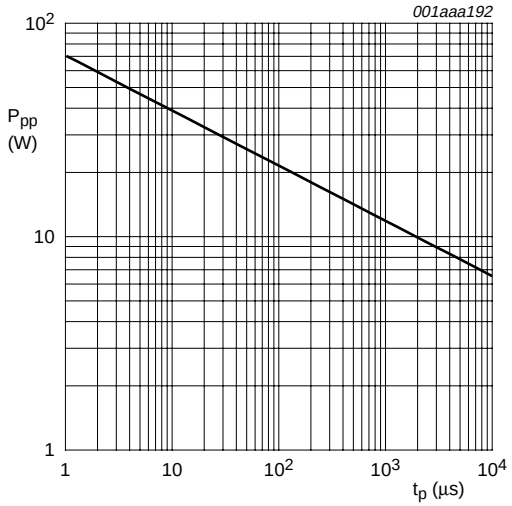
Table 9. Characteristics

T_{amb} = 25 °C unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per diode							
V_{RWM}	reverse stand-off voltage			-	-	5	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V		-	8	25	nA
$V_{(CL)R}$	clamping voltage	I_{PP} = 1 A	[1][2]	-	-	10	V
		I_{PP} = 2.5 A	[1][2]	-	-	15	V
$V_{(BR)}$	breakdown voltage	I_R = 1 mA		6.4	6.8	7.2	V
r_{dif}	differential resistance	I_R = 1 mA		-	-	100	Ω
C_d	diode capacitance	V_R = 0 V; f = 1 MHz; see Figure 5		-	16	19	pF

[1] Non-repetitive current pulse 8/20 µs exponentially decay waveform according to IEC 61000-4-5; see Figure 1.

[2] Measured between each cathode on pins 1, 2, 3, 4, 5 or 8 and anode on pin 6 or 7.



T_{amb} = 25 °C

Fig 3. Peak pulse power as a function of exponential pulse duration t_p; typical values

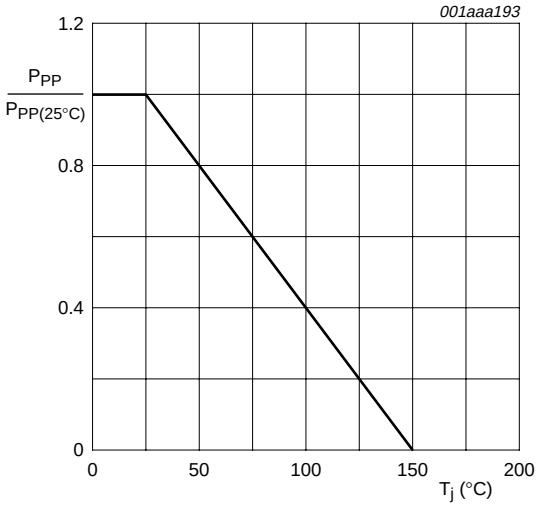
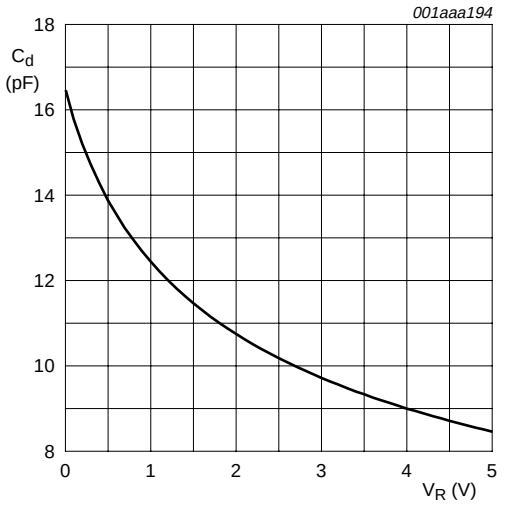


Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values



T_{amb} = 25 °C; f = 1 MHz

Fig 5. Diode capacitance as a function of reverse voltage; typical values

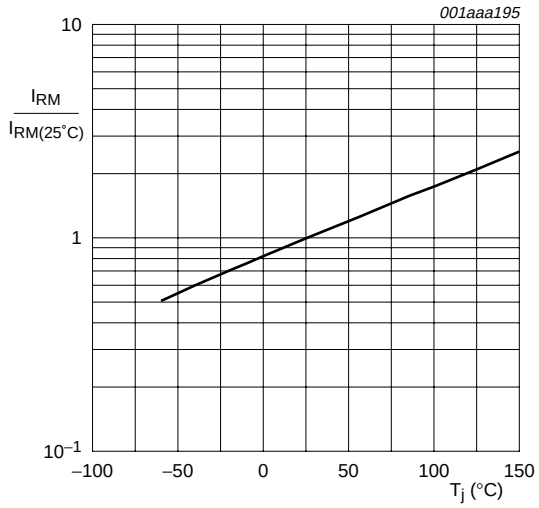


Fig 6. Relative variation of reverse leakage current as a function of junction temperature; typical values

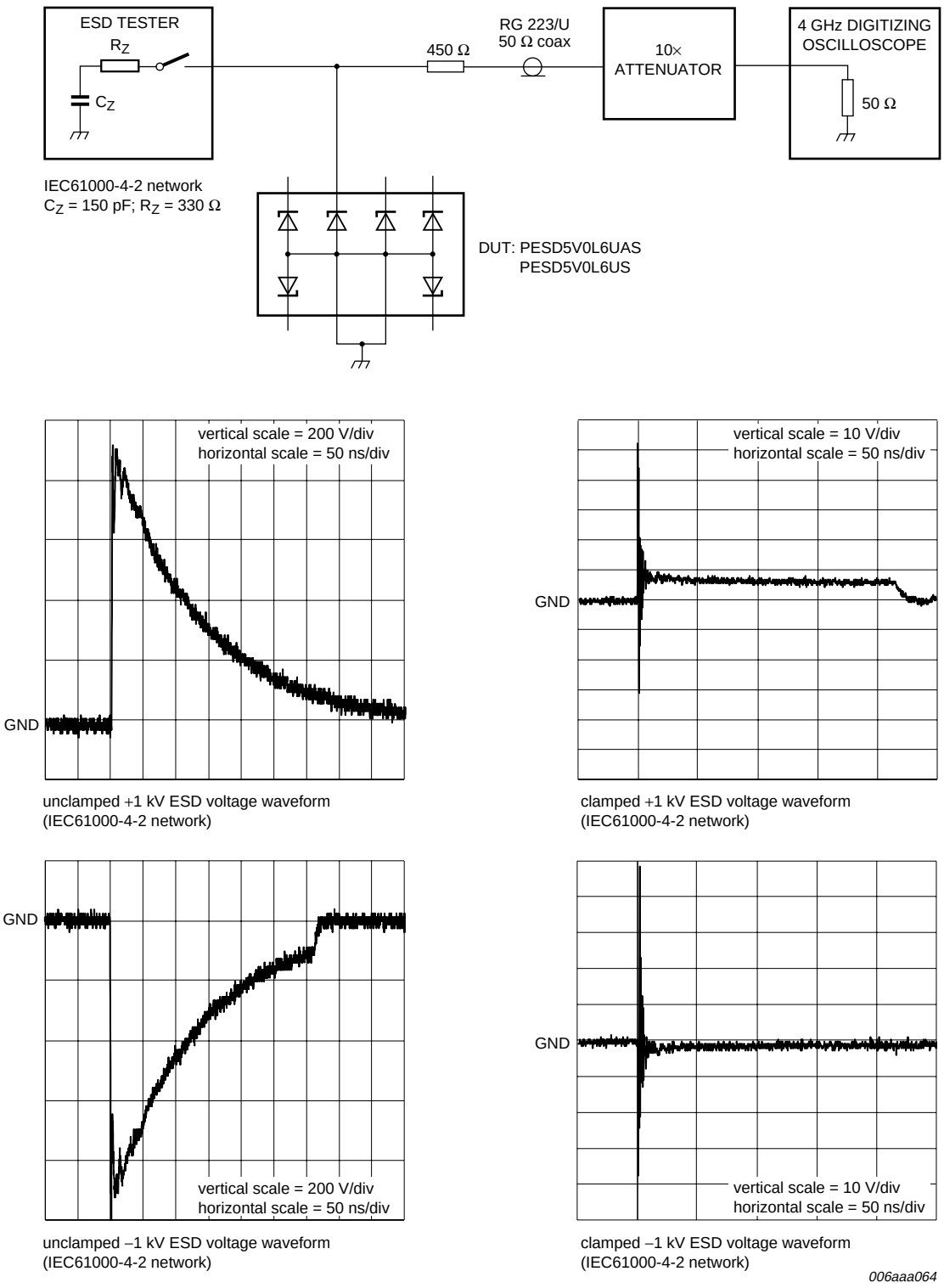


Fig 7. ESD clamping test setup and waveforms

7. Application information

The PESD5V0L6UAS and the PESD5V0L6US are designed for protection of up to six unidirectional data lines from the damage caused by ElectroStatic Discharge (ESD) and surge pulses. The PESD5V0L6UAS and the PESD5V0L6US may be used on lines where the signal polarity is above or below ground.

The PESD5V0L6UAS and the PESD5V0L6US provide a surge capability of 35 W per line for a 8/20 μs waveform.

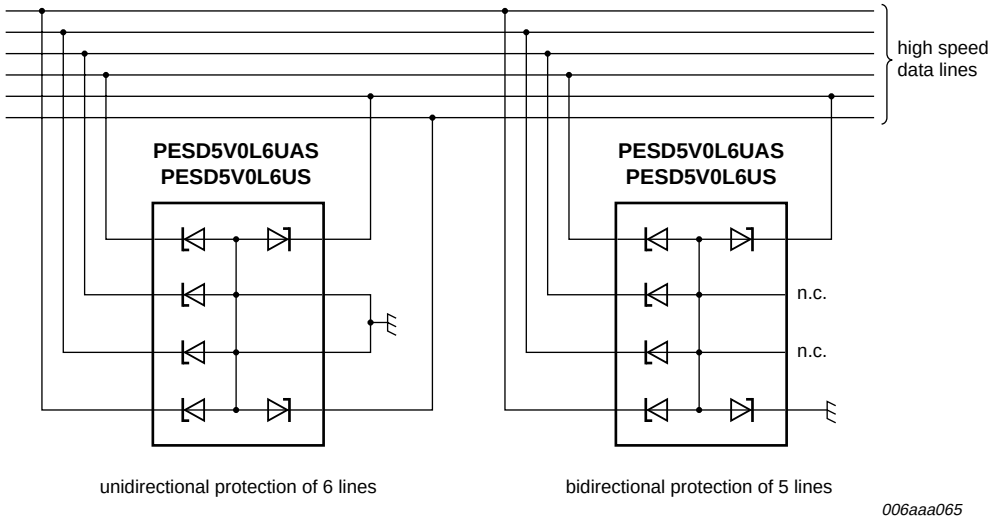


Fig 8. Typical application for ESD protection of data lines

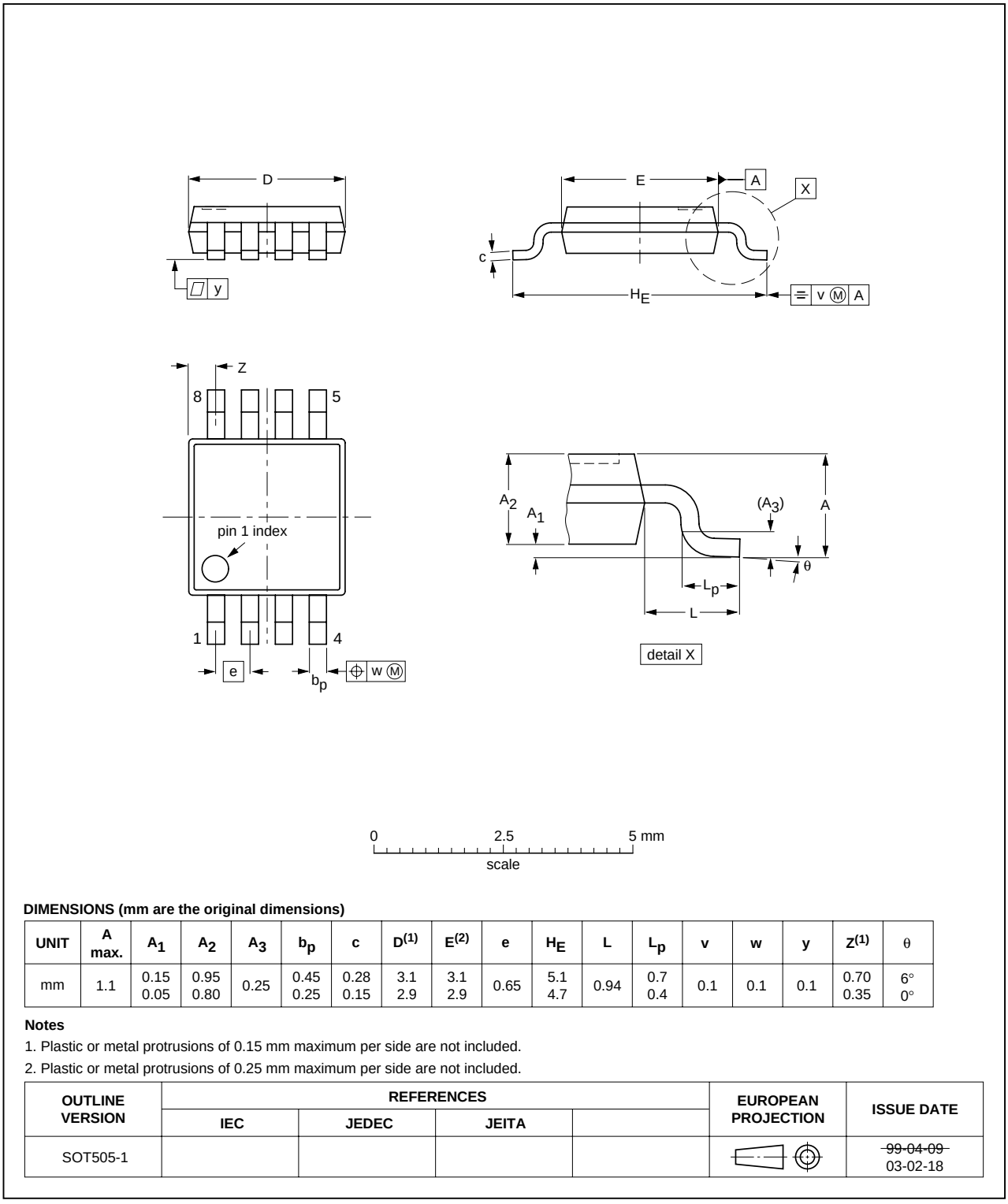
Circuit board layout and protection device placement:

Circuit board layout is critical for the suppression of ESD, EFT and surge transients. The following guidelines are recommended:

1. Place the protection device as close to the input terminal or connector as possible.
2. The path length between the protection device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protection conductors in parallel with unprotected conductor.
5. Minimize all printed-circuit board conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer printed-circuit boards, use ground vias.

8. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

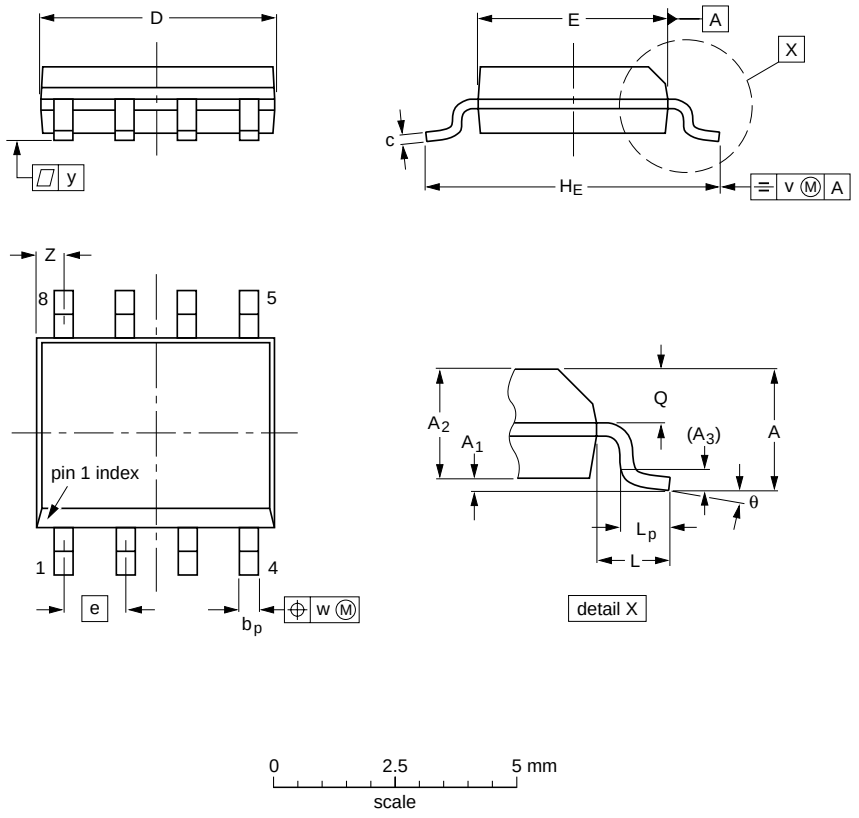
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 9. Package outline SOT505-1 (TSSOP8)

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 10. Package outline SOT96-1 (SO8/MS-012)

9. Packing information

Table 10. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity	
			1000	2500
PESD5V0L6UAS	SOT505-1	8 mm pitch, 12 mm tape and reel	-	-118
PESD5V0L6US	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

[1] For further information and the availability of packing methods, see Section 12.

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V06UAS_US_3	20090818	Product data sheet	-	PESD5V06UAS_US_2
Modifications:	• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content. • Table 3 “Discrete pinning”: amended			
PESD5V06UAS_US_2	20041109	Product data sheet	-	PESD5V0L6US_1
PESD5V0L6US_1	20040315	Product specification	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contents

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