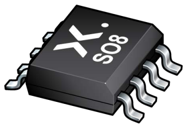


PHK18NQ03LT

N-channel TrenchMOS logic level FET

Rev. 03 — 17 March 2011 Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Notebook computers
- Switched-mode power supplies
- Voltage regulators

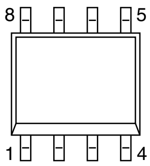
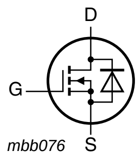
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	30	V
I_D	drain current	$T_{sp} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 3	-	-	20.3	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; see Figure 2	-	-	6.25	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 10; see Figure 11	-	7.1	8.9	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5$ V; $I_D = 15$ A; $V_{DS} = 12$ V; see Figure 12; see Figure 13	-	2.5	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 SOT96-1 (SO8)	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

3. Ordering information

Table 3. Ordering information

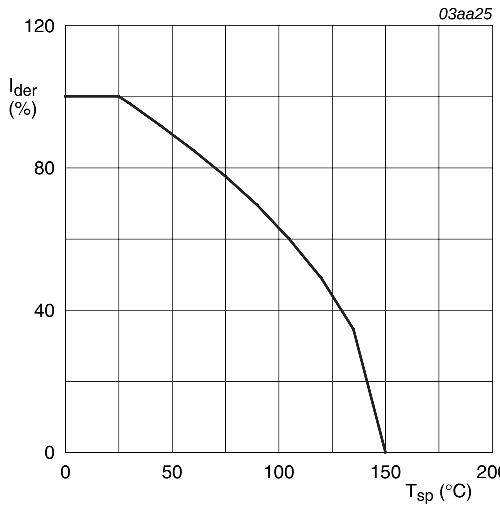
Type number	Package		
	Name	Description	Version
PHK18NQ03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

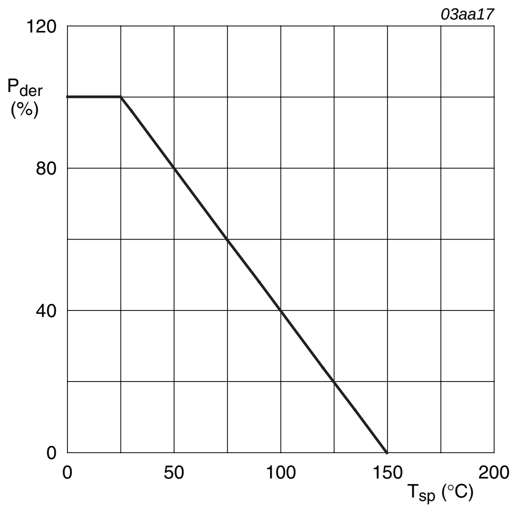
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; $R_{GS} = 20$ kΩ	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{sp} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 3	-	20.3	A
		$T_{sp} = 100$ °C; $V_{GS} = 10$ V; see Figure 1	-	12.1	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ µs; see Figure 3	-	80	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; see Figure 2	-	6.25	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25$ °C	-	5.2	A
I_{SM}	peak source current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ µs	-	20.8	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 31.5$ A; $V_{sup} \leq 25$ V; unclamped; $t_p = 0.07$ ms; $R_{GS} = 50$ Ω	-	50	mJ



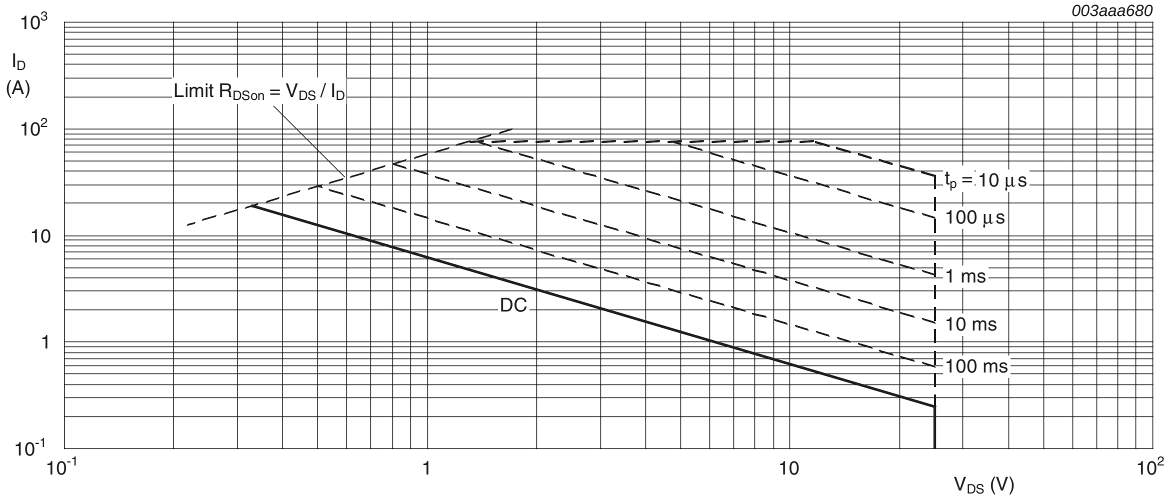
$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	20	K/W

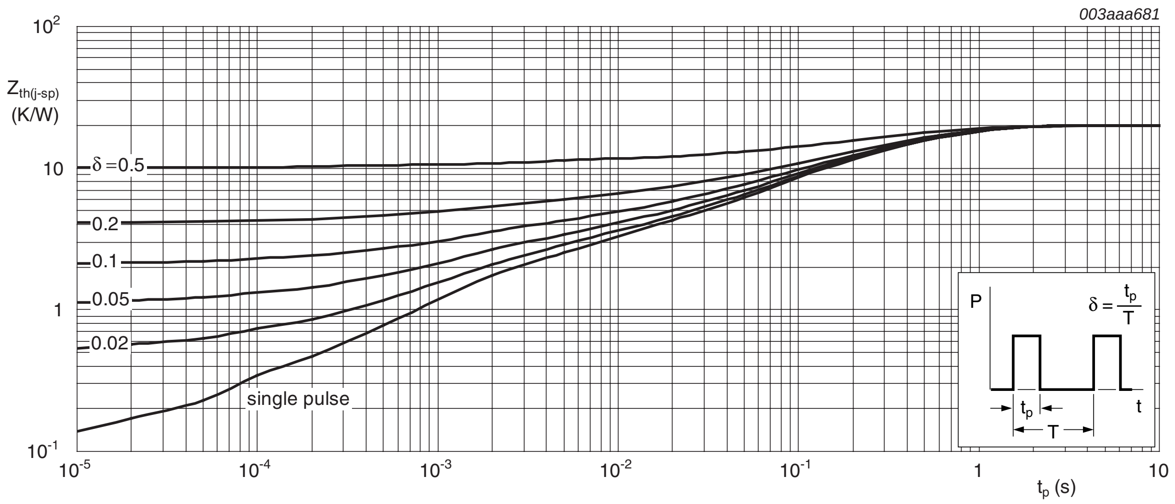


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

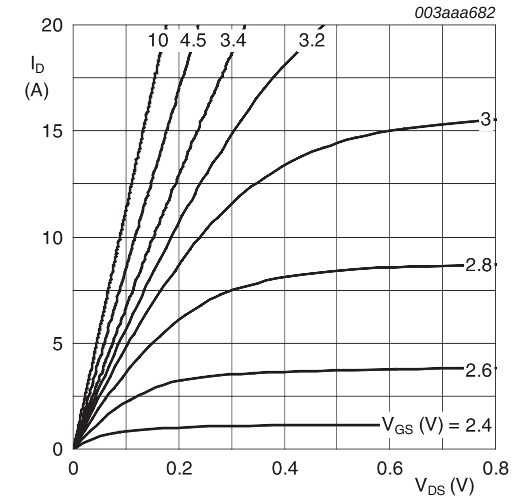
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 8; see Figure 9	1.3	1.7	2.15	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 8; see Figure 9	0.8	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 8; see Figure 9	-	-	2.6	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 10; see Figure 11	-	7.1	8.9	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C; see Figure 10	-	12.1	15.1	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; see Figure 10; see Figure 11	-	10.1	12.5	mΩ
R_G	gate resistance	f = 1 MHz	-	1.6	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 15 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see Figure 12; see Figure 13	-	10.6	-	nC
Q_{GS}	gate-source charge		-	4.85	-	nC
Q_{GS1}	pre-threshold gate-source charge		-	2.4	-	nC
Q_{GS2}	post-threshold gate-source charge		-	2.45	-	nC
Q_{GD}	gate-drain charge		-	2.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 15 A; V_{DS} = 12 V; see Figure 12; see Figure 13	-	3	-	V
C_{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 14	-	1380	-	pF
		V_{DS} = 0 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 14	-	1590	-	pF
C_{oss}	output capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 14	-	290	-	pF
C_{rss}	reverse transfer capacitance		-	135	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.8 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5.6 Ω	-	19	-	ns
t_r	rise time		-	22	-	ns
$t_{d(off)}$	turn-off delay time		-	19	-	ns
t_f	fall time		-	11	-	ns

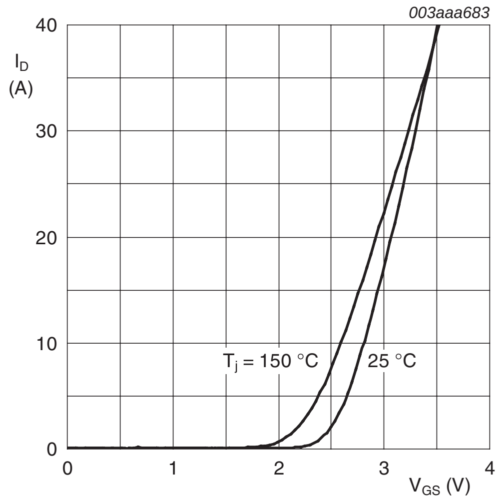
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 20 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 15	-	0.95	1.2	V
t_{rr}	reverse recovery time	I_S = 15 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V	-	34	-	ns
Q_r	recovered charge	I_S = 15 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V	-	14	-	nC



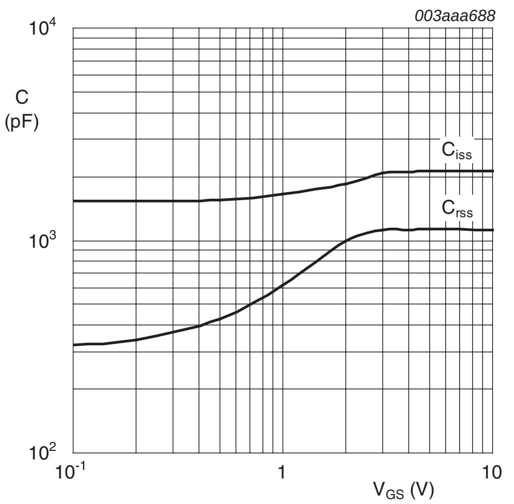
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



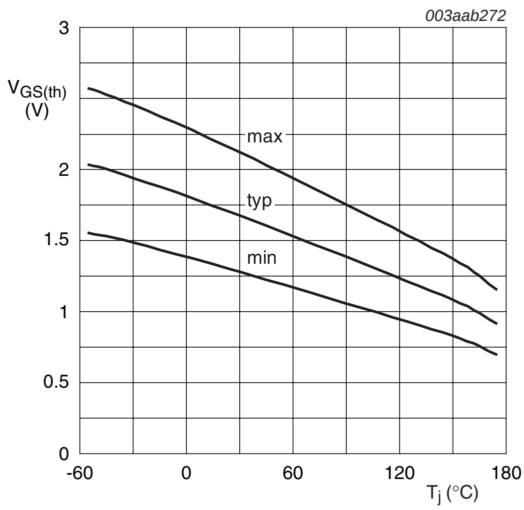
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



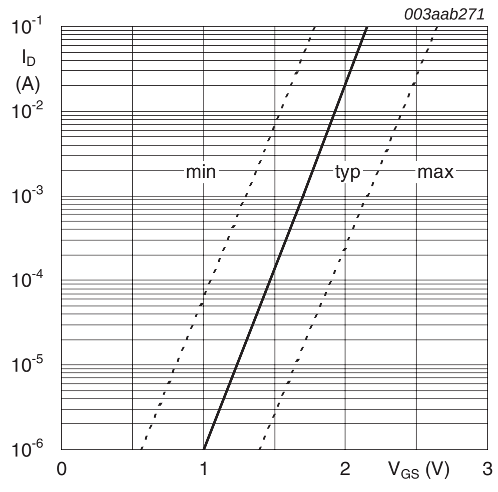
V_{GS} = 0 V; f = 1 MHz

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



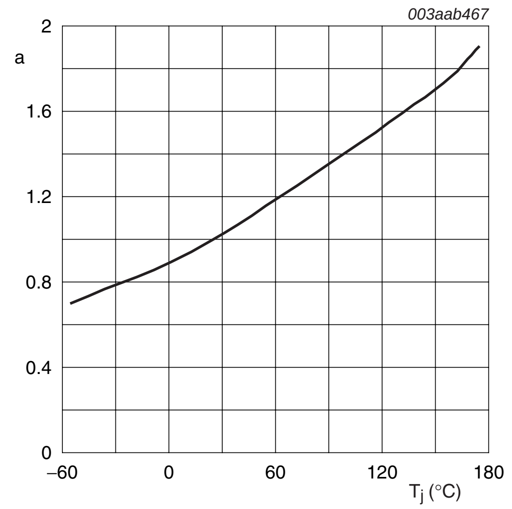
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



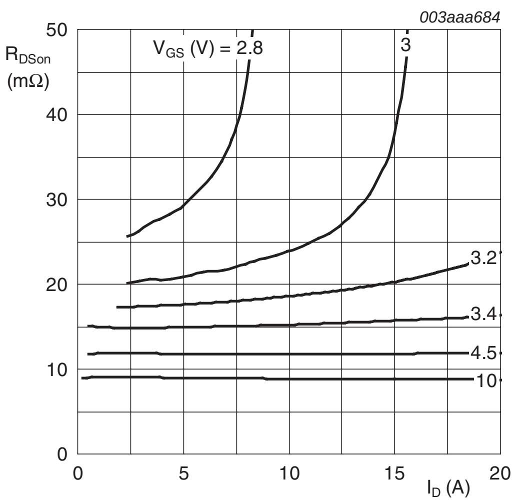
$T_j = 25\,°C; V_{DS} = 5\,V$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25\,°C$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values

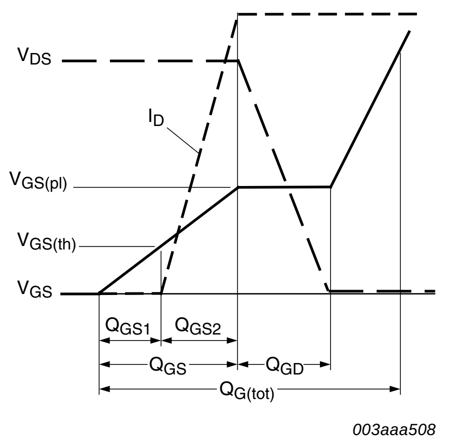
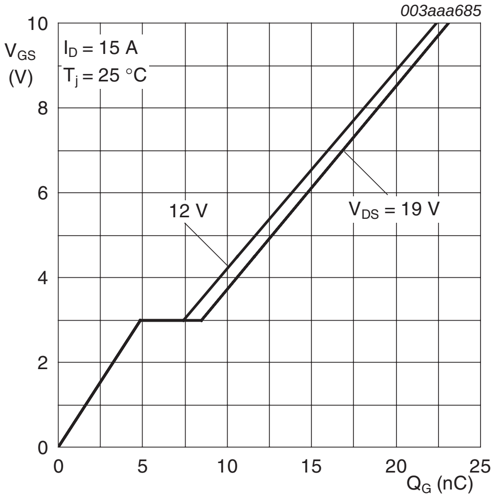
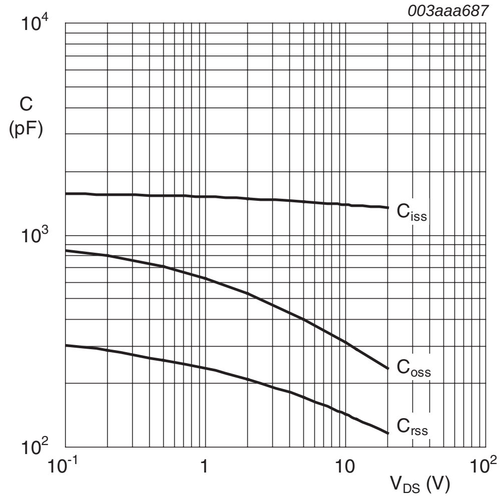


Fig 12. Gate charge waveform definitions



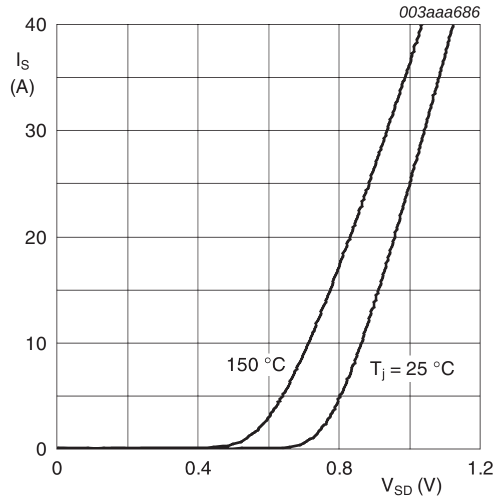
I_D = 15 A; V_{DS} = 12 V and 19 V

Fig 13. Gate-source voltage as a function of gate charge; typical values



V_{GS} = 0 V; f = 1 MHz

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

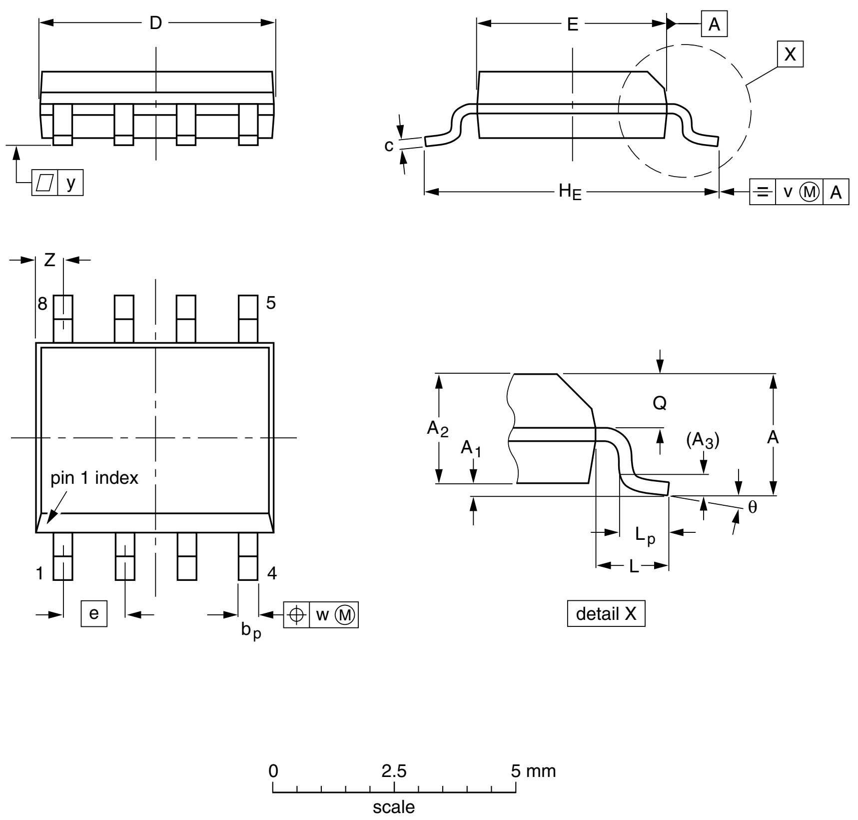


T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHK18NQ03LT v.3	20110317	Product data sheet	-	PHK18NQ03LT v.2
Modifications:	• Various changes to content.			
PHK18NQ03LT v.2	20101221	Product data sheet	-	PHK18NQ03LT v.1

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

11. Contents