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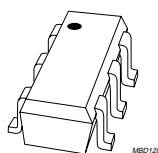
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Kind regards,

Team Nexperia



# PMGD400UN

Dual N-channel  $\mu$ TrenchMOS™ ultra low level FET

Rev. 01 — 3 March 2004

Product data

## 1. Product profile

### 1.1 Description

Dual N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

### 1.2 Features

- Surface mounted package
- Dual device
- Low on-state resistance
- Footprint 40% smaller than SOT23
- Fast switching
- Low threshold voltage.

### 1.3 Applications

- Driver circuits
- Switching in portable appliances.

### 1.4 Quick reference data

- $V_{DS} \leq 30$  V
- $I_D \leq 0.71$  A
- $P_{tot} \leq 0.41$  W
- $R_{DSon} \leq 480$  m $\Omega$ .

## 2. Pinning information

Table 1: Pinning - SOT363 (SC-88), simplified outline and symbol

| Pin | Description | Simplified outline     | Symbol        |
|-----|-------------|------------------------|---------------|
| 1   | source (s1) | <p>Top view MSA370</p> | <p>MSD901</p> |
| 2   | gate (g1)   |                        |               |
| 3   | drain (d2)  |                        |               |
| 4   | source (s2) |                        |               |
| 5   | gate (g2)   |                        |               |
| 6   | drain (d1)  |                        |               |

**SOT363 (SC-88)**



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### 3. Ordering information

**Table 2: Ordering information**

| Type number | Package |  | Version |
|-------------|---------|--|---------|
|             | Name    | Description                              |         |
| PMGD400UN   | SC-88   | Plastic surface mounted package; 6 leads | SOT363  |

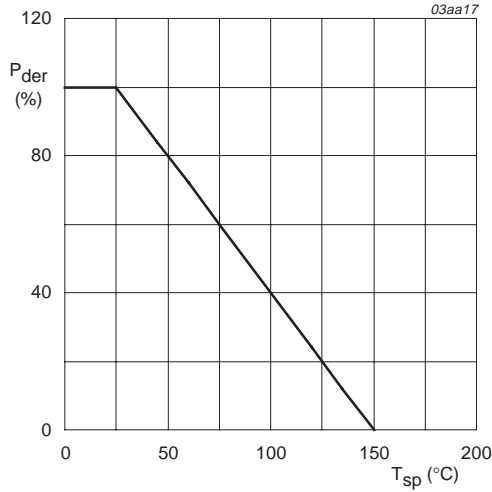
### 4. Limiting values

**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

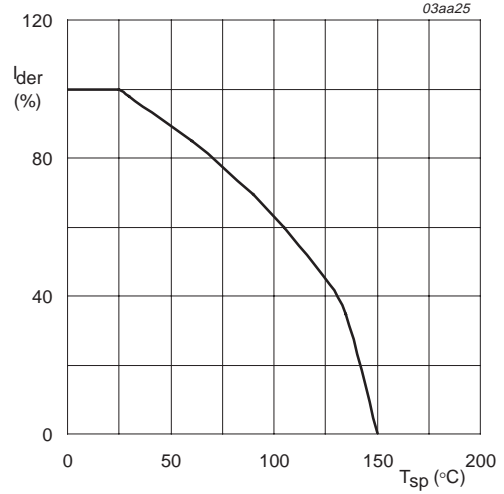
| Symbol                    | Parameter                           | Conditions   | Min   | Max     | Unit |
|---------------------------|-------------------------------------|--|-------|---------|------|
| $V_{DS}$                  | drain-source voltage (DC)           | $25\text{ °C} \leq T_j \leq 150\text{ °C}$   | -     | 30      | V    |
| $V_{DGR}$                 | drain-gate voltage (DC)             | $25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$            | -     | 30      | V    |
| $V_{GS}$                  | gate-source voltage (DC)            |  | -     | $\pm 8$ | V    |
| $I_D$                     | drain current (DC)                  | $T_{sp} = 25\text{ °C}$ ; $V_{GS} = 4.5\text{ V}$ ; <b>Figure 2 and 3</b>            | [1] - | 0.71    | A    |
|                           |                                     | $T_{sp} = 100\text{ °C}$ ; $V_{GS} = 4.5\text{ V}$ ; <b>Figure 2</b>                 | [1] - | 0.45    | A    |
| $I_{DM}$                  | peak drain current                  | $T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <b>Figure 3</b> | [1] - | 1.42    | A    |
| $P_{tot}$                 | total power dissipation             | $T_{sp} = 25\text{ °C}$ ; <b>Figure 1</b>  | -     | 0.41    | W    |
| $T_{stg}$                 | storage temperature                 |  | -55   | +150    | °C   |
| $T_j$                     | junction temperature                |  | -55   | +150    | °C   |
| <b>Source-drain diode</b> |                                     |  |       |         |      |
| $I_S$                     | source (diode forward) current (DC) | $T_{sp} = 25\text{ °C}$  | [1] - | 0.34    | A    |
| $I_{SM}$                  | peak source (diode forward) current | $T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$                   | [1] - | 0.69    | A    |

[1] Single device conducting.



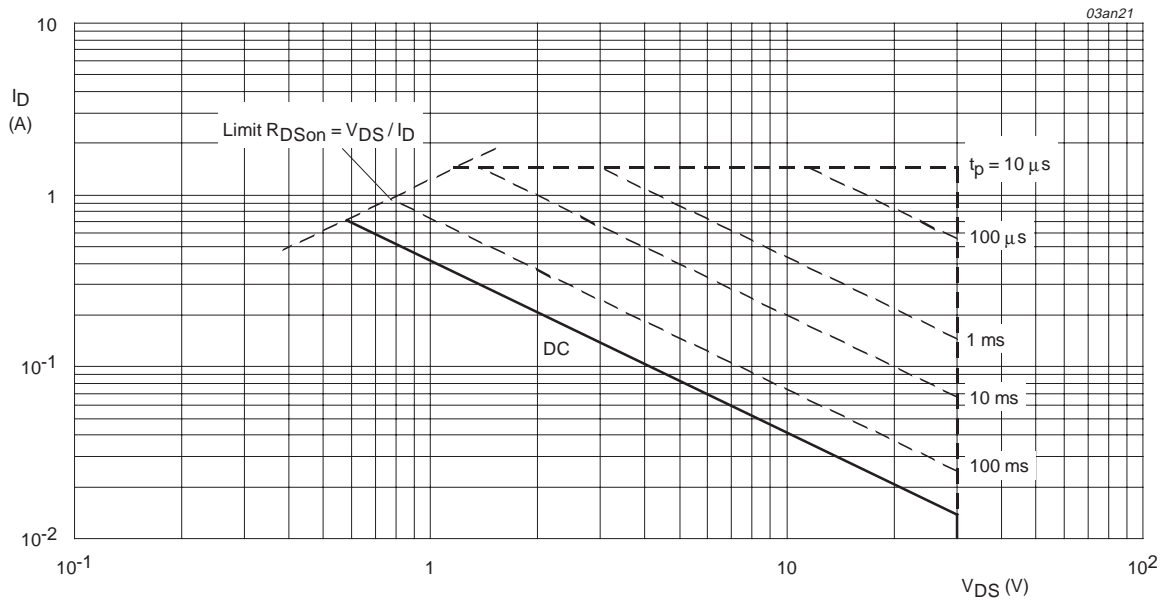
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T<sub>sp</sub> = 25 °C; I<sub>DM</sub> is single pulse; V<sub>GS</sub> = 4.5 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 5. Thermal characteristics

Table 4: Thermal characteristics

| Symbol         | Parameter  | Conditions | Min | Typ | Max | Unit |
|----------------|--|------------|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | Figure 4   | -   | -   | 300 | K/W  |

### 5.1 Transient thermal impedance

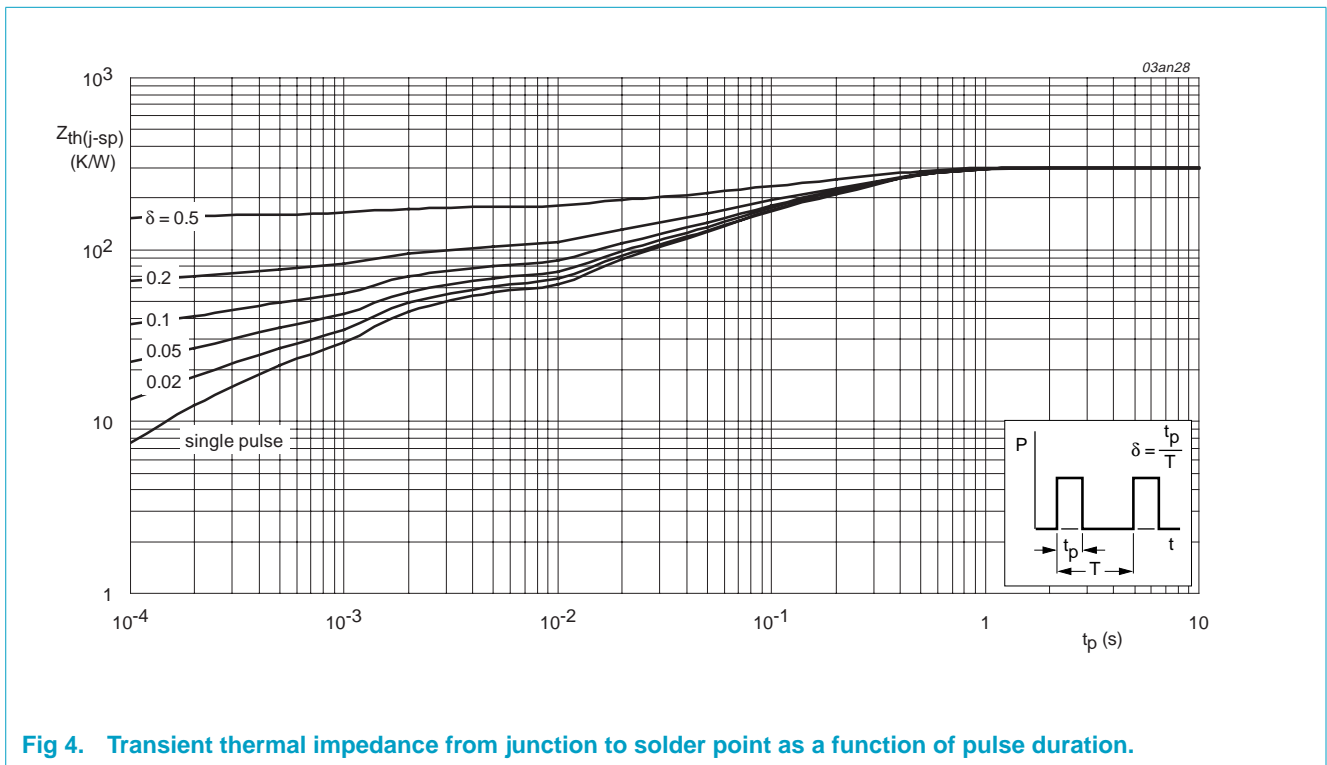


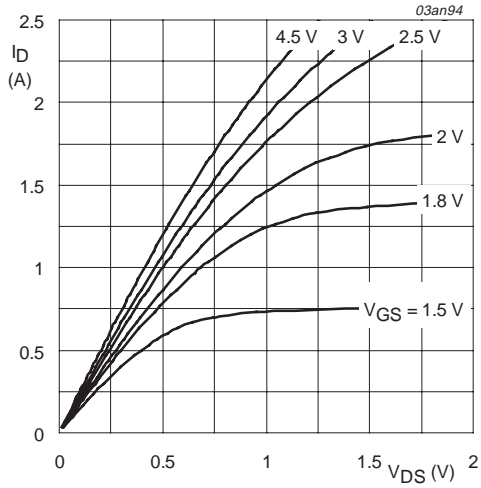
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

## 6. Characteristics

**Table 5: Characteristics**

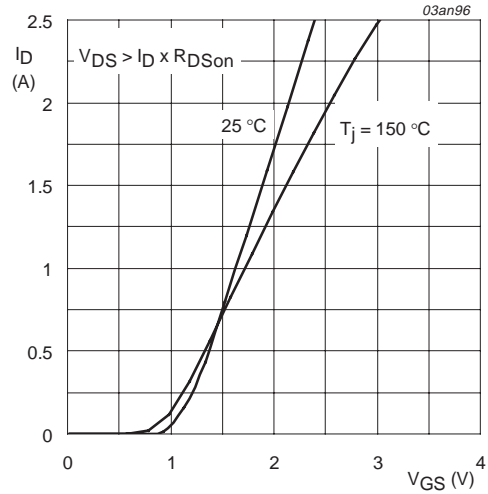
$T_j = 25\text{ °C}$  unless otherwise specified.

| Symbol                         | Parameter                            | Conditions   | Min               | Typ                      | Max                      | Unit   |
|--------------------------------|--------------------------------------|--|-------------------|--------------------------|--------------------------|--|
| <b>Static characteristics</b>  |                                      |  |                   |                          |                          |  |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage       | $I_D = 1\ \mu\text{A}; V_{GS} = 0\ \text{V}$<br>$T_j = 25\text{ °C}$<br>$T_j = -55\text{ °C}$  | 30<br>27          | -<br>-                   | -<br>-                   | V<br>V   |
| $V_{GS(th)}$                   | gate-source threshold voltage        | $I_D = 0.25\ \text{mA}; V_{DS} = V_{GS}$ ; <b>Figure 9</b><br>$T_j = 25\text{ °C}$<br>$T_j = 150\text{ °C}$<br>$T_j = -55\text{ °C}$   | 0.45<br>0.25<br>- | 0.7<br>-<br>-            | 1<br>-<br>1.2            | V<br>V<br>V  |
| $I_{DSS}$                      | drain-source leakage current         | $V_{DS} = 30\ \text{V}; V_{GS} = 0\ \text{V}$<br>$T_j = 25\text{ °C}$<br>$T_j = 150\text{ °C}$   | -<br>-<br>-       | -<br>-<br>-              | 1<br>100                 | $\mu\text{A}$<br>$\mu\text{A}$                       |
| $I_{GSS}$                      | gate-source leakage current          | $V_{GS} = \pm 8\ \text{V}; V_{DS} = 0\ \text{V}$   | -                 | 10                       | 100                      | nA   |
| $R_{DS(on)}$                   | drain-source on-state resistance     | $V_{GS} = 4.5\ \text{V}; I_D = 0.2\ \text{A}$ ; <b>Figure 7 and 8</b><br>$T_j = 25\text{ °C}$<br>$T_j = 150\text{ °C}$<br>$V_{GS} = 2.5\ \text{V}; I_D = 0.1\ \text{A}$ ; <b>Figure 7 and 8</b><br>$V_{GS} = 1.8\ \text{V}; I_D = 0.075\ \text{A}$ ; <b>Figure 7 and 8</b> | -<br>-<br>-<br>-  | 400<br>660<br>480<br>580 | 480<br>816<br>580<br>830 | m $\Omega$<br>m $\Omega$<br>m $\Omega$<br>m $\Omega$ |
| <b>Dynamic characteristics</b> |                                      |  |                   |                          |                          |  |
| $Q_{g(tot)}$                   | total gate charge                    | $I_D = 1\ \text{A}; V_{DD} = 15\ \text{V}; V_{GS} = 4.5\ \text{V}$ ;<br><b>Figure 13</b>   | -                 | 0.89                     | -                        | nC   |
| $Q_{gs}$                       | gate-source charge                   |  | -                 | 0.1                      | -                        | nC   |
| $Q_{gd}$                       | gate-drain (Miller) charge           |  | -                 | 0.2                      | -                        | nC   |
| $C_{iss}$                      | input capacitance                    | $V_{GS} = 0\ \text{V}; V_{DS} = 25\ \text{V}; f = 1\ \text{MHz}$ ;<br><b>Figure 11</b>   | -                 | 43                       | -                        | pF   |
| $C_{oss}$                      | output capacitance                   |  | -                 | 7.7                      | -                        | pF   |
| $C_{rss}$                      | reverse transfer capacitance         |  | -                 | 4.8                      | -                        | pF   |
| $t_{d(on)}$                    | turn-on delay time                   | $V_{DD} = 15\ \text{V}; R_L = 15\ \Omega$ ;<br>$V_{GS} = 4.5\ \text{V}; R_G = 6\ \Omega$   | -                 | 4                        | -                        | ns   |
| $t_r$                          | rise time                            |  | -                 | 7.5                      | -                        | ns   |
| $t_{d(off)}$                   | turn-off delay time                  |  | -                 | 18                       | -                        | ns   |
| $t_f$                          | fall time                            |  | -                 | 4.5                      | -                        | ns   |
| <b>Source-drain diode</b>      |                                      |  |                   |                          |                          |  |
| $V_{SD}$                       | source-drain (diode forward) voltage | $I_S = 0.3\ \text{A}; V_{GS} = 0\ \text{V}$ ; <b>Figure 12</b>   | -                 | 0.76                     | 1.2                      | V  |



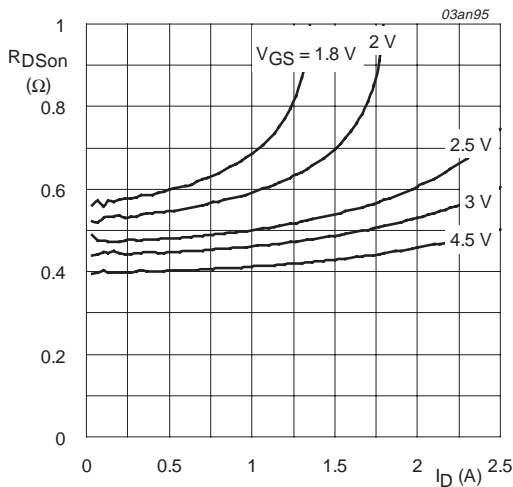
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



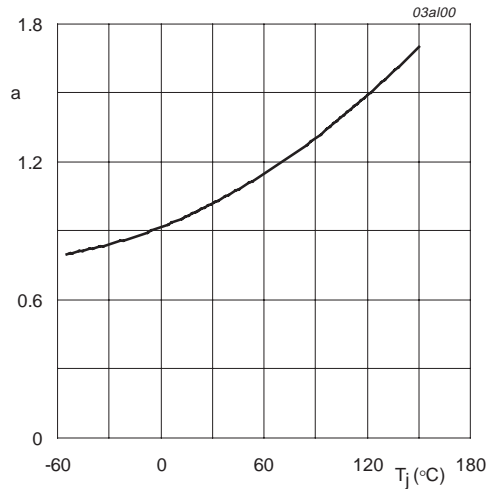
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



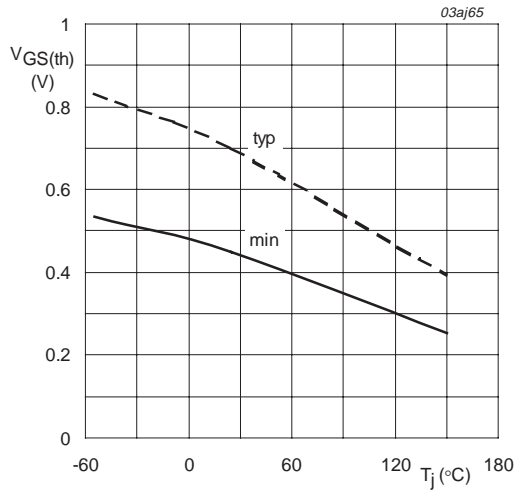
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



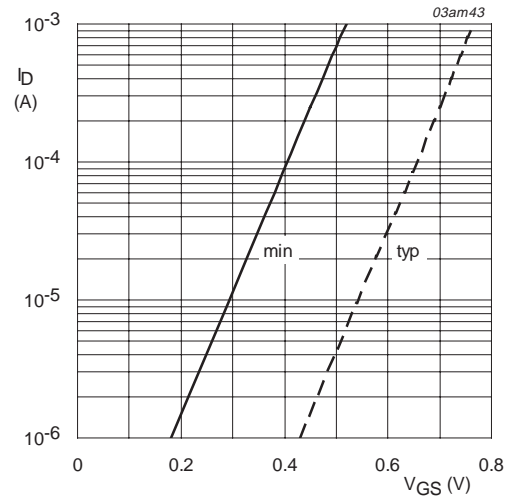
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



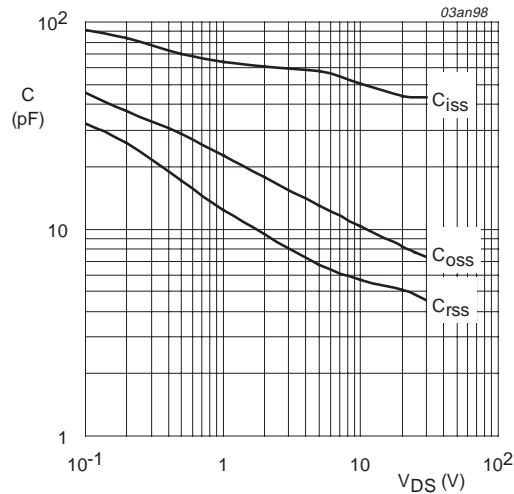
$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

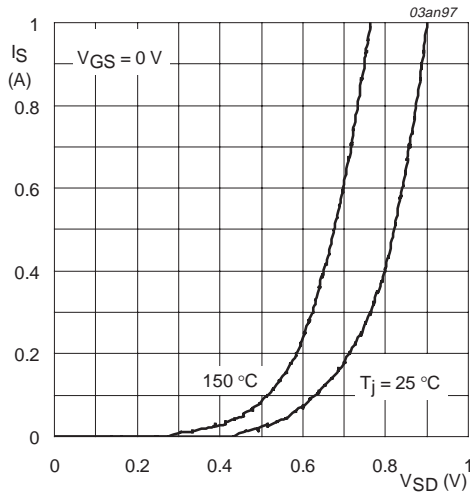
Fig 10. Sub-threshold drain current as a function of gate-source voltage.



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

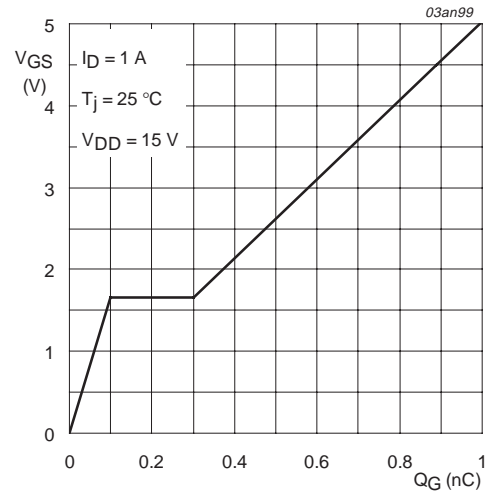
Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.





$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 1\text{ A}$ ;  $V_{DD} = 15\text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**

7. Package outline

Plastic surface mounted package; 6 leads

SOT363

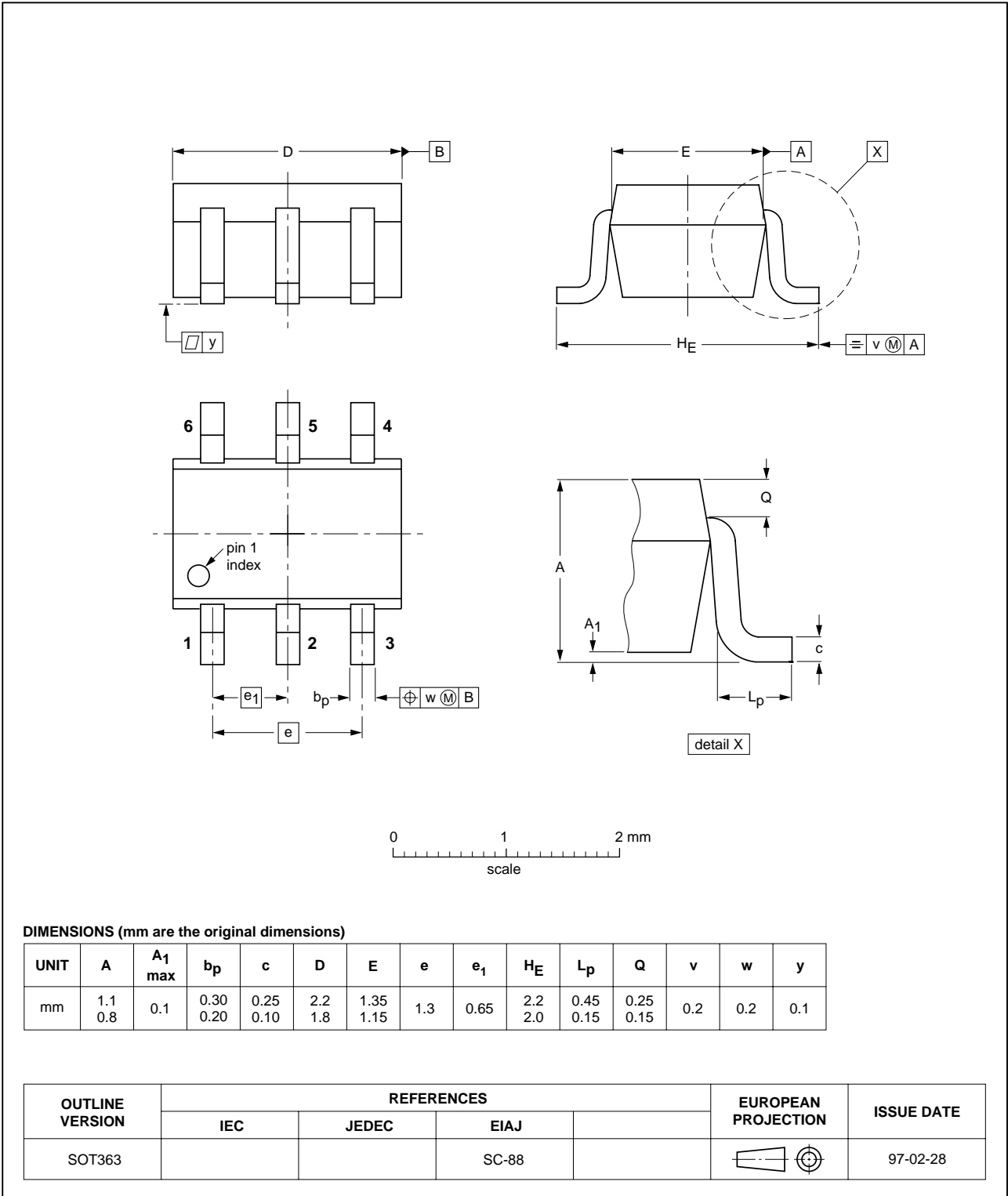
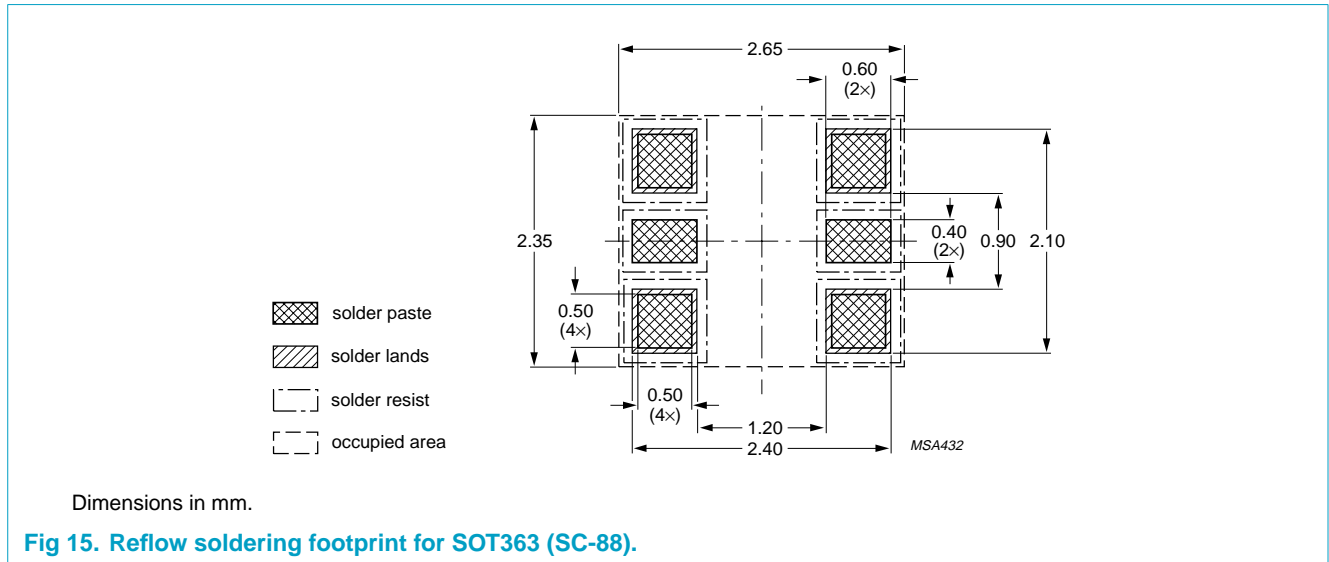


Fig 14. SOT363 (SC-88).

## 8. Soldering



## 9. Revision history

Table 6: Revision history

| Rev | Date     | CPCN | Description                   |
|-----|----------|------|-------------------------------|
| 01  | 20040303 | -    | Product data (9397 750 12759) |

## 10. Data sheet status

| Level | Data sheet status <sup>[1]</sup> | Product status <sup>[2][3]</sup> | Definition   |
|-------|----------------------------------|----------------------------------|--|
| I     | Objective data                   | Development                      | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
| II    | Preliminary data                 | Qualification                    | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.             |
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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