



# PSMN2R3-100SSE

N-channel 100 V, 2.3 mOhm MOSFET with enhanced SOA in LFPAK88

7 September 2021

Preliminary data sheet

## 1. General description

N-channel enhancement mode MOSFET in a LFPAK88 package qualified to 175 °C. Part of Nexperia's "ASFETs for hotswap" portfolio, the PSMN2R3-100SSE delivers very low  $R_{DSon}$  and a very strong linear-mode (SOA) performance in a high-reliability copper-clip LFPAK88 package.

PSMN2R3-100SSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn-on, low  $R_{DSon}$  to minimize  $I^2R$  losses and deliver optimum efficiency when turned fully ON.

## 2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low  $R_{DSon}$  for low  $I^2R$  conduction losses
- LFPAK88 package for applications that demand the highest performance and reliability

## 3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	255	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	341	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	-	1.8	2.28	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 100\text{ °C}$ ; <a href="#">Fig. 12</a>	-	2.9	3.6	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 50\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 13</a>	8	27	62	nC
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$ ; $V_{DS} = 50\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 13</a>	80	161	242	nC

## N-channel 100 V, 2.3 mOhm MOSFET with enhanced SOA in LFPAK88

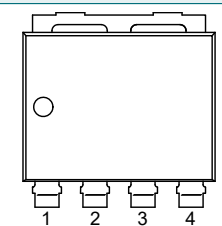
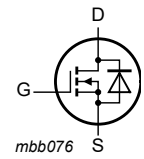
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 82\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; unclamped; $t_p = 137\ \mu\text{s}$ ; <a href="#">Fig. 4</a>	[1]	-	-	732 mJ
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 50\text{ V}$ ; <a href="#">Fig. 18</a>	[2]	-	68	nC

[1] Protected by 100% test

[2] includes capacitive recovery

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LFPAK88 (SOT1235)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R3-100SSE	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R3-100SSE	X2E3S10S

## 8. Limiting values

Table 5. Limiting values

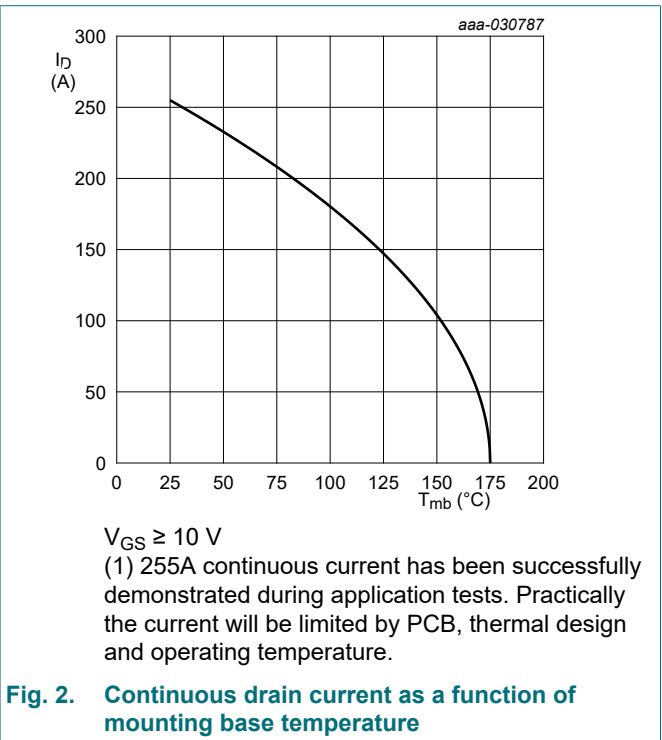
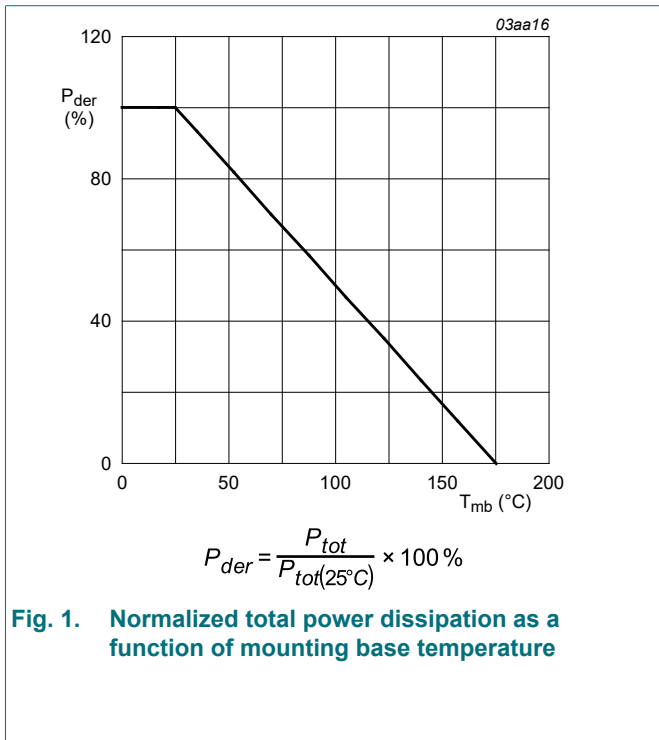
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	341	W

N-channel 100 V, 2.3 mOhm MOSFET with enhanced SOA in LPAK88

Symbol	Parameter	Conditions	Min	Max	Unit
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; Fig. 2	-	255	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; Fig. 2	-	180	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3	-	1020	A
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	255	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	1020	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 82 A; V <sub>sup</sub> ≤ 100 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 137 μs; Fig. 4	[1]	732	mJ
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> ≤ 100 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω; Fig. 4	[1]	82	A

[1] Protected by 100% test



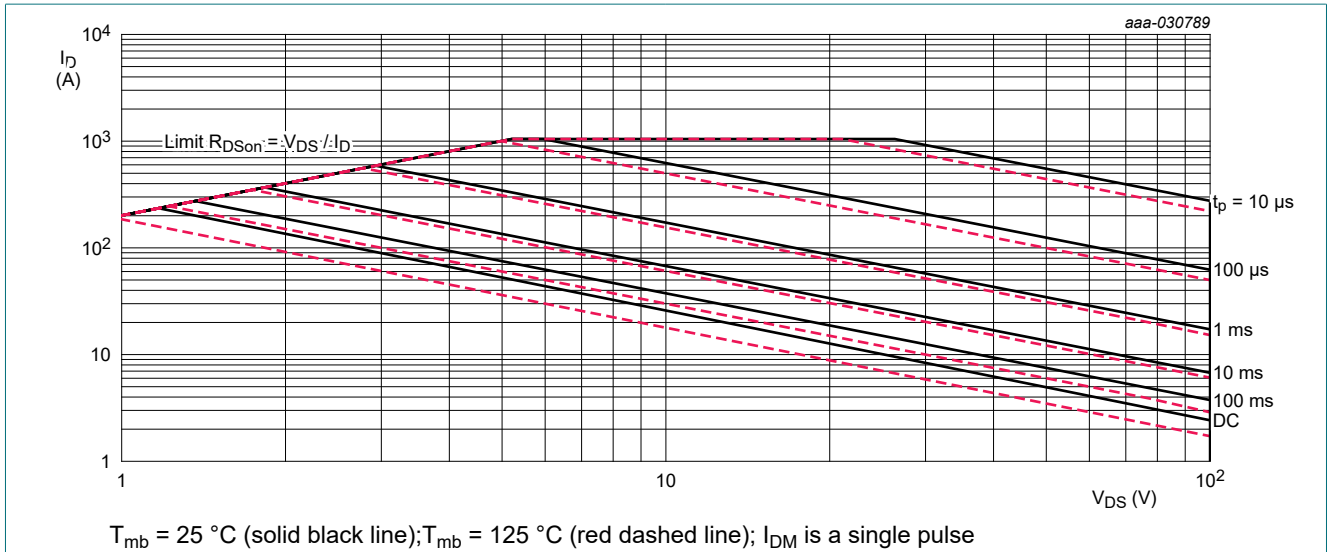


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

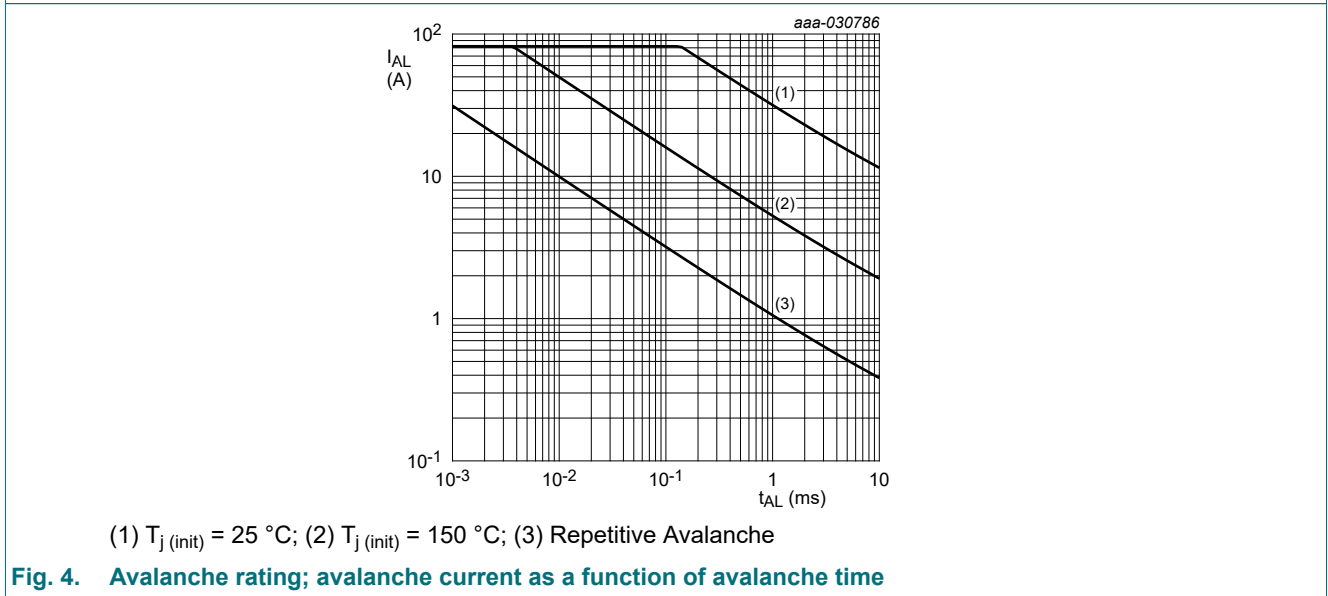


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	0.2	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 6</a>	-	35	-	K/W
		<a href="#">Fig. 7</a>	-	70	-	K/W

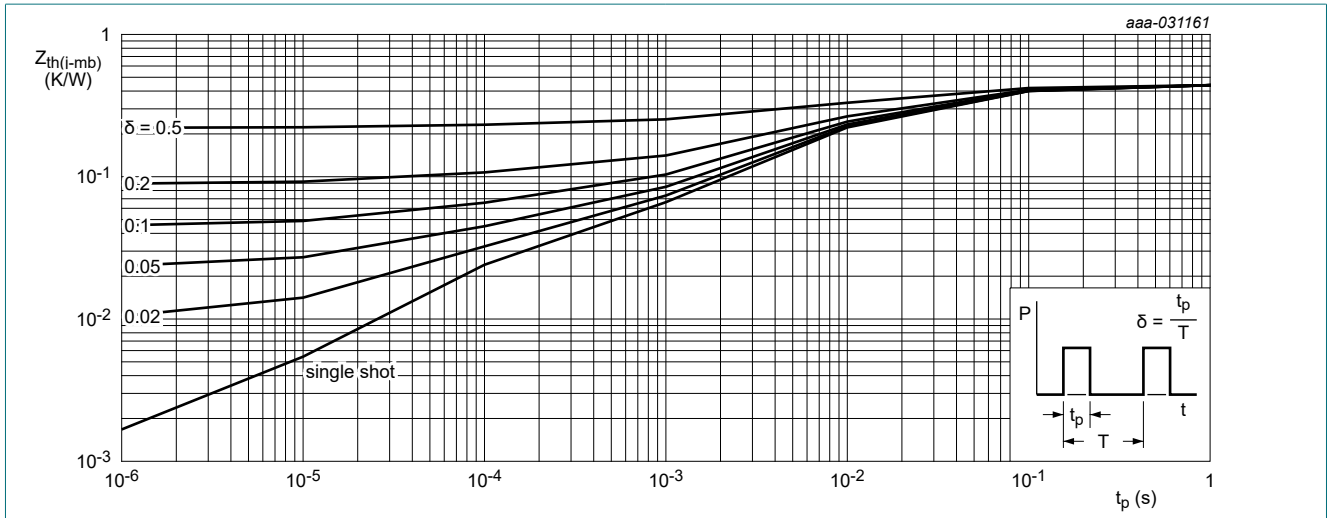


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

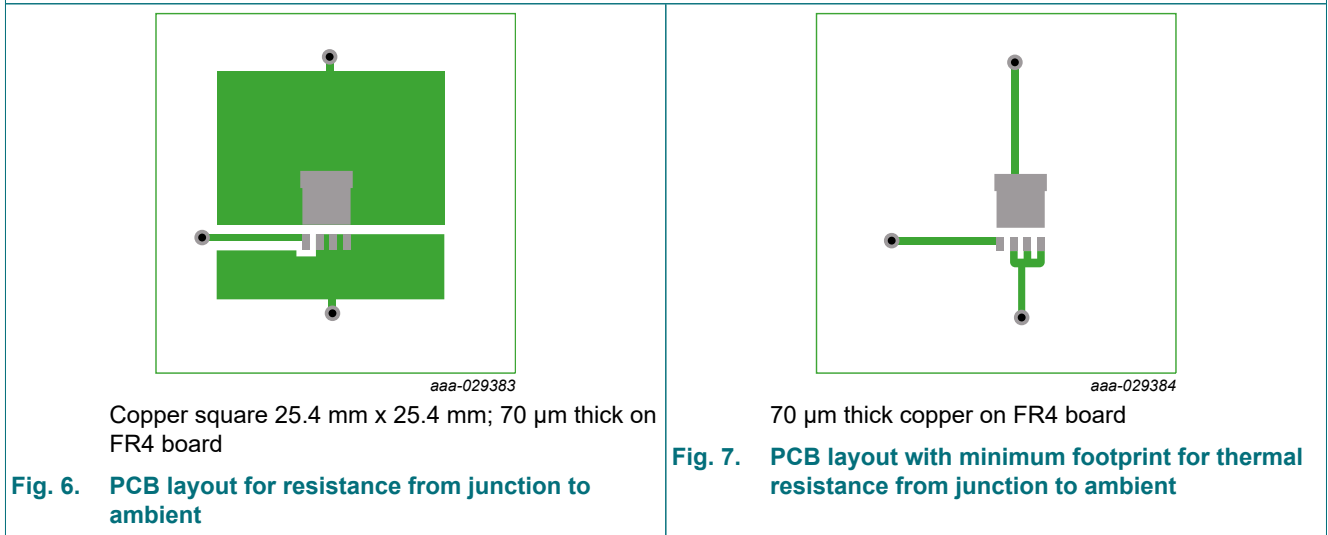


Fig. 6. PCB layout for resistance from junction to ambient

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

## 10. Characteristics

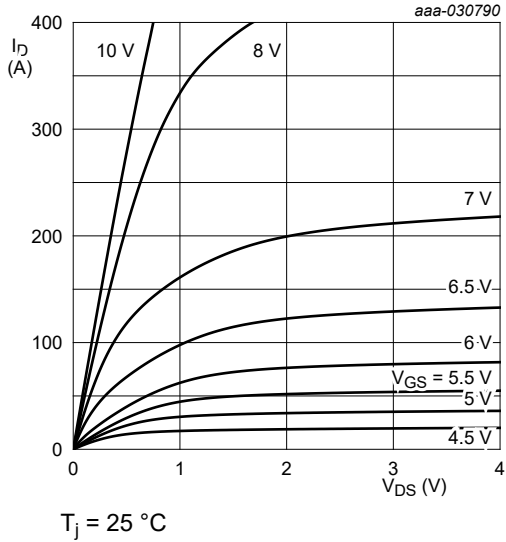
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$	2	2.6	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.6	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-6.2	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.1	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	20	100	μA
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

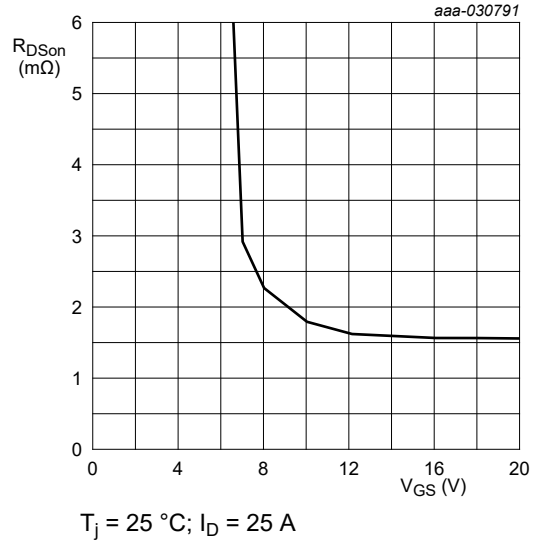
## N-channel 100 V, 2.3 mOhm MOSFET with enhanced SOA in LPAK88

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 11</a>	-	1.8	2.28	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 100 °C; <a href="#">Fig. 12</a>	-	2.9	3.6	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 175 °C; <a href="#">Fig. 12</a>	-	3.7	5.2	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>J</sub> = 25 °C	0.5	1	2	Ω
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 13</a>	80	161	242	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 13</a>	-	84	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 13</a>	32	54	76	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	34	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	20	-	nC
Q <sub>GD</sub>	gate-drain charge		8	27	62	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 13</a>	-	4.7	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>J</sub> = 25 °C; <a href="#">Fig. 16</a>	7380	12300	17200	pF
C <sub>oss</sub>	output capacitance		1600	2670	4300	pF
C <sub>rss</sub>	reverse transfer capacitance		4	36	94	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 50 V; R <sub>L</sub> = 2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω	-	41	-	ns
t <sub>r</sub>	rise time		-	41	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	88	-	ns
t <sub>f</sub>	fall time		-	54	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.8	1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; <a href="#">Fig. 18</a>	-	56	-	ns
Q <sub>r</sub>	recovered charge		[1]	68	-	nC

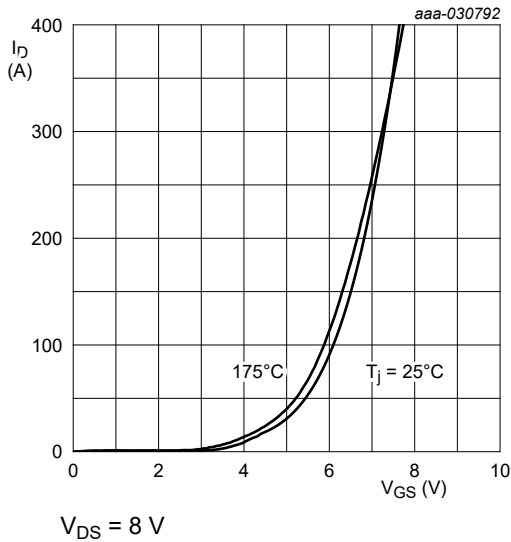
[1] includes capacitive recovery



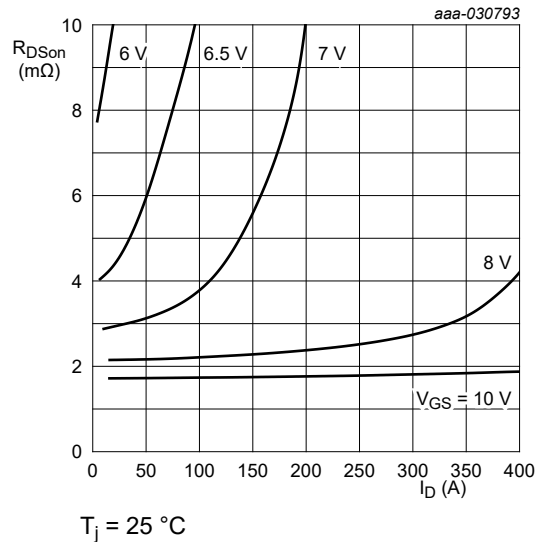
**Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values**



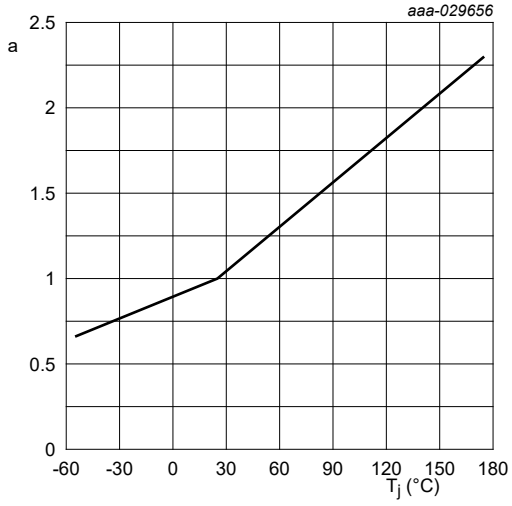
**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



**Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

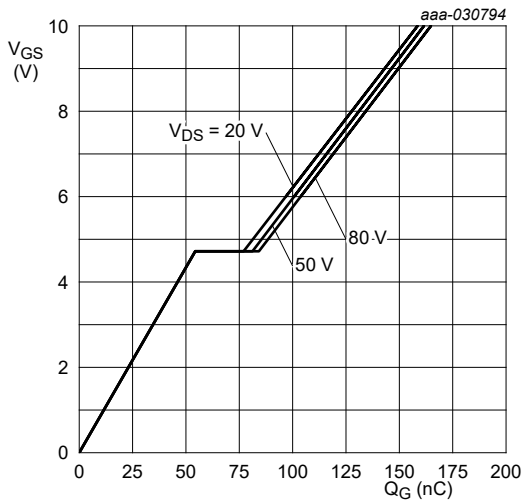


$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

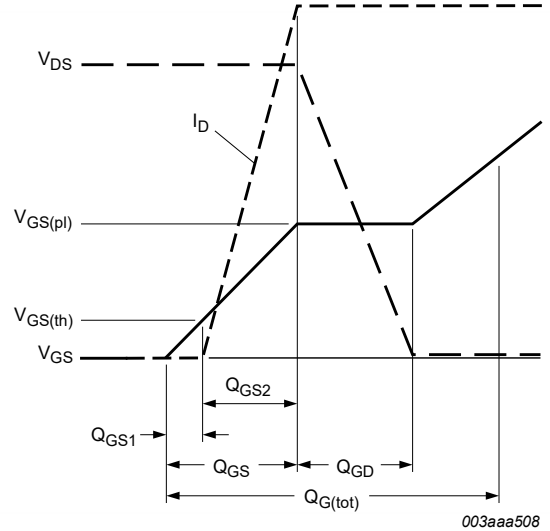


**Fig. 13. Gate charge waveform definitions**



$T_j = 25^\circ C; I_D = 25 A$

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**



**Fig. 15. Gate charge waveform definitions**



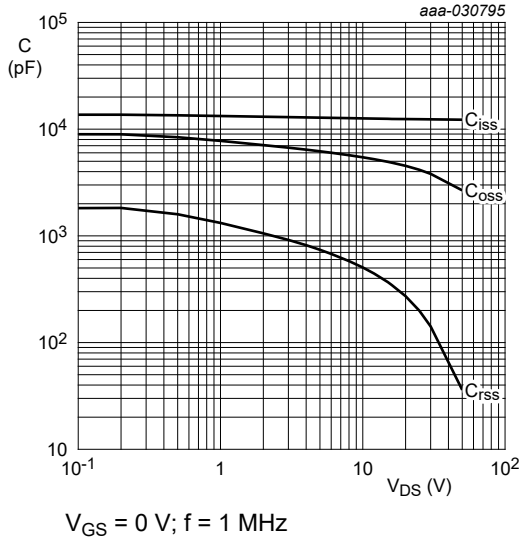


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

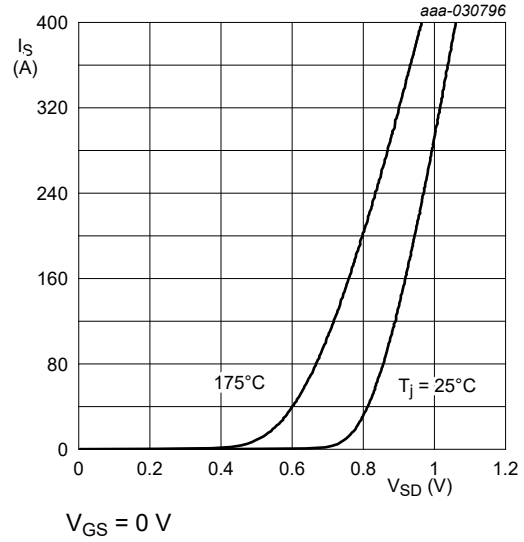


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

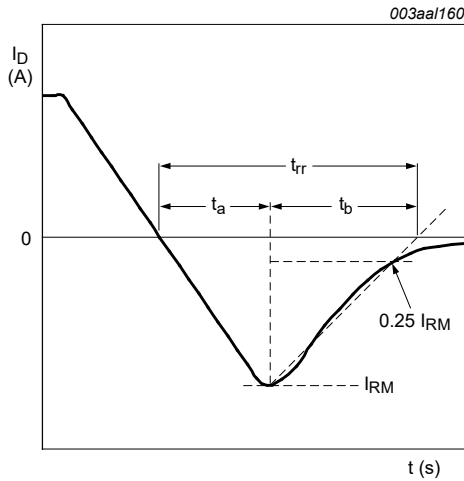


Fig. 18. Reverse recovery timing definition

11. Package outline

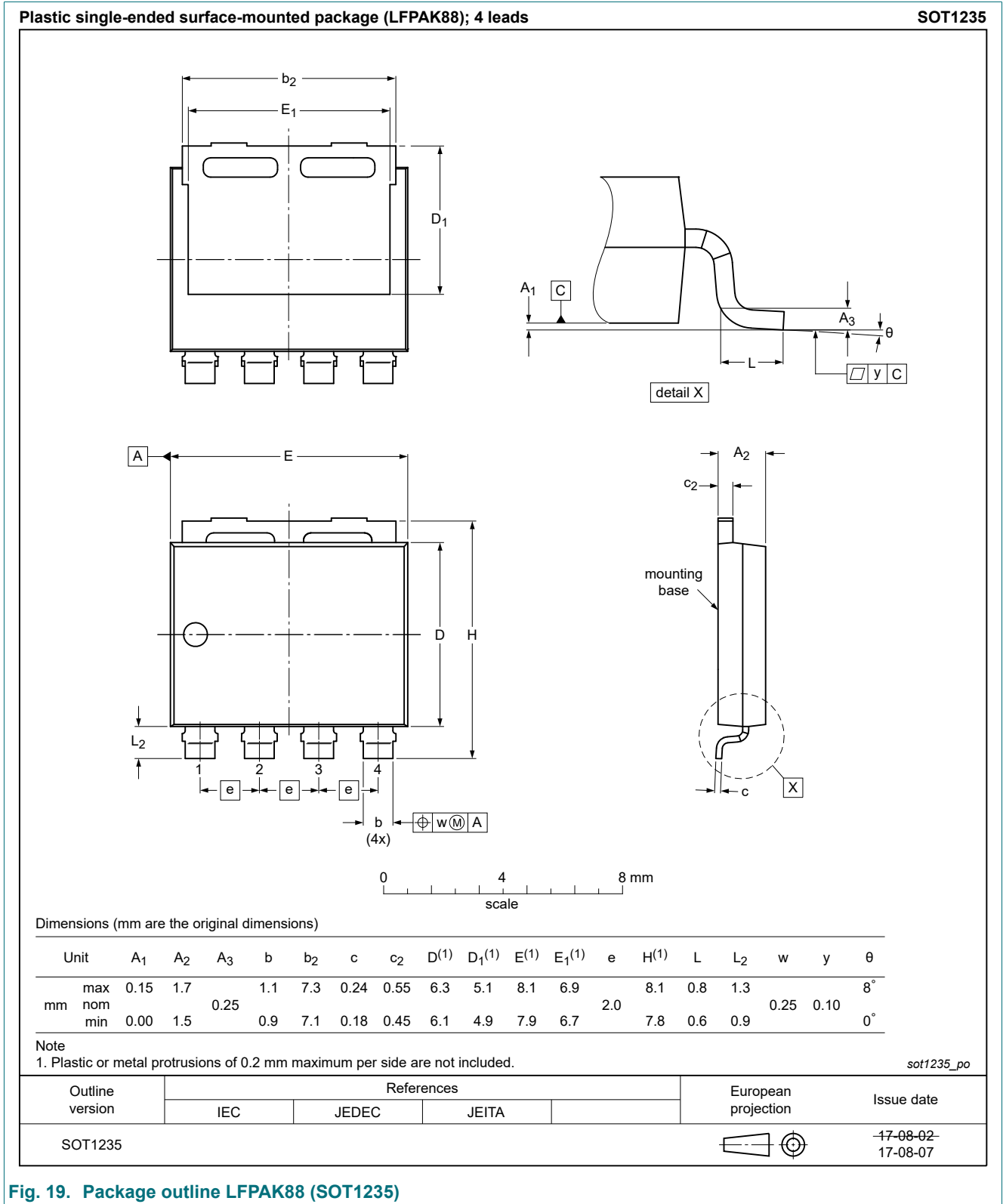
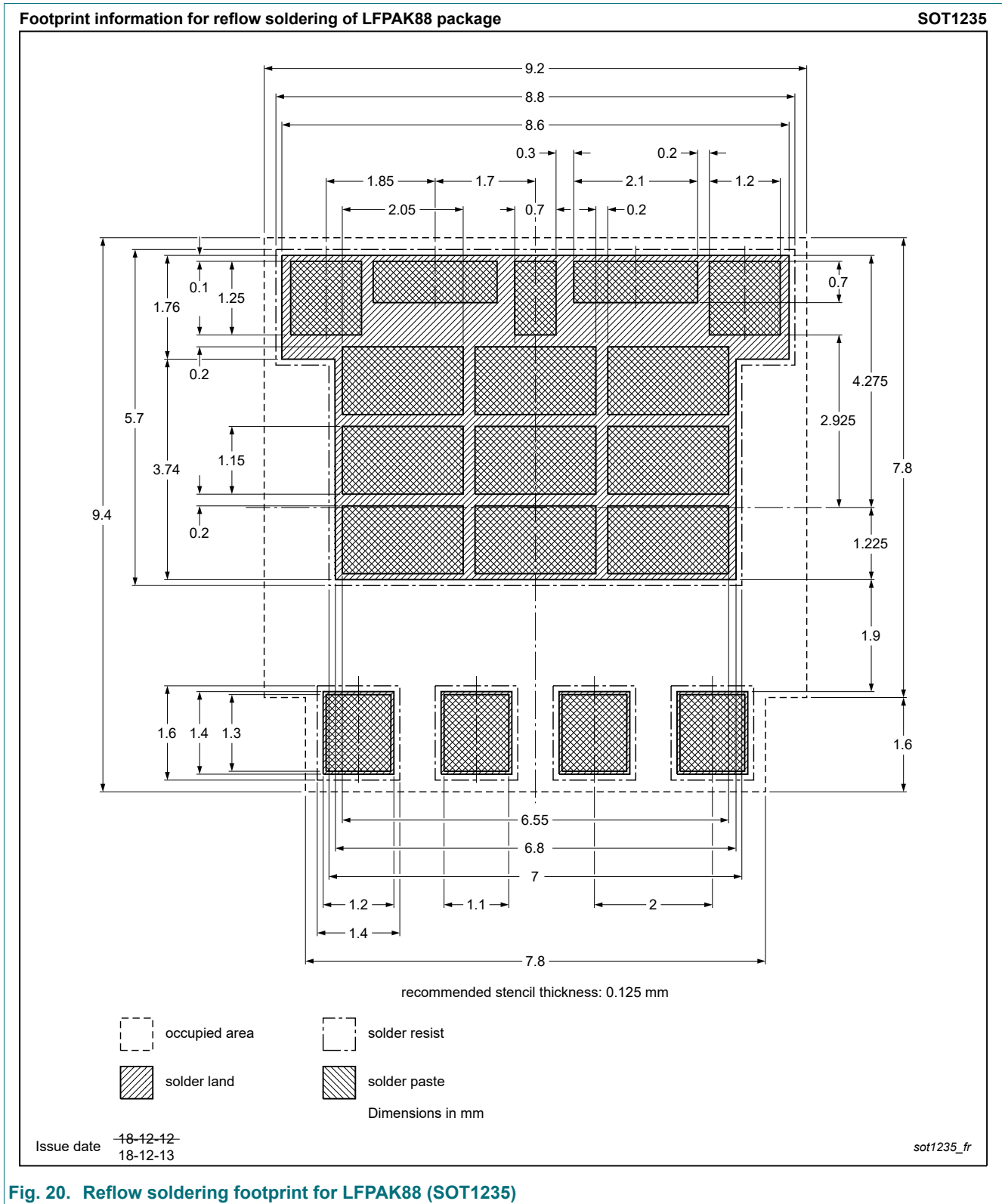


Fig. 19. Package outline LPAK88 (SOT1235)

## 12. Soldering



**Fig. 20. Reflow soldering footprint for LPAK88 (SOT1235)**

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 7 September 2021

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