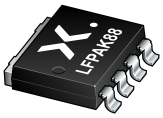



# PSMNR90-50SLH

## N-channel 50 V, 0.90 mOhm, 410 A logic level Application Specific MOSFET in LFPAK88

15 March 2022 Product data sheet

## 1. General description

410 Amp continuous current, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK88 package. Part of the ASFETs for Battery Isolation and DC Motor control family and using Nexperia's unique "SchottkyPlus" technology delivers high efficiency and low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. The ASFET is particularly suited to 36 V battery powered applications requiring strong avalanche capability, linear mode performance, use at high switching frequencies, and also safe and reliable switching at high load-current.

## 2. Features and benefits

- 410 Amp continuous current capability
- LFPAK88 (8 x 8 mm) LFPAK-style low-stress exposed lead-frame for ultimate reliability, optimum soldering and easy solder-joint inspection
- Copper-clip and solder die attach for low package inductance and resistance, and high $I_{D(max)}$ rating
- Ideal replacement for D2PAK and 10 x 12 mm leadless package types
- Qualified to 175 °C
- Avalanche rated, 100 % tested
- Low $Q_G$, $Q_{GD}$ and $Q_{OSS}$ for high efficiency, especially at higher switching frequencies
- Superfast switching with soft body-diode recovery for low-spiking and ringing, recommended for low EMI designs
- Unique "SchottkyPlus" technology for Schottky-like switching performance and low $I_{DSS}$ leakage
- Narrow $V_{GS(th)}$ rating for easy paralleling and improved current sharing
- Very strong linear-mode / safe operating area characteristics for safe and reliable switching at high-current conditions

## 3. Applications

- Brushless DC motor control
- Synchronous rectifier in high-power AC-to-DC applications, e.g. server power supplies
- Battery protection
- eFuse and load switch
- Hotswap / in-rush current management
- 10 cell lithium-ion battery applications (36 V – 42 V)

## 4. Quick reference data

**Table 1. Quick reference data**

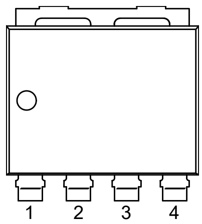
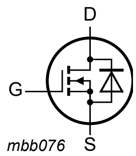
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 50 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | - | 410 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 375 | W |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.7 | 0.9 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.8 | 1.01 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 25 A; $V_{DS}$ = 25 V; $V_{GS}$ = 4.5 V; Fig. 12; Fig. 13 | | - | 26 | 57 | nC |
| $Q_{G(tot)}$ | total gate charge | | | - | 112 | 174 | nC |

[1] 410A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

### Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | G | gate |  LFPAK88 (SOT1235) |  |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | S | source | | |
| mb | D | mounting base; connected to drain | | |

## 6. Ordering information

### Table 3. Ordering information

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMNR90-50SLH | LFPAK88 | plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body | SOT1235 |

## 7. Marking

### Table 4. Marking codes

| Type number | Marking code |
|---|---|
| PSMNR90-50SLH | XH90L50S |

## 8. Limiting values

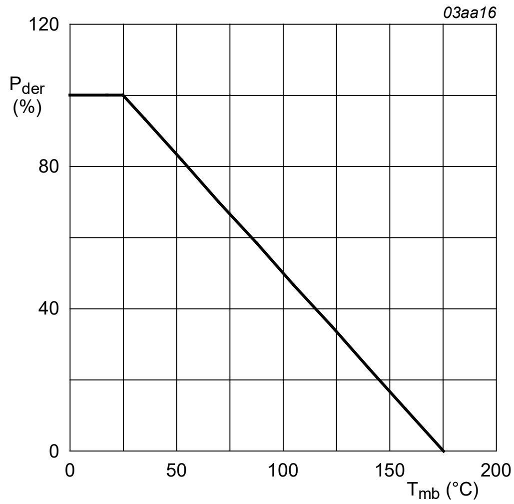
### Table 5. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 50 | V |
| $V_{DGR}$ | drain-gate voltage | 25 °C ≤ $T_j$ ≤ 175 °C; $R_{GS}$ = 20 kΩ | | - | 50 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |

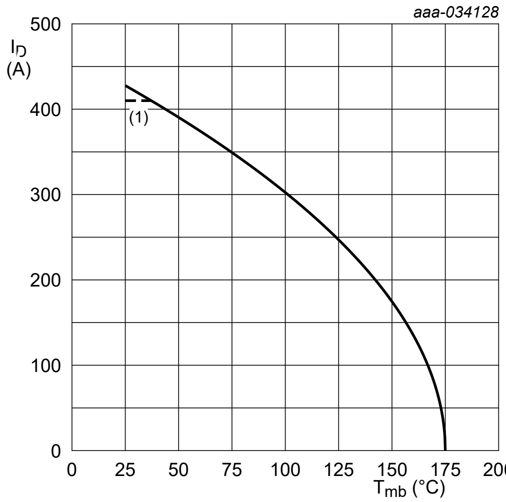
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 375 | W |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | 410 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 2 | | - | 302 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 1711 | A |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | | - | 410 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C | | - | 1711 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 50 A; $V_{sup}$ ≤ 50 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 1.8 ms | [2] | - | 3 | J |
| | | $I_D$ = 25 A; $V_{sup}$ ≤ 50 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 9.1 ms | [2] | - | 7.4 | J |
| $I_{AS}$ | non-repetitive avalanche current | $V_{sup}$ ≤ 50 V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $R_{GS}$ = 50 Ω | [2] | - | 175 | A |

[1] 410A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test



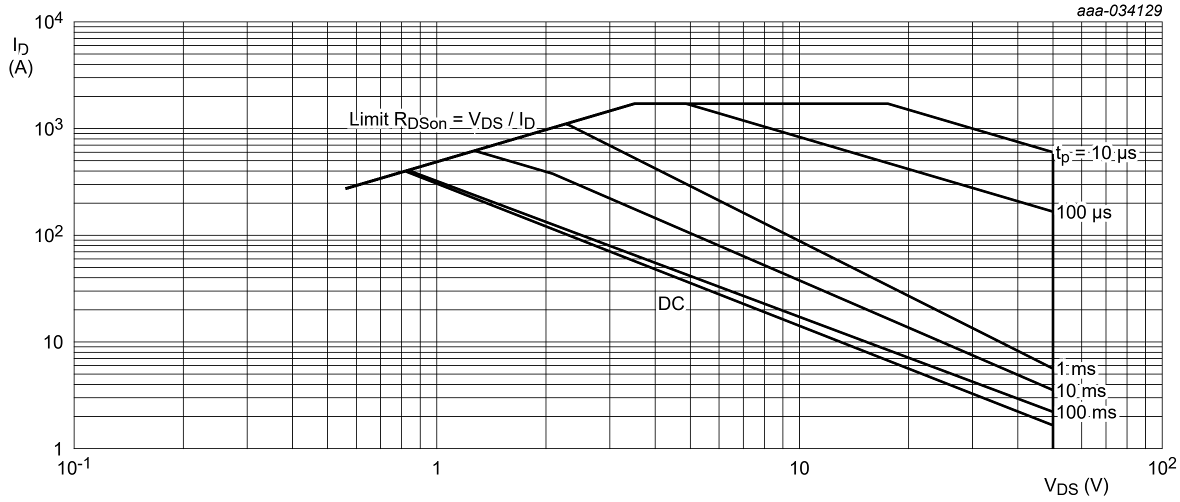

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**




$V_{GS}$ ≥ 10 V
(1) 410A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

**Fig. 2. Continuous drain current as a function of mounting base temperature**




$T_{mb}$ = 25 °C; $I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 4 | | - | 0.35 | 0.4 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 5 | | - | 35 | - | K/W |
| | | Fig. 6 | | - | 70 | - | K/W |

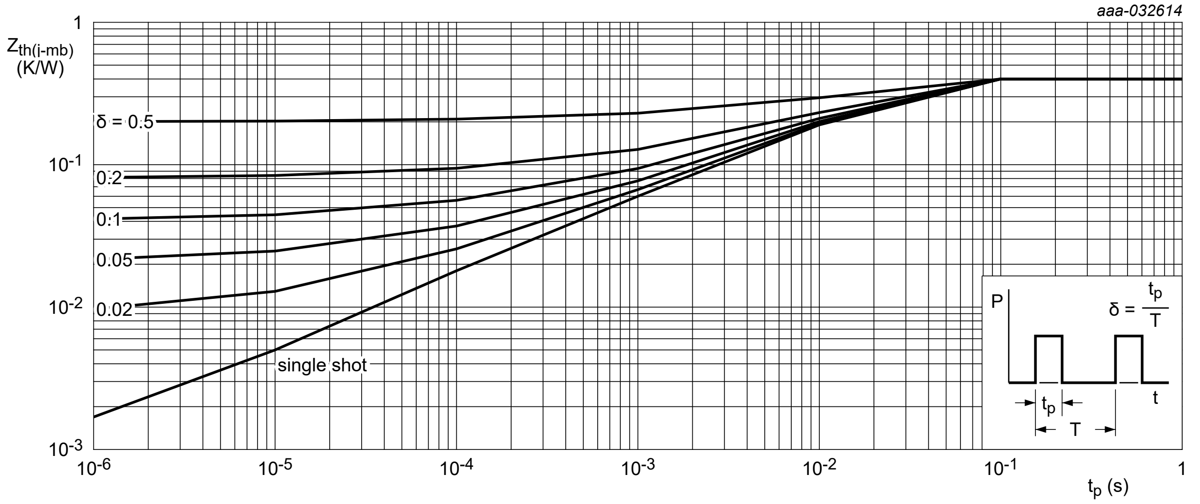
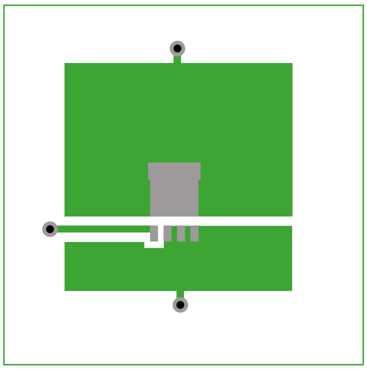
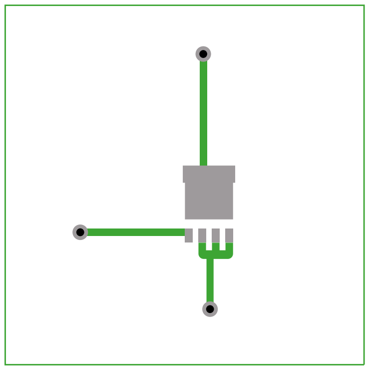



**Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**




Copper square 25.4 mm x 25.4 mm; 70 µm thick on FR4 board

**Fig. 5. PCB layout for resistance from junction to ambient**




70 µm thick copper on FR4 board

**Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient**

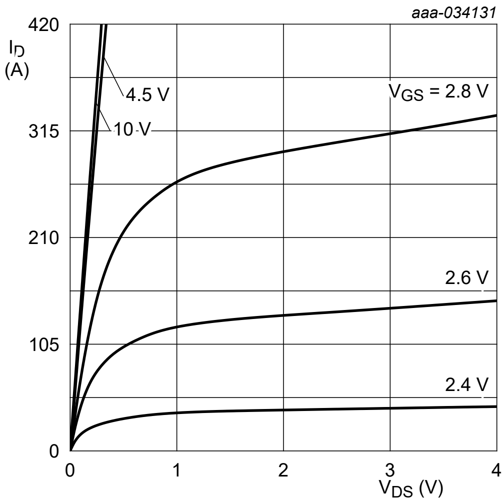
## 10. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 50 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 45 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C | | 1.2 | 1.6 | 2.2 | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | 25 °C ≤ $T_j$ ≤ 150 °C | | - | -4.9 | - | mV/K |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.01 | 1 | µA |
| | | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | 7 | - | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = -16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.7 | 0.9 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 150 °C; Fig. 11 | | - | - | 1.82 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.8 | 1.01 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 150 °C; Fig. 11 | | - | - | 2.03 | mΩ |
| $R_G$ | gate resistance | f = 1 MHz; $T_j$ = 25 °C | | 0.4 | 1 | 2.5 | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 25 V; $V_{GS}$ = 4.5 V; Fig. 12; Fig. 13 | | - | 112 | 174 | nC |
| | | $I_D$ = 25 A; $V_{DS}$ = 25 V; $V_{GS}$ = 10 V; Fig. 12; Fig. 13 | | - | 247 | 383 | nC |
| | | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V | | - | 139 | - | nC |

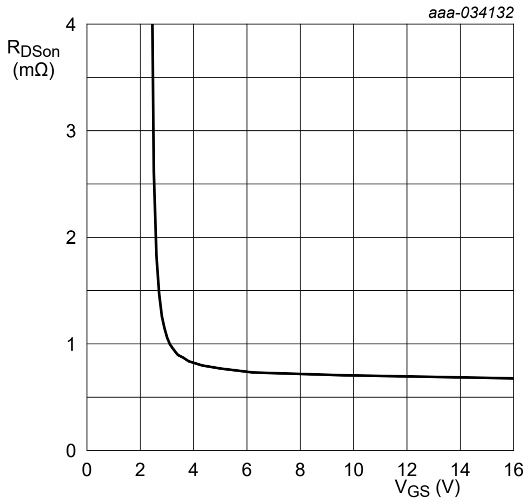
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $Q_{GS}$ | gate-source charge | $I_D$ = 25 A; $V_{DS}$ = 25 V; $V_{GS}$ = 4.5 V; Fig. 12; Fig. 13 | | - | 34 | 51 | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | | - | 24 | 36 | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | | - | 11 | 17 | nC |
| $Q_{GD}$ | gate-drain charge | | | - | 26 | 57 | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 25 A; $V_{DS}$ = 25 V; Fig. 12; Fig. 13 | | - | 2.4 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 25 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 14 | | - | 17829 | 24961 | pF |
| $C_{oss}$ | output capacitance | | | - | 1554 | 2176 | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 485 | 1163 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 25 V; $R_L$ = 1.1 Ω; $V_{GS}$ = 4.5 V; $R_{G(ext)}$ = 5 Ω | | - | 74 | - | ns |
| $t_r$ | rise time | | | - | 66 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 134 | - | ns |
| $t_f$ | fall time | | | - | 55 | - | ns |
| $Q_{oss}$ | output charge | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; $T_j$ = 25 °C | | - | 82 | - | nC |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 15 | | - | 0.73 | 1 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; Fig. 16 | | - | 48 | - | ns |
| $Q_r$ | recovered charge | | [1] | - | 66 | - | nC |
| $t_a$ | reverse recovery rise time | | | - | 29 | - | ns |
| $t_b$ | reverse recovery fall time | | | - | 19 | - | ns |

[1] includes capacitive recovery



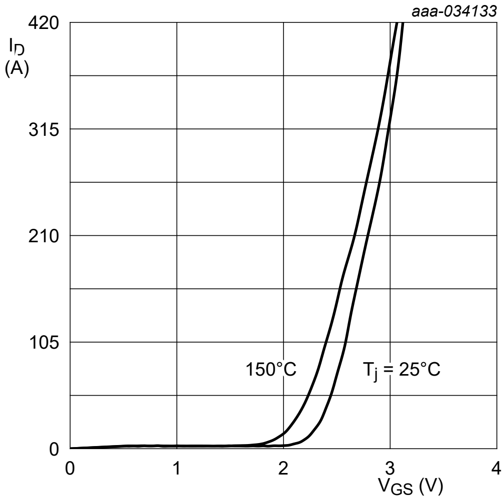

$T_j$ = 25 °C

**Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values**



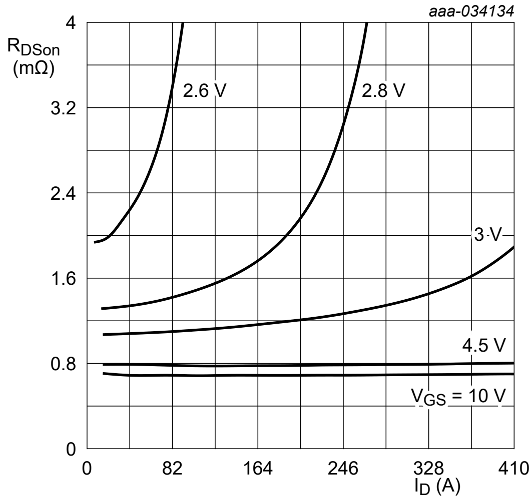

$T_j$ = 25 °C; $I_D$ = 25 A

**Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**



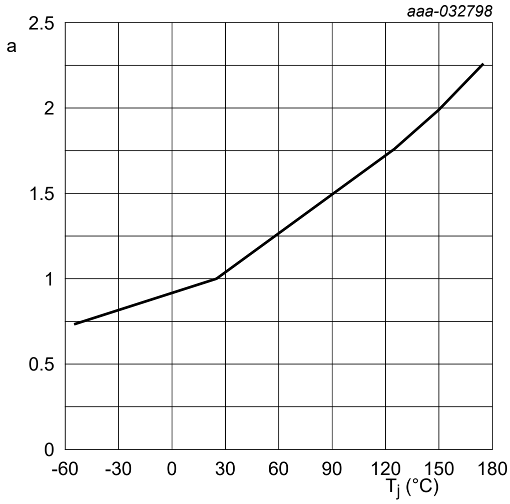

$V_{DS}$ = 8 V

**Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



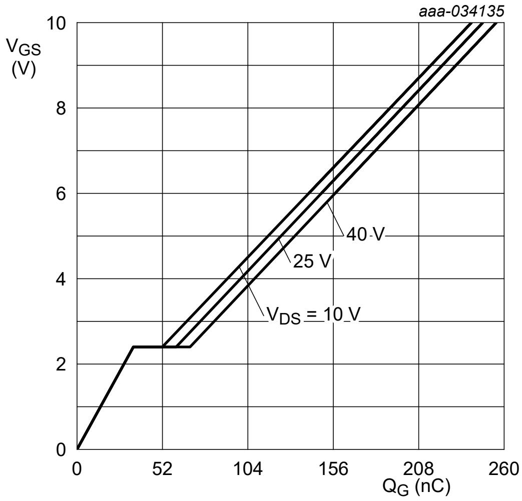

$T_j$ = 25 °C

**Fig. 10. Drain-source on-state resistance as a function of drain current; typical values**




$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

**Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature**




$T_j$ = 25 °C; $I_D$ = 25 A

**Fig. 12. Gate-source voltage as a function of gate charge; typical values**

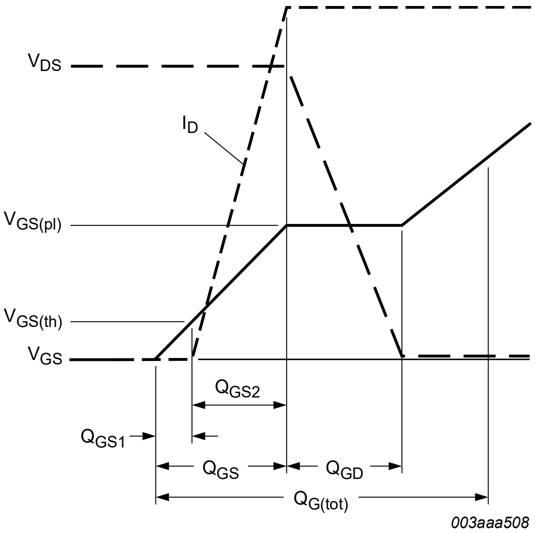



Fig. 13. Gate charge waveform definitions

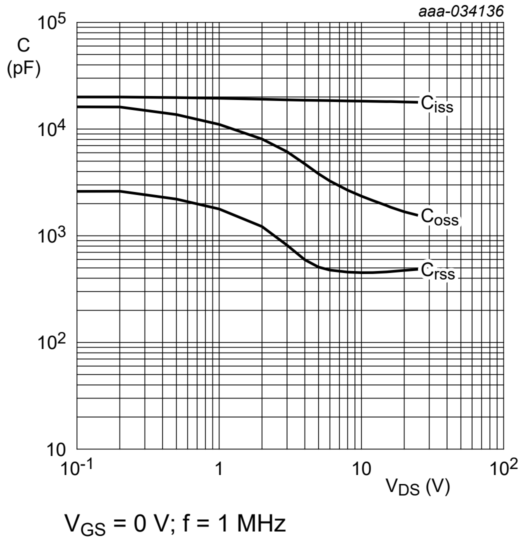



Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

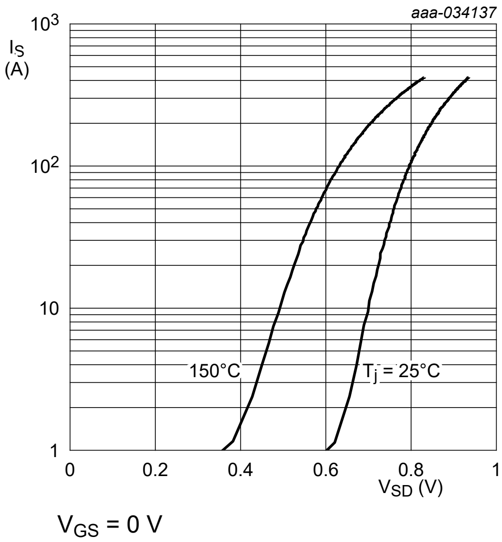



Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

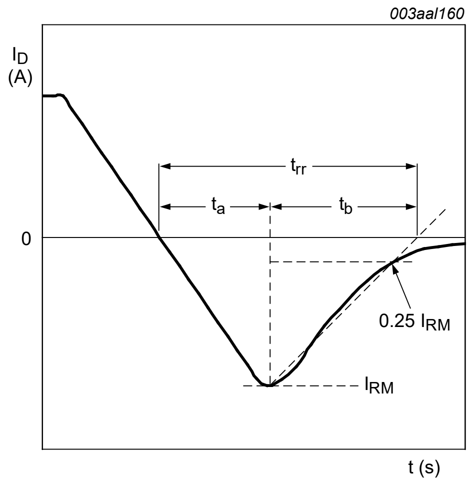
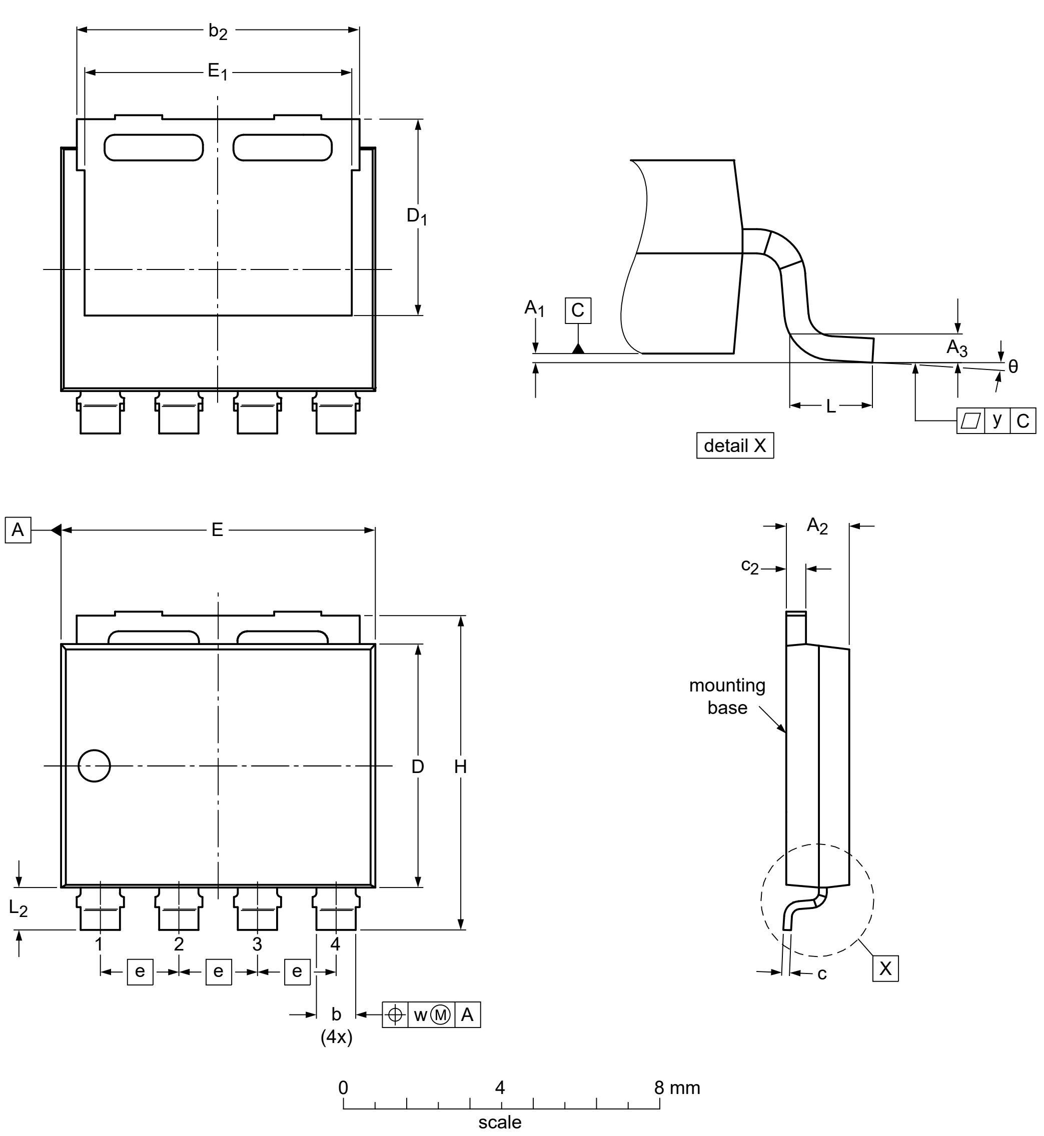



Fig. 16. Reverse recovery timing definition

# 11. Package outline

**Plastic single-ended surface-mounted package (LFPAK88); 4 leads** **SOT1235**




Dimensions (mm are the original dimensions)

| Unit | | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | c | $c_2$ | D(1) | $D_1$(1) | E(1) | $E_1$(1) | e | H(1) | L | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.15 | 1.7 | | 1.1 | 7.3 | 0.24 | 0.55 | 6.3 | 5.1 | 8.1 | 6.9 | | 8.1 | 0.8 | 1.3 | | | 8° |
| | nom | | | 0.25 | | | | | | | | | 2.0 | | | | 0.25 | 0.10 | |
| | min | 0.00 | 1.5 | | 0.9 | 7.1 | 0.18 | 0.45 | 6.1 | 4.9 | 7.9 | 6.7 | | 7.8 | 0.6 | 0.9 | | | 0° |

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

*sot1235_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1235 | | | | | | ~~17-08-02~~<br>17-08-07 |

**Fig. 17. Package outline LFPAK88 (SOT1235)**

## 12. Soldering

**Footprint information for reflow soldering of LFPAK88 package** **SOT1235**

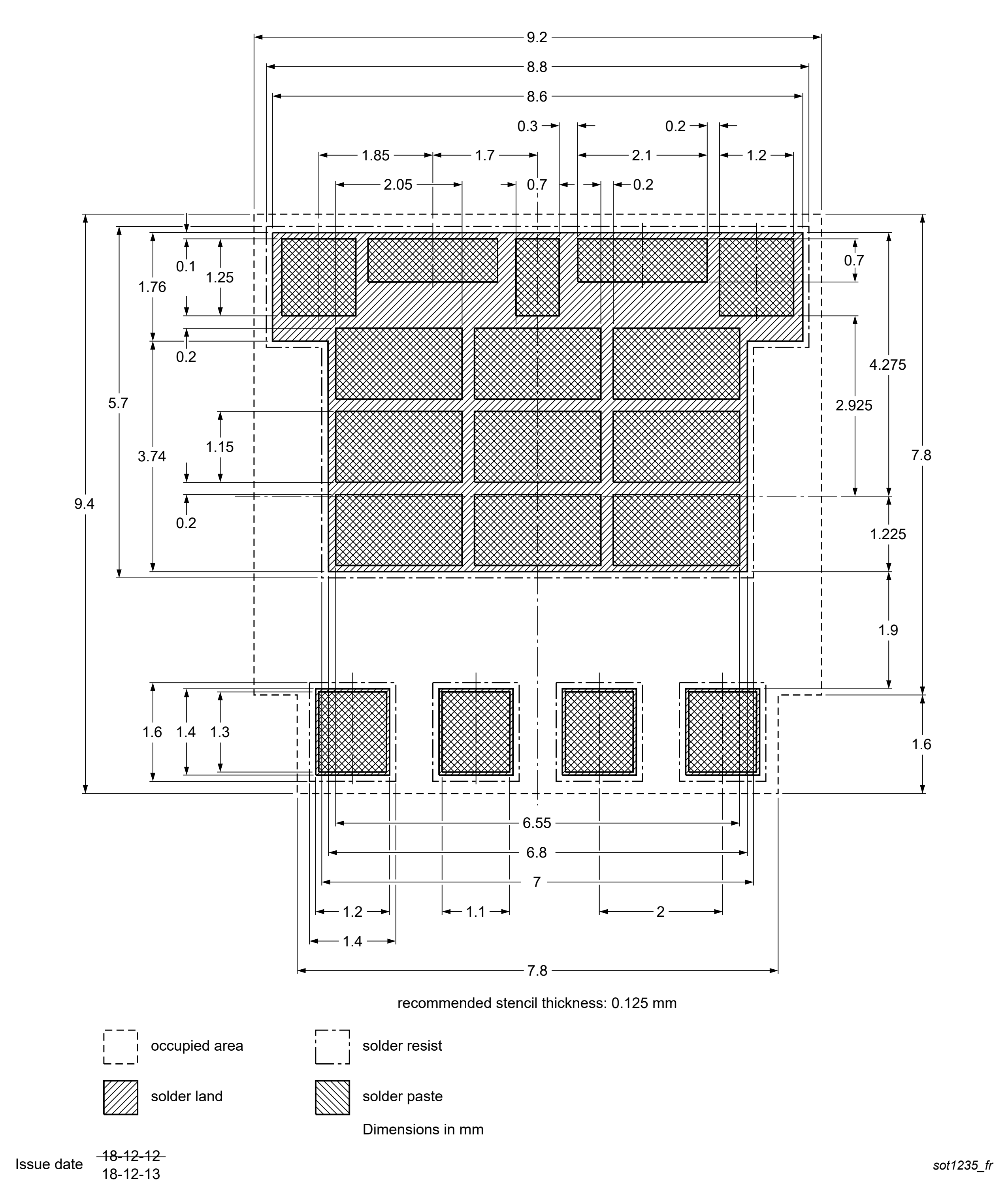



**Fig. 18. Reflow soldering footprint for LFPAK88 (SOT1235)**

# 13. Legal information

### Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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