AN11009

Pin FMEA for LVC family

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Document information

Information	Content
Keywords	FMEA, LVC, CMOS, 5 V and 3 V systems
Abstract	This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia's LVC family under typical failure situations

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1. Introduction

Low-Voltage CMOS (LVC) has become a logic industry standard for 3.3 V applications both in the telecommunications and EDP market segment. LVC offers a direct interface with TTL levels, is manufactured in a CMOS process, specified and guaranteed for industrial operating temperatures.

2. LVC family overview

The LVC family from Nexperia Semiconductors supports live insertion and provides speeds of 4.5 ns to 5 ns and a drive capability of 24 mA while operating at 3 V with very low static and dynamic power consumption. The 5 V tolerance capabilities make the LVC family extremely attractive for mixed 5 V and 3 V systems.

The LVC devices are available as either non-bus hold, or bus hold with, or without, damping resistor features. Bus hold types eliminate the need for pull-up and pull-down resistors for floating inputs. Series damping resistors help prevent signal undershoots and overshoots.

The LVC family range includes standard gates and octals to complex 16-bit bus interface functions for buffering, multiplexing and interfacing in mixed 5 V and 3 V systems. The broad portfolio and feature set of the LVC family provide designers with the flexibility and reliability necessary to minimize manufacturing costs, eliminate floating inputs and design ‘‘worry-free” systems.

3. Pin FMEA

This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia’s LVC family under typical failure situations such as a short-circuit to V_{CC} or GND or to a neighboring pin, or if a pin is left open.

Some LVC family devices have special functions, such as translators and level-shifters, that can have different behaviors.

A failure is classified according to its effect on the LVC device and the functionality of the application; see Table 1.

Table 1. Classification of failure effects

Class	Failure effect
A	damage to device
	affects application functionality
B	no damage to device
	may affect application functionality
C	no damage to device
	no affect to application functionality

Table 2. FMEA matrix for pin short-circuit to V_{CC}

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined HIGH, no damage, no leakage, no output level change
Output	A	if output defined LOW, short-circuits and high currents can damage device, output level changes
GND	B	short-circuits and high currents can damage device, will affect functionality

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Table 3. FMEA matrix for pin short-circuit to GND

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined LOW, no damage, no leakage, no output level change
Output	A	if output defined HIGH, short-circuits and high currents can damage device, output level changes
V_{CC}	B	no damage to device, will affect functionality

Table 4. FMEA matrix for pin left open

Pin	Class	Remarks
Input	B	undefined operating condition, no damage, increases leakage (except bus hold types), may affect functionality
Output	C	normal operating condition, no damage, no leakage
GND	B	undefined operating condition, no damage, increases leakage, will affect functionality
V_{CC}	B	undefined operating condition, no damage, increases leakage(only for I/O types), will affect functionality

Table 5. FMEA matrix for pin short-circuits between neighbor pins

Pin	Class	Remarks
Input to input	C	if inputs have same voltage levels: no damage, no leakage
	B	if inputs have different voltage levels: leakage increases, will affect functionality
Input to output	A	if input and output have different voltage levels, can cause high current and can damage device, will affect functionality
	C	if input and output have same voltage levels, no damage, no leakage
Input to GND	-	see Table 3
Input to V_{CC}	-	see Table 2
Output to output	C	if outputs have same voltage levels, no damage, no leakage
	A	if outputs have different voltage levels, can cause high current and can damage device, will affect functionality
Output to input	-	same effect as ‘input to output’ condition
Output to GND	-	see Table 3
Output to V_{CC}	-	see Table 2
GND to V_{CC}	-	not applicable, these pins are not neighbors

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4. Abbreviations

Table 6. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
EDP	Electronic Data Processing
FMEA	Failure Modes and Effects Analysis
LVC	Low-Voltage CMOS
TTL	Transistor-Transistor Logic

5. Revision history

Table 7. Revision history

Rev	Date	Description
v.2	20190109	AN11009, updated to latest Nexperia documentation standard
v.1	20110204	AN11009 initial version

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