AN11106

Pin FMEA for AHC/AHCT family

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Document information

Information	Content
Keywords	FMEA, AHC, AHCT, CMOS
Abstract	This application note provides a Failure Modes and Effects Analysis (FMEA) for Nexperia's AHC/AHCT family under typical failure situations

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1. Introduction

The Advanced High-Speed CMOS (AHC and AHCT) family of logic devices from Nexperia Semiconductors, offers many of the same functions found in the High-Speed CMOS (HC and HCT) family. However, it has higher performance and lower power consumption than the HC/HCT while maintaining competitive prices. In addition, Nexperia Semiconductors guarantees AHC/AHCT products to operate over an extended temperature range of -40 °C to +125 °C. The increase in product specification is at no extra cost to the customer..

The AHC/AHCT family of products is ideally suited for notebooks, telecom infrastructure, and portable applications. The capability to operate at both 5 V and 3.3 V, further extends its integration into new designs. The dual voltage facilitates the migration of existing designs to low-voltage systems and establishes it as a truly mixed-voltage product.

The AHC/AHCT family includes gates, octals, MSI, and 16 bit-wide devices. It is both functionally and pin-for-pin compatible with the HC/HCT family of products.

2. Pin FMEA

This chapter provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia's AHC/AHCT family under typical failure situations such as a short-circuit to V_{CC} or GND or to a neighboring pin, or if a pin is left open.

A failure is classified according to its effect on the AHC/AHCT device and the functionality of the application; see Table 1.

Table 1. Classification of failure effects

Class	Failure effect
A	damage to device
	affects application functionality
B	no damage to device
	may affect application functionality
C	no damage to device
	no affect to application functionality

Table 2. FMEA matrix for pin short-circuit to V_{CC}

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined HIGH, no damage, no leakage, no output level change
Output	A	if output defined LOW, short-circuits and high currents can damage device, output level changes
GND	B	short-circuits and high currents can damage device, will affect functionality

Table 3. FMEA matrix for pin short-circuit to GND

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined LOW, no damage, no leakage, no output level change
Output	A	if output defined HIGH, short-circuits and high currents can damage device, output level changes
V_{CC}	B	no damage, affects functionality

Table 4. FMEA matrix for pin left open

Pin	Class	Remarks
Input	B	undefined operating condition, no damage, increases leakage, may affect functionality
Output	C	normal operating condition, no damage, no leakage
GND	B	undefined operating condition, no damage, increases leakage, will affect functionality
V_{CC}	B	undefined operating condition, no damage, increases leakage (only for I/O types), affects functionality

Table 5. FMEA matrix for pin short-circuits between neighbor pins

Pin	Class	Remarks
Input to input	C	if inputs have same voltage levels: no damage, no leakage
	B	if inputs have different voltage levels: leakage increases, will affect functionality
Input to output	A	if input and output have different voltage levels, can cause high current and can damage device, will affect functionality
	C	if input and output have same voltage levels, no damage, no leakage
Input to GND	-	see Table 3
Input to V_{CC}	-	see Table 2
Output to output	C	if outputs have same voltage levels, no damage, no leakage
	A	if outputs have different voltage levels, can cause high current and can damage device, will affect functionality
Output to input	-	same effect as ‘input to output’ condition
Output to GND	-	see Table 3
Output to V_{CC}	-	see Table 2
GND to V_{CC}	-	not applicable, these pins are not neighbors

3. Abbreviations

Table 6. Abbreviations

Acronym	Description
AHCT	Advanced High-Speed CMOS TTL
CMOS	Complementary Metal-Oxide Semiconductor
FMEA	Failure Modes and Effects Analysis
LSTTL	Low power Schottky TTL
TTL	Transistor-Transistor Logic

4. Revision history

Table 7. Revision history

Rev	Date	Description
v.2	20190109	AN11106, updated to latest Nexperia documentation standard
v.1	20111104	AN11106 initial version

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