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AN11358

Parallel Schottkys as secondary rectifiers in flyback adapter: power losses and junction temperatures

Rev. 1 — 3 July 2013 **Application note**

Document information

Info	Content
Keywords	Low power adapter (LPA), flyback, charger, secondary side parallel Schottky rectifier, thermal simulation, SPICE simulation, PMEG4050ETP, PMEG6030EVP, PMEG6045ETP, PMEG6030ETP, AN11310
Abstract	This document gives an overview of power losses and the consequential junction temperature rise of two parallel Schottkys as secondary side rectifiers in flyback power adapters with up to 12.5 W output power. The focus is set on a comparison of the parallel configuration to a single rectifier under full load conditions. SPICE and thermal simulations were performed to calculate electrical power losses and the rise of junction temperatures above ambient.

Revision history

Rev	Date	Description
1	20130703	Initial version

Contact information

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1. Introduction

Chargers for smartphones and tablet PCs are today designed for an increased output power, as fast charging cycles make a real difference to users. 10 W to 12.5 W are typical power ratings and mainly Switched Mode Power Supply (SMPS) flyback topology is used. Schottky rectifiers are popular as secondary side rectifiers in these designs, as they are cost-efficient solutions and offer significantly lower forward power losses compared to PN-diodes, increasing power efficiency.

Chargers also need to be compact and circuit elements in small packages are preferred. One issue with slim designs is the high junction temperature of the secondary side rectifiers under full load conditions. A common solution to reduce losses and generation of heat is to use two parallel rectifiers instead of one. But how much will the losses decrease and what is the impact on junction temperatures of the rectifiers? Certainly, the assumption that losses and temperatures are cut in half is too simple. One reason is because nonlinear effects play a certain role on power losses. On the other hand, because of limited heat sink capabilities of Printed-Circuit Boards (PCB), devices will heat up each other.

The following chapters give an overview of the main effects on the performance of two parallel rectifiers. Power losses and the consequential temperature rise are calculated by SPICE and thermal simulations with NXP Semiconductors 40 V, 5 A $I_{F(AV)}$ PMEG4050ETP MEGA Schottky rectifier for a typical condition in a 12.5 W charger for smart phones and tablets.

This document is an extension to Ref. 1 “Application Note AN11310 FlatPower Schottky rectifier in low power adapter.”, where the basic operation of flyback adapter and the performance of a single, secondary side rectifier are described.

Figure 1 shows the basic application schematic of a flyback converter with two parallel secondary side Schottky rectifiers.

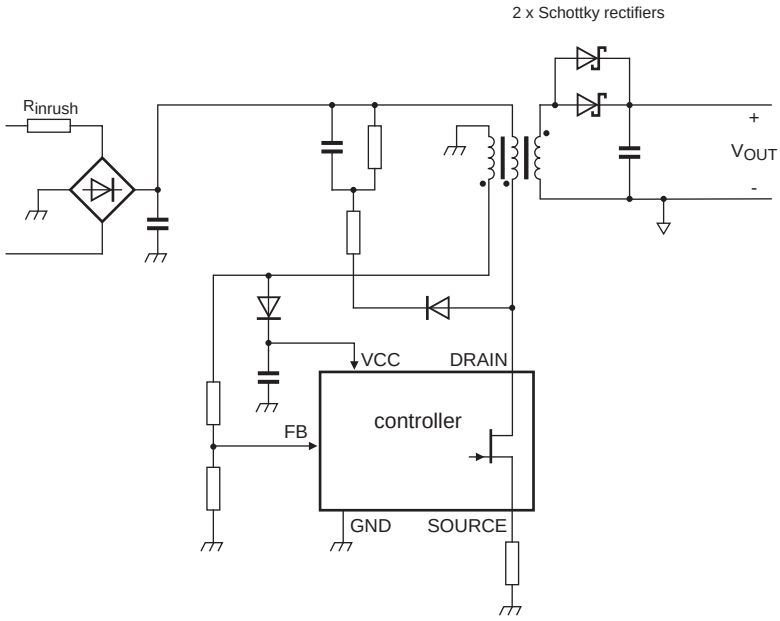


Fig 1. Basic application schematic of a flyback converter with parallel secondary side Schottky rectifiers

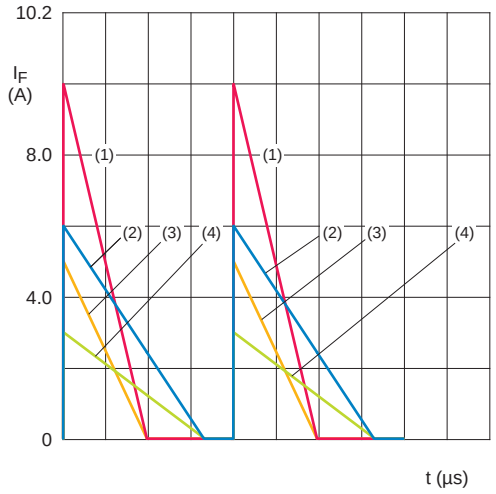
2. Current balancing and forward power losses of parallel rectifiers

When two Schottkys are connected in parallel, forward current I_F is distributed among them. In case of ideal devices, each rectifier will take half of the current. Unfortunately, the electrical characteristics of two semiconductors are not 100 % matched and one rectifier will have a lower typical forward voltage V_F than another. As a consequence, more than half of the total forward current I_F will flow through the device with the lower V_F and its junction temperature T_j will rise faster. With increased junction temperature, V_F is further reduced, resulting in further increasing current and so on and so forth. To limit this effect, a good thermal coupling between the rectifiers is essential, ideally at cathode and anode terminals.

The necessary thermal coupling leads to mutual heating up of the rectifiers. The thermal resistance of PCB material limits conduction of heat from each solder point into the PCB, from where it is dissipated into the ambient environment.

This document will not further deal with matching of electrical characteristics but assume, that forward current through the rectifiers is distributed equally. This simplified condition is a good starting point to show the principal effects on power losses and junction temperatures of two parallel devices. For the following analyses we assume that a flyback converter is operating in discontinuous mode and a simplified, triangular forward current is flowing through the secondary side rectifiers, as described in Ref. 1.

Figure 2 shows simplified current waveforms for different peak currents $I_{F(peak)}$ and duty cycles δ for single and parallel rectifiers. The average forward current $I_{F(AV)}$ through a single rectifier is 2.5 A, while 1.25 A $I_{F(AV)}$ represents the condition for each rectifier of the parallel configuration. 2.5 A / 5 V output is the typical condition for 12.5 W charger. The switching frequency is set to 100 kHz.



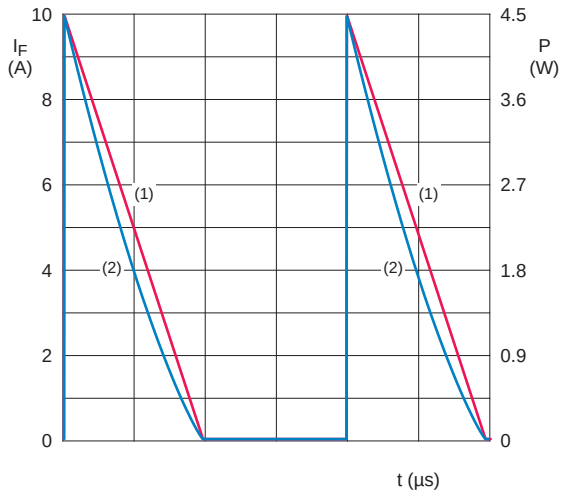
(1) $I_{F(AV)}$ = 2.5 A; $I_{F(peak)}$ = 10 A
(2) $I_{F(AV)}$ = 2.5 A; $I_{F(peak)}$ = 6 A
(3) $I_{F(AV)}$ = 1.25 A; $I_{F(peak)}$ = 5 A
(4) $I_{F(AV)}$ = 1.25 A; $I_{F(peak)}$ = 3A

Fig 2. Simplified current waveforms of single and parallel rectifier configuration

The waveforms of Figure 2 take account of the high peak current that can occur in the secondary side rectifier of a non-synchronous flyback converter. The peak value is important as it influences forward power losses. In case of a linear device, for example a resistor, a doubling of forward current would result in a doubling of forward voltage. But a Schottky rectifier is a nonlinear device. When the current rises to higher values, the nonlinear dependence of forward voltage on forward current becomes visible. It causes an overproportional increase of the forward power losses.

This behavior is depicted in Figure 3. Power losses versus the 10 A peak current waveform from Figure 2 are shown for PMEG4050ETP. Although the current through the rectifier decreases linearly, the power decreases overproportionally as the current falls.

A configuration of two parallel rectifiers makes use of this effect to reduce total forward power losses in the output stage of a flyback. With each rectifier's forward current cut in half, total forward power losses are reduced.



(1) Forward current i_F

(2) Forward losses p_F

Fig 3. Power losses versus forward current of a diode

3. SPICE and thermal simulations of power losses and junction temperatures

To simulate the junction temperatures of Schottky rectifiers, the average power losses must be known. There are two conditions that cause losses in a semiconductor: switching and conduction state. Both give rise to the temperature in the device, whereas conduction state losses are more critical for a secondary side rectifier in a non-synchronous flyback.

When the junction temperature of a Schottky rectifier rises, forward voltage V_F is reduced and this results in lower conduction state losses. To simulate losses for the secondary side rectifier under elevated temperatures, a SPICE model at T_j = 85 °C was extracted for NXP Semiconductors 40 V, 5 A $I_{F(AV)}$ MEGA Schottky rectifier PMEG4050ETP. The model card is shown in Ref. 1 “Application Note AN11310 FlatPower Schottky rectifier in low power adapter.”

The design of the power and output stage of a flyback converter affects peak levels of forward current I_F through a secondary side rectifier. As discussed in Section 2, peak current and duty cycle result in different power losses of a Schottky rectifier and therefore the design is important for the efficiency of the output stage. A design where peak currents are kept to a minimum reduces losses.

Table 1 shows SPICE simulation results of average power losses $P_{(AV)}$ for different peak current and on-time conditions of the repetitive current pulses as shown in Figure 2. Single and parallel configuration are represented by $I_{F(AV)}$ = 2.5 A and $I_{F(AV)}$ = 1.25 A respectively. The simulation results are based on the PMEG4050ETP SPICE model at T_j = 85 °C.

Table 1. PMEG4050ETP SPICE simulation results of average power losses

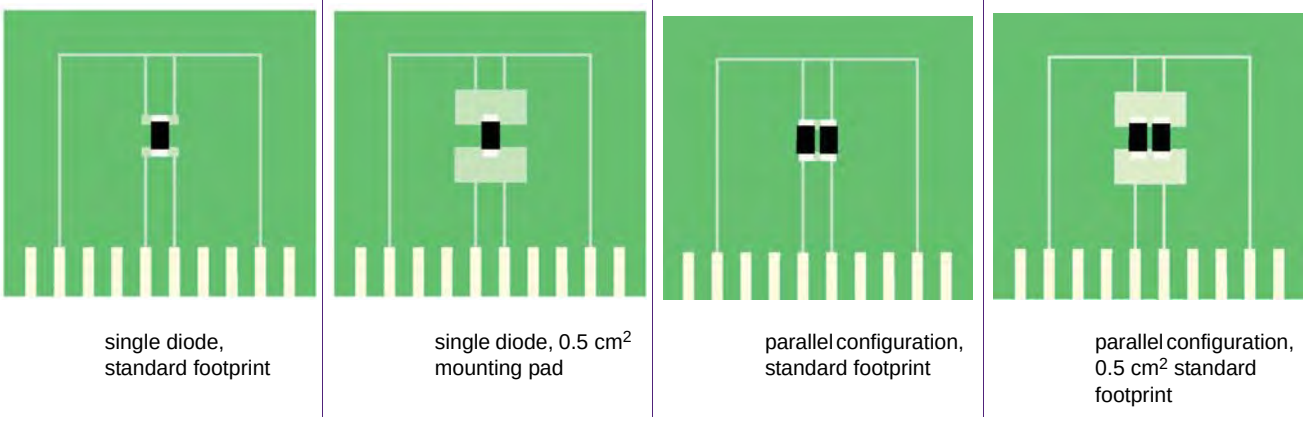
Parameter	Unit	Parallel config. $I_{F(peak)}$ = 5 A	Single config. $I_{F(peak)}$ = 10 A	Parallel config. $I_{F(peak)}$ = 3 A	Single config. $I_{F(peak)}$ = 6 A
$I_{F(AV)}$	A	1.25 + 1.25	2.5	1.25 + 1.25	2.5
t_{on} / t_{period}	µsec/ µsec	9.8 / 20	9.8 / 20	16.6 / 20	16.6 / 20
$P_{(AV)}$	mW	400 + 400	965	360 + 360	840

The results in Table 1 show, that total power losses will be reduced by more or less 10 % when two Schottky rectifier are operated in parallel, while total average output current is kept constant at 2.5 A.

Besides the reduction of power losses, junction temperatures of the Schottky rectifier will rise less in a parallel configuration because of the improved thermal resistance from junction to solder point $R_{th(j-sp)}$. By using two rectifiers and distributing the power, the total area of silicon on leadframe and the available amount of metals for leadframes, leads and die bonds is doubled and the heat generated in the semiconductors has a lower thermal resistance into the mounting base. The lower the thermal resistance of the system, the lower the rise of the silicon temperature above ambient. But the PCB and signal traces represent a big thermal resistance in series to $R_{th(j-sp)}$, limiting dissipation of heat to the ambient environment. The thermal limits of the PCB lead to a mutual heating up of the devices.

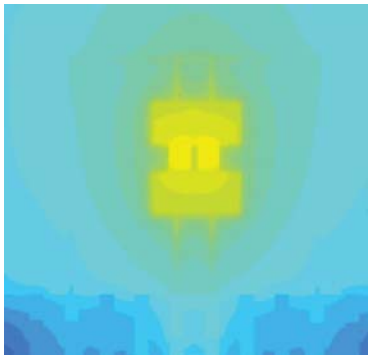
To quantify junction temperatures for the different $P_{(AV)}$ conditions as shown in Table 1, thermal simulations were performed with a physical model of PMEG4050ETP in SOD128 package. The PCBs used for the simulations are either single layer or dual layer with 50 % copper coverage on the bottom side. In addition, standard footprint and 0.5 cm^2 mounting pad sizes were simulated. Copper thickness for PCB layers is 35 µm and ambient temperature T_{amb} is set to 25 °C. Top side PCB layouts are shown in Figure 4, pictures of heat distribution across the PCBs for different setups and a 3D picture of the SOD128 package are shown in Figure 5 to 10.

The thermal simulation software applied to carry out the analyses is FloTHERM of Mentor Graphics Corporation.



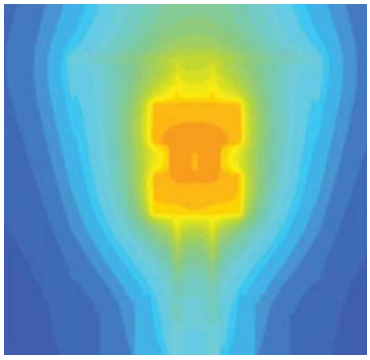
single diode, standard footprint | single diode, 0.5 cm^2 mounting pad | parallel configuration, standard footprint | parallel configuration, 0.5 cm^2 standard footprint

Fig 4. Simulation PCB layouts for single and parallel configuration



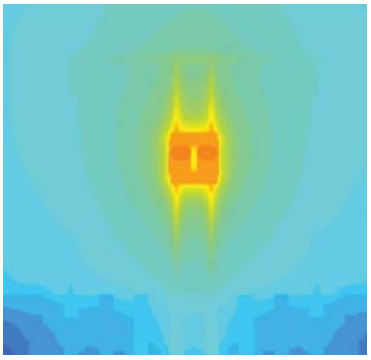
400 + 400 mW
dual layer
0.5 cm^2 mounting pads

Fig 5. Setup 1



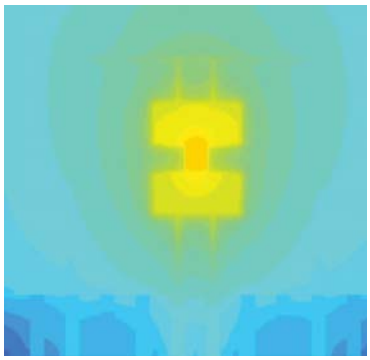
400 + 400 mW
single layer
0.5 cm^2 mounting pads

Fig 6. Setup 2



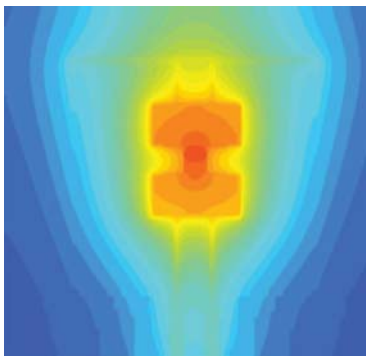
400 + 400 mW
dual layer
standard footprint

Fig 7. Setup 3



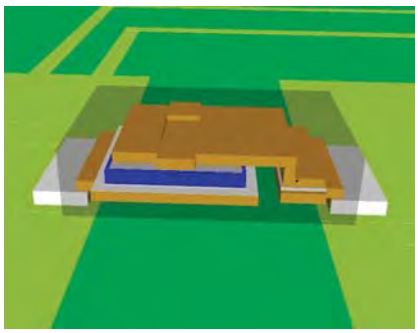
965 mW
dual layer
0.5 cm^2 mounting pads

Fig 8. Setup 4



965 mW
single layer
0.5 cm^2 mounting pads

Fig 9. Setup 5



SOD128 FlatPower package

Fig 10. 3D picture

$P_{(AV)}$ = 965 mW for a single and 400 mW for the parallel rectifier represent worst case conditions of a design with high peak currents levels. The two different values for $P_{(AV)}$ again show the effects of the nonlinear electrical characteristic. The different board layouts highlight the improved thermal resistance from junction to solder point of the parallel configuration as well as the effects of dual layer PCB and increased mounting pads on heat distribution across PCB. Results of the thermal simulations are summarized in Table 2.

Table 2. Thermal simulation results for single and parallel PMEG4050ETP rectifier.

$P_{(AV)}$ rectifier 1 / rectifier 2	400 mW / 400 mW	400 mW / 400 mW	400 mW / 400 mW
Layer stack	dual, 50 % copper on bottom side	single	dual, 50 % copper on bottom side
Mounting size pad	0.5 cm^2	0.5 cm^2	standard footprint
Junction temperature T_j	79 °C	107 °C	108 °C
Total $R_{th(j-a)}$	67.5 K/W	102.5 K/W	104 K/W
$P_{(AV)}$ rectifier 1 / rectifier 2	965 mW / not present	965 mW / not present	965 mW / not present
Layer stack	dual, 50 % copper on bottom side	single	dual, 50 % copper on bottom side
Mounting size pad	0.5 cm^2	0.5 cm^2	standard footprint
Junction temperature T_j	100 °C	132 °C	140 °C
Total $R_{th(j-a)}$	78 K/W	111 K/W	120 K/W
$P_{(AV)}$ rectifier 1 / rectifier 2	360 mW / 360 mW	360 mW / 360 mW	360 mW / 360 mW
Layer stack	dual, 50 % copper on bottom side	single	dual, 50 % copper on bottom side
Mounting size pad	0.5 cm^2	0.5 cm^2	standard footprint
Junction temperature T_j	73.5 °C	98.5 °C	100 °C
Total $R_{th(j-a)}$	67.5 K/W	102.5 K/W	104 K/W
$P_{(AV)}$ rectifier 1 / rectifier 2	840 mW / not present	840 mW / not present	840 mW / not present
Layer stack	dual, 50 % copper on bottom side	single	dual, 50 % copper on bottom side
Mounting size pad	0.5 cm^2	0.5 cm^2	standard footprint
Junction temperature T_j	90.5 °C	118 °C	126 °C
Total $R_{th(j-a)}$	78 K/W	111 K/W	120 K/W

Thermal resistance junction to ambient is calculated by:

$$R_{th(j-a)} = (T_j - T_{amb}) / P_{(AV)}$$

4. Conclusion

There are two main causes for a reduction of junction temperatures of two parallel rectifiers compared to a single one:

a. Electrical power losses are reduced due the nonlinear V_F versus I_F characteristic of Schottky rectifiers

b. Thermal resistance junction to solder point $R_{th(j-sp)}$ is reduced because of the doubled amount of silicon, leadframes, leads and die bonds, resulting in a smaller total thermal resistance from junction to ambient $R_{th(j-a)}$.

On dual layer PCB with 0.5 cm^2 mounting pads, thermal simulation results show between 73.5 °C and 79 °C junction temperature for two parallel PMEG4050ETP Schottky rectifiers, depending on peak current conditions. This is a temperature decrease of about 20 % compared to T_j of a single rectifier.

Both the reduction of forward power losses and the lowered $R_{th(j-sp)}$ add to more or less 10 % decrease of junction temperatures in a 2.5 A total forward current application, independent from the PCB layout.

Comparison of the results from single layer to dual layer PCB with 50 % copper coverage on the bottom side shows the importance of heat distribution across the PCB. Even if no thermal vias are used, copper on the backside supports heat flow across the complete PCB, from where it dissipates away in the ambient environment. A similar effect is reached when the mounting pads on the top layer are increased from standard footprint to 0.5 cm^2 at cathode and anode terminals, as the area from where heat is conducted into the PCB is increased. Both measures result in lower junction temperature rise above ambient. Increased mounting pads and the dual layer PCB setup are intended to represent real conditions inside a charger, where the Schottky rectifiers are connected via thick signal traces and are surrounded by other circuit elements, like capacitors or the transformer and PCBs are dual layer.

NXP's low V_F Schottky rectifier in FlatPower SOD128 package are ideal for compact, cost efficient designs of low power adapter in the range from 5 W to 12.5 W, whether a single rectifier is used for the lower power range or parallel rectifiers for higher output power. Table 3 shows a selection of 40 V to 60 V rectifiers suited for chargers.

Table 3. Schottky rectifiers in SOD128 for LPA, 40 to 60 V.

Type number	V_R (V)	$I_{F(AV)}$ (A)	$V_{F(typ)}$ (mV); T_{amb} = 25 °C		$I_{R(typ)}$ (μA); T_{amb} = 25 °C
			I_F = 1 A	I_F = 3 A	
PMEG4050ETP	40	5	340	390	8
PMEG6030ETP	60	3	380	460	4
PMEG6030EVP	60	3	355	420	7
PMEG6045ETP	60	4.5	355	420	7

5. References

[1] Application Note AN11310 FlatPower Schottky rectifier in low power adapter.

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