AN11882

High-speed interfaces - ESD protection and EMI filtering

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Document information

Info	Content
Keywords	USB2.0, USB3.0, USB3.1, USB Type-C, HDMI, Display Port, MIPI
Abstract	Details are provided concerning physical layer facts of interface standards, ESD protection approaches, EMI filter solutions, as well as ESD and surge testing methods.

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Revision history

Rev	Date	Description
1	31 August 2017	Initial revision

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1. Introduction

All modern high-speed interfaces use differential data signals and operate with reduced signal levels. High data speed, up to 20 Gbit/s, requires a carefully designed Printed-Circuit Board (PCB) layout to maintain signal integrity, which is achieved by proper impedance matching. Thus, avoiding inacceptable losses and reflections. Various EMI aspects have to be considered also because sensitive GSM, WIFI or GPS receivers are located close to potentially radiating high-speed interfaces (e.g. USB 3).

2. Differential Interfaces

2.1 General considerations

In a single-ended interface, the data signal is transmitted on a single wire, which connects the transmitter to the source. Both connected to the same ground. The receiver measures the incoming voltage level against ground potential. The input low level of the binary signal has to stay below a defined maximum voltage V_{IL}(max) which ensures safe detection as logical state. Likewise, the high level state has to exceed a defined minimum level V_{IH} (min), which ensures correct receiver detection.

Under inappropriate conditions, risk of errors increases for data transmissions. Errors can occur when ground level is disturbed, or when ground level is not identical for source and receiver, or when noise is coupled into the signal line.
For high-speed signals there is a trend to reduce the level of the data voltage swing. Modern semiconductor processes work with lower supply voltages and lower levels resulting in lower power consumption and less radiation.

Single-ended low level signals are very sensitive to overlaid noise and distortions at the receiver’s input point, which increases the risk of erroneous data reception.

2.2 Signal leveling for single-ended data signal

Figure 1 shows a single-ended data signal with voltage levels VIH(min) and VIL(max) as reference lines, which enclose the undefined signal level area between these levels. Levels within the undefined area make it impossible to determine the correct digital state in the receiver.

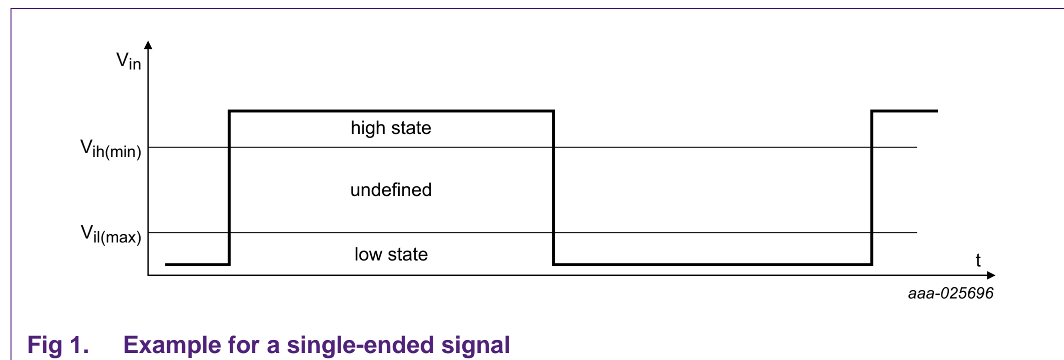

Fig 1. Example for a single-ended signal

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2.3 Structure of differential interfaces

In a differential interface two complementary signals are transmitted, as shown in Figure 2. A differential pair is also called a data lane. In order to derive an output signal, positive and negative inputs are subtracted. Thus, the output signal can be calculated, as follows: In a binary system, the output level of the subtractor is either $V_{IH} - V_{IL}$ or $-(V_{IH} - V_{IL})$. The output voltage level swing between the two logical states (SX_{OUT}) is twice as high compared to the height of the swing of a single input. Detection of the digital states high and low is quite simple because only the polarity of the detector output has to be determined.

Typically, differential lines are routed close to each other - as a pair on the board - in compliance with the impedance target of the related interface. Therefore, noise coupling into a data lane is mostly the same, for both the respective positive and the negative signal lines of one differential pair. This type of noise is referred to as common-mode noise. The overlaid common-mode noise is canceled out in the subtraction block. This makes differential signals almost immune against noise, compared to single-ended data transmission. The voltage levels of differential data can be reduced without a significant error rate increase. This makes it easier to increase data rates without high energy consumption in the data transmitter.

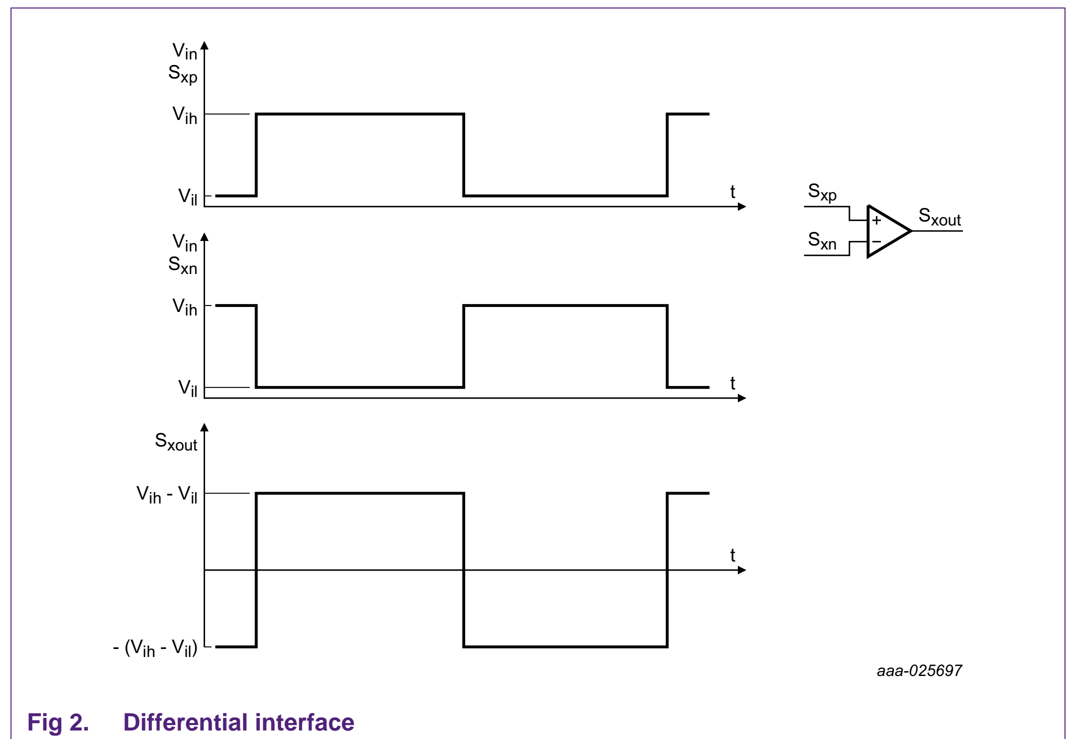

Fig 2. Differential interface

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2.4 Common-mode noise on differential signal lines

Figure 3 shows an overlaid distortion on both differential signal lines. The distortion is eliminated by the subtraction block in the data receiver. It is cancelled out and does not appear at the output of the subtraction block. Best is to avoid common-mode signal content because it creates electrical and magnetic fields that can radiate into the environment.

Whenever a differential wire pair changes direction on a Printed Circuit Board (PCB), this leads to areas where the wires start radiating because the fields from the single lines are not compensated exactly. This effect occurs because of a skew or phase shift between the signals of a data lane. which Figure 3 illustrates.

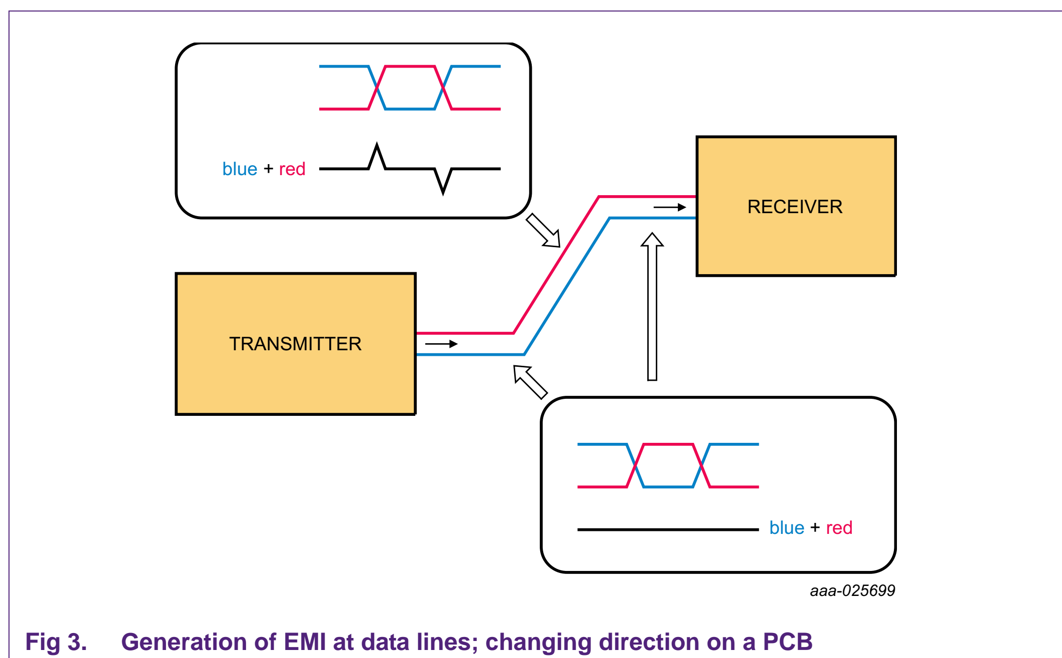

Fig 3. Generation of EMI at data lines; changing direction on a PCB

3. USB standards, data speeds and coding methods

3.1 USB 1.0 and USB 2.0 interfaces

Table 1 shows an overview of contemporary USB standards and their related symbol rates.

Table 1. Overview of data rates for USB interfaces

USB Type	Speed class	Data Rate	Symbol rate (Baud rate) Coding method
USB 1.0	Low Speed (LS)	1.5 Mbit/s = 187.5 kByte/s	1.5 Mbit/s NRZI-Code with Bit-Stuffing
USB 1.0	Full Speed (FS)	12Mbit/s = 1.5 MByte/s	12 Mbit/s NRZI-Code with Bit-Stuffing

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Table 1. Overview of data rates for USB interfaces

USB Type	Speed class	Data Rate	Symbol rate (Baud rate) Coding method
USB 2.0	High Speed (HS)	480 Mbit/s = 60MByte/s	480 Mbit/s NRZI-Code with Bit-Stuffing
USB 3.0	Super Speed	4000Mbit/s = 500MByte/s	5000 Mbit/s 8b10b-Code
USB 3.1	Super Speed +	9697 Mbit/s = 1212 MByte/s	10000 Mbit/s 128b132b-Code

USB 1.0 and USB 2.0 use a Non-Return-to-Zero-Inverted (NRZI) coding. Typically, NRZI coding, which is also referred to as NRZ coding, follows a simple rule:

For USB the coding rule is: `state 0:toggle state 1:constant`

When this method is applied, the polarity of a connecting wire pair in a cable has no impact on the bit sequence, which is an advantage. The reason is that a change in polarity represents a 0 state, regardless of the transition direction.

Figure 4 shows the schematic of the logic that is required for the hardware implementation of an NRZI encoder. The input signal is fed to an inverted input of an EXCLUSIVE-OR (XOR) gate.

The XOR gate is a digital logic gate that gives a true (1 or high state) output, whenever one of the inputs has a 1-state. If both inputs are 1, or both are 0, the output equals false (0 or low state).

Behind the XOR gate a flip-flop is placed, which samples the output of the gate by the system clock. The output of the flip-flop represents the output of the coder. It feeds back into the XOR gate; as second input signal for this gate.

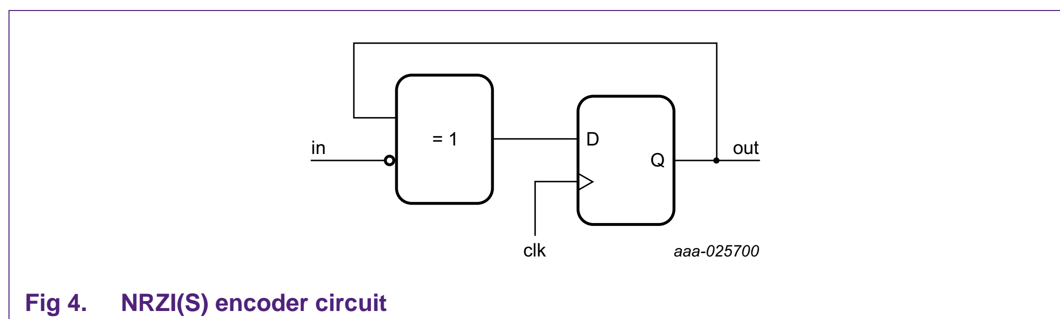

Fig 4. NRZI(S) encoder circuit

In Table 2 an exemplary bit stream in encoded by the NRZI coder. The second row of the table is the inverted input bit stream. The third row shows the output of the XOR. In the forth row the coded output signal is depicted.

The output bit stream shows the desired logic of a polarity toggle, which is created by a logical 0 in the input stream — with no change in the output stage for a logical 1 in the input data stream.

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Table 2. Example for the NRZI(S) encoding

Input	1	0	0	0	1	1	1	0	1	0	1	1	0
Inverted input	0	1	1	1	0	0	0	1	0	1	0	0	1
Output XOR	0	1	0	1	1	1	1	0	0	1	1	1	0
Encoder output	0	0	1	0	1	1	1	1	0	0	1	1	1

Figure 5 shows a simplified schematic of a decoder for an NRZI data stream, which shall detect a signal change with an output as logical state 0 and no signal change as logical state 1.

The function is realized by an XOR gate, in which the data stream is connected to one input and to the output of a flip flop at the second input. The output of the XOR has to be inverted in order to derive the correct polarity.

Table 3 shows how the decoder works, showing the bit stream at the input in row 1, the output of the flip-flop, the output of the XOR gate before the inversion and the final output of the decoder in the last row. It is shown that the output stream of the decoding stage is identical with the input stream of Table 2.

Please note that in signal transmission, it is preferable to have a DC-free system. Consequently, it is not required to have a direct galvanic connection for cable transmission between transmitter and receiver. The frequency band of the data channel does not need to start at 0 Hz but can be designed to a higher value. This ensures that data transmission can operate within a smaller frequency band.

Whenever a 0-state is transmitted, NRZI coding ensures that changes are incurred on the data during transmission. If a constant high occurs, the signal can get stuck, with no oscillations occurring. For this reason, a signal change has to be enforced after 6 bits in high state, which is applicable to all USB standards.

Please note that seven subsequent high states indicate a bit sequence error.

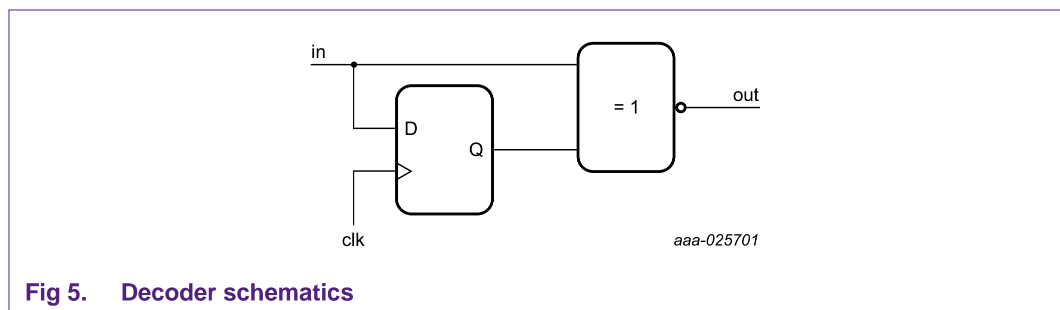

Fig 5. Decoder schematics

Table 3. Example for NRZ decoding

input to decoder	0	0	1	0	1	1	1	1	0	0	1	1	1
output of flip-flop	x	0	0	1	0	1	1	1	1	0	0	1	1
output XOR	x	0	1	1	1	0	0	0	1	0	1	0	0
output decoder	x	1	0	0	0	1	1	1	0	1	0	1	1

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The USB bus data line state is called K-state, whenever D+ signal is in low state and D– in is in high state. J-state describes the opposite condition, at which D+ is in high state and D– at in low state. Whenever both signal lines are pulled low, the system is in single-ended zero condition, referred to as SE0.

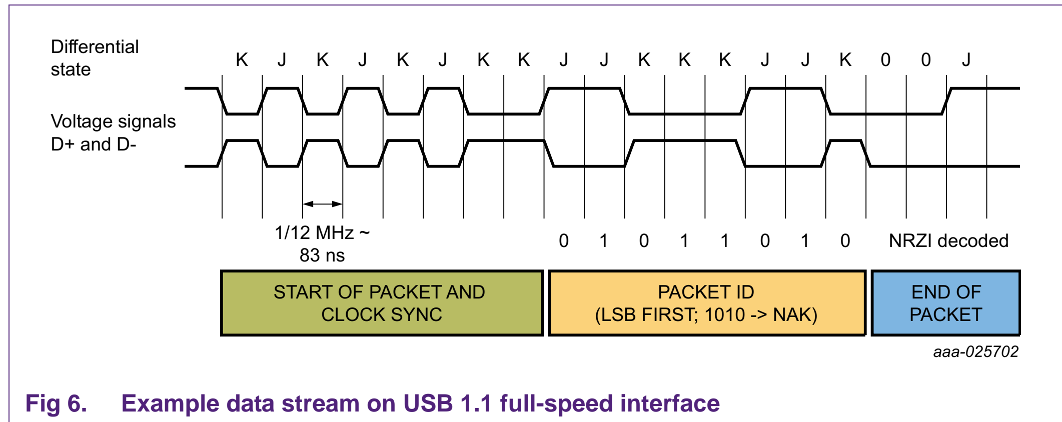

Fig 6. Example data stream on USB 1.1 full-speed interface

Figure 6 shows a brief data stream example that transmits an NAK (Not Acknowledged Packet) at a bit rate of 12 Mbit/s; via USB 1.1 full-speed. NAK indicates that data cannot be read out (e.g. because of problems with receiving and/or sending device/s).

Whenever real data content is transmitted, data packets are placed between the packet ID and the End-Of-Packet (EOP) block. The last placement of the sequence is implemented with two SE0 states, which is then followed by one idle J-state. Data transmission begins with an idle J-state: With a 00000001 sequence; i.e. with a KJKJKJKK sequence.

In USB 2.0 high-speed mode, the start sequence is 32 bits long, which provides more transitions. This allows the clock recovery PLL circuit to synchronize in exact correspondence to the timing of the bit stream.

When no device is connected, the host pulls low both signal lines to ground via a 15 kΩ pull-down resistor. If an USB device is connected, one of the signal lines is pulled high via a 1.5 kΩ resistor and overwrites the pull-down state of the host.

USB 1.x speed is determined whenever D+ or D– line is pulled high via the 1.5 kΩ USB pull-up resistor. J-state signifies the idle state for USB full-speed mode. K-state signifies low-speed. A reset to SE0 condition occurs when both signal lines are pulled low by the host for 10 to 20 ms.

If an USB 2.0 ready device is connected, the above described procedure for USB 1.1 devices is initially performed but then continued with another process.

After reset the device puts a K-state on the bus informing the host that it can handle the higher speed. After this the host toggles 3 times between J and K state to tell the USB device that also the host can support the high-speed data rate. This handshaking procedure for the speed capability of host and device is known as ‘chirping’ in USB literature.

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3.2 USB 3.0 and USB 3.1 interfaces

USB 3.0 and USB 3.1 use a different DC content removal method on signal lines, which is referred to as 8b10b-coding: 8-bit data is replaced by 10b-data. Thus, redundancy is added to obtain both a DC-free bit stream and a limited disparity of transmitted 0-states and 1-states. In a row of 20 bits, the counts of the two possible states shall never differ by more than ± 2.

Please note that after several 8b10b code words, the signal is completely DC-free. Thus, the number of ones and zeros is identical. The 8-bit original data is split into 5 bits, which are coded in 6 bits with a 5b6b-code. The remaining 3 bits are coded in 4 bits with a 3b4b-code. Thus, forming the final 8b10b-coding scheme.

The coding operates on a running disparity (RD): After each symbol, the count of ones and zeros differs either by 1 or –1. Table 4 lists the RD coding rules.

For clarification, two processes based on the rules in Table 4, are explained:

- If a code word has a disparity of zero, no disparity change occurs for the next coded word.
- If a code word has a disparity option +/– 2, a disparity is selected that prompts a sign change for the next word. In order to achieve this change there have to be two coding options for words, which do not have an equal number of zeros and ones.

Table 4. Rules for Running Disparity coding

Previous RD	Disparity of Code word	Disparity chosen	Next RD
–1	0	0	–1
–1	+/– 2	+2	+1
+1	0	0	+1
+1	+/–2	–2	–1

Table 5. 5b6b code table

Input		RD = –1		RD = +1
	EDCBA		abcdei	
D.00	00000	100111		011000
D.01	00001	011101		100010
D.02	00010	101101		010010
D.03	00011		110001	
D.04	00100	110101		001010
D.05	00101		101001	
D.06	00110		011001	
D.07	00111	111000		000111
D.08	01000	111001		000110
D.09	01001		100101	
D.10	01010		010101	
D.11	01011		110100	
D.12	01100		001101	
D.13	01101		101100	

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Table 5. 5b6b code table

	Input	RD = −1		RD = +1
	EDCBA		abcdei	
D.14	01110		011100	
D.15	01111	010111		101000
D.16	10000	011011		100100
D.17	10001		100011	
D.18	10010		010011	
D.19	10011		110010	
D.20	10100		001011	
D.21	10101		101010	
D.22	10110		011010	
D.23	10111	111010		000101
D.24	11000	110011		001100
D.25	11001		100110	
D.26	11010		010110	
D.27	11011	101110		001001
D.28	11100		001110	
D.29	11101	101110		001110
D.30	11110	011110		100001
D.31	11111	101011		010100

Table 5 above shows the way how the original 5-bit code words are coded into 6-bit code words. Each new 6-bit code word contains either:

- 3 zeros and ones
- 2 ones and 4 zeros
- 4 zeros and 2 ones

The 6-bit code word in column RD = + 1 can be created easily by inverting all bits of the code word in column RD = – 1.

Table 6. 3b4b-code table

	Input	RD = −1		RD = +1
	HGF		fghj	
D.x.0	000	1011		0100
D.x.1	001		1001	
Dx.2	010		0101	
D.x.3	011	1100		0011
D.x.4	100	1101		0010
D.x.5	101		1010	
D.x.6	110		0110	
D.x.P7	111	1110		0001
D.x.A7	111	0111		1000

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Table 6 is the coding scheme from 3-bit to 4-bit.

Please note that Table 5 and Table 6 each contain one exception from the rule. The word codes 111000 (RD = –1) and respectively 000111 (RD = +1) in Table 5 (EDCBA column value 00111) each contain the same number of zeros and ones. The same applies for the word codes 0011 and 1100 in Table 6 (HGF column value 011).

High-speed interfaces like PCI Express, Serial ATA, Display Port, Fibre Channel Gigabit, Ethernet and DVB make use of 8b10b-coding, which also supports AC-coupling. This support makes clock recovery much easier.

Clock recovery with a phase-locked loop (*PLL*) clock generator is required in all scenarios in which no separate clock signal is sent with the data. The PLL of the data receiver has to synchronize to the data signal transitions in order to allow safe sampling of incoming data.

USB high-speed and the slower modes, make use of one differential pair with signal lines D+ and D– for data transmission, which allows half duplex data transmission.
USB 3.x makes use of two differential pairs, which allows data flow in both directions in full duplex mode.

Figure 7 shows the termination of the D+ and D– lines. On both sides of the connection a 45 Ω single-ended termination to ground is implemented. This results in a 90 Ω differential termination of the signal lines. In practice, the 45 Ω serial resistor behind the LS/HS drivers are switched to ground. By doing so, the serial resistor functions as 45 Ω termination for this high-speed use case.

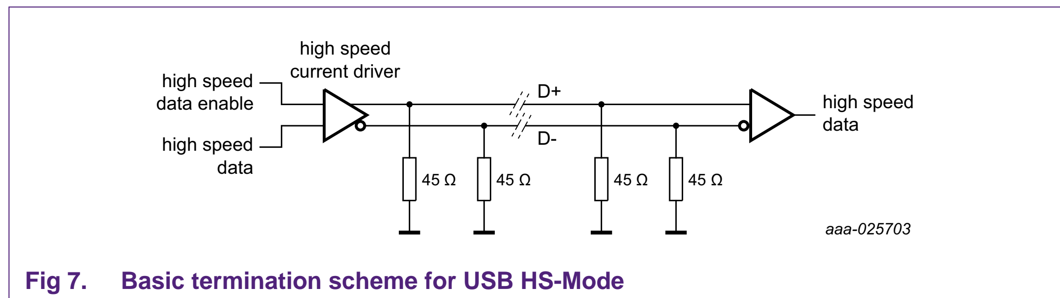

Fig 7. Basic termination scheme for USB HS-Mode

The high-speed drivers are implemented as switched current sources that deliver 17.78 mA in single-ended in high state. Figure 8 shows this basic driver structure.

The high stae voltage at the 45 Ω resistors in parallel operation is:

V_{SEhigh} = 17.78 mA / 22.5 W = 400 mV

The nominal differential voltage swing on the D+/D– signal pair is therefore ± 400 mV = 17.78

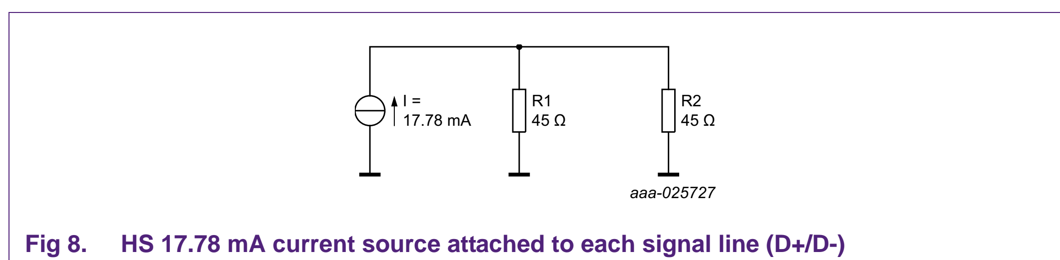

Fig 8. HS 17.78 mA current source attached to each signal line (D+/D-)

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In Figure 9 the coupling of the two differential signal pairs for the super speed signals RX and TX is depicted. At every transmitter side, the TX lines contain capacitors that realize AC-coupling for both differential connection lanes. The nominal capacitance of these capacitors is 100 nF. The figure shows the cable connection of a host and an USB device that is plugged into mated connectors.

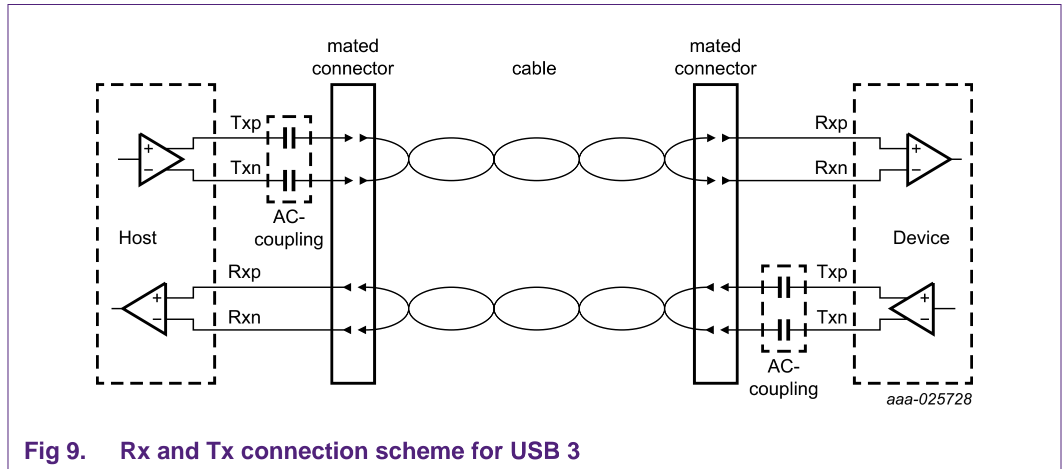

Fig 9. Rx and Tx connection scheme for USB 3

Currently it is discussed to place additional 330 nF capacitors at the data inputs RXp and RXn and a 100 kΩ termination to ground at the cable side of the capacitors as an extension of the USB 3 standard.

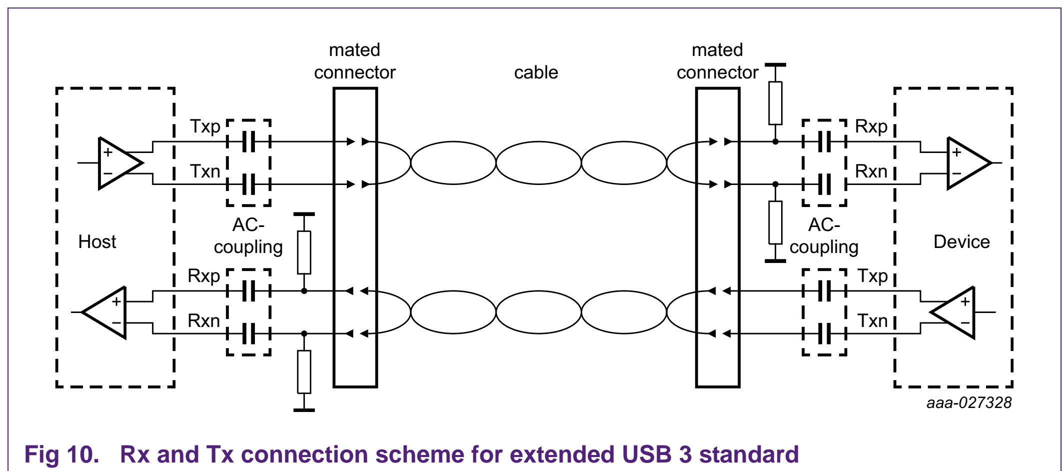

Fig 10. Rx and Tx connection scheme for extended USB 3 standard

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3.3 USB 2.0 eye diagrams

The USB standard specification defines four measurement planes that are used to test a USB interface, as depicted in Figure 11. TP1 connects directly to the signal lines of the transceiver of the hub circuit board. TP2 connects the USB cable. TP3 is located directly at the input connection point of the USB device. TP4 connects directly to the pins of the receiving block of the device circuit board.

In an eye diagram measurement, an oscilloscope shows the bit transitions of a data path as an overlay of many single traces with random data content. The oscilloscope is triggered with a recovered bit clock signal because no separate clock signal is provided on an extra signal line. A data clock recovery PLL provides the data sampling clock, synchronized to data transitions.

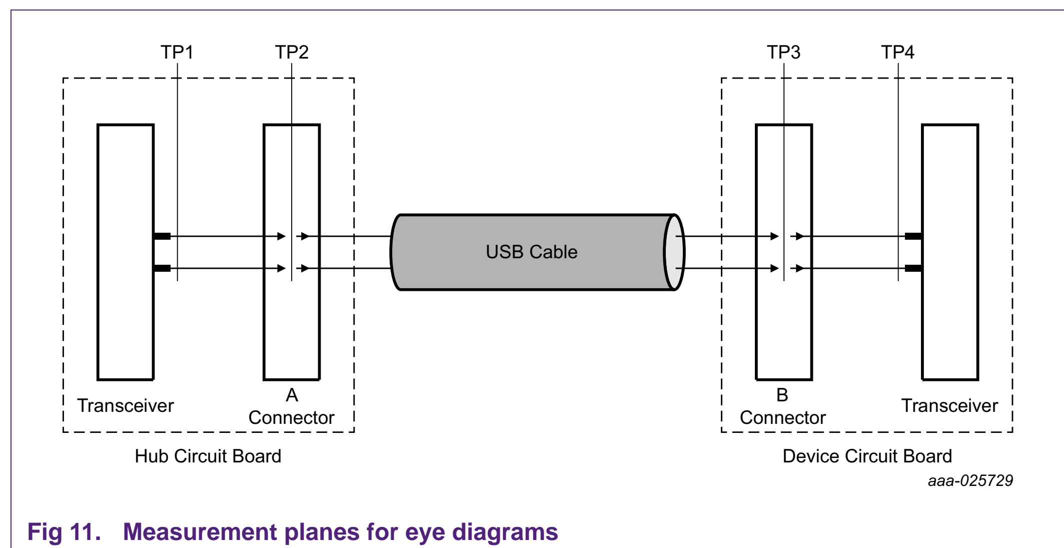

Fig 11. Measurement planes for eye diagrams

The data eye diagram is a methodology that helps to analyze the signal quality of a high speed digital signal. Ideally, an eye diagram with a binary signal shows a row of rectangular boxes. In real scenarios the rise and fall times are not zero but are extended by parasitic capacitances in the data path and the limited speed of the transmitter stages.

Reflections, overlay of noise and jitter of the PLL clock render a graph with a smaller open temporal window the part of the eye diagram where no signal transitions occur. Data transitions are not located at the exact temporal location of `n * Tsymbol`. Jitter can have both a random distribution and a deterministic distribution, depending on its root cause. The nature of the jitter can be analyzed with a histogram. The width of the complete histogram represents the peak-to-peak jitter.

Figure 12 shows how the waveforms of transmitted data for a hub - measured at TP2 or for a device measured at TP3 - have to look like. In an standard-compliant scenario, no signal traces are noticeable within the inner mask of the diagram, which is defined by points 1 to 6, as listed in Table 7. Each of these points is defined by a certain voltage and time within the unit interval. The unit interval is equal to the symbol length.

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USB high speed shows:

T_{symbol} = 1/ f_{symbol} = 1/480 Mhz = 2.0833 ns

The temporal location is listed as a percentage value of the unit interval in the table. The nominal voltage swing of USB 2.0 is 400 mV to -400 mV. The diagram shows a second mask, which limits the signal in terms of higher voltages. The maximum voltage for the signal is ± 475 mV, for a time at which no transitions occur. The voltage limit at transitions is ± 525 mV, transitions, which allows some room for over- and undershoots.

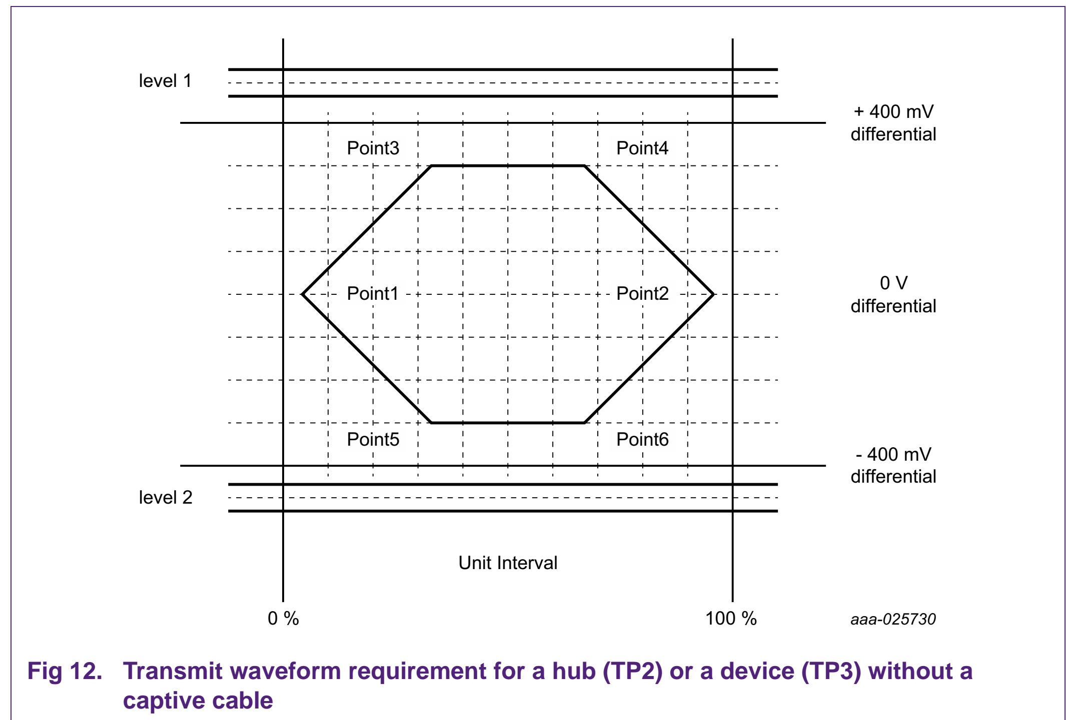

Fig 12. Transmit waveform requirement for a hub (TP2) or a device (TP3) without a captive cable

Table 7. Parameters for the USB 2.0 transmitter eye for the test case according to Fig.11

	Voltage Level (D+, D-)	Time (% of Unit Interval; 1/480 MHz = 2.0833 ns nominal
Point 1	0V	5%
Point 2	0V	95%
Point 3	300 mV	35%
Point 4	300 mV	65%
Point 5	– 300 mV	35%
Point 6	– 300 mV	65%

Figure 13 shows a receiver waveform requirement scheme for a signal applied to TP4/device transceiver or to TP1/hub transceiver. The receiver mask is typically smaller than the transmitter mask, as stated above. The height of the eye is 300 mV, with a –150 mV to + 150 mV range. The width of the eye is reduced to 60% of the unit interval.

Table 8 contains the details for the keep-out area for this particular test condition, which shows the smaller inner mask, as well as the upper and lower boundaries as outside limitation for the D+ and D– signal waveforms.

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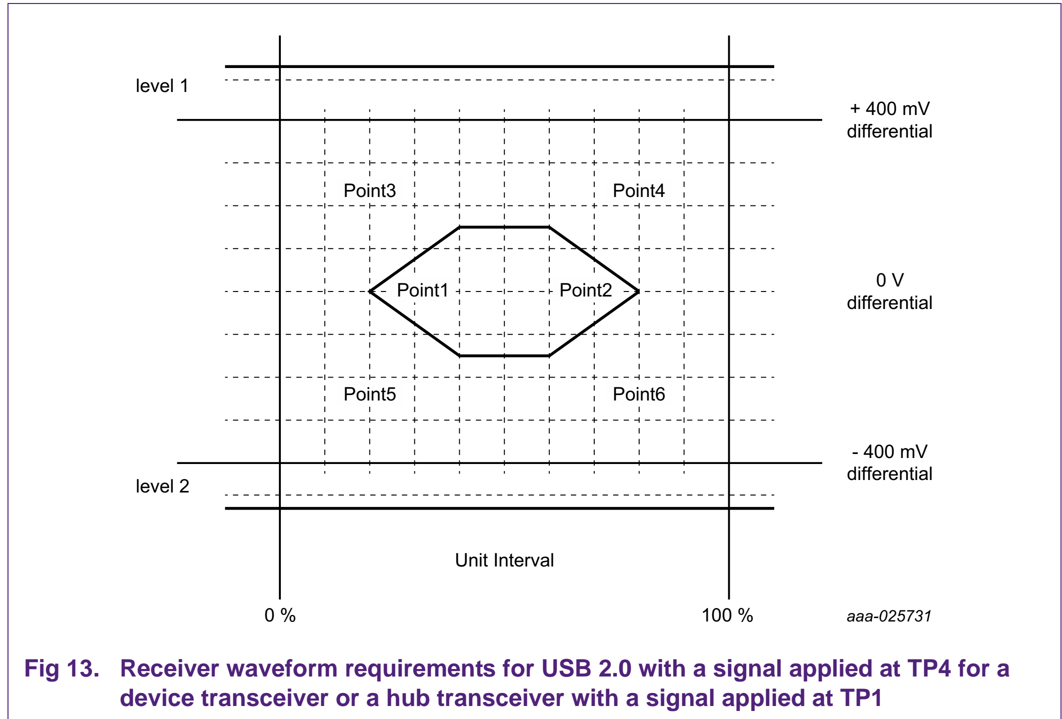

Fig 13. Receiver waveform requirements for USB 2.0 with a signal applied at TP4 for a device transceiver or a hub transceiver with a signal applied at TP1

Table 8. Parameters for the USB 2.0 receiver eye

	Voltage level (D+, D−)	Time (% of Unit Interval; 1/480 MHz = 2.0833 ns nominal
Level 1	575 mV	-
Level 2	− 575 mV	-
Point 1	0 V	20%
Point 2	0 V	80%
Point 3	150 mV	40%
Point 4	150 mV	60%
Point 5	−150 mV	40%
Point 6	−150 mV	60%

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3.4 USB 3.0 eye diagrams

If a connection is set up via a USB Gen1 or USB Gen 2 connection, a link training is performed as sequence, with the following steps:

1. Configuring and initializing of link
2. Bit-lock and symbol lock
3. Rx equalization training
4. Lane polarity inversion
5. Block alignment (USB Gen 2 only)

Training sequences are always 8b10b coded and not scrambled. Table 9 shows the most important normative requirements for USB3 Gen 1 and Gen 2 transmitters.

Table 9. Basic requirements for the USB3 transmitter

Symbol	explanation	Gen 1, 5 Gbit/s	Gen 2, 10 Gbit/s
UI	Unit Interval	199.94 ps (min); 200 ps (nom); 200.06 ps (max)	99.97 ps (min); 100 ps (nom); 100.03 ps (max)
$V_{TX\text{-}Diff\text{-}PP}$	Differential peak to peak TX voltage swing	0.8 V (min); 1V (nom); 1.2 V (max)	0.8 V (min); 1 V (nom); 1.2 V (max)
$V_{TX\text{-}DE_RATIO}$	TX de-emphasis	3 dB (min); 4 dB (max)	3-tap FIR equalizer
$R_{TX\text{-}DIFF\text{-}DC}$	DC differential impedance	72 Ω (min); 90 Ω (nom); 120 Ω (max)	72 Ω (min); 90 Ω (nom); 120 Ω (max)
$C_{AC\text{-}COUPLING}$	AC coupling capacitor	75 nF - 200 nF	75 nF - 265 nF
$T_{TX\text{-}EYE}$	Transmitter eye width	0.625 UI (incl. all jitter sources)	0.625 UI (incl. all jitter sources)

Table 10 is the equivalent list for the receiver side of the super-speed USB interface. The minimum height of the receiver eye is quite low. The open width is also much smaller compared to USB super-speed.

Table 10. Basic requirements for the USB3 receiver

Symbol	explanation	Gen 1, 5 Gbit/s	Gen 2, 10 Gbit/s
UI	Unit Interval	199.94 ps (min); 200 ps (nom); 200.06 ps (max)	99.97 ps (min); 100 ps (nom); 100.03 ps (max)
$V_{RX\text{-}DIFF\text{-}PP\text{-}POST\text{-}EQ}$	Differential peak to peak RX voltage swing	100 mV (min)	70 mV (min)
RX equalizer	receiver equalizer	0 dB - 6 dB	0 dB - 6 dB
T_j	total jitter	0.66 unit intervals	0.714 unit intervals
$R_{RX\text{-}DIFF\text{-}DC}$	DC differential impedance	72 Ω (min); 90 Ω (nom); 120 Ω (max)	72 Ω (min); 90 Ω (nom); 120 Ω (max)
$C_{AC\text{-}COUPLING}$	AC coupling capacitor	75 nF - 200 nF	75 nF - 265 nF

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Figure 14 shows the receiver mask for 5 Gbit/s, and Figure 15 depicts the related mask for 10 Gbit/s. The mask in the USB 3.0 Gen 1 scenario has a minimum eye height of 100 mV whereas the eye height in USB 3.0 Gen 2 scenario is only 70 mV. The minimum eye width is 0.34 unit intervals, respectively 0.286 unit intervals, in the 10 Gbit/s scenario. Moreover, the shape of the mask is also different. In the 5 Gbit/s scenario the mask has the shape of a rhombus whereas the shape in the 10 Gbit/s scenario is like the USB 2.0 scenario, with a 0.1-unit interval width for the upper and lower mask borders.

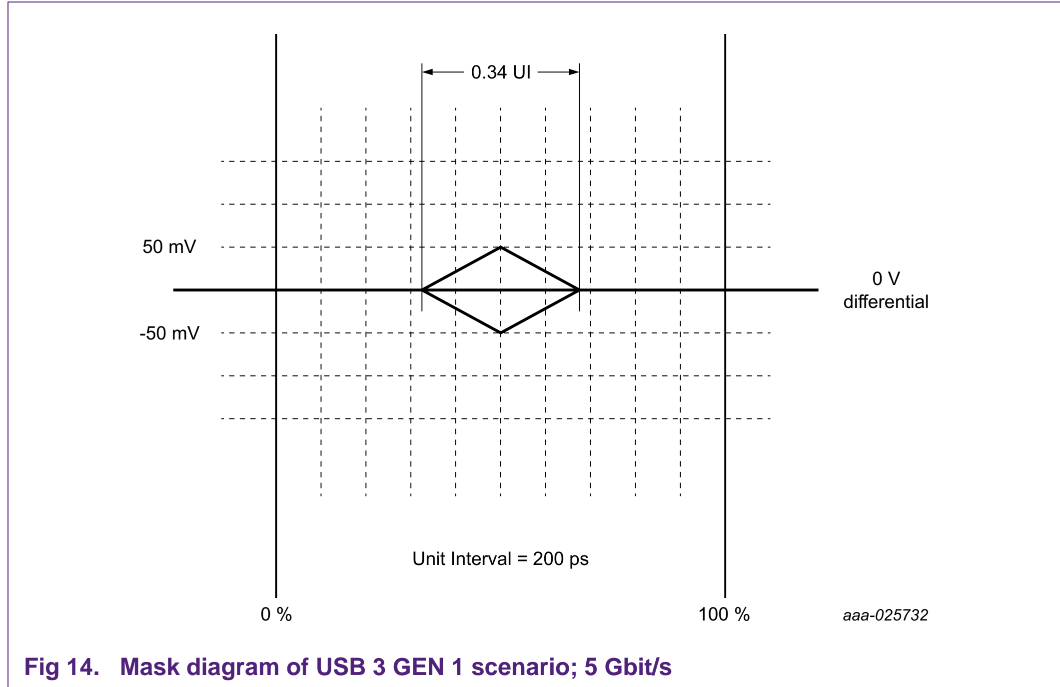

Fig 14. Mask diagram of USB 3 GEN 1 scenario; 5 Gbit/s

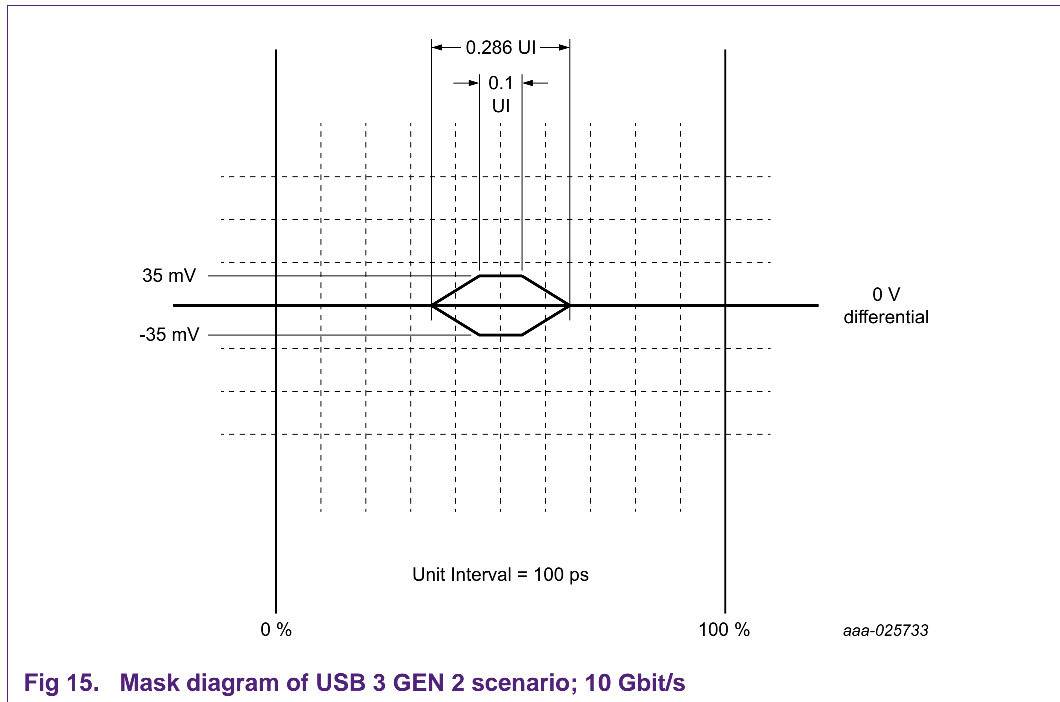

Fig 15. Mask diagram of USB 3 GEN 2 scenario; 10 Gbit/s

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3.5 USB Type-C

The user-friendly 24-pin connector allows reversible plugs. The innovative connector type supports up to USB 3.0 Gen 2 speed with10 Gbit/s, as well as USB power delivery 2.0. Full-feature cables are electronically marked with an identification IC. Alternate modes can be set up via the dedicated configuration channels, with vendor defined messages (VDM).

The Type-C connector can support various other standards beside USB. These are Display Port (DP), Thunderbolt 3, MHL, PCI Express and Base-T Ethernet. Various dongles that convert from USB Type-C to legacy connectors or other interface standards like HDMI are available on the market.

In Table 11 the USB operation with Type-C connector is listed. The 24 pins are organized in two groups of 12 pins each; i.e. group A and group B. Pins are available for four differential pairs with Super Speed operation (two lanes each for RX_P/RX_N and TX_p/TX_n). Moreover, two pins for USB 2.0 lane pair (Dp/Dn), two configuration channel pins (CC1 and CC2) and two sideband usage (SBU) pins. Additionally 4 Ground and 4 V_{BUS} pins that ensure low resistance for the power path.

Table 11. USB Type-C pin assignment

Pin number	Signal name	explanation
A1	GND	Ground
A2	SSTXp1	Super Speed differential TX pair 1, positive signal
A3	SSTXn1	Super Speed differential TX pair 1, negative signal
A4	V_{BUS}	Bus Power line
A5	CC1	Configuration Channel 1
A6	Dp1	USB 2.0 differential pair 1, positive signal
A7	Dn1	USB 2.0 differential pair 1, negative signal
A8	SBU1	Sideband Usage signal 1
A9	V_{BUS}	Bus Power line
A10	SSRXn2	Super Speed differential RX pair 2, negative signal
A11	SSRXp2	Super Speed differential RX pair 2, positive signal
A12	GND	Ground
B1	GND	Ground
B2	SSTXp2	Super Speed differential TX pair 2, positive signal
B3	SSTXn2	Super Speed differential TX pair 2, negative signal
B4	V_{BUS}	Bus Power line
B5	CC2	Configuration Channel 2
B6	Dp2	USB2 differential pair 2, positive signal
B7	Dn2	USB2 differential pair 2, negative signal
B8	SBU2	Sideband Usage signal 2
B9	V_{BUS}	Bus Power line
B10	SSRXn1	Super Speed differential RX pair 1, negative signal
B11	SSRXp1	Super Speed differential RX pair 1, positive signal
B12	GND	Ground

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As soon as the connection is established, the orientation of the cable connection is detected via the CC pins. The type-C cable has one physical CC wire only. With this single connection both ends of the cable can detect the appropriate super-speed lines needed for data exchange:

For example, the connection process of a downstream facing port (DFP) to an upstream facing port (UFP) occurs, as follows:

1. DFP to UFP attach/detach detection
2. Plus orientation/cable twist detection
3. Initial DFP-to-UFP (host to device) and power relationship detection
4. USB Type-C VBUS current detection and usage
5. USB power delivery (PD) communication
6. Discovery and configuration of functional extensions

Figure 16 depicts a DFP to UFP connection scenario. On the DFP side, pull-up resistors Rp are implemented towards a positive supply voltage. On the other end of the cable pull-down resistors are connected to ground.

Please note that per default, a current source can be configured instead of using RP pull-up resistors. The node with the higher voltage of the two
CC pins indicates the direction of the connection. Ra is available for powered cables and audio adapters, as shown in Table 14 below. The Rp value can detect 5 V-current capability.

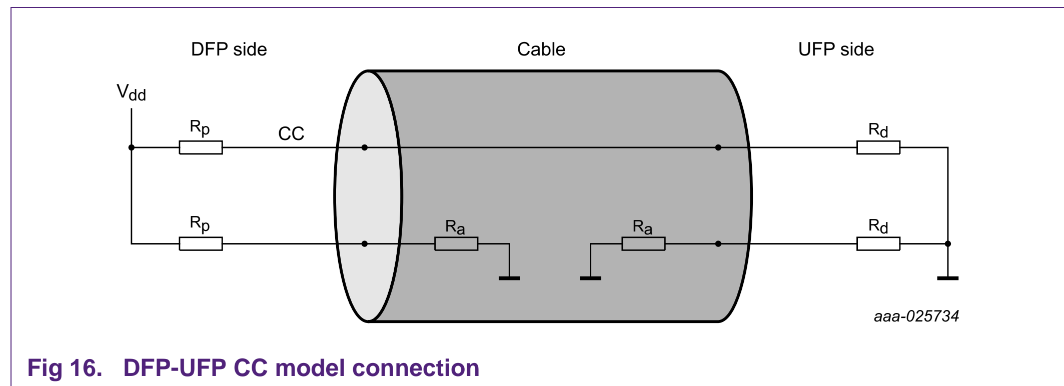

Fig 16. DFP-UFP CC model connection

In Table 12 the value for the pull-up resistor Rp and the related power rating is shown for either a 5 V or 3.3 V supply connected to the pull-up as supply voltage. Alternatively, the standard also allows the use of a current source instead of pull-up resistors.

Table 13 defines how the pull-down resistor Rd is specified. The nominal termination is a 5 kΩ resistor. Voltage clamping does not allow detection of power capability. For this function the tolerance of Rd needs to be ± 10% at least.

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Table 12. Down-stream port (DFP) Rp requirements

DFP Dedication	Current Source to 1.7 V - 5.5 V	Pull-up resistor to 4.75 V - 5.5 V	Pull-up resistor to 3.135 V - 3.465 V
Default USB power	80 μA ± 20%	56 k ± 20%	36 ± 20%
1.5 A/5 V	180 μA ± 8%	22 k ± 5%	12 ± 5%
3.0 A/5 V	330 μA ± 8%	10 k ± 5%	4.7 k ± 5%

Table 13. Up-stream port (UFP) Rd requirements

Rd implementation	Nominal value	Power detection capability	Maximum voltage at the CC pin
± 20% voltage clamp	1.1 V	no	1.32 V
± 20% resistor to GND	5.1 k Ω	no	2.18 V
± 10% resistor to GND	5.1 k Ω	yes	2.04 V

The Ra termination resistor has a nominal resistance of 1 kΩ, as shown in Figure 16. It is often applied via a depletion FET that limits the current after detection process, as shown in Figure 17

As soon as the pitch-off voltage of the depletion FET is reached, the current increases the voltage level in Ra at the source of the depletion FET until it clamps the current to a maximum value. Thus, reducing power loss whenever the 5 V supply voltage Vconn is switched to the CC line.

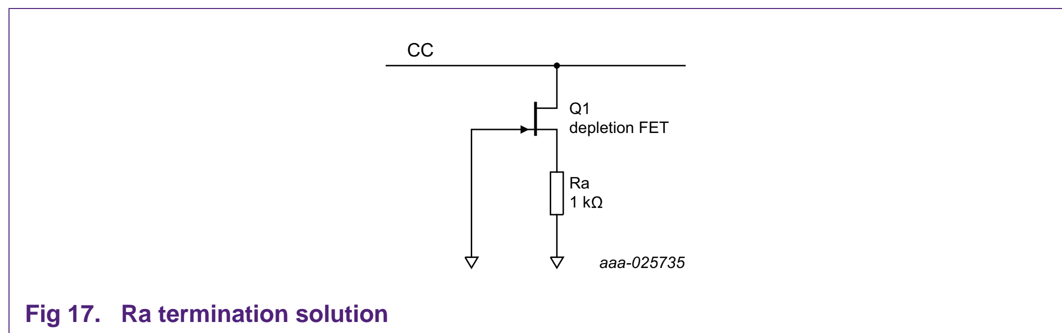

Fig 17. Ra termination solution

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Table 14 is a list of states that result from CC line termination in a DFP-UFP connection.

Table 14. CC connection model for a DFP-UFP scenario

CC1	CC2	State
open	open	nothing attached
Rd	open	UFP attached
open	Rd	UFP attached
Ra	open	powered cable, no UFP attached
open	Ra	powered cable, no UFP attached
Ra	Rd	powered cable and UFP attached
Rd	Ra	powered cable and UFP attached
Rd	Rd	debug accessory mode attached
Ra	Ra	audio adapter accessory mode attached

4. HDMI interfaces

4.1 Introduction to HDMI interfaces

High Definition Multimedia Interface (HDMI) is a digital interface in consumer and computing applications. HDMI is similar to DVI but also includes consumer electronics control (CEC). Video data is transmitted without data compression whereas audio can be used with or without data compression.

The interface is HDCP copy-protected. High-speed data is transmitted via transition minimized differential signaling (TMDS) lines. The interface uses three TMDS lanes and one additional channel for the clock signal.

As of HDMI 1.4, HDMI also supports an ethernet data channel on the HEC lane. The display data channel (DDC), that is similar to I2C, is used to exchange information. The resolution compatibility is supported whenever an HDMI connection is established. Thus, extended display identification data (EDID) can be read out.

4.2 Contact assignment for connectors

In Table 15 the contact assignments for Type A connectors, which are the most commonly used connectors in TVs, monitors, DVD players and computers, are listed. Type D micro-HDMI connectors are used for tablets, cameras and other mobile devices.

Table 15. Contact assignment for HDMI Type A and Type C connector

Contact Type A	Contact Type D	Signal description
Pin 1	Pin 3	TMDS Data2+
Pin 2	Pin 4	TMDS Data2 shielding
Pin 3	Pin 5	TMDS Data2-
Pin 4	Pin 6	TMDS Data1+
Pin 5	Pin 7	TMDS Data1 shielding

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Table 15. Contact assignment for HDMI Type A and Type C connector

Contact Type A	Contact Type D	Signal description
Pin 6	Pin 8	TMDS Data1–
Pin 7	Pin 9	TMDS Data0+
Pin 8	Pin 10	TMDS Data0 shielding
Pin 9	Pin 11	TMDS Data0–
Pin 10	Pin 12	TMDS clock+
Pin 11	Pin 13	TMDS clock shielding
Pin 12	Pin 14	TMDS clock–
Pin 13	Pin 15	CEC
Pin 14	Pin 2	reserved (HDMI1.0 -1.3), HEC data– (HDMI 1.4)
Pin 15	Pin 17	DDC clock (I²C-Bus, SCL)
Pin 16	Pin 18	DDC data (I²C-Bus, SDA)
Pin 17	Pin 16	Ground for DDC,CEC and HEC
Pin 18	Pin 19	– 5 V supply with 55 mA maximum current
Pin 19	Pin 1	Hot-Plug-Detection (all standards), HEC Data+ (HDMI 1.4)

4.3 HDMI key parameters connection structure

HDMI introduced consecutively additional standards with higher data rates that are necessary for high resolution displays. Table 16 shows a brief overview of HDMI versions and contains maximum pixel rates, as well as maximum clock rates and TMDS bit rates. The table also lists maximum screen resolutions for consumer applications, and supported maximum color depths of the pixels. TMDS lines have a ratio between clock and bit rate of factor 10 for HDMI 1.4, and factor 100 for HDMI 2.0.

Table 16. List of HDMI key parameters for the different versions

HDMI version	1.0	1.1	1.2	1.3	1.4	2.0
Maximum pixel clock rate (MHz)	165	165	165	340	340	600
Maximum TMDS bit rate per lane including 8b/10b coding overhead (Gbit/s)	1.65	1.65	1.65	3.4	3.4	6
Maximum total TMDS throughput including 8B/10b coding overhead (Gbit/s)	4.95	4.95	4.95	10.2	10.2	18
Maximum audio throughput bit rate (Mbit/s)	36.86	36.86	36.86	36.86	36.86	49.152
Maximum video resolution over 24 bit/pixel single link	1920*1200 p/ 60 Hz	1920*1200 p/ 60 Hz	1920*1200 p/ 60 Hz	2560*1600 p/ 60 Hz	4096*2160 p/ 30 Hz	4096*2160 p/ 60 Hz
Maximum color depth (bit/pixel)	24	24	24	48	48	48

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Figure 18 shows the basic HDMI TMDS data connection structure of transmitters and sink connectors. The transmitter has a switched current source of 10 mA. A differential signal connection with matched impedance builds the data path to the receiver. The receiver terminates each signal line of the differential interface with 50 Ω to a 3.3 V supply line. This leads to a single-ended nominal voltage swing of:

500 mV with VSE= 10 mA x 50 Ω.

Consequently, the nominal differential voltage swing is 1 V, which is twice the value of a single-ended data line. The differential nominal termination is 100 Ω, which is twice the value of the single-ended pull-up resistors of the HDMI sink connectors. The impedance matching has to be kept in a 85 Ω to 115 Ω window, i.e. 100 Ω ± 15%; in order to comply with HDMI specification.

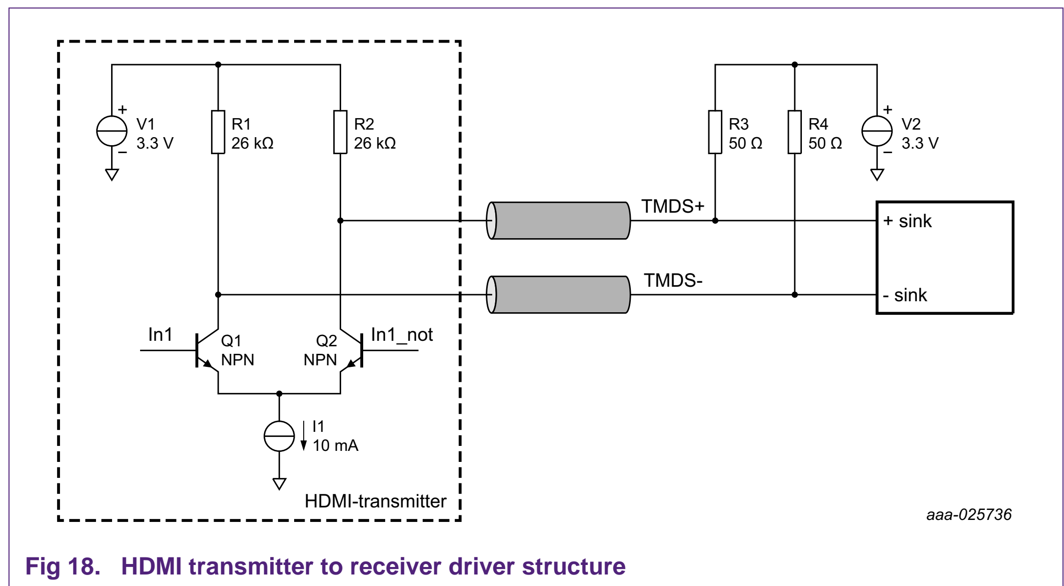

Fig 18. HDMI transmitter to receiver driver structure

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Figure 19 shows the HDMI 1.4 transmitter mask, as well as upper and lower limits of the TMDS line voltage. The eye has a minimum height of 400 mV, and a width of 0.7 unit intervals.

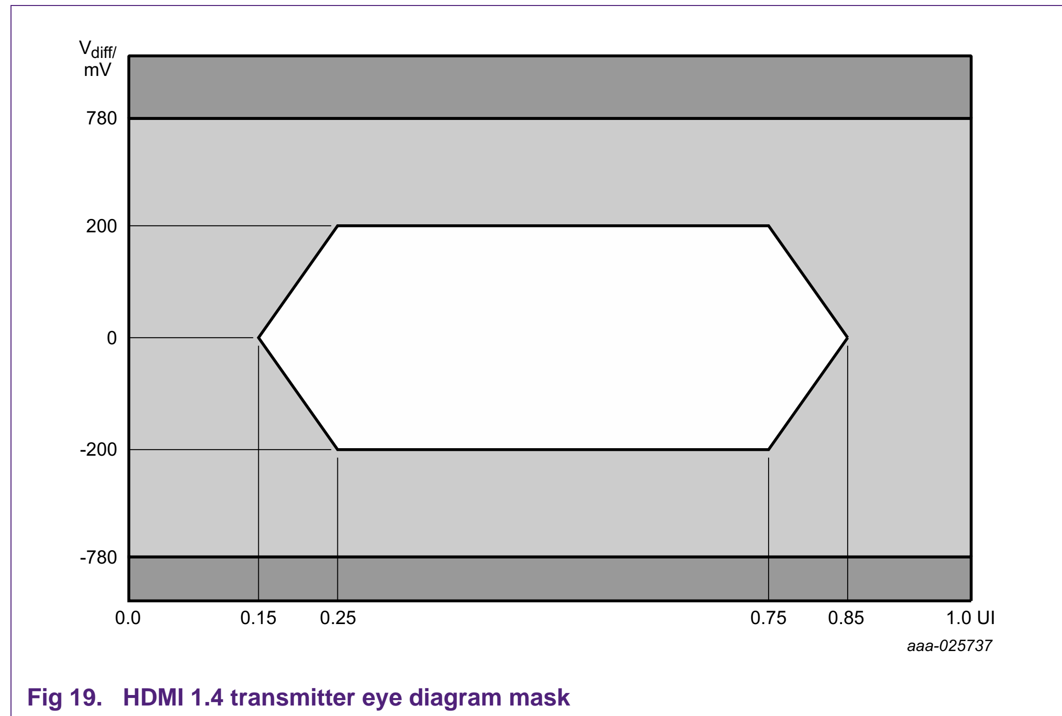

Fig 19. HDMI 1.4 transmitter eye diagram mask

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Figure 20 depicts the HDMI 1.4 receiver mask. Eye height is 300 mV (± 50 mV) and eye width has to be at minimum 50% of the unit interval.

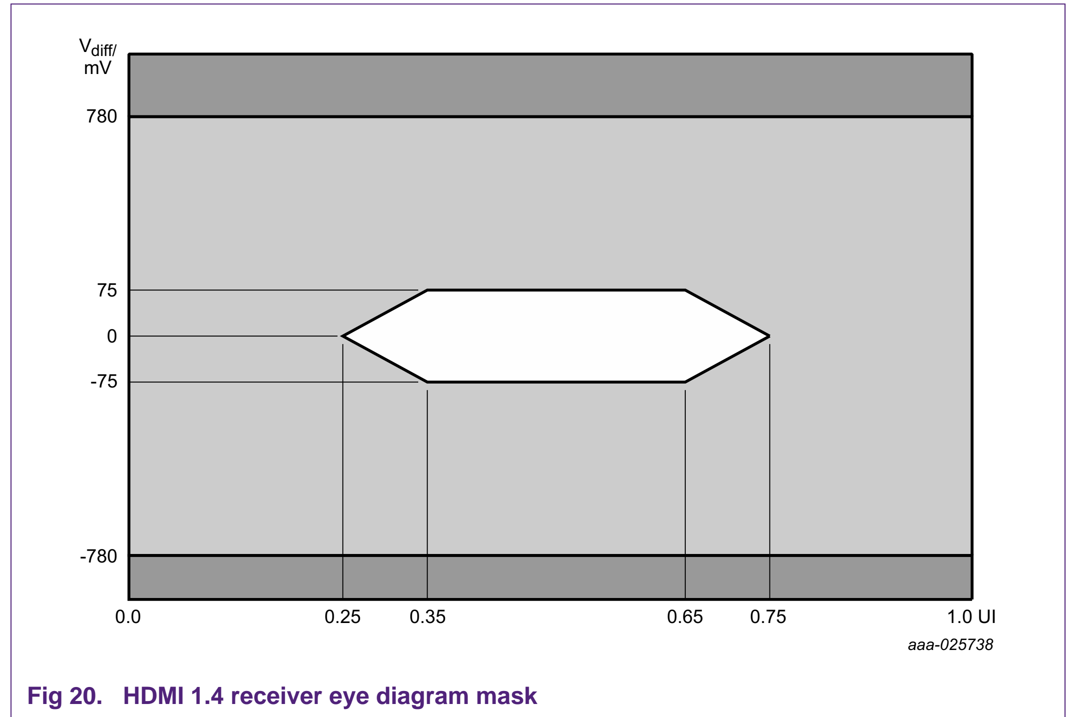

Fig 20. HDMI 1.4 receiver eye diagram mask

Figure 21 shows the set-up of eye diagrams for eye diagram measurements with HDMI 2.0 at the source test points. TP1 is located on the receptacle plug of the pattern generator, with the test point adapter (TPA). A worst cable emulator is placed between TPA-P and reference cable equalizer, followed by the TP1_EQ.

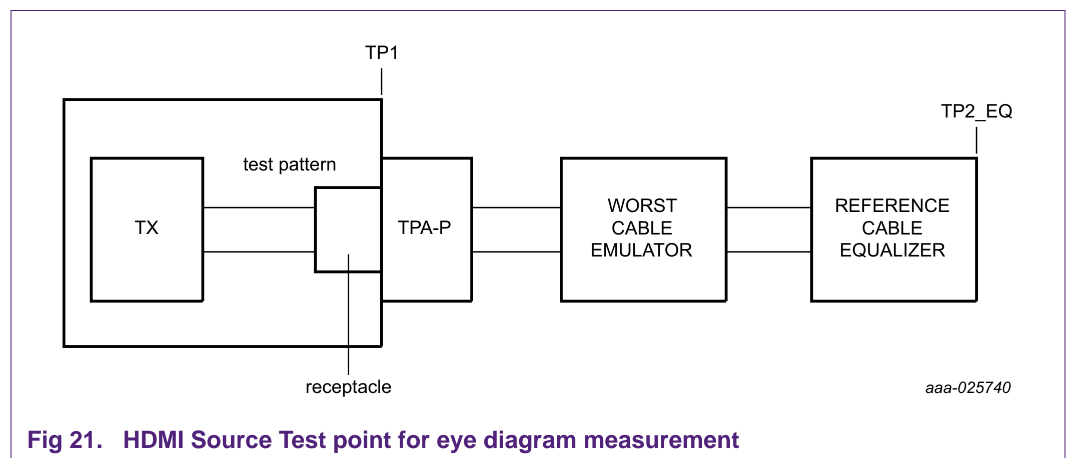

Fig 21. HDMI Source Test point for eye diagram measurement

Figure 22 depicts the HDMI 2.0 mask diagram for test point TP2_EQ. Eye height H and eye width V depend on the HDMI bit rate, as shown in Table 17. In order to achieve the maximum bit rate of 6 Gbit/s, a minimum eye height of 150 mV and a maximum data jitter of 0.6 unit intervals is necessary; with total data jitter T_j = 1 -H.

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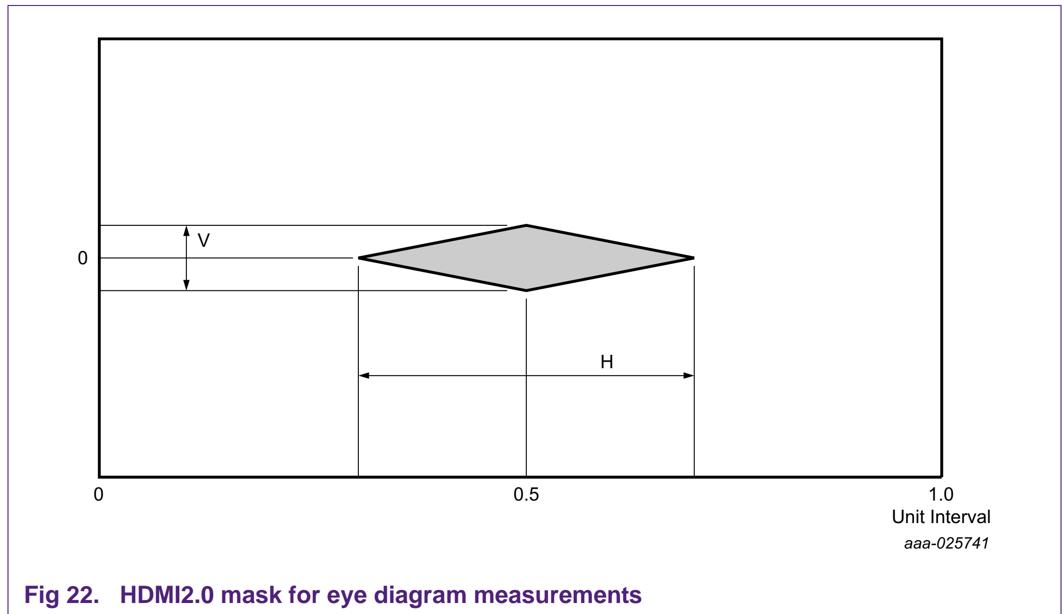

Fig 22. HDMI2.0 mask for eye diagram measurements

Table 17. Mask size in dependency of the Bit Rate (Gbit/s)

TMDS Bit Rate (Gbit/s)	Mask width H (UI)	mask height V (mV)
3.4 < bit rate ≤ 3.712	0.6	335
3.712 < bit rate ≤ 5.94	– 0.0332 * (bit rate)² + 0.2312 * (bit rate) + 0.1998	– 19.66 * (bit rate)² + 106.74* (bit rate) + 209.58
5.94 < bit rate ≤ 6.0	0.4	150

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5. ESD testing standards and TLP testing

5.1 ESD testing standard IEC6100-4-2

IEC61000-4-2 is a testing standard for ESD robustness testing that defines test methods and configuration environment. The IEC61000-4-2 standard is commonly used to certify electronic equipment. Devices have to be protected against electrostatic discharges using components able to clamp and resist the high voltages, as defined by the respective IEC standards. The robustness of these devices has to be checked and guaranteed.

Most ESD discharges occur unnoticed by users but can seriously damage gate oxides of MOSFETs that are used in the data path of most interfaces. In some cases, small flashes indicate that sudden ElectroStatic Discharge (ESD) have occurred. The aftereffects are high leakage currents and malfunction of input and output circuits. The triboelectric charging effect is caused by contact and/or rubbing of different materials against each other. Electrostatic induction is a redistribution of electrical charge in an object that is caused by the influence of nearby charges.

Please note that when ESD protection components are mounted in a product to protect some of its sensitive parts, the behavior of this component must be tested in its final application environment.

ESD pulses are generated with an ESD gun that consists of an adjustable high voltage source with maximum of 30 kV. A 150 pF capacitor is charged through a resistor with 50 to 100 M Ω, using a charging switch. The capacitor is discharged through a 330 Ω resistor if the discharge switch is closed.

Figure 23 shows a basic ESD pulse generator schematic.

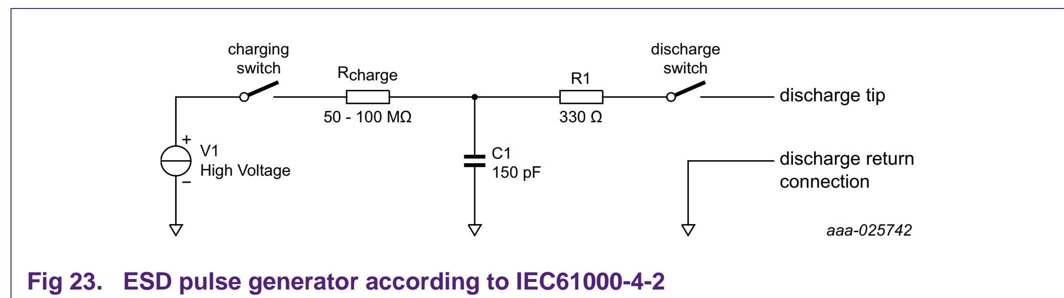

Fig 23. ESD pulse generator according to IEC61000-4-2

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Figure 24 shows the shape of the IEC61000-4-2 discharge current waveform of the described generator. The curve behaves in the following way:

1. The pulse rises within 0.7 ns to 1 ns
2. The first spike reaches its peak current with peak value I_{PP}
3. The pulse then declines within about 80 ns and includes a shoulder-shape curve

Most of the surge pulse energy is carried by the shoulder. The first spike stresses the target with high voltage and high current but with less energy; because duration is short.

Two methods are used for ESD testing: The contact measurement method and the air discharge measurement method.

The contact measurement method is the recommended IEC61000-4-2 method for ESD protection components and is set-up as described below:

- The component is connected to ground. The ESD gun is connected to ground via the discharge return connection as well.
- The tip of the ESD gun is connected to the contact of the DUT to be tested.

Please note that no additional resistors are used in the ground path of the gun like described in IEC61000-4-2 (2 × 470 kΩ). The contact discharge connection allows good reproducibility of test results. Please refer to IEC61000-4-2, for more details.

Table 18 lists current values for predefined IEC61000-4-2 levels, i.e. ESD levels 1 to 4, for respective peak currents, 30 ns and 60 ns.

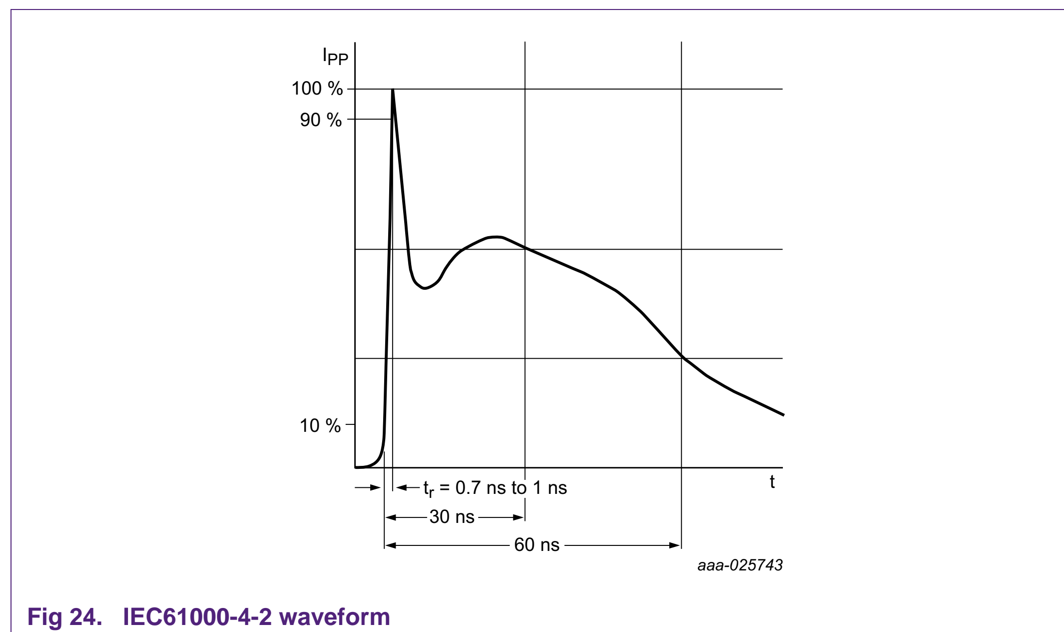

Fig 24. IEC61000-4-2 waveform

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Table 18. ESD test waveform parameters

ESD level	voltage	first peak current, +/- 10%	Current (+-30%) at 30 ns	Current (+-30%) at 60 ns
1	2 kV	7.5	4	2
2	4 kV	15	8	4
3	6 kV	22.5	12	6
4	8 kV	30	16	8

Figure 19 shows the definition of IEC61000-4-2 ESD levels with the related minimum discharge voltages for contact and air discharge testing.

Table 19. ESD levels as defined in IEC61000-4-2

ESD level	contact discharge	air discharge
1	2 kV	2 kV
2	4 kV	4 kV
3	6 kV	8 kV
4	8 kV	15 kV

For air discharge the tip of the ESD gun is narrowed slowly towards the target until a flash strikes over. The results depend very much on air humidity, speed of the decreasing of distance between target and gun and shape of electrodes and the level of reproducibility is low. Often corona discharge can be noticed and no flash if the shape of one of the two electrodes has a sharp end. In such case the stress for the ESD device is very low and do not lead to usable results. For the gun side a tip with a round end is defined for air discharge whereas the tip for contact discharge has a sharp end. The air discharge waveform has a less steep rising edge and the peak values of the surge pulses are lower.

Therefore air discharge robustness is higher or equal compared to contact discharge.

Please note that technical documents must be regarded with much scepticism if air discharge ratings are presented with much higher values than for contact discharge; often with a factor of roughly 2 like the ESD level 4 definition in Table 19. It is a proven fact that for low capacity ESD protection devices the air discharge robustness is a few kV higher or equal compared to contact discharge robustness.

5.2 Reproducibility aspects for IEC61000-4-2 testing

Figure 25 shows that the ESD gun waveform is not fully reproducible: A NoiseKen gun is shooting in repeat mode at a target while an F-65 current probe is measuring the current waveform. The second peak, which is located on the shoulder behind the first peak, is stable and is well within the IEC61000-4-2 specification. However, the voltage of the first peak shows a big variation from +25% to -35%. If target systems are sensitive to the first peak of an ESD event, test results can show a big spread and wrong decisions can be taken in the selection process of protection devices.

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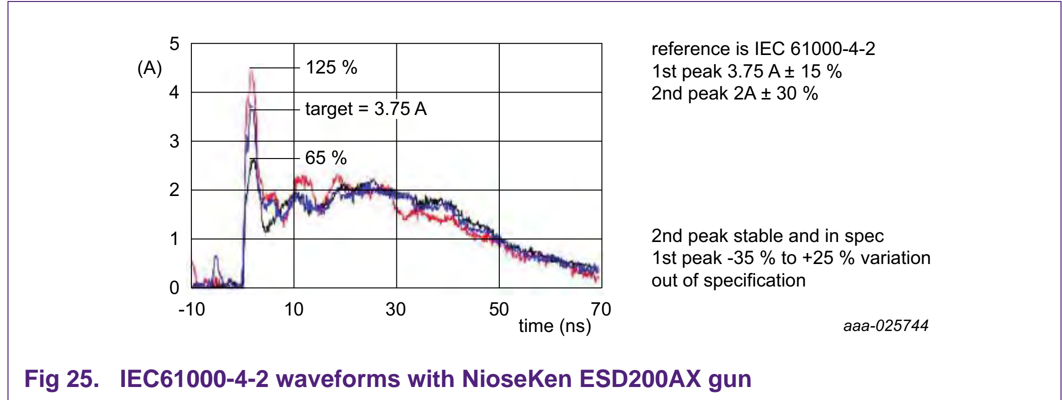

Fig 25. IEC61000-4-2 waveforms with NioseKen ESD200AX gun

Please note that the grounding condition has a big impact on the voltage level of the first peak as well. If there is no proper ground close to the DUT, a small residual capacitance to ground occurs. If this is the case, the first peak loses its height and can mostly disappear.

Figure 26 shows the current waveforms of two ESD gun types with and without proper grounding. In set ups without proper grounding test results are unreliable.

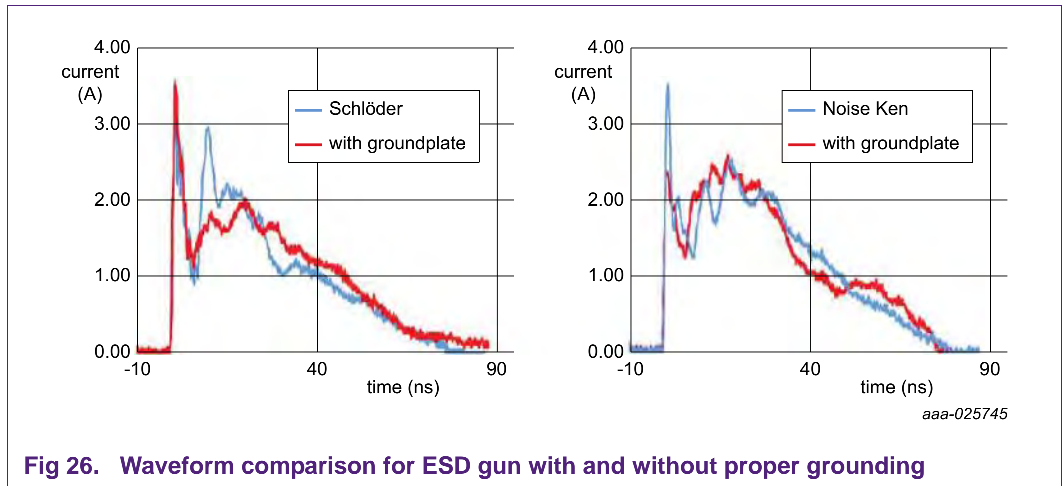

Fig 26. Waveform comparison for ESD gun with and without proper grounding

Another risk in ESD gun testing arises when the gun is not safely connected to the DUT for contact discharge. Figure 27 shows the circuit of an ESD gun with a parasitic tip capacitance Ct, which is roughly 40 pF. The 40 pF are significantly high compared to the nominal 150 pF of the ESD gun.

When a triggered gun misses the target or when charge moves across the switch S2, the Ct charge can discharge into the DUT with mostly no series impedance. This is the reason that the first peak of a stray pulse can exceed the regular pulse by factor 2, as illustrated by the red curve in the diagram.

In conclusion, if a system is tested that shows an ESD sensitivity on the first peak, unsafe ESD gun connection can lead to a damage at a comparably low testing voltage, wrong test results and ESD device selection.

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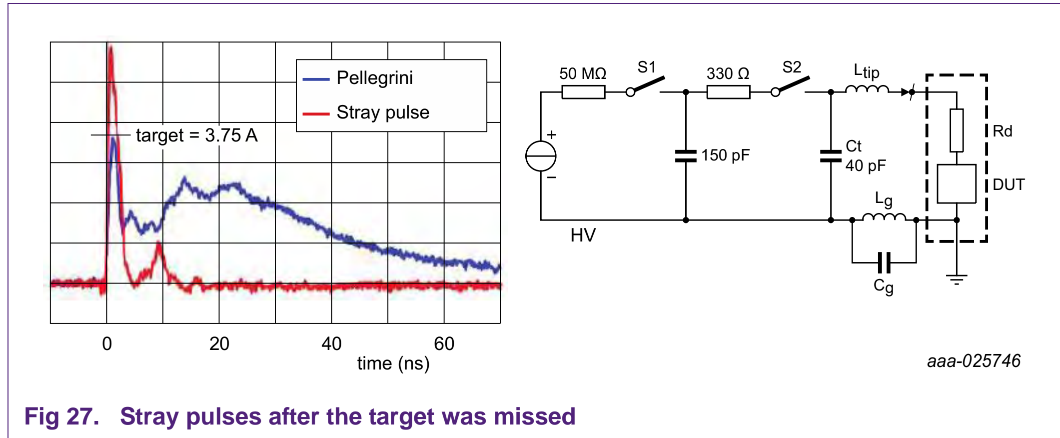

Fig 27. Stray pulses after the target was missed

5.3 Surge testing standard IEC 61000-4-5

Testing according to IEC 61000-4-5 makes use of test pulses that are much wider than the ESD testing according to IEC61000-4-2 discussed in the previous chapter.

The energy of surge pulses, as defined by the IEC61000-4-5 standard, is much higher. Consequently, an ESD protection part has to dissipate more heat. The IEC61000-4-5 standard approach simulates surge events, for instance in scenarios like power supply voltage overshoots created by load changes or overshoots caused by the plug-in procedure of chargers.

Table 20 lists key waveform data of IEC61000-4-5 surge pulses. For the short-circuit condition of the surge generator, 8 μs rise time and 20 μs fall time to 50% voltage level are defined and well known as 8/20 μs surge test.

Table 21 depicts the relation between the peak voltage for the open circuit condition and the peak current for the short circuit case. Output impedance of a surge generator is considered to be 2 Ω.

Table 20. Surge pulse waveform parameters

operating mode	Front time in μs	time down to 50% value in μs
open-circuit voltage	1.2 +/- 30%	50 +/- 20%
short-circuit voltage	8 +/- 20%	20 +/- 20%

Table 21. Open-circuit peak voltage and related peak current for the short-circuit

open circuit peak voltage +/-10%	short-circuit peak current +/-10%
0.5 kV	0.25 kA
1.0 kV	0.50 kA
2.0 kV	1.00 kA
4.0 kV	2.00 kA

Figure 28 shows the waveform for the open circuit condition, whereas Figure 29 depicts the surge pulse waveform for the short circuit scenario.

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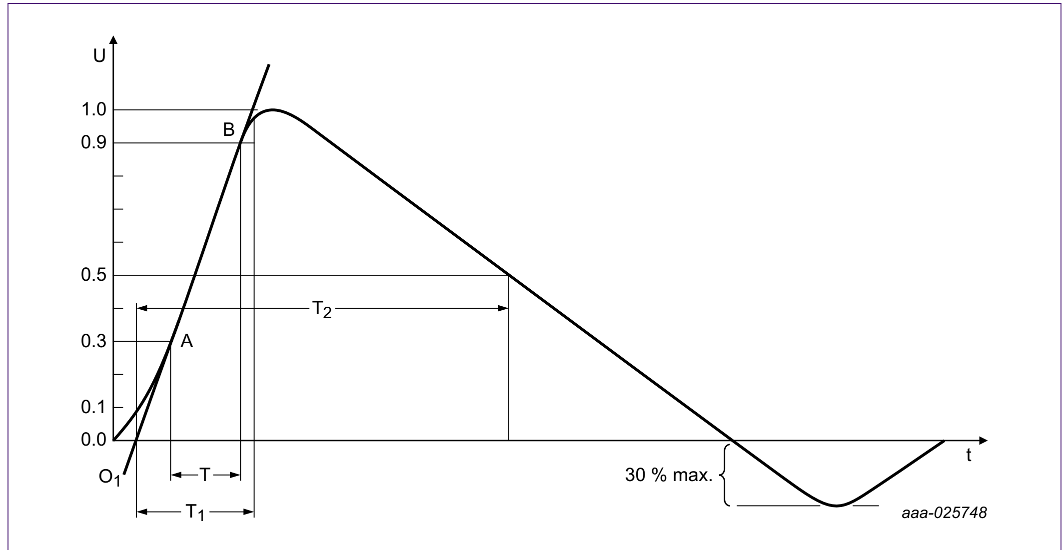

Fig 28. IEC61000-4-5 waveform for open circuit condition

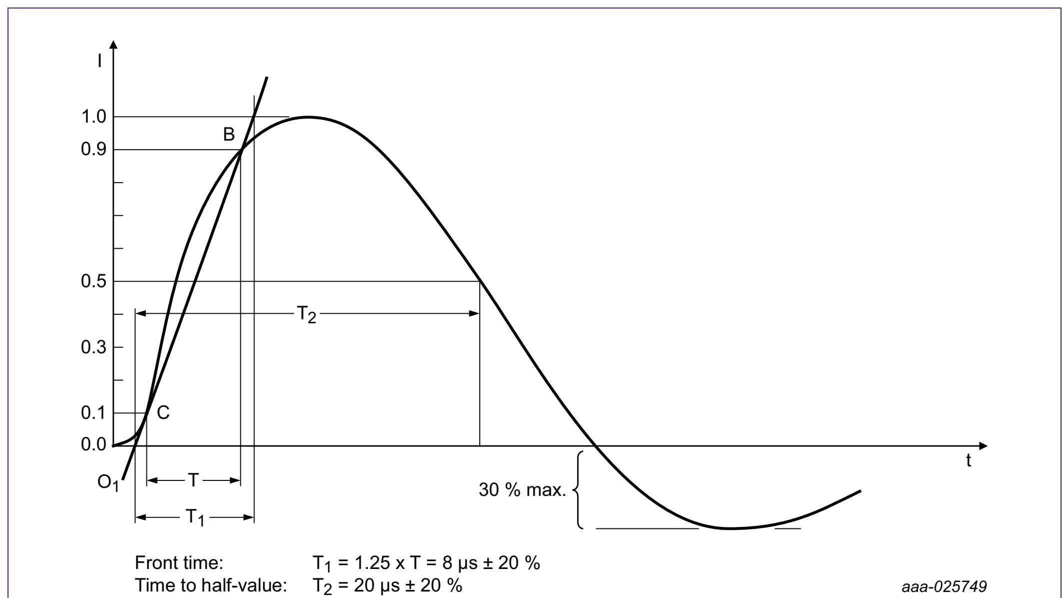

Fig 29. IEC61000-4-5 waveform for short circuit condition

IEC61000-4-5 test results deliver important data sheet parameters for ESD and surge protection devices:

- Maximum surge current — I_{PP}
- Peak power — P_{PP}
- Clamping voltage — V_{CL}
- Dynamic resistance — R_{dyn} - derived from the steepness of the V_{CL} versus I_{PP} curve

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5.4 TLP testing

Transmission-Lne Pulse (TLP) is a new measurement technique which is used to characterize complete interfaces or ESD protection components.

TLP is a short-duration rectangular pulse in a controlled-impedance environment of 50 Ω. The controlled impedance improves test accuracy and reproducibility of measurements. TLP characterizes performance attributes of devices under stresses that have a short pulse width and fast rise time. Low duty cycles prevent heating.

The TLP test environment shown in Figure 30, can be described as follows: A generator charges a 50 Ω transmission line with pre-adjusted voltage. The energy is applied to a Device Under Test (DUT). The current into the DUT is measured with a current probe and the voltage at the device is fed to a high-speed oscilloscope. The pulse length and rise and fall times can be changed at the generator. The typically applied standard pulse duration is 100 ns and rise and fall times are each 10 ns.The minimum programmable transition times are 300 ps.

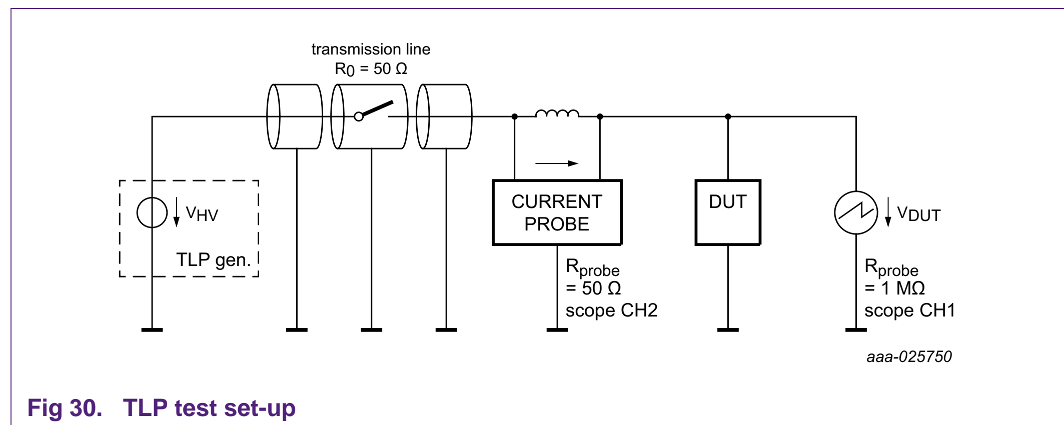

Fig 30. TLP test set-up

The TLP test is performed starting gradually from low pulse voltages to higher voltages, with a pre-defined step width.

As shown in the TLP measurement voltage and current traces depicted in Figure 31 the voltage and current samples are averaged for a window of 20 ns, which is located in a temporal window from 70 ns to 90 ns within the 100 ns test pulse. This window-based method eliminates noise. The location of the window ensures that the system is settled so that run-in effects like overshoots are neglected. Each measurement result becomes a point on the TLP graph that shows a TLP I-V characteristic; i.e. the TLP-curve.

The steepness of the TLP curve ΔV/ΔI is equal to Rdyn; and an important parameter for the selection of ESD and surge protection devices.

TLP testing can be done with ESD protection devices but also with interface pins of complete systems with and without ESD protection. From the derived TLP curves conclusions can be drawn which protection device is suitable for a safe and reliable protection of a product.

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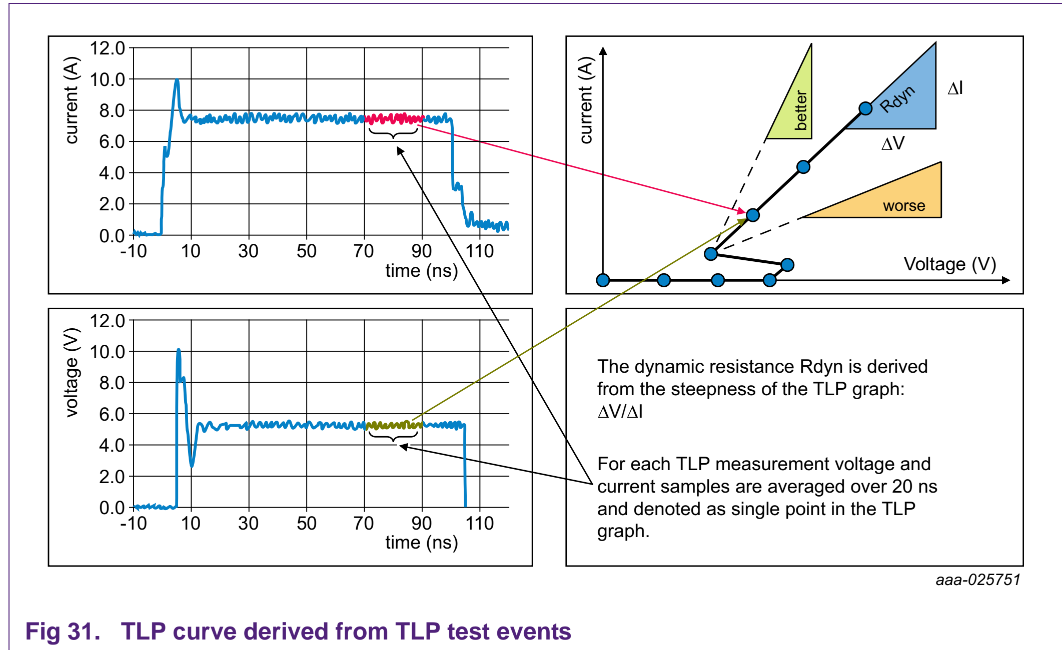

Fig 31. TLP curve derived from TLP test events

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5.5 vfTLP testing

A very similar testing method to TLP is very fast TLP (vfTLP). The test pulses that are applied to the target system have a length of 1 ns to 10 ns, as well as short rise and fall times of 100 ps to 600 ps. This is the major difference compared to conventional TLP testing.

Figure 32 shows the vfTLP measurement set-up. Due to short pulses, the current is not measured with a current probe. Instead, it is derived from separately measuring incident and reflected voltages with an oscilloscope. This is done in a similar way to time domain reflection (TDR) measurement. The current in the tested device (DUT) is calculated, as follows: $I_{DUT} = I_{incient} + I_{reflected} = (V_{incident} - V_{reflected}) / 50\ \Omega$

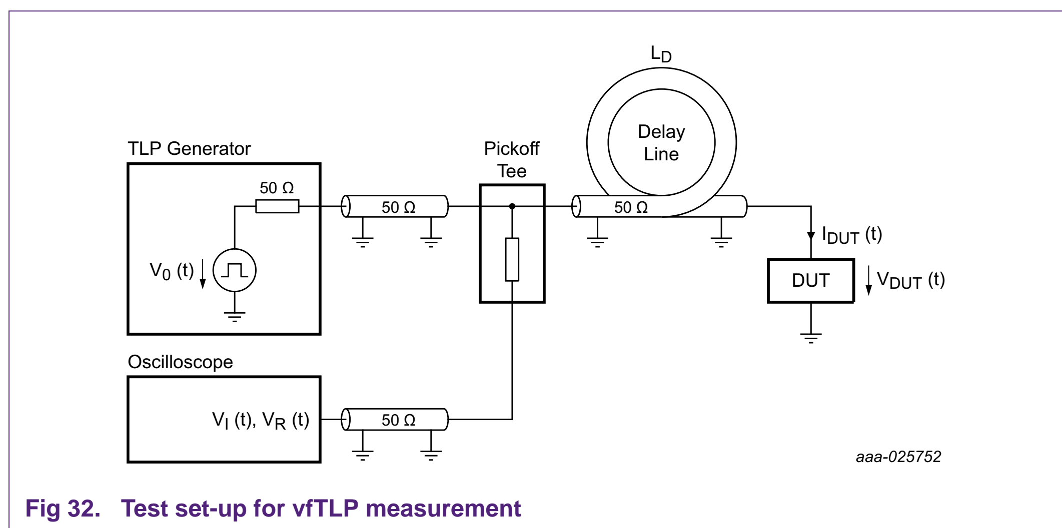

Fig 32. Test set-up for vfTLP measurement

In conclusion, vfTLP tests provide a good indication for determining the switching speed of ESD protection devices. The small pulse length is useful because the impact of the first overshoot of an ESD event on a target system, can be investigated.

In contrast to that, the 100 ns standard TLP pulses are roughly equivalent to the energy of a complete ESD pulse, in which the larger proportion of energy is carried in the wider second shoulder of the pulse.

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6. ESD protection and EMI filtering

6.1 Topology of ESD protection products

6.1.1 Introduction into ESD protection choices

A number of different approaches can be used to protect electronic devices against ESD and surge events:

- Narrow gap or spark gap approach:

  An easy and inexpensive approach is to add a narrow gap from ground to signal line. Whenever a bigger ESD event occurs, an air discharge limits a high voltage pulse. Spark gap components operate on the same physical principal. Thus, adding a spark gap to a signal line is a straightforward approach. The disadvantage of this kind of ESD protection is a poor performance in terms of the achieved clamping voltage that has a slow turn-on time and a very high trigger voltage. The average dielectric air strength is about 3.3 kV/mm. This is why a spark gap is not a good protection device choice for modern high-speed interfaces.

- Use of varistors:

  Often, varistors are used for ESD protection. These parts are made with ceramic ZiO grain material in a mixture with other metal oxides. Varistors have a symmetrical non-linear I-V curve which shows a high resistance for lower voltages. When the varistor reaches breakdown voltage, it starts conducting. Varistors deteriorate after high exposure to surge events. Older generation varistors show a very high first spike in IEC61000-4-2 testing. Newer generation varistors are much improved to predecessors. Unfortunately, the clamping voltage for the second shoulder remains significantly higher compared to silicon-based solutions. This is why varistors are not the first choice for protecting modern system chip interfaces.

- Silicon-based ESD protection:

  Silicon-based ESD protection shows no degradation after surge events, as long as the specified limits are obeyed. This is why they are preferred. Several topologies are available that provide ESD protection, ranging from a simple topology, as presented in Figure 33, to more sophisticated topologies, as presented in several scenarios on the subsequent pages.

Silicon-based ESD protection is recommended with best and lowest clamping voltage performance, as explained on the subsequent pages of this section.

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6.1.2 Unidirectional ESD protection with Zener diode

A very plain topology is when a Zener diode is put between ground and signal line, as depicted in Figure 33. Surge pulses are clamped to a voltage V_{CL} that is based on the following V_{CL} equation:

$$V_{CL} = V_{BR} + I_{PP} \times R_{DYN}$$

V_{BR} — breakdown voltage of ESD diode
Ipp — peak pulse current of surge pulse
Rdyn — steepness of I-V curve

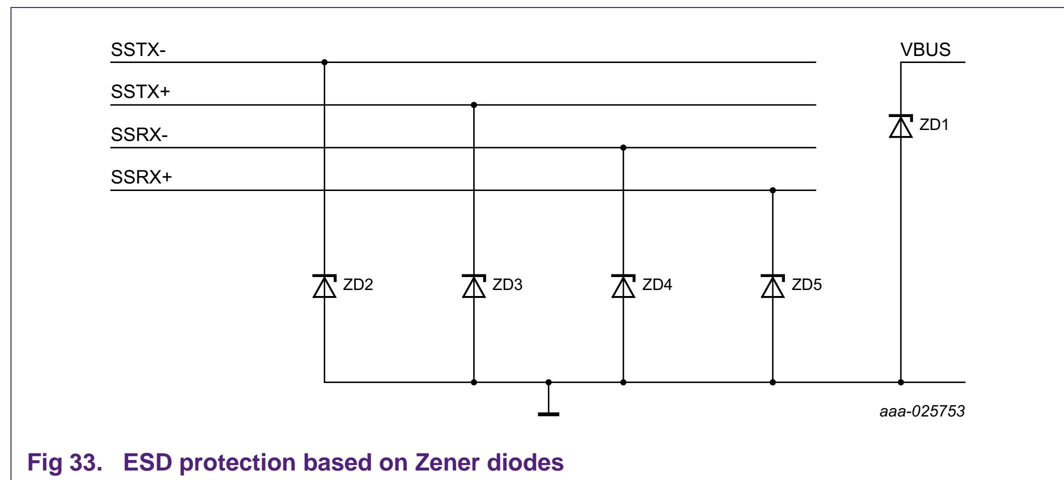

Fig 33. ESD protection based on Zener diodes

Figure 34 shows a typical Zener diode I-V curve.

The left half side of the curve shows the Zener diode in the reverse bias region. The current is very small, as long as the test or operating voltage remains below VRWM. VRWM is referred to as stand-off working voltage. Below this voltage, reverse leakage current is smaller than the specified IRM. When the voltage increases, current increases suddenly, at which the avalanche region begins; marked by the breakdown voltage VBR. The breakdown voltage is measured in a current-driven test set-up that pushes 1 mA through the diode.

The right half side of the curve shows the Zener diode in the forward bias region. The current is picking up if the voltage exceeds VF. Negative surge pulses are clamped to relatively low voltages (VF ~ -0.7 V). The described topology forms a unidirectional protection.

A Zener diode creates a unidirectional protection for an interface, clamping at considerably low voltages for negative surge events above Vf, as well as clamping voltage - according to the Vclamp equation - for positive surge events.

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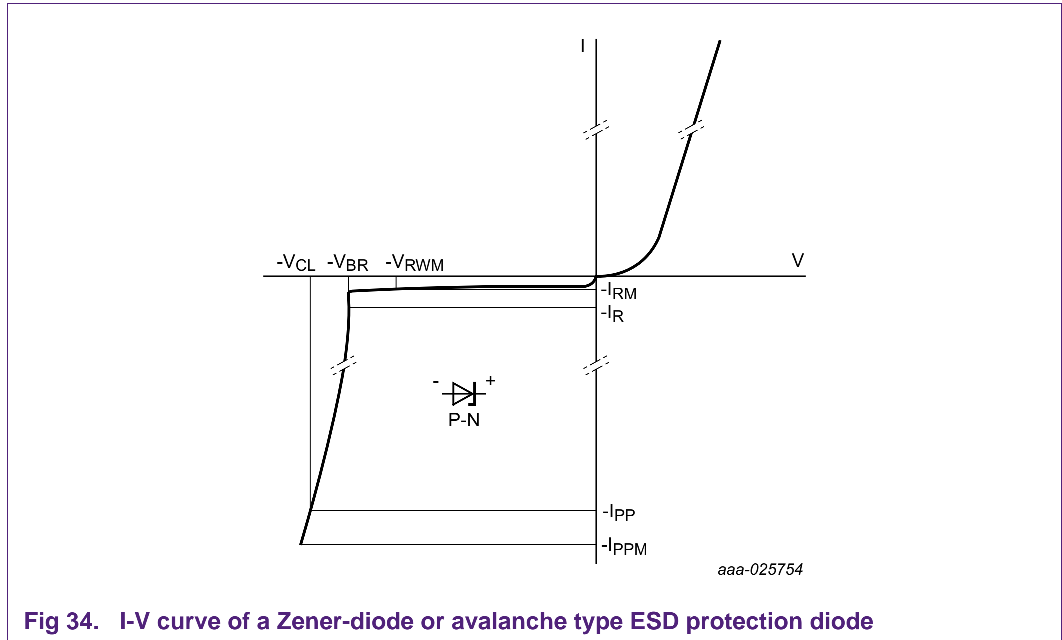

Fig 34. I-V curve of a Zener-diode or avalanche type ESD protection diode

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6.1.3 Bidirectional ESD protection with Zener diodes

If two Zener diodes with opposite directions are connected in a series, as shown in Figure 35, a bidirectional ESD device is created. If the two diodes are identical, the I-V curve is symmetrical, as depicted in Figure 36.

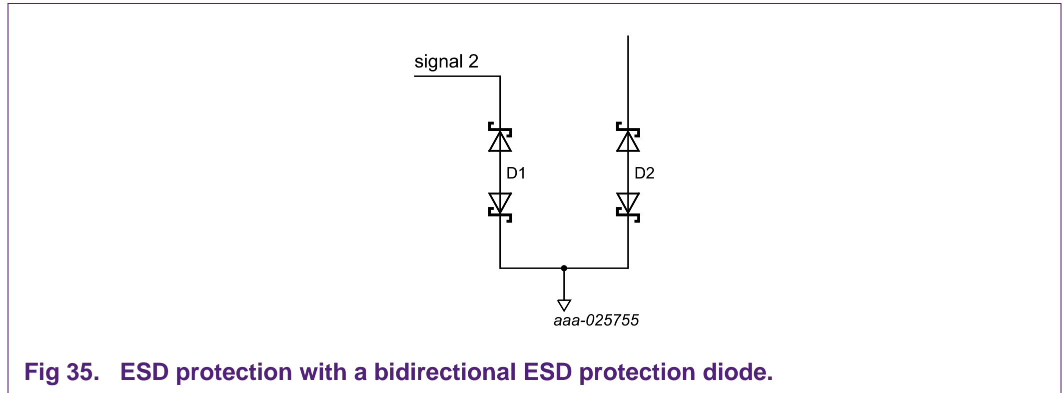

Fig 35. ESD protection with a bidirectional ESD protection diode.

Figure 36 shows the above mentioned characteristic, when both Zener diodes are identical.

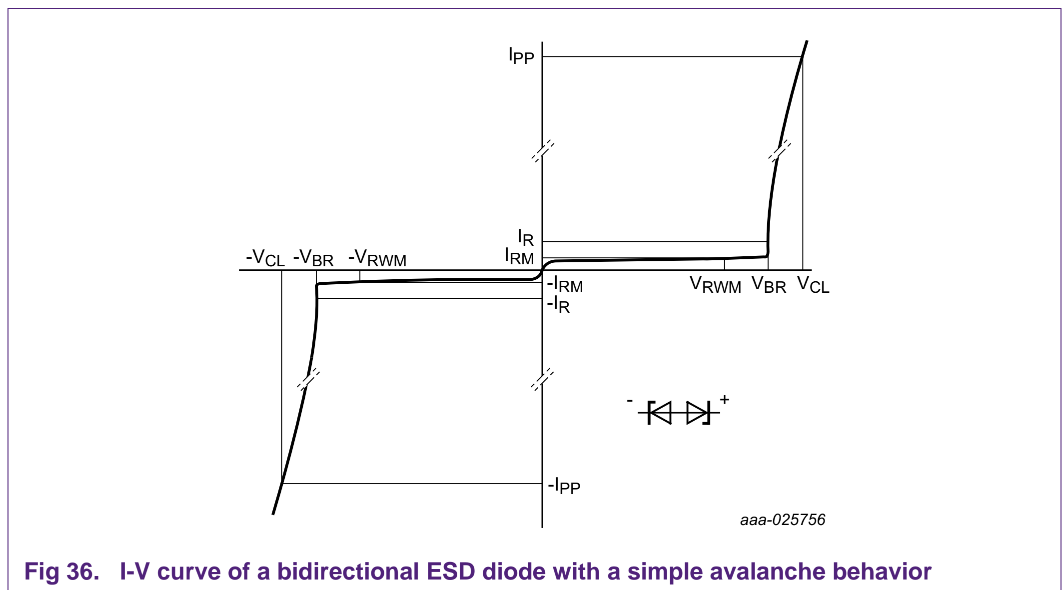

Fig 36. I-V curve of a bidirectional ESD diode with a simple avalanche behavior

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The calculation of the clamping voltage is the same as the equation for the reverse direction of unidirectional ESD diodes:

$$V_{CL} = V_{BR} + I_{PP} \times R_{DYN}, \text{ with } V_{BR} = V_{BR1} + V_F$$

The V_F value is adding a portion to V_{br} and the reverse breakdown V_{br1} of the other diode.

Bidirectional ESD protection has to be applied to interfaces that operate with positive and negative voltage ranges. For example, analog audio signals operate in this way. Most digital interfaces that only operate with positive operating voltages can be protected with an unidirectional solution. Neglecting this fact many designers make use of bidirectional ESD protection. The products are exposed to much higher negative clamping voltages for negative ESD strikes. This should be avoided if possible because the system level robustness can be badly affected by it.

This problem is relevant specifically when a system chip has to be protected against negative surge events with higher energy and longer pulse duration, as specified in the IEC61000-4-5 standard. If the surge protection addresses only ESD pulses according to IEC61000-4-2, a relatively insensitive chip might be sufficiently protected with a bidirectional topology.
For the design of low capacitance ESD protection components it can be helpful to choose a structure with two ESD diodes in series because the parasitic capacitance is lower compared to a unidirectional device as the below commonly known equation shows:
Another reason for choosing bidirectional ESD diodes is that the direction of mounting is

$$C_t = \frac{(C1 \times C2)}{C1 + C2}$$

not important.

6.1.4 Rail-to-rail topology with pn-diodes and Zener diode

Figure 37 shows an ESD protection environment with a rail-to-rail topology:

- From each signal line, one pn-diode is connected to the upper rail, while another pn-diode is connected from the signal node to the ground rail (GND).
- A Zener diode is connected between ground and upper rail.
- Positive surge pulses push the energy through the upper diodes towards the upper rail.
- Negative surge pulses push the energy through the lower diodes towards ground.

The Zener diode functions as clamping device, and limits the voltage of positive surge events. If the upper rail is connected to a supply line or Vbus, current can flow into the supply as well, where capacitors typically can damp incoming pulses. As a negative side effect, micro-controllers circuits can show soft fails generated by the supply voltage overshoot created.

The rail-to-rail structure allows a very robust structure with a high capacitance of the Zener diode. The pn-diodes are comparably small with a small parasitic capacitance. Cd on the signal line is roughly twice the capacitance of the pn-diode, assuming that the top

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and ground rail works like a short circuit for RF-components. This short is caused by the big capacitance of the Zener diode and comparably big capacitors connected to the supply line.

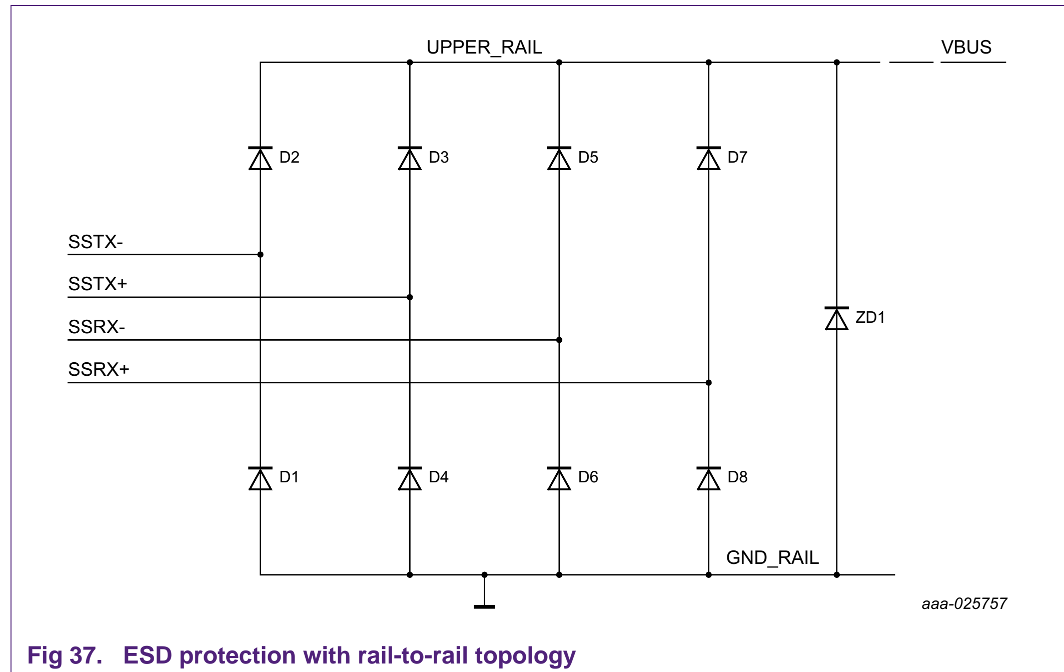

Fig 37. ESD protection with rail-to-rail topology

6.1.5 Rail-to-rail topology with SCR

Figure 38 contains a modification of the conventional rail-to-rail topology. Instead of a Zener diode, an SCR (Silicon-Controlled Rectifier) is put between upper rail and ground. If the voltage of the upper rail exceeds a specified trigger voltage, the SCR switches into on-state and connects the two rails. If the current through SCR falls below a specified hold current, the SCR switches off again and becomes high-ohmic again.

Please note that when this topology for protection is used, it is not allowed to connect a supply line to the upper rail or to the signal inputs.
In case of a trigger event, the SCR would not return into the off-state because a DC-supply can easily provide a constant current above the hold current I_H. The ESD protection component could be damaged or the supply line stays in a short-circuit condition.

The advantage of the SCR-based approach is that very low clamping voltages can be achieved for surge events. The turn-on effect is often called snap-back because the voltage at the ESD protection device jumps down from a trigger voltage towards a low

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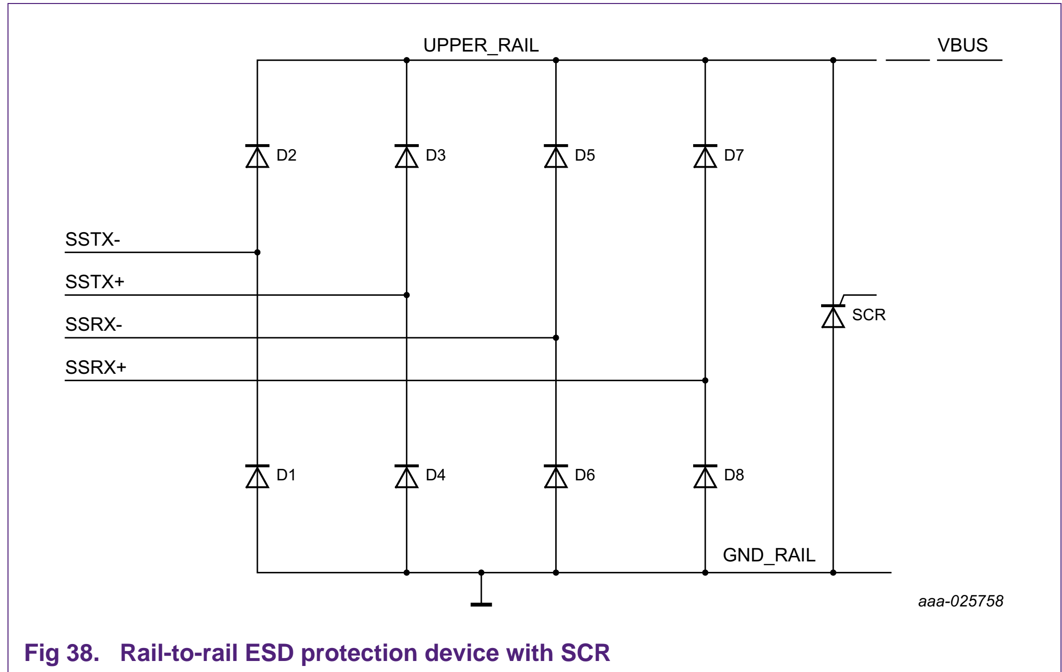

Fig 38. Rail-to-rail ESD protection device with SCR

voltage in on-state. The snap-back voltage can be designed to drop lower than the high state voltage of a signal line and below V_{RWM}. Although this appears to be a conflict it does not create a problem in most cases. Many high-speed interfaces are designed to be free of DC content in the data stream. Therefore, the data lines do not stay in single-ended high-state. Once the signal toggles back to low-state, the hold current or hold voltage condition for then SCR is violated and the ESD component switches off again.

Beside simple I-V curve tracer testing, the snap-back characteristic can be evaluated best with a TLP test. Figure 39 shows a TLP curve of PESD3V3Z1BSF as an example for a snap-back device. The device triggers at about 9 V and snaps back to 2.5 V. From there the TLP I-V-graph shows a mostly linear curve with a steepness of Rdyn = 0.19 Ω.

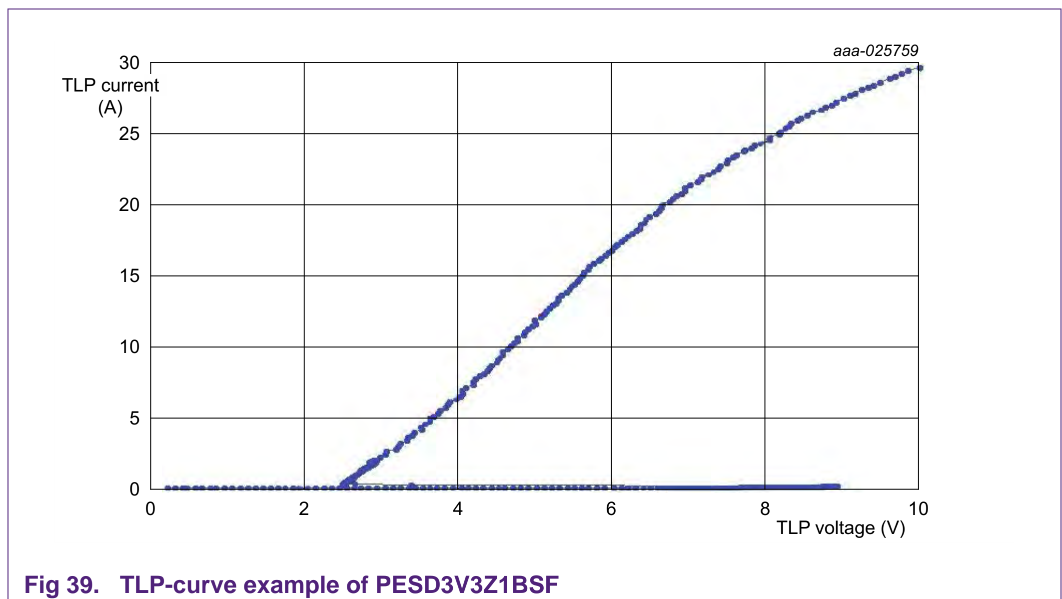

Fig 39. TLP-curve example of PESD3V3Z1BSF

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Figure 40 compares typical TLP curves with each other:

- Green TLP curve: ESD protection products that are based on an avalanche effect clamping topology that are specified for operating with V_{RWM} 5 V to 5.5 V. They have a breakdown voltage V_{BR} that is equal to or greater than 7 V.
- Red TLP curve: Parts that are specified for operating at V_{RWM} 3.3 V have a lower breakdown voltage of equal to or greater than 5 V. Thus, clamping voltages are lower and more current of the surge event is dissipated in the protection device compared to the 5 V type.The overall system level robustness is improved.
- Yellow TLP curve: TLP testing can also be applied to interface pins and complete electronic products. Modern integrated chips often show TLP curves that start at relatively low voltages. As soon as the pulse voltage is raised, they show a steep increase of current, which is due to a low dynamic interface resistance.
  Please note that many ICs can only cope with a relatively low maximum TLP current. This can be I_{PP} = 5 A, for instance.
- Black TLP curve: Shows a deep snap-back topology example. An ideal result is a perpendicular TLP curve, where the clamping voltage does not increase with the surge current.

In conclusion, effective ESD protection requires a TLP curve for the ESD protection device that is located left of the TLP curve of the SoC. The curve must show a high steepness with no cross point to the SoC curve. In this way it can be ensured that most of the surge current flows through the protection; and only a lower current through the IC input structure. The point where the system is destroyed is shifted to higher currents.

With an avalanche topology, the breakdown voltage cannot be decreased any further down into the operating voltage range of the interface without causing leakages. This means that further improvement for a low clamping voltage can be driven in the direction of a perpendicular TLP curve only. Dynamic resistance decrease has technological limits. Therefore snap-back topology allows lowest clamping voltages and highest system protection levels for sensitive interfaces.

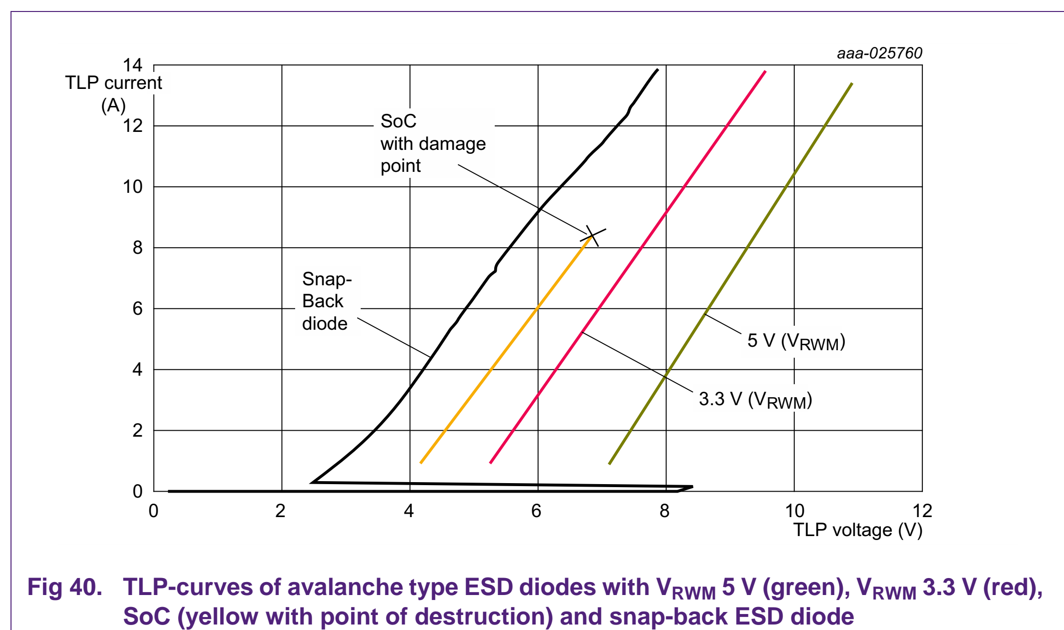

Fig 40. TLP-curves of avalanche type ESD diodes with V_{RWM} 5 V (green), V_{RWM} 3.3 V (red), SoC (yellow with point of destruction) and snap-back ESD diode

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6.1.5.1 Comparison of Intel Z77 IC-HUB and PUSB3FR4

Figure 41 compares two ESD protection scenarios with each other: The magenta curve shows the TLP curve of an RX input of the Intel Z77 IC-Hub, while the cyan TLP curve shows the same device with PUSB3FR4 as ESD protection:

- The magenta TLP curve shows a relatively high dynamic impedance of around 3 Ω. The SOC manages up to 3.5 A pulse current.
- The cyan TLP curve shows the characteristics achieved with the 4-line PUSB3FR4 protection device. The curve shows a I-V characteristic with a deep snap-back and a steep linear line after the ESD protection device has triggered. Most of the surge current flows via the ESD protection device and not into the SoC. This is achieved by a very low dynamic resistance, which is only one tenth of the resistance of the system chip. Thus, most of the surge energy is dissipated in the protection device. The system chip is therefore very effectively protected very with an excellent level of system robustness. An extremely high TLP current would be required to reach the TLP voltage for destruction for the SoC again (about 9.5 V)

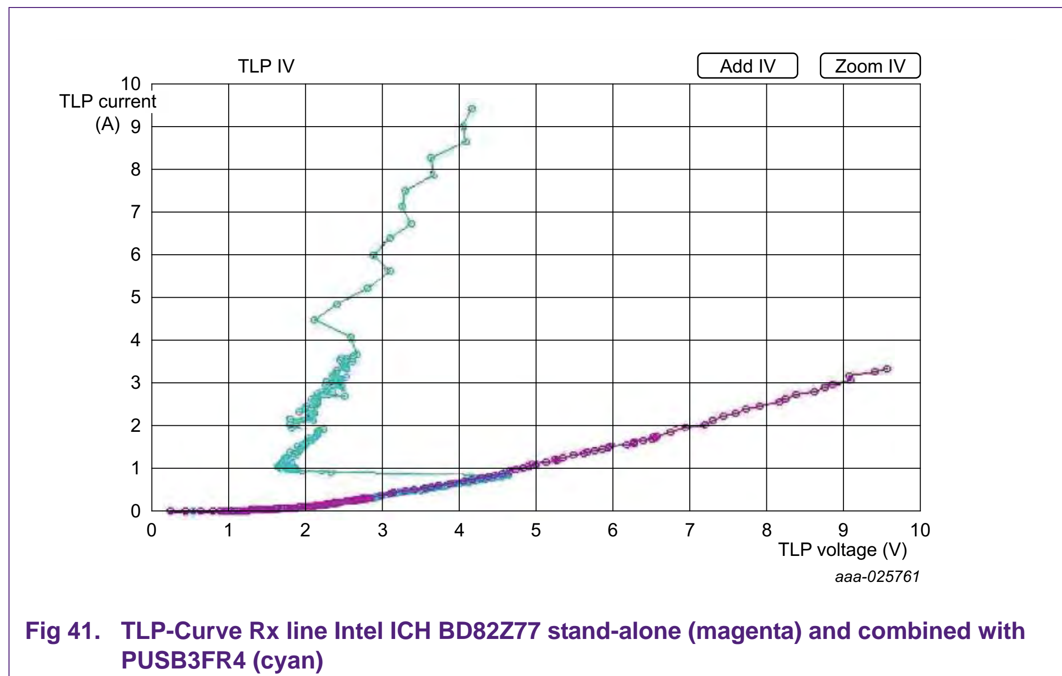

Fig 41. TLP-Curve Rx line Intel ICH BD82Z77 stand-alone (magenta) and combined with PUSB3FR4 (cyan)

6.1.5.2 Latch-up scenarios

In case a snap-back device is triggered, a latch-up can happen if the on-state current is higher than the hold current of the ESD protection device. However, most of the ESD protection devices withstand the current arising from this condition. The Nexperia parts were tested in latch-up with 100 mA for several hours without showing any damage. If an interface is affected, a soft fail occurs but no hardware fail. For many interfaces the snap-back device will automatically return into it’s off-state once the affected data line is in single-ended low state.

An HDMI interface requires some attention with respect to possible latch-up conditions. The HDMI interface topology is given in Figure 18.

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Many HDMI input circuits are designed with active silicon circuits for the 50 Ω pull-up resistors. HDMI interfaces have to be safe for short-circuits on the TMDS lines from the requirement list of the HDMI standard. In order to avoid overheating of active pull-up resistors, the pull-up voltage is shortly removed, whenever a short is detected at the TMDS lines. This mechanism releases a latch-up condition.

Please note that TMDS lines begin data transfer after the connection is established. The risk of ESD strikes is much higher during the connecting process of a cable and very unlikely to happen at a connected cable with fully established connection. In practice no field returns are known created by latch-up failures with HDMI interfaces.

The maximum latch-up current for HDMI can be calculated in a straightforward way. The pull-up voltage can be 3.5 V (3.3 V + 5%) as maximum and the pull-up resistors can have a minimum resistance of 45 Ω (50 Ω – 10%). Assuming a snap-back voltage of 1.24 V, the maximum potential latch-up current can be calculated to 50 mA. If the hold current of the ESD protection is smaller than this value, there is a potential risk to hang-up the interface.

I^2C bus interface are another example that can be affected by latch-up conditions. The maximum high-state current of this interface is defined by the selected pull-up resistors. There is no potential problem, if the high-state current is lower than the hold current of the ESD protection device. If it is higher, the master of the I^2C-bus detects the hang-up situation on the bus and can initiate a power cycle in order to release the bus again.

6.1.5.3 Analyzing load lines to judge a risk of latch-up scenarios

Figure 42 shows an I-V characteristic of an interface output driver with a detailed I-V diagram of a snap-back ESD device.

The load line of an interface starts at a short circuit current on the y-axis. It shows a linear decay toward the open circuit case where the x-axis is crossed at the drive voltage V_{DD} of the data line.

The I-V curve of the ESD protection shows a hysteresis. The arrows mark which trace is valid for the direction of test voltage change. If the voltage increases, the snap-back triggers as soon as the trigger voltage is reached. From that point onwards, the curve continues on a steep on-state path. When the testing current is decreased below I_H, the ESD protection device turns off again, utilizing the lower paths, shown in the diagram, to leap to higher voltage. In similar scenarios as shown in the diagram, an ESD strike can produce a latch-up condition. An interface can get stuck at operating point 1.

Please note that the load line of an interface should only cross the I-V curve of the protection device once.

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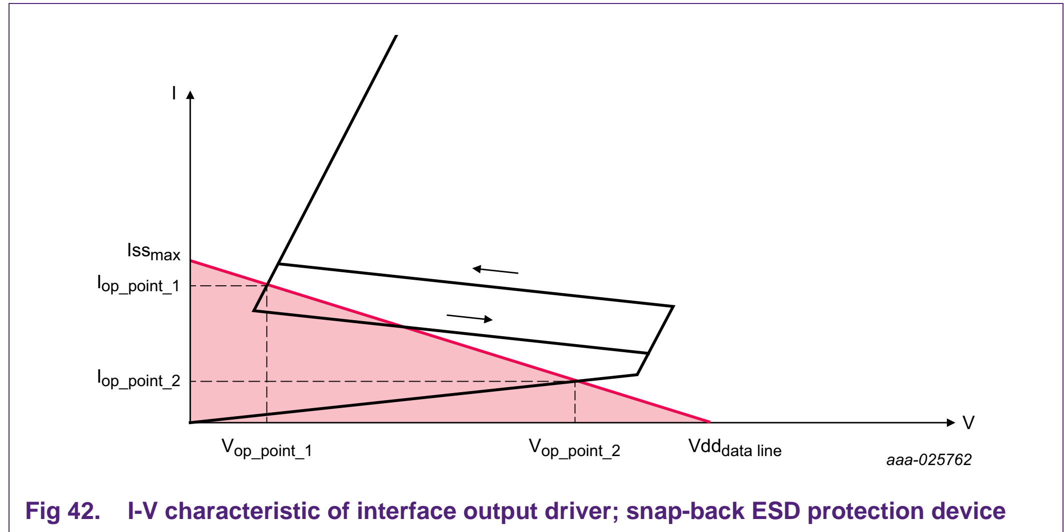

Fig 42. I-V characteristic of interface output driver; snap-back ESD protection device

In an established USB Type-C connection (pin assignment Table 11), the configuration channels CC1 or CC2 are connected to V_{CONN}. V_{CONN} is a 5 V DC supply. Sideband usage signals SBU1 and SBU2 can be overlaid by an DC. This applies to analog audio use cases in which the DC supplies amplifiers. A snap-back ESD diode that can snap below a DC level of a signal line should not be selected for these cases. Also, VBUS is not suitable for snap-back devices in this context of course.

6.1.5.4 I_H and V_H of TrEOS ESD protection devices; unidirectional and bidirectional

In Figure 43 the I-V curve shows measurement results with a current-driven curve tracer for the unidirectional TrEOS product PESD5V0C1USF. The curve delivers a hold current of I_H 16 mA and a hold voltage of V_H 1.4 V. An hysteresis curve can be seen, as explained above.

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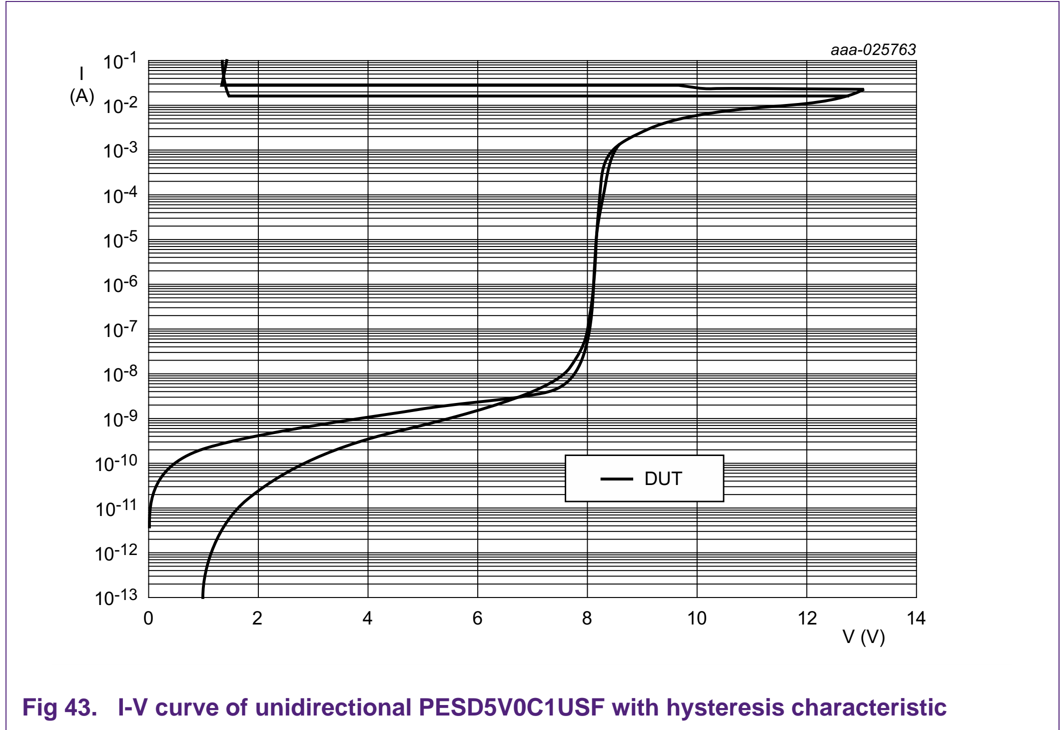

Fig 43. I-V curve of unidirectional PESD5V0C1USF with hysteresis characteristic

The **I**-V curve of Figure 44 shows measurement results with a current-driven curve tracer for the bidirectional TrEOS product PESD5V0H1BSF. The curve delivers the same hold current as for the unidirectional part, which is $I_H \pm 16$ mA. The hold voltage is $\pm V_H$ 2.2 V. The hold voltage V_H is higher because of the series structure of the bidirectional solution, which also includes an additional V_F value of 0.8 V of the diode that is driven in forward direction.

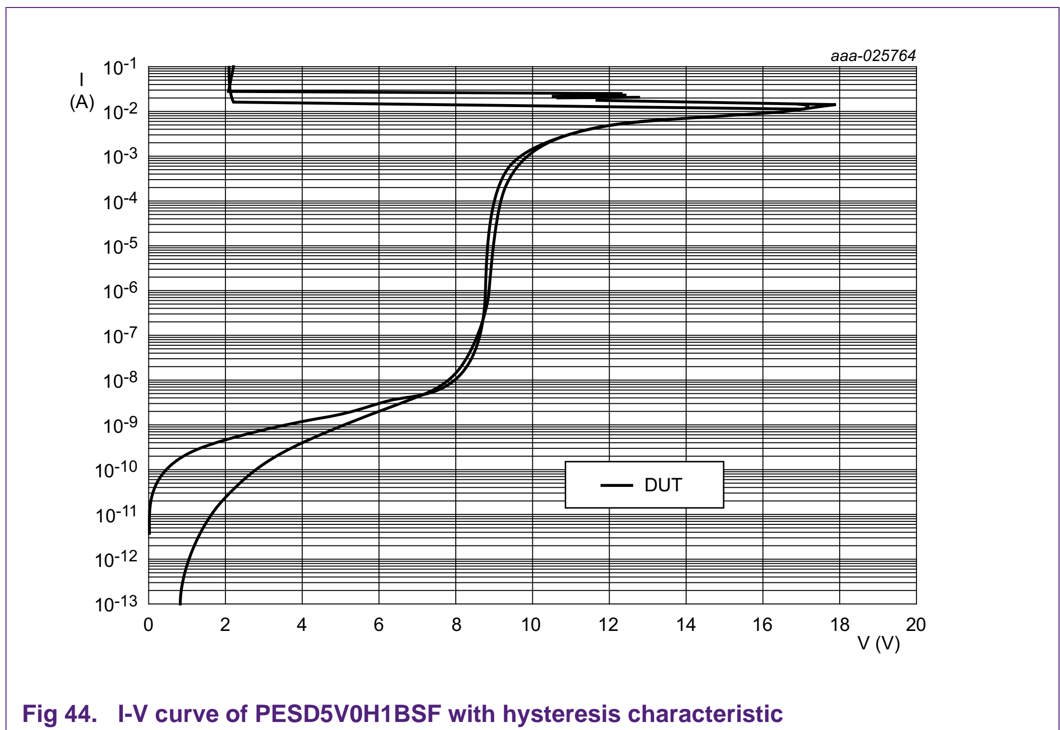

Fig 44. I-V curve of PESD5V0H1BSF with hysteresis characteristic

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6.1.5.5 Switching speed of snap-back ESD protection

An effective ESD protection limits a surge pulse to a safe clamped voltage within a short time without excessive and wide overshoots. This temporal behavior as shown in Figure 45 can be evaluated with a vfTLP test if the voltage traces of the single test events are analyzed.

Figure 45 shows a voltage and current trace of a vfTLP test for PESD5V0H1BSF at a peak current I_{PP} of 15 A, with the following characteristics: The pulse width is 5 ns; with a rise and fall time of 600 ps.The voltage trace shows a narrow overshoot. After turn-on of device, the comparably low clamping voltage is reached.

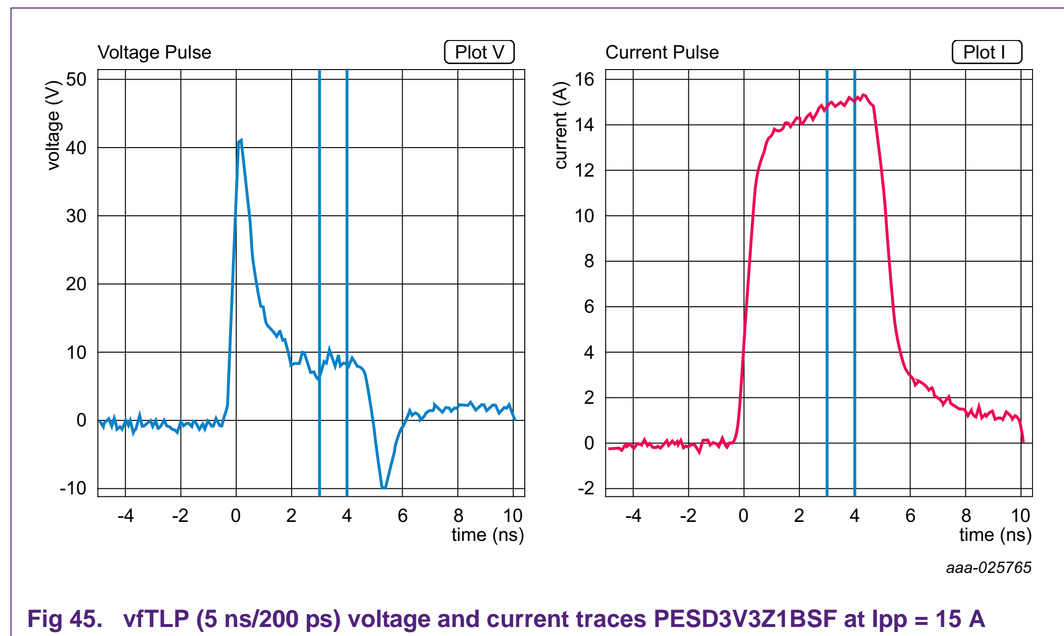

Fig 45. vfTLP (5 ns/200 ps) voltage and current traces PESD3V3Z1BSF at Ipp = 15 A

Figure 46 shows a proposal how the turn-on time can be derived from a vfTLP voltage scope trace. The average value in the 70 to 90% window is taken as zero percent reference value for the falling edge. The TrEOS devices turn on within approximately 1 ns, as Figure 45 shows. The switching time interval is derived from the 30% values at the rising and falling edges for the voltage overshoot in the scope trace.

For many products in the market, the turn-on time is relatively long. This prevents the device from switching on at all in a vfTLP pulse. Turn-on times of about 10 ns are often encountered. Please note that devices that show this weakness cannot protect very sensitive high-speed interfaces and cannot achieve the required system robustness.

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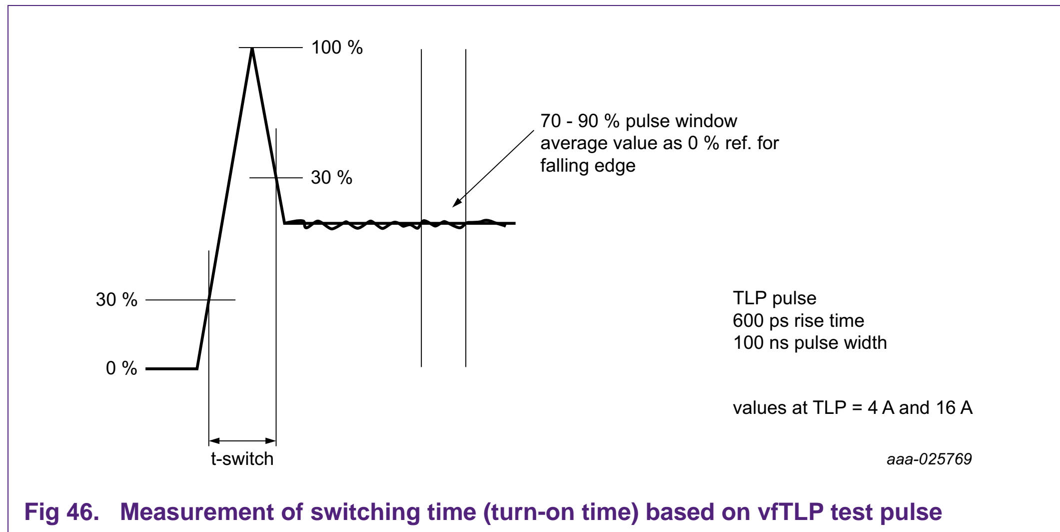

Fig 46. Measurement of switching time (turn-on time) based on vfTLP test pulse

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6.2 Findings for ultra high-speed interfaces and SoCs

As stated in Section 5.2, tests with ESD guns have a wide spread destruction level, should the first overshoot be critical for the system chip. Tests with HMM, TLP and vfTLP pulses deliver much more stable and reproducible results.

Figure 47 shows an HMM current trace marking the limit of a sensitive SoC for this kind of test pulse. The IC was tested without an external ESD protection. The peak current of the first overshoot is 2.4 A. The current peak of the second shoulder is 1.8 A.

In Figure 48 a device with vfTLP pulses is tested. The device is destroyed when 2.4 A are reached; like in the first overshoot the HMM test above. The peak voltage for this pulse is 21 V.

In an additional test, as shown in Figure 49, the interface chip is tested with a 100 ns wide TLP pulse. The destruction level is 4.1 A, which is much more than the value of the shoulder of the HMM pulse. This means that the tested SoC device is damaged by the first overshoot of an ESD strike. Note that the damage does not occur during the shoulder, where the higher energy of the overall surge pulse is located.

For latest generation of ESD sensitive ICs an effective ESD protection must limit the first overshoot effectively, which is achieved by a fast reaction time and low clamping.

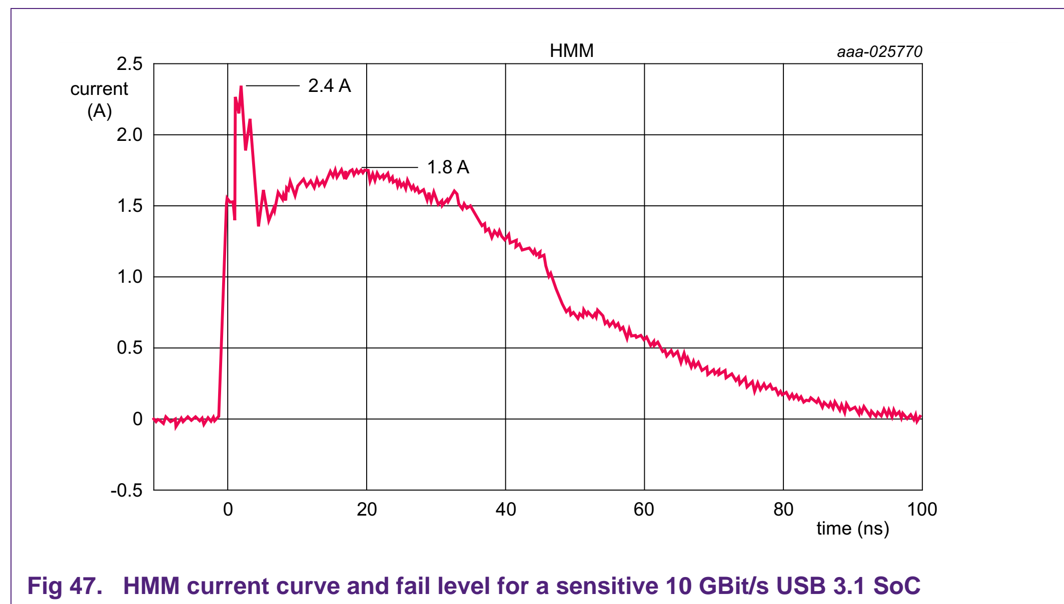

Fig 47. HMM current curve and fail level for a sensitive 10 GBit/s USB 3.1 SoC

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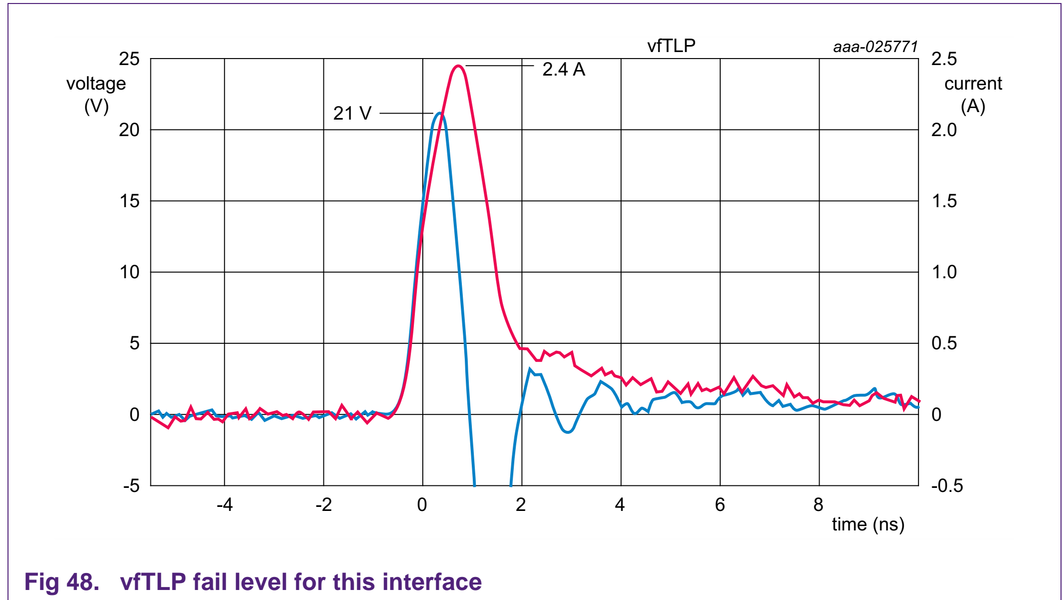

Fig 48. vfTLP fail level for this interface

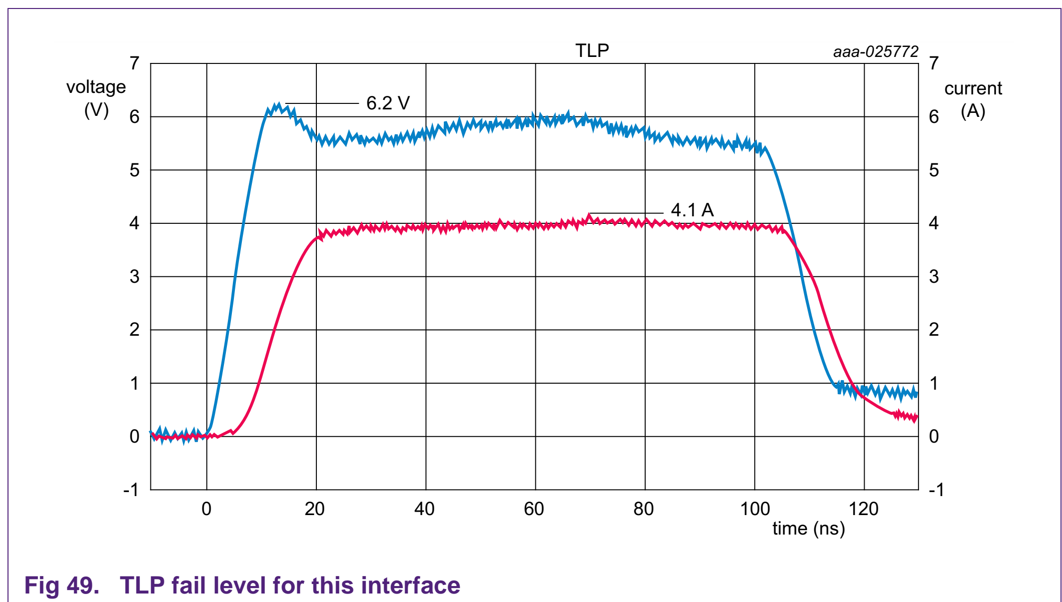

Fig 49. TLP fail level for this interface

6.3 Simulation of ESD events

Figure 50 shows an equivalent circuit for an IC input with an additional external ESD protection that can be used to simulate a surge event:

- The IC has a rail-to-rail ESD protection structure for the input pin.
- The upper diode is connected to a voltage clamping element with an additional serial resistance of R_S.
- LS and RB represent the inductances of the IC bond wires or internal connections and the parasitic inductance of the signal routing on the PCB.
- R_B is the serial ohmic impedance between interface and IC input.

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- The external ESD protection component is represented by a voltage clamping element, a serial resistor Rc and a parasitic capacitance Lc.

In order to achieve an effective ESD protection and a good system level robustness, it is helpful that Lc is very small in relation to Lb + Ls. This improves the damping of the first overshoot of an ESD strike.

ESD protection components with comparably long bond wires show a bigger parasitic inductance than components with CSP-like concepts.The DSN0603-2 package has an extremely low parasitic inductance of about 1nH only. The SOT1176 package, which is used extensively in computing applications, has an inductance of about 3 nH. With longer traces on the board - for example from the connector to the SoC - the inductance of the connection to the IC can be increased. This increase shifts the balance towards a safer region.

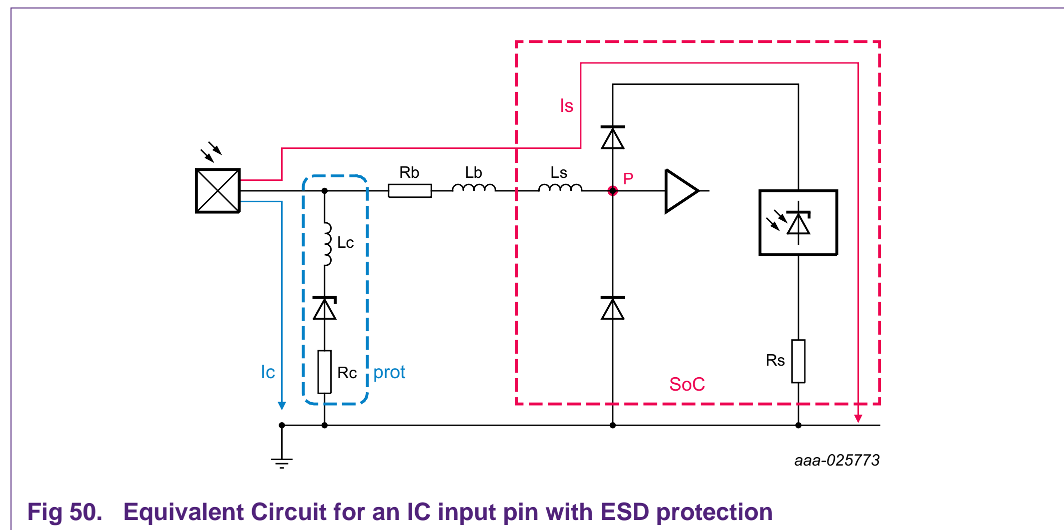

Fig 50. Equivalent Circuit for an IC input pin with ESD protection

7. Making use of common mode filters

7.1 Introduction to common mode filters

A common mode filter consists of two coupled coils. If current flows in the same direction in both coils, the filter has a high impedance. If the currents flow in opposite direction, the impedance is low.

If a common mode filter is applied to a differential data line, the differential part of the data carrying the information can pass. At the same time, the overlaid common signal content is blocked, as depicted in Figure 51.

Magnetic and electrical fields are canceled out for a differential signal in the far field, if the single signals are routed within a small distance. In contrast, common mode signals can radiate into the environment. Especially in compact designs, EMI can reduce the sensitivity of receiver blocks. For example an activated USB 3.0 interface can hinder proper reception of WIFI data.

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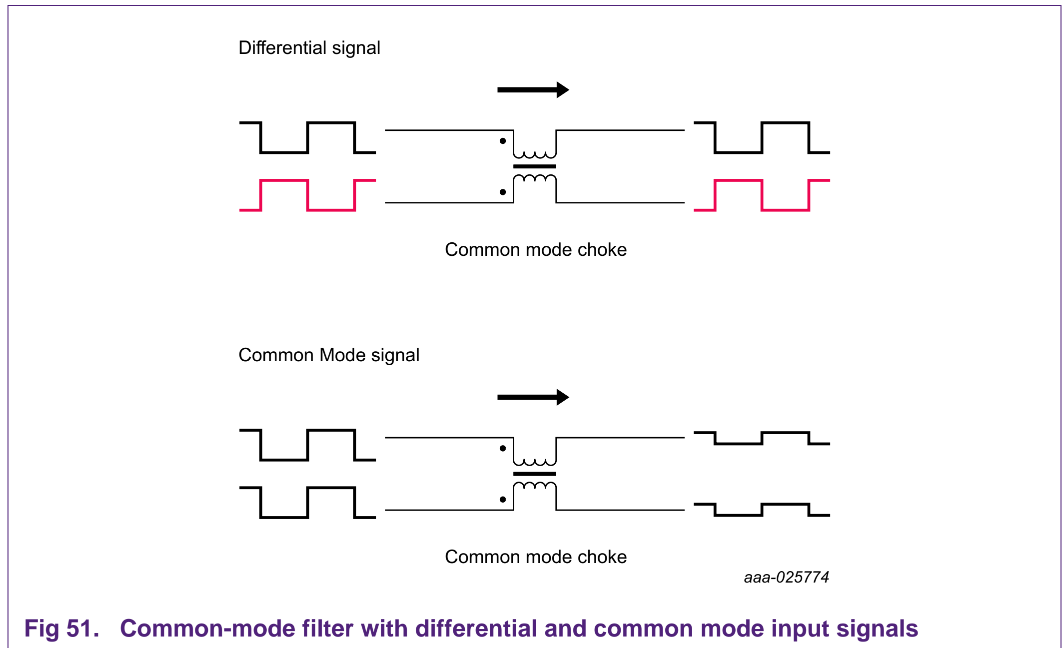

Fig 51. Common-mode filter with differential and common mode input signals

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In Figure 52 an overview of the frequency bands of RF transmission standards is shown, which are in use for mobile devices. A red marker at 2.5 GHz is added. This frequency is the fundamental USB 3.0 wave.

Please note that 2.5 GHz EMI components create EMI problems for some WiFi, LTE and Bluetooth bands. In some scenarios the use of common mode filters prevents loss of the WiFi connection while a USB 3.0 interface is active. Consequently, this eliminates the need to force down the USB data speed from super speed to high speed.

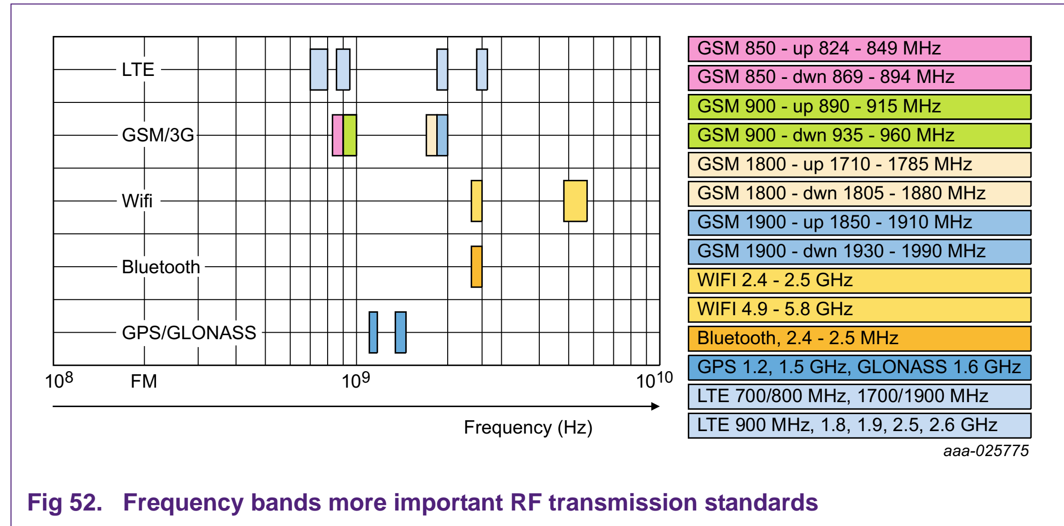

Fig 52. Frequency bands more important RF transmission standards

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7.2 PCMFxUSB3S and PESDxUSB3S product solutions

With product series PCMFxUSB3S a silicon-based common mode filter combined with TrEOS ESD protection is available. Advantages of the all-in-one packaging are:

- Overall mounting space on the PCB is reduced.
- Prevention of additional impedance drops in the signal traces, which can be expected at each of the separate parts.

Available are one lane, two lane and three lane devices:

- PCMF**1**USB3S
- PCMF**2**USB3S
- PCMF**3**USB3S

This allows maximum flexibility for board design, depending on board design preferences.

The common mode filter is also available as a separate TrEOS ESD protection with the same packages as for the PCMFxUSB3S solution. The PESDxUSB3S solution is also available with one, two or three lanes:

- PESD**1**USB3S
- PESD**2**USB3S
- PESD**3**USB3S

PESDxUSB3S parts are especially helpful for designers that need to consider whether an EMI filter is needed or not at a later stage.

Please note that there is no need to mount zero-ohm resistors as short circuits for a conventional common mode filter that shall not be assembled, because either a PCMFxUSB3S is mounted or a PESDxUSB3S.

7.3 Differential passband of PCMFxUSB3S

Figure 53 shows the differential passband of the PCMFxUSB3S. The -3 dB bandwidth is 6 GHz. The attenuation for 2.5 GHz, which is the fundamental wave of USB 3.0 Gen 1 (5 Gbit/s), is about –1.5 dB. For USB 3.0 Gen 2, the corresponding value is about –2.5 dB.

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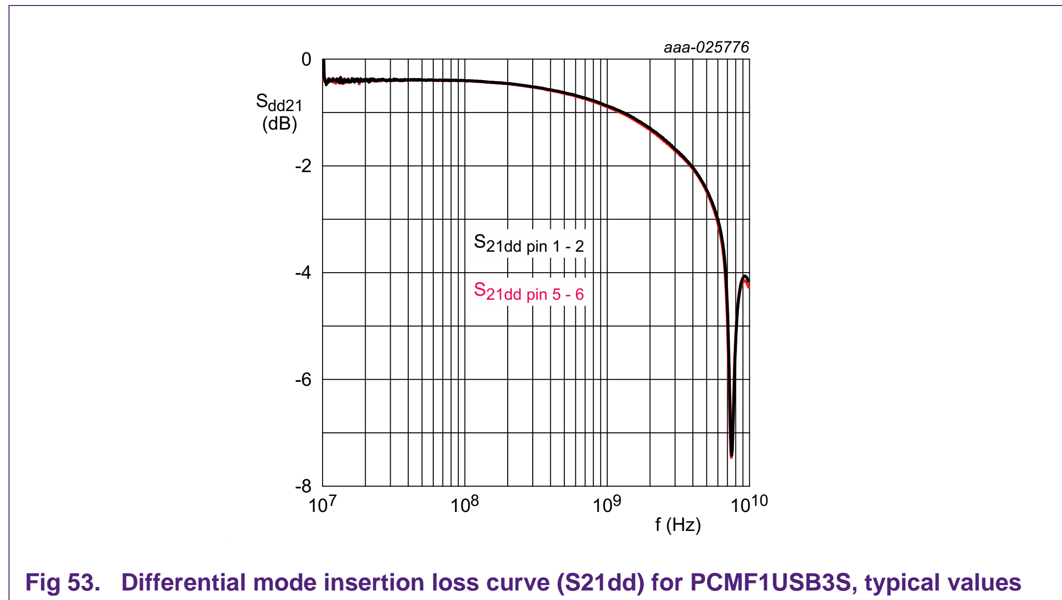

Fig 53. Differential mode insertion loss curve (S21dd) for PCMF1USB3S, typical values

It is not correct to compare the frequency response curves of the PCMFxUSB3S with the combined common-mode filter ESD protection to a standalone common-mode filter. This form of comparison would disregard the deterioration of the passband caused by the separate ESD protection. Consequently, the passband of the complete circuit of a common mode filter and ESD protection must be compared to the PCMF solution.

To highlight this in more detail, the following example is given. A ferrite filter with –3 dB bandwidth of 6.3 GHz is combined with an ultra-low capacitance ESD protection device. In the combination of the two devices a bandwidth deterioration occurs, down to 4.9 GHz.

Please also note that PCMFxUSB3S compliance tests are available for: USB 3.0 Gen 1 and Gen 2, HDMI 2.0 and MIPI M-Phy.

Figure 54 shows the S21DD curves for a high runner ferrite-based common mode filter for USB 3, and the combination with ESD protection diodes with different passbands:

- The gray curve represents the stand-alone common-mode filter with –3 dB bandwidth of 6.3 GHz.
- Combined with a 14 GHz ESD protection device: The overall bandwidth is reduced to 4.9 GHz.
- Combined with a 7 GHz ESD protection device: The yellow –3 dB line is crossed at 4 GHz.

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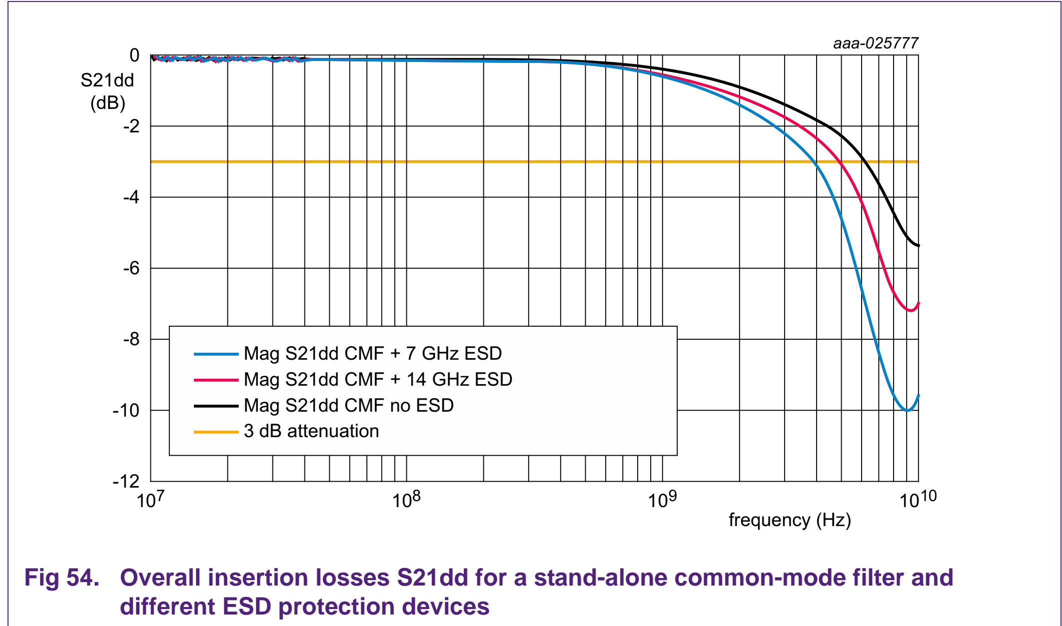

Fig 54. Overall insertion losses S21dd for a stand-alone common-mode filter and different ESD protection devices

7.4 Commode-mode rejection of PCMFxUSB3S

Figure 55 shows the common mode rejection frequency curve of the PCMFxUSB3S. The transfer curve shows a notch at 2.5 GHz down to about -40 dB. Power is attenuated by 4 magnitudes and potential common mode noise of a 5 Gbit/s data signal can be blocked very effectively. In customer-designed applications the benefit of the PCMFxUSB3S shows its particular strength. Especially concerning the maximum WIFI reception distance, which is achieved regardless of an active USB3 data interface.

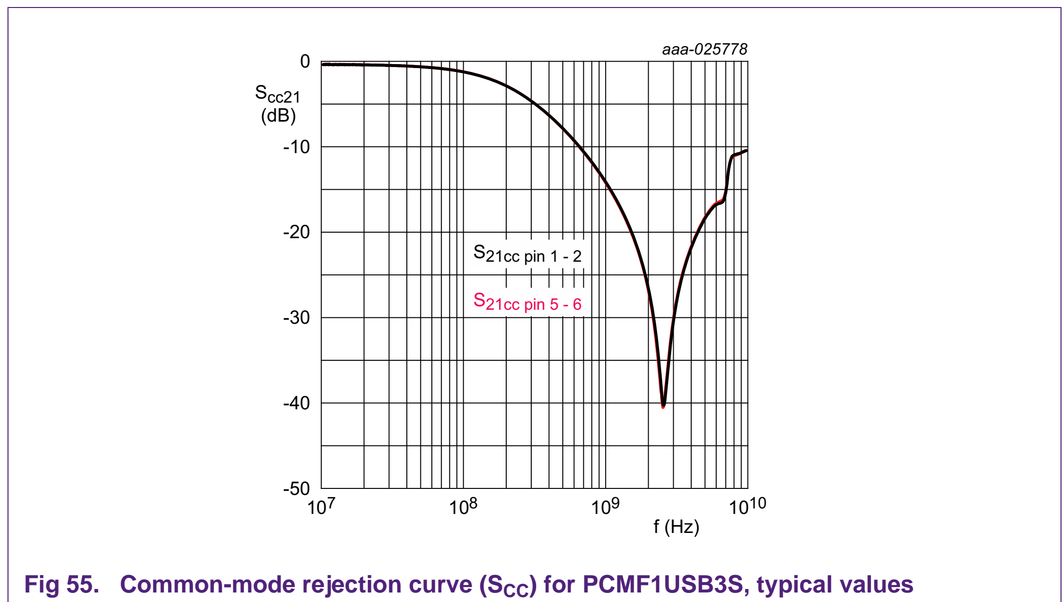

Fig 55. Common-mode rejection curve (S_{CC}) for PCMF1USB3S, typical values

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7.5 ESD protection performance of PCMFxUSB3S

ESD protection performance of PCMFxUSB3S

The approach of putting the PCMFxUSB3S into a data line provides a very good protection for sensitive SoCs. As stated before regarding Figure 50, a common mode filter creates a comparably high inductance towards an SoC input.

Measurement test and simulation test results correspond very well, as shown in Figure 56.

Measurement results for the residual first peak voltage at the SoC input are shown in solid lines. Simulated results are presented in dotted lines for a wire-bonded package as red curve, SOD962 (0201”) package as blue curve, and common mode filter WLCSP-5 as green curve.

A wire-bonded package (DFN1006-2) is compared to a DSN0603-2 (SOD962 or 0201”) package and the common-mode filter WL-CSP package. The DSN and WL-CSP packages have no bond wires, and this is why they have very low peak voltages. As the green curve shows, the inductance of the common-mode filter improves the result even more. The curves that are measured look very similar to simulated results concerning the peak voltages.

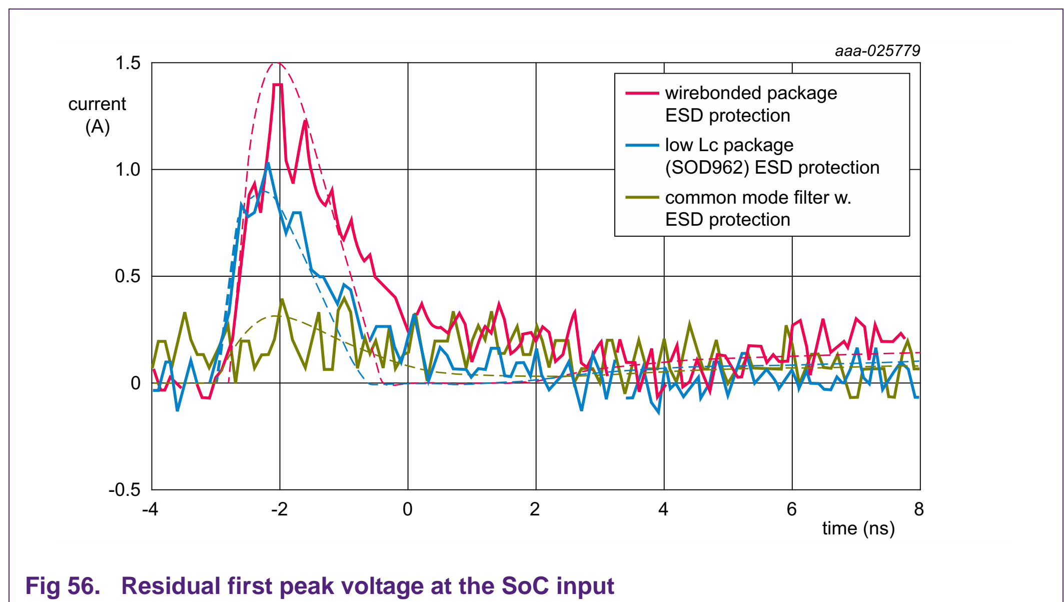

Fig 56. Residual first peak voltage at the SoC input

The PCMFxUSB3S is typically placed close to the connectors on the PCB. The ESD protection diodes face in the direction of the connectors, as shown in Figure 57. In this case the ESD protection works is most effective. Sometimes it is useful to deviate from this rule and to put the common-mode filter close to a transmitter stage, in case common-mode signal content is generated there. In this case, additional care is necessary to avoid a generation of common-mode signal content in the routing path behind the filters.

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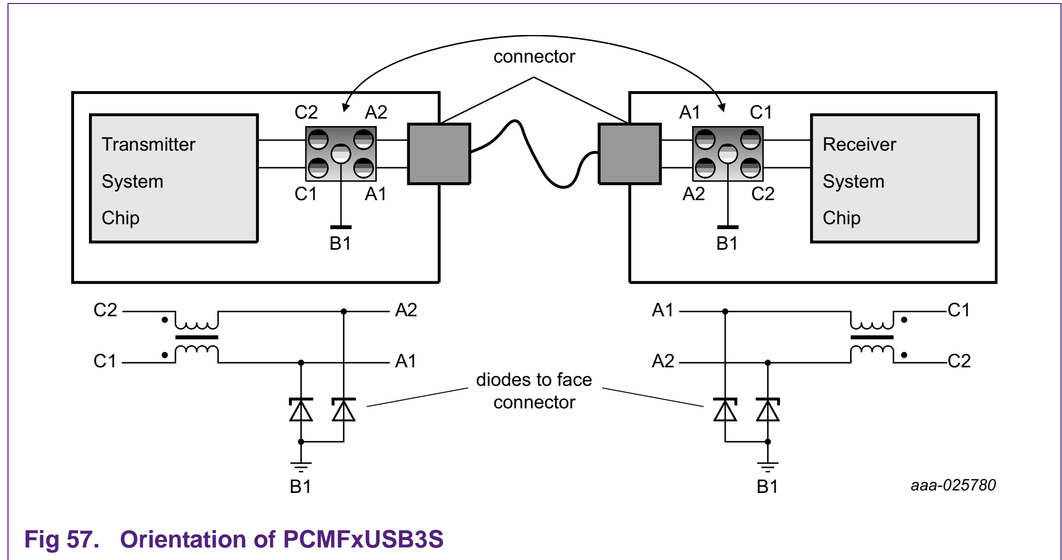

Fig 57. Orientation of PCMFxUSB3S

8. TrEOS portfolio

In Table 22 an overview of the TrEOS key products is provided. TrEOS stands for the Nexperia ESD protection technology that combines deep snap-back, low dynamic resistance and high ESD robustness.

Single ESD diodes in a DSN0603 package contain progressive ESD technology in an ultra-small package (0.6 mm x 0.3 mm x 0.3 mm), in which no bond wires are required. PESD5V0C1USF is a unidirectional ESD-diode with an extremely low dynamic resistance. Bidirectional variants are also available; with different Cd ratings and ESD robustness levels.

Available are 4-line and 6-line ESD protection devices. For instance, in DFN2510A-10 (SOT1176) 4-line packages as standard solution in many computing applications. And also in DFN2111-7 (SOT1358) 6-line packages that can protect all the 3 differential pairs of a USB 3 Type-A connection with one component.

The PCMFxUSB3S series provides an integrated combination of a common mode filter and TrEOS ESD protection technology. The product is available for one, two or three lanes. Thus, allowing a higher flexibility in the customer PCB design. The PESDxUSB3S series is a direct pin-to-pin replacement product with ESD protection only. It has no common-mode filter function

Table 22. Product overview of TrEOS components

Type name	description	package	Cd in pF @1MHz	Rdyn in Ω @TLP	ESD robustness in +/- kV
PESD5V0C1USF	unidirectional ESD diode	DSN0603-2	0.45	0.1	20
PESD5V0C1BSF	bidirectional ESD diode	DSN0603-2	0.2	0.23	20
PESD5V0H1BSF	bidirectional ESD diode	DSN0603-2	0.15	0.25	15

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Table 22. Product overview of TrEOS components

Type name	description	package	Cd in pF @1MHz	Rdyn in Ω @TLP	ESD robustness in +/- kV
PESD5V0R1BSF	bidirectional ESD diode	DSN0603-2	0.1	0.45	10
PESD3V3Z1BSF	bidirectional ESD diode	DSN0603-2	0.28	0.19	18
PUSB3FR4	4-line unidirectional	DFN2510A-10	0.29	0.27	15
PUSB3FR6	6-line unidirectional	DFN2111-7	0.35	0.29	15
PUSB3AB4	4-line bidirectional	DFN2510A-10	0.17	0.4	15
PUSB3AB6	6-line bidirectional	DFN2111-7	0.15	0.4	15
PCMF1USB3S	1-lane Common mode filter + unidirectional ESD protection	WLCSP5	0.25	0.14	15
PCMF2USB3S	2-lane Common mode filter + unidirectional ESD protection	WLCSP10	0.25	0.14	15
PCMF3USB3S	3-lane Common mode filter + unidirectional ESD protection	WLCSP15	0.25	0.14	15
PESD1USB3S	1-lane unidirectional ESD protection	WLCSP5	0.45	0.16	15
PESD2USB3S	2-lane unidirectional ESD protection	WLCSP10	0.45	0.16	15
PESD3USB3S	3-lane unidirectional ESD protection	WLCSP15	0.45	0.16	15

9. Summary

Nowadays, high-speed interfaces of modern mobile communication and computing equipment are more sensitive to ESD strikes and surge events because the IC technology has become miniaturized and because of the high data rates that have to be processed.

Higher data rates at the I/O-pins make design changes necessary; and also low-pass characteristics in the input had to be removed. This has made the system chips more sensitive towards the first overshoot of incoming ESD events. This new sensitivity has to be managed well by the ESD protection devices. This is achieved by low clamping voltages, low dynamic resistance and low parasitic impedances, inside the package

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technology. Snap-back technology allows very low clamping voltages. High switching speed is another important requirement for devices using this topology. This avoids interface damages caused by surge events.

Proper placement of the ESD protection and SoC help achieve dissipation of surge energy in the protection device. The use of common-mode filters in combination with modern ESD protection technology improves system level robustness even further.

10. Abbreviations

Table 23. Abbreviations

Acronym	Description
DFP	Down Facing Port
DUT	Device Under Test
GSM	Global System for Mobile communication
NAK	Not Acknowledged Package
PLL	Phase Locked Loop
Ra	adapted Register
Rd	pull down Register
Rp	pull up Register
SoC	System on Chip
TMDS	Transmission Minimized Differential Signaling
UFP	Up Facing Port

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