AN50002

Automotive LED side light SEPIC DC-to-DC converter design example

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Document information

Information	Content
Keywords	SEPIC converter, DC-to-DC, MOSFET, LED dimming
Abstract	This application note provides a general guideline of Single-Ended Primary Inductance Converter (SEPIC) DC-to-DC converter design using Nexperia Power MOSFET devices.

1. Introduction

In modern automotive applications, electrical systems are widely used in vehicles. They usually powered by lead-acid or Li-ion batteries whose output voltage varies with the State of Charge (SOC), temperature, load dump and other loading operations. This requires DC-to-DC converters to accommodate a wide input voltage and generate a stable regulated output voltage for electrical loads. A Single-Ended Primary Inductance Converter (SEPIC) design can be a good fit for a battery powered system. It can generate output voltage higher or lower than the input voltage with less components comparing to other topologies. Additionally, its AC coupled capacitor inherently separates the output from the input. LED lighting is one example where SEPIC converters can be used in an automotive application.

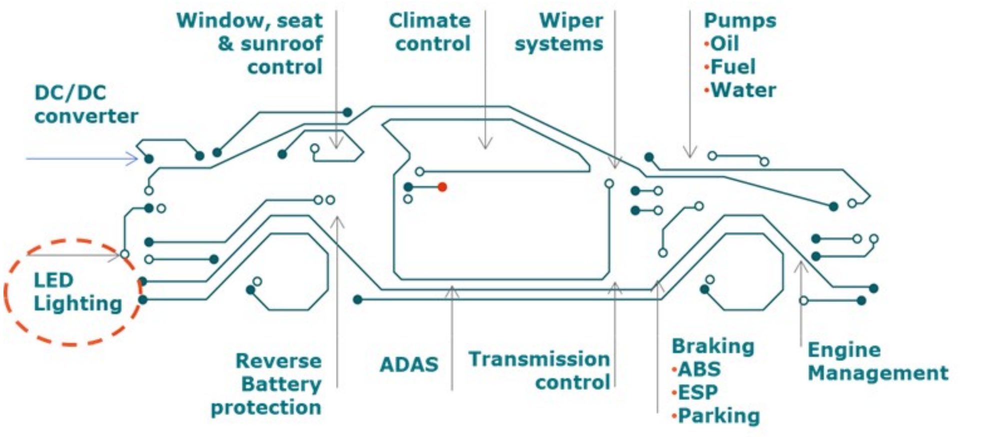

Fig. 1. Automotive application - LED lighting

In this application note, a general guideline of SEPIC converter design using Nexperia Power MOSFET devices will be described.

2. SEPIC converter design example

A Synchronous SEPIC DC-to-DC converter design example is shown in Fig. 2. One of the features of SEPIC converters is that the currents flowing through the two inductors are proportional to each other [1]. Hence, a coupled inductor can be used in the design for reducing PCB footprint size and system cost.

Design specifications:

- Input voltage: 9 ~ 16 V
- Output voltage: 20 V
- Maximum output power: 20 W
- Switching frequency: 380 kHz

Key features:

- Reverse battery protection (RBP)
- Synchronous topology improves converter efficiency
- Configurable light load operation modes:
  - Burst mode improves efficiency but causes higher output ripple and switching noise
  - Forced continuous mode for lower output ripple and switching noise but higher switching loss
  - Pulse-skiping mode comprises of the above two operation modes

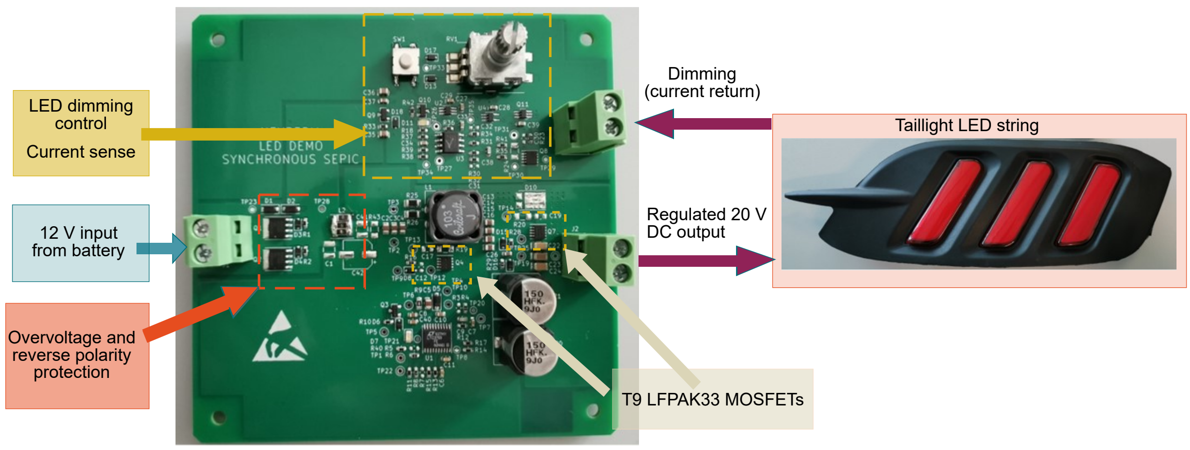

Fig. 2. SEPIC converter PCB for LED lighting

3. System design

SEPIC topology is a combined topology consisting of two building blocks as shown in Fig. 3 below.

At the input side, there is a common Boost configuration formed by an inductor and a power switch. This eases the RMS current seen by input capacitor [1].

At the output side, a Buck block is formed by a synchronous MOSFET or diode and an inductor. As these two inductors are being charged and discharged during the whole operation period, a coupled inductor can be used to reduce size and cost.

With this configuration, a SEPIC converter is able to accommodate a wide input voltage range and provide a regulated output.

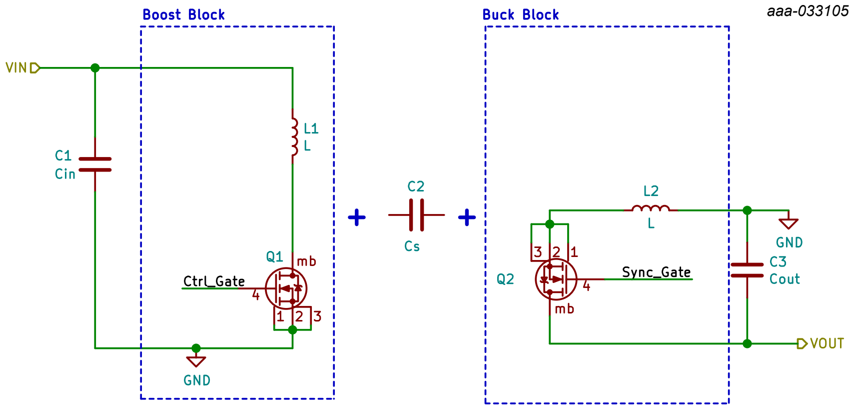

Fig. 3. SEPIC converter building block

To ensure proper energy transfer and operation of a SEPIC converter, a coupling capacitor with low ESR is required. The RMS current rating of this capacitor is proportional to output power, since all output current is passing through coupling capacitor. And maximum input voltage plus some ripple will determine the voltage rating. This capacitor is also the inter-connection between two building blocks. Please refer to AC coupling capacitor section for more details.

The basic operation of a SEPIC converter is shown in Fig. 4 (a) below.

During the period that switch Q1 = ON the coupled inductor (two windings) and coupling capacitor are being charged and energy is stored inside them. Current flow is indicated in Fig. 4 (b). In this period, all output power is provided by output capacitor to maintain regulated output voltage rating.

When Q1 = OFF, and synchronous MOSFET Q2 = ON, Fig. 4 (c), energy is released from inductors and delivered to the load.

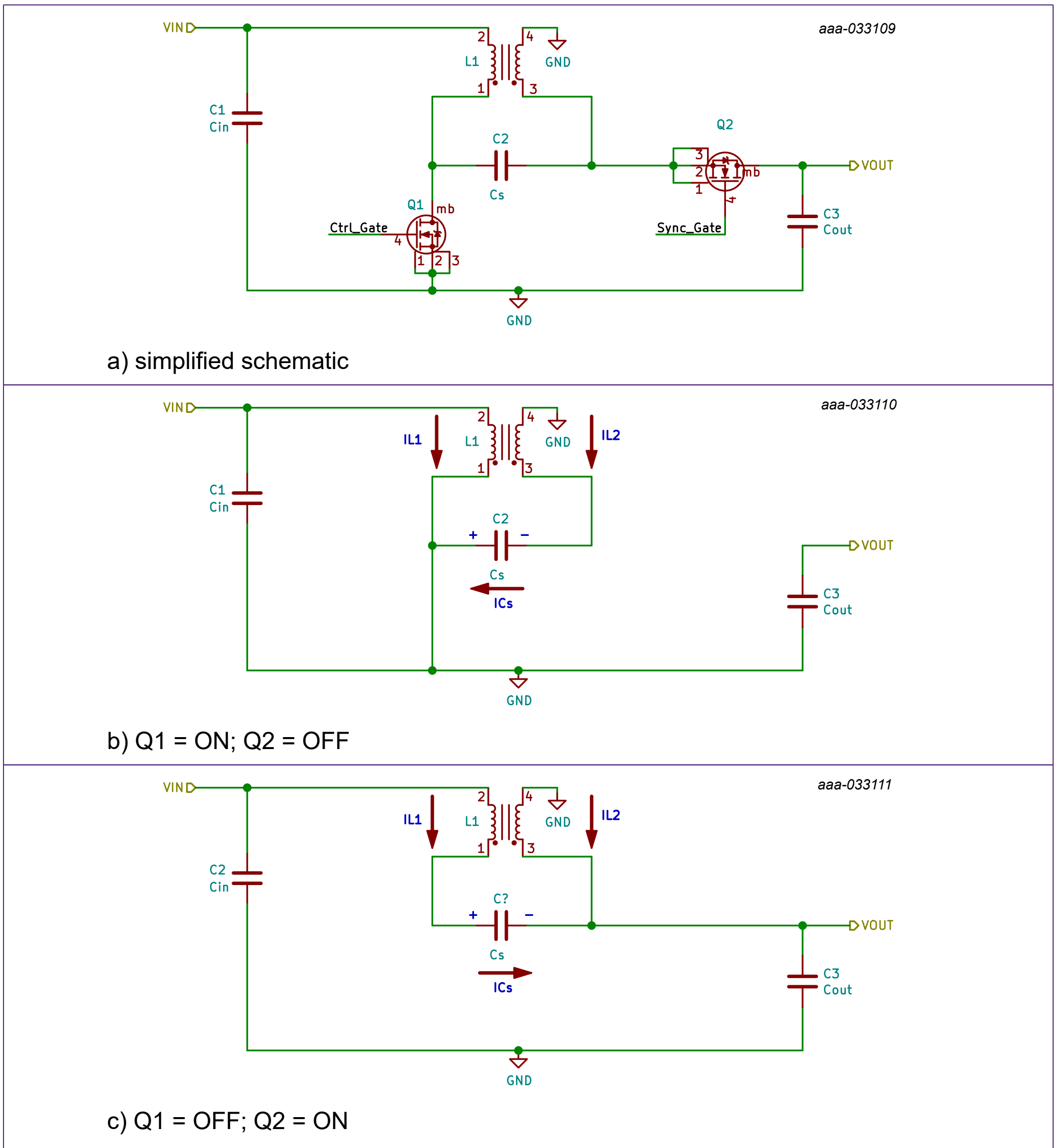

Fig. 4. SEPIC converter phases

3.1. Power MOSFET

Power MOSFET selection plays a critical part for the whole design as it determines the whole system's thermal design requirements, cost and efficiency. Theoretical analysis can be performed with mathematical equations.

In the SEPIC topology, the voltage stress on the main and synchronous MOSFET is the sum of maximum input voltage and regulated output voltage:

$$V_{DS(max)} = V_{i(max)} + V_o \quad (1)$$

During the main switch on state, both inductor currents will pass through the main control MOSFET [1]. Therefore, the peak and RMS current can be calculated:

$$I_{M1(peak)} = I_{L1(peak)} + I_{L2(peak)} \quad (2)$$

$$I_{M1(RMS)} = \sqrt{\left(I_{M1(peak)}^2 - I_{M1(peak)} \times (\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1}+\Delta I_{L2})^2}{3}\right) D_{max}} \quad (3)$$

During the main switch off state, both inductor current will through the synchronous MOSFET, consequently the peak and RMS current are expressed as:

$$I_{M2(peak)} = I_{L1(peak)} + I_{L2(peak)} \quad (4)$$

$$I_{M2(RMS)} = \sqrt{\left(I_{M2(peak)}^2 - I_{M2(peak)} \times (\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1}+\Delta I_{L2})^2}{3}\right)(1 - D_{max})} \quad (5)$$

With current and voltage rating known, we can calculate the switching and conduction losses for the main MOSFET:

$$P_{M1CON} = I_{M1(RMS)}^2 \times R_{ds(on)} \quad (6)$$

$$P_{M1SW} = V_{M1(peak)} \times I_{M1(peak)} \times \frac{C_{iss} \times \Delta V_g}{I_g} \times 2 \times f_{sw} \quad (7)$$

Where ΔV_g is gate voltage sweeping range, and C_{iss} is the MOSFET input parasitic capacitance, I_g is the gate drive sinking and sourcing current.

And for synchronous MOSFET the switching and conduction losses can be obtained by:

$$P_{M2CON} = I_{M2(RMS)}^2 \times R_{ds(on)} \quad (8)$$

$$P_{M2SW} = V_{M2(peak)} \times I_{M2(peak)} \times \frac{C_{iss} \times \Delta V_g}{I_g} \times 2 \times f_{sw} \quad (9)$$

During converter design, theoretical analysis utilizes complicated mathematical equations. Some of these can be only approximations. For instance, the entire switching process of a MOSFET is non-linear. There is always some discrepancy between theoretical calculation results and the measured ones. In addition, in thermal aspect only steady state junction temperature can be estimated through mathematical equations. It is very difficult to estimate instantaneous junction temperature through theoretical equations since the current profile could be very complex. Several iterations of calculation are usually needed to choose the right MOSFET that meets the system efficiency, cost and size requirement. For initial performance estimation, calculation can be verified by computer simulation. Please refer to Nexperia interactive application note *IAN50002* for an example SEPIC converter simulation. In the embedded simulation, any voltage or current waveform can be viewed using the probes available from the toolbar. For thermal estimation using RC models, please refer to Nexperia application note *AN11261* RC Thermal Models [2].

3.2. Duty cycle calculation

The following consideration is based on SEPIC converter operating in Continuous Conduction Mode (CCM) [1].

In CCM operation, the duty cycle *D* of a SEPIC converter can be obtained as:

$$D = \frac{V_o + V_D}{V_i + V_o + V_D} \tag{10}$$

Where V_D is the voltage across the diode or the synchronous MOSFET.

3.3. Inductor Selection

There are several factors affecting the choice of inductance value like RMS current, peak-to-peak current ripple, current to ripple ratio (r), maximum input current (at minimum V_{in}), and switching frequency. One of the important factors among them is the current ripple ratio (r) which is defined as the ratio between inductor ripple current and average current. As a rule of thumb, the r value of 0.4 would be a good starting point [1]. A higher value will bring high stress to the input capacitor (see input capacitor selection in later section.) A lower value will require higher inductor energy handling capability, which means thicker wire and larger physical size. Therefore, an inductor value can be calculated by the following equations:

$$\Delta I_L = I_i \times 0.4 = I_o \times \frac{V_o}{V_{i(min)}} \times 0.4 \tag{11}$$

$$L_1 = L_2 = \frac{V_{i(min)}}{2 \times \Delta I_L \times f} \tag{12}$$

In practice, inductor RMS and peak current should also be considered to ensure proper operation and design efficiency. They can be obtained by:

$$I_{L1(peak)} = I_o \times \frac{D_{max}}{1 - D_{max}} + \frac{\Delta I_{L1}}{2} \tag{13}$$

$$I_{L2(peak)} = I_o + \frac{\Delta I_{L2}}{2} \tag{14}$$

$$I_{L1(RMS)} = \sqrt{\left(I_{L1(peak)}{}^2 - I_{L1(peak)} \times \Delta I_{L1} + \frac{\Delta I_{L1}{}^2}{3}\right)} \quad (15)$$

$$I_{L2(RMS)} = \sqrt{\left(I_{L2(peak)}{}^2 - I_{L2(peak)} \times \Delta I_{L2} + \frac{\Delta I_{L2}{}^2}{3}\right)} \quad (16)$$

3.4. Bootstrap circuit design

In order to fully turn-on synchronous high side MOSFET, a floating power supply rail is required to provide at least 5 V above the MOSFET source voltage level. A bootstrap circuit formed by a capacitor, a diode and a series resistor (limiting the capacitor charging inrush current) is often used in practice. The capacitance value should be selected according to MOSFET gate charge requirement. In other words, this capacitor should provide full charge to the MOSFET gate.

3.5. AC coupling capacitor

One of the distinguishing advantages of a SEPIC converter is that input and output terminal is separated by the AC coupling capacitor. However, the RMS rating of this capacitor is proportional to the output power. Hence, this topology is mainly used in low and medium power application. During main control MOSFET turn-on period, I_{L2} pass through coupling capacitor [1]. In turned-off period, I_{L1} goes through coupling capacitor [1]. Therefore, the RMS current and capacitance of AC coupling capacitor can be obtained by following equations:

$$I_{Cs(RMS)} = \sqrt{I_{L1}^2 \times D_{max} + I_{L2}^2 \times (1 - D_{max})} \quad (17)$$

$$C_S \geq \frac{I_o \times D_{max}}{\Delta V_{C_S} \times f} \quad (18)$$

Where I_{L1} and I_{L2} are average current of the inductor.

In addition, when the primary control switch is on, this coupling capacitor will be charged to input voltage and some added ESR ripple. Therefore, the voltage rating should be higher than the maximum input voltage.

3.6. Input and output capacitor

The SEPIC is a combined topology which has a BOOST part at input and BUCK configuration at output. The input side has an inductor like a boost converter. Due to the existence of this inductor, the input current is triangular and continuous. Therefore, the RMS current of the input capacitor can be obtained by following equation. The voltage rating should be higher than the maximum input voltage.

$$I_{Ci(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \quad (19)$$

As the output capacitor is required to provide charge to the load during control MOSFET on state. Large ripple current would be seen by the output capacitor. Hence, RMS current should be calculated:

$$I_{Co(RMS)} = \sqrt{\left(I_{M2(peak)}^2 - I_{M2(peak)} \times (\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1}+\Delta I_{L2})^2}{3}\right)(1 - D_{max}) - I_o^2} \quad (20)$$

In practice, any parasitic parameters like ESR or ESL of a bulk capacitor will contribute to output voltage ripple. Thus, the output capacitor should be selected according to converter output ripple requirements. The relationship between output voltage ripple and ESR as well as capacitance is described by the following equations:

$$ESR \leq \frac{V_{ripple} \times 0.5}{I_{L1(peak)} + I_{L2(peak)}} \quad (21)$$

$$C_o \geq \frac{I_{out} \times D_{max}}{V_{ripple} \times 0.5 \times f} \quad (22)$$

3.7. Output voltage

The output voltage can be set easily through the ratio of a potential divider. The internal feedback reference voltage is 1.2 V.

$$V_o = V_{ref} \times (1 + \frac{R_B}{R_A}) \quad (23)$$

3.8. Soft start-up

A soft start-up operation is realized by using a capacitor connected to SS pin of the controller IC. In this case the controller used is the LTC3769 from Analog Devices. Other control ICs can be used. An internal current charger of 10 μA will continuously charge this capacitor until the voltage reaches the preset feedback threshold value of 1.2 V.

$$C_{SS} = \frac{t_{SS} \times I_{charge\_internal}}{V_{Feedback}} \quad (24)$$

3.9. LED dimming control

The LED dimming control (shown in Fig. 5) is realized by three sub-circuits formed by Nexperia logic and transistor products. PWM generation is done by using a relaxation oscillator consists of U2, RV1, and capacitor C29. The PWM frequency can be obtained by following formula:

$$f = \frac{1}{T} \approx \frac{1}{RC} \quad (25)$$

The above equation decides the total duration of capacitor charge and discharge time. However, the charge time and discharge time can be altered by potential meter RV1. With slide more close to pin 1 of RV1, it takes less time to charge capacitor, as charge current will go through diode D17 (PMEG2005EJ) and small portion of RV1. While discharge time will be much longer, since larger portion of RV1 resistance appears in the capacitor discharge path. This means lower duty cycle. For increasing the duty cycle, move the slider toward pin 3 of RV1.

A logic AND gate (74AHCT1G08) is added in between output of the oscillator and MOSFET gate driver for two purposes. The first one is increasing the current driving capability and the second one is disabling the gate driver during over current fault event.

A pair of NPN and PNP transistor (in one package, BC846BPN) is used to drive the dimming control MOSFET.

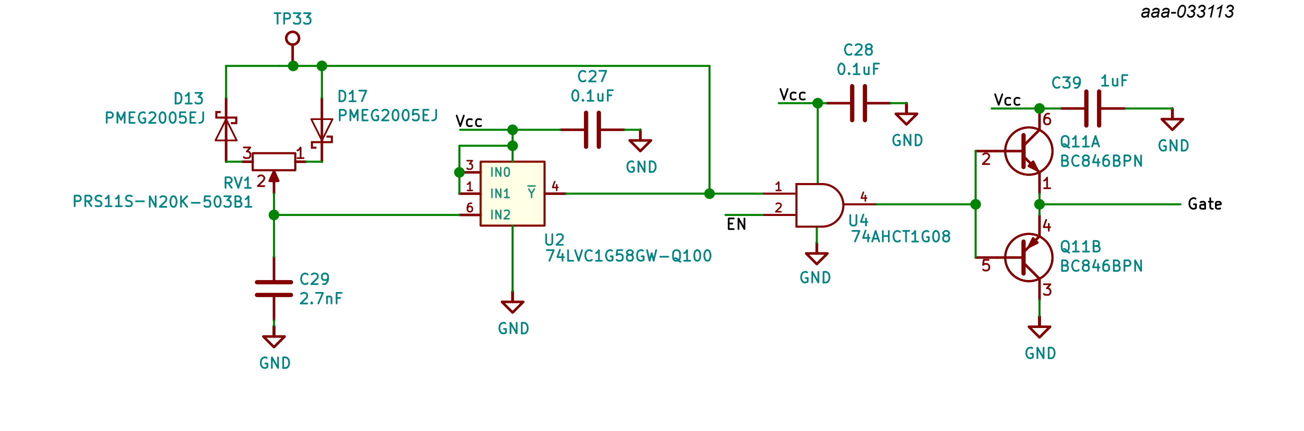

Fig. 5. PWM generation, duty cycle, enable and gate driver circuit

In order to sense current, a shunt resistor is connected in series with PWM controlled MOSFET. The current through LEDs will convert to voltage signal and amplified by a factor of 33. A comparator will compare amplified voltage signal with reference value 4 V. Once the amplified voltage signal exceed threshold, signal ‘EN’ is pull down and disabling the gate driver. This state will be held until a button is pressed.

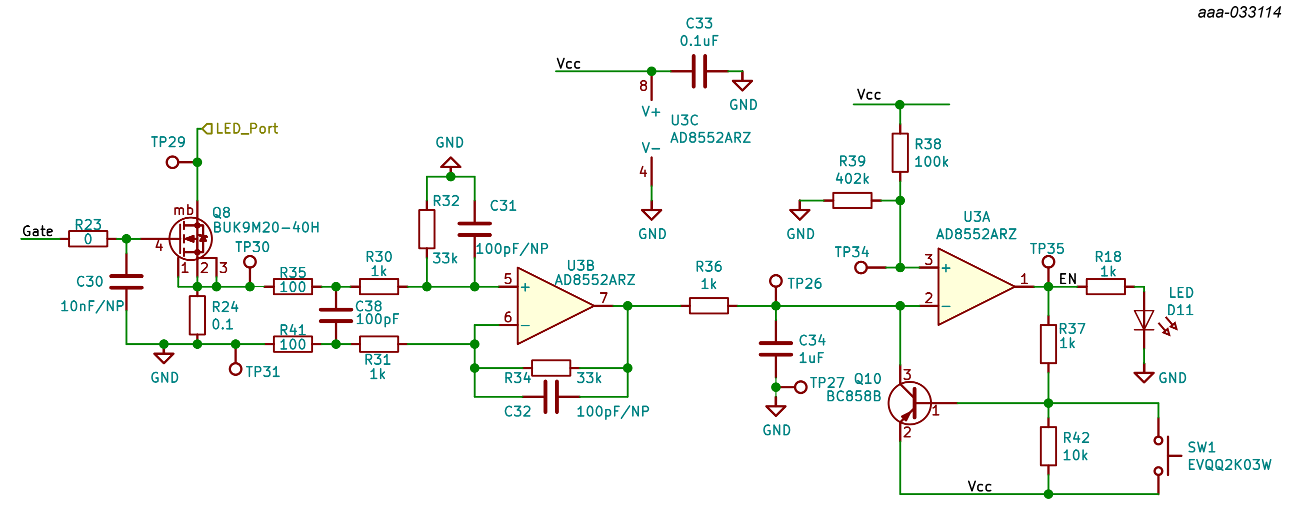

Fig. 6. Dimming MOSFET, current sense, and latch circuit

4. Schematics

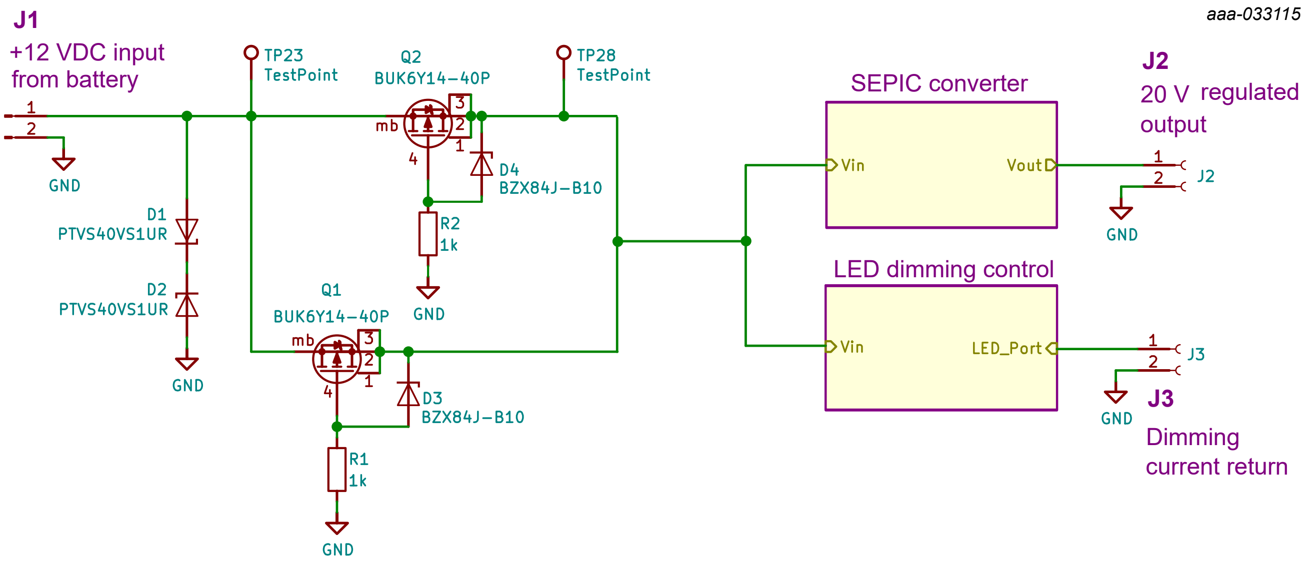

Fig. 7. Overview schematic

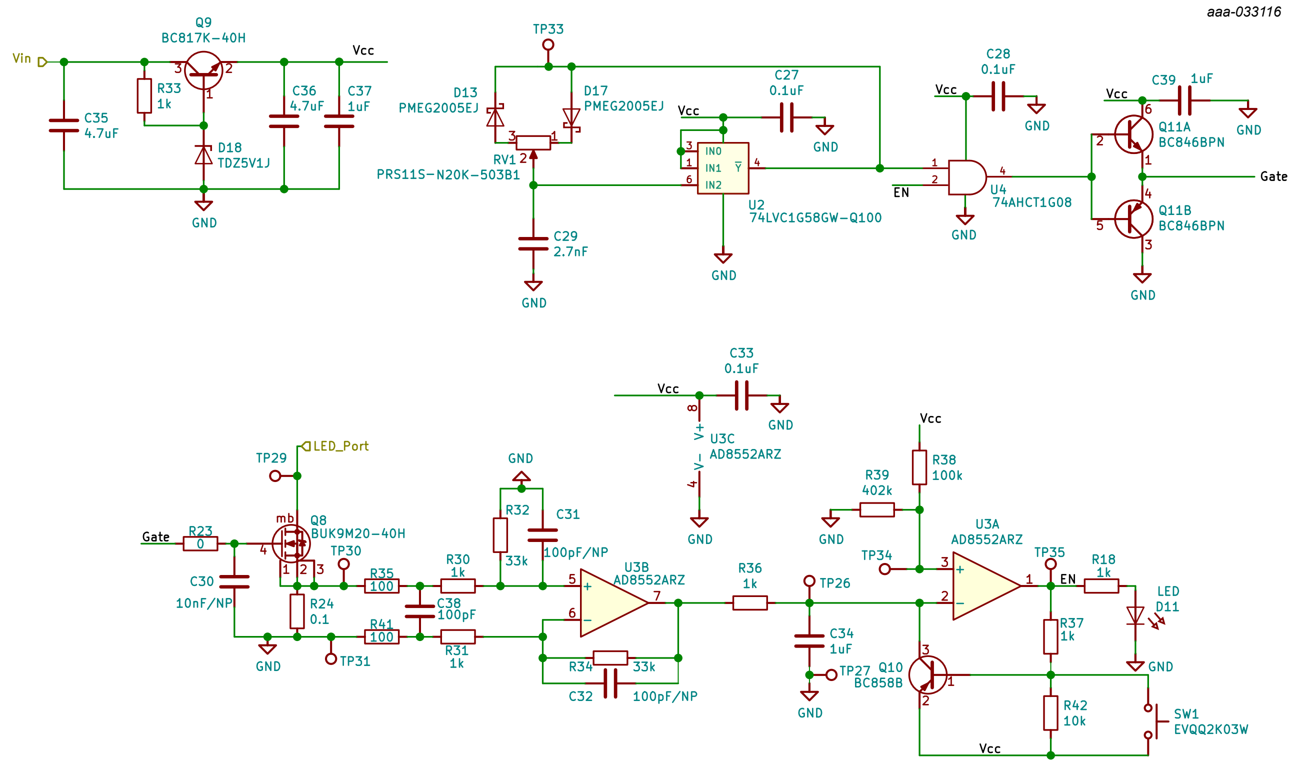

Fig. 8. PWM, duty cycle, current sense and latch circuits

4.1. SEPIC converter schematic

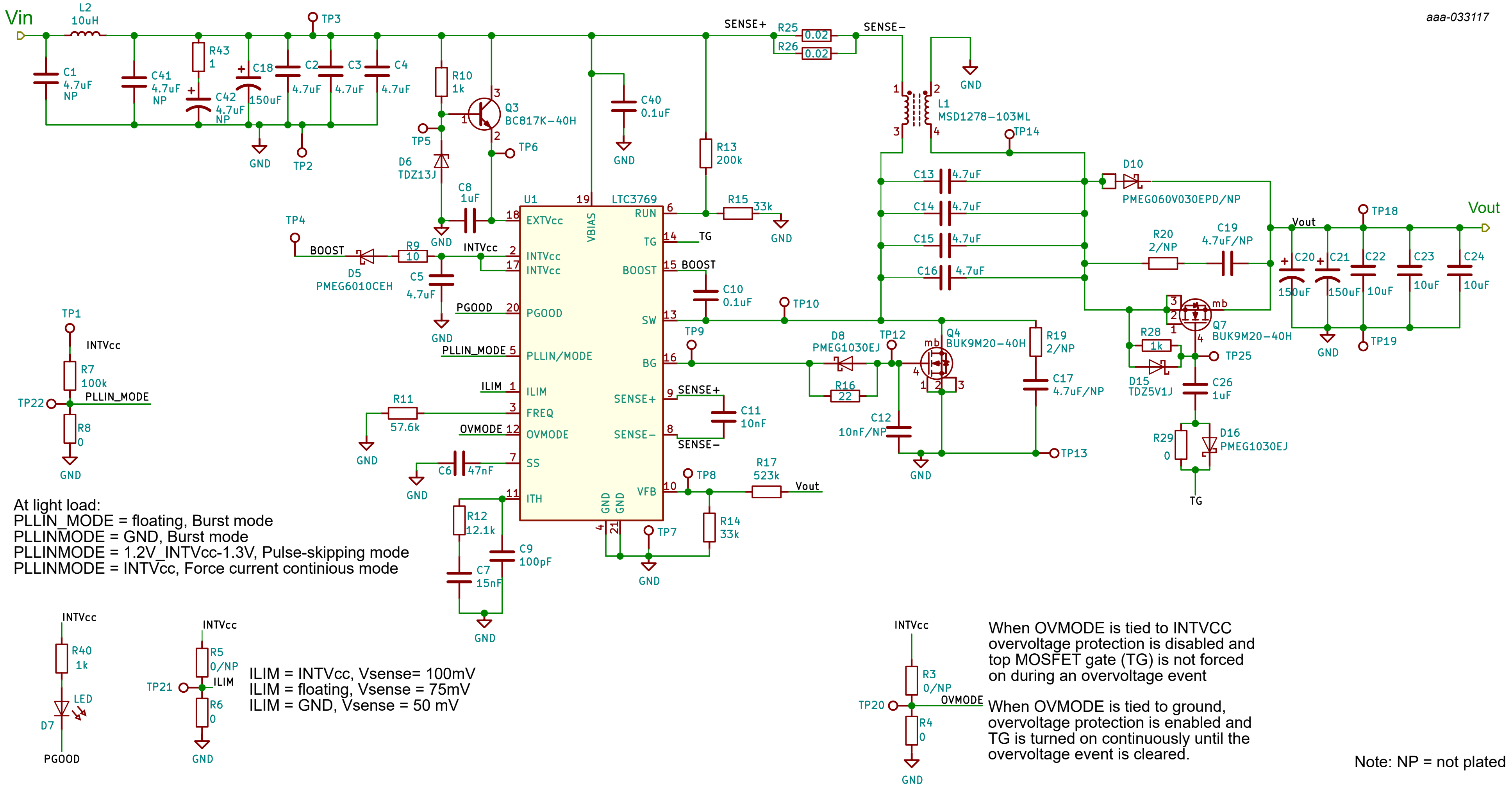

Fig. 9. SEPIC converter schematic diagram

5. Printed Circuit Board

A 4-layer PCB has been designed to demonstrate and verify the Nexperia SEPIC LED converter circuit.

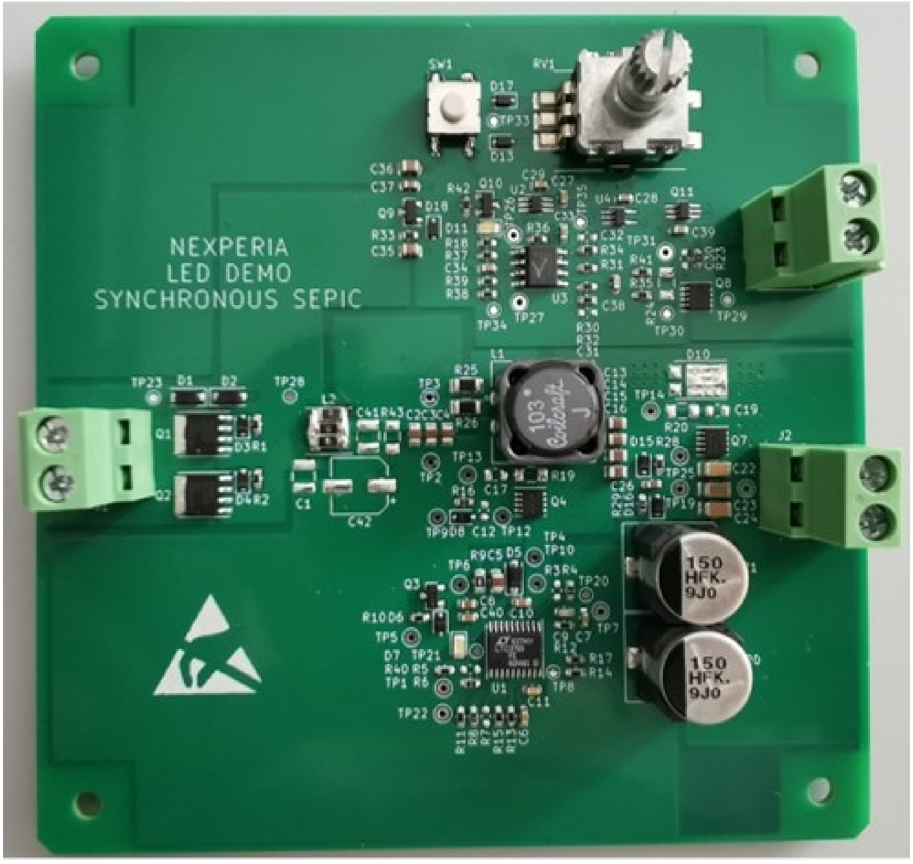

Fig. 10. SEPIC DC-to-DC converter PCB

Fig. 11, Fig. 12, Fig. 13, Fig. 14 and Fig. 15 show the PCB layers.

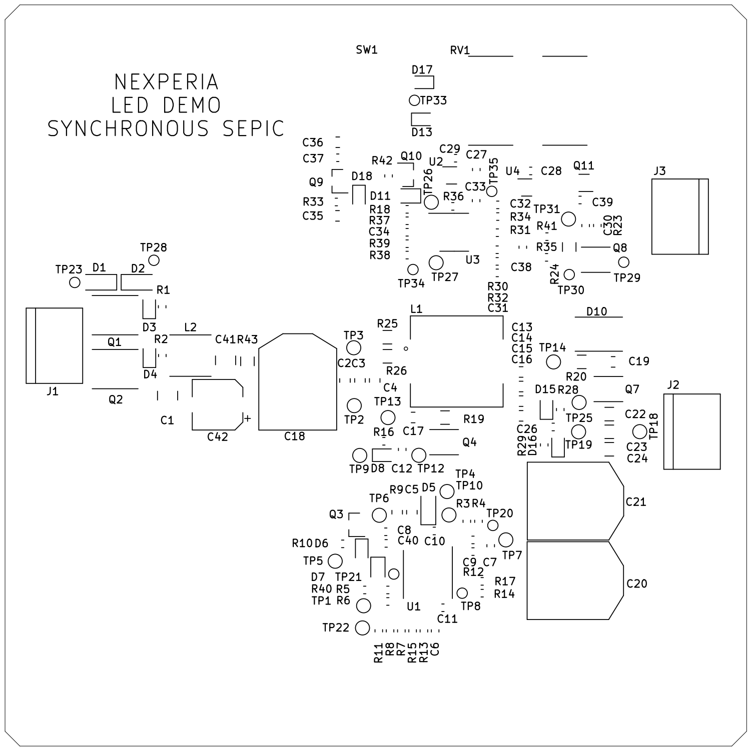

Fig. 11. PCB front silk screen layer

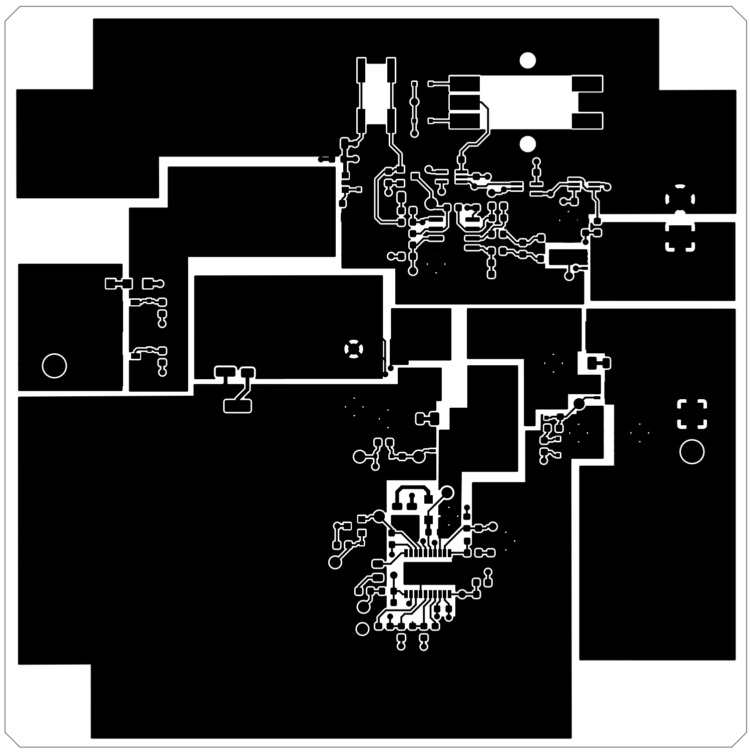

Fig. 12. PCB front copper layer

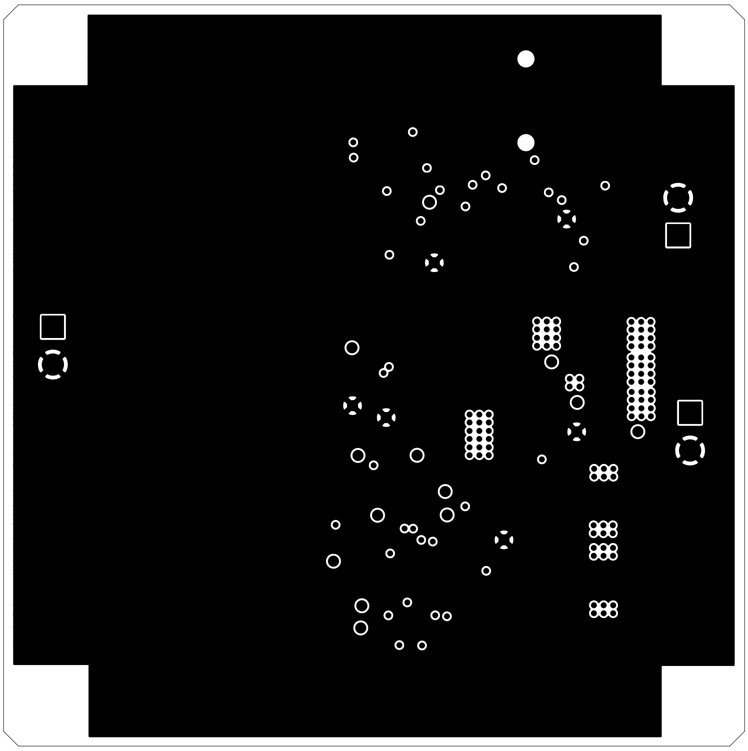

Fig. 13. PCB ground copper layer

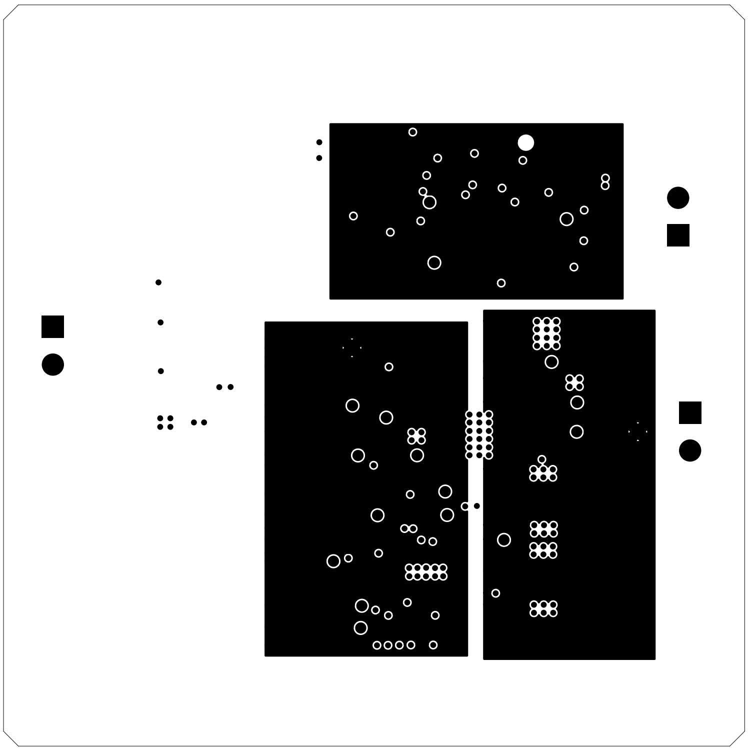

Fig. 14. PCB power copper layer

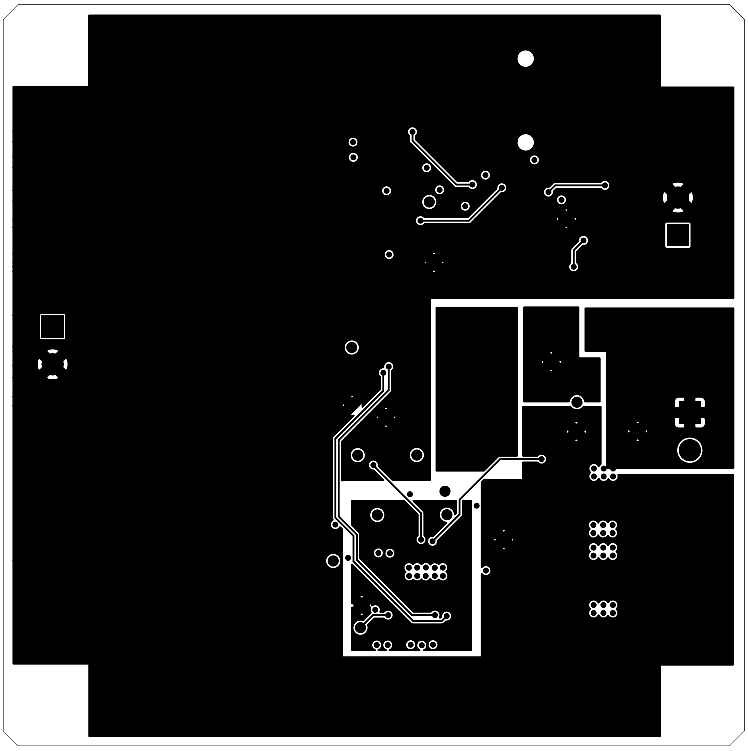

Fig. 15. PCB bottom copper layer

6. Bill of Materials

Table 1. BOM (Nexperia part)

Reference	Qty	Value	Part Number	Footprint
D1, D2	2	PTVS40VS1UR	PTVS40VS1UR	Diode_SMD: D_SOD123W
D3, D4	2	BZX84J-B10	BZX84J-B10	Diode_SMD: D_SOD-323F
D5	1	PMEG6010CEH	PMEG6010CEH	Diode_SMD: D_SOD-123F
D6	1	TDZ13J	TDZ13J	Diode_SMD: D_SOD-323F
D10	1	PMEG060V030EPD/NP	PMEG060V030EPD	Package_TO_SOT_SMD: SOT1289
D15, D18	2	TDZ5V1J	TDZ5V1J	Diode_SMD: D_SOD-323F
D8, D16	2	PMEG1030EJ	PMEG1030EJ	Diode_SMD: D_SOD-323F
D13, D17	2	PMEG2005EJ	PMEG2005EJ	Diode_SMD: D_SOD-323F
Q1, Q2	2	BUK6Y14-40P	BUK6Y14-40P	LFPAK56
Q3, Q9	2	BC817K-40H	BC817K-40H	Package_TO_SOT_SMD: SOT-23
Q4, Q7, Q8	3	BUK9M20-40H	BUK9M20-40H	LFPAK33
Q10	1	BC858B	BC858B	Package_TO_SOT_SMD: SOT-23
Q11	1	BC846BPN	BC846BPN	Package_TO_SOT_SMD: SOT-363_SC-70-6_ Handsoldering
U2	1	74LVC1G58GW-Q100	74LVC1G58GW-Q100	Package_TO_SOT_SMD: SOT-363_SC-70-6_ Handsoldering
U4	1	74AHCT1G08	74AHCT1G08GW-Q100	Package_TO_SOT_SMD: SOT-353_SC-70-5_ Handsoldering

Table 2. BOM (non-Nexperia)

Reference	Qty	Value	Part Number	Footprint
U1	1	LTC3769	LTC3769	TSSOP20
U3	1	AD8552ARZ	AD8552ARZ	Package_SO: SOIC-8_3.9x4.9mm_P1.27mm
C6	1	47nF	06033C473KAT2A	Capacitor_SMD: C_0603_1608Metric
C11	1	10nF	06033C103K4T2A	Capacitor_SMD: C_0603_1608Metric
RV1	1	PRS11S-N20K-503B1	PRS11S-N20K-503B1	PRS11S
L1	1	MSD1278-103ML	MSD1278-103ML	Coupled_Inductor
C9, C38	2	100pF	C0603C101J3GAUTO	Capacitor_SMD: C_0603_1608Metric
C22, C23, C24	3	10uF	GRT31CR61H106ME1L	Capacitor_SMD: C_1206_3216Metric
C7	1	15nF	GCJ188R71E153KA1D	Capacitor_SMD: C_0603_1608Metric
C29	1	2.7nF	GCD188R71H272KA1D	Capacitor_SMD: C_0603_1608Metric
C20, C21	2	150uF	EEE-FK1H151GV	CP_Elec_10.5x12

Reference	Qty	Value	Part Number	Footprint
R1, R2, R10, R18, R28, R30, R31, R33, R36, R37, R40	11	1k	ERJ-3EKF1001V	Resistor_SMD: R_0603_1608Metric
R9	1	10	ERJ-6GEYJ100V	Resistor_SMD: R_0805_2012Metric
R11	1	57.6k	ERJ-3EKF5762V	Resistor_SMD: R_0603_1608Metric
R12	1	12.1k	ERJ-3EKF1212V	Resistor_SMD: R_0603_1608Metric
R13	1	200k	ERJ-3EKF2003V	Resistor_SMD: R_0603_1608Metric
R14, R15, R32, R34	4	33k	ERJ-3EKF3302V	Resistor_SMD: R_0603_1608Metric
R17	1	523k	ERJ-3EKF5233V	Resistor_SMD: R_0603_1608Metric
R24	1	0.1	ERJ-8CWFR020V	Resistor_SMD: R_1206_3216Metric
R25, R26	2	0.02	ERJ-8CWFR020V	Resistor_SMD: R_1206_3216Metric
R4, R6, R8, R16, R23, R29	6	0	ERJ-3GEY0R00V	Resistor_SMD: R_0603_1608Metric
R35, R41	2	100	ERJ-3EKF1000V	Resistor_SMD: R_0603_1608Metric
R38	1	100k	ERJ-3EKF1003V	Resistor_SMD: R_0603_1608Metric
R39	1	402k	ERJ-3EKF4023V	Resistor_SMD: R_0603_1608Metric
R42	1	10k	ERJ-3EKF1002V	Resistor_SMD: R_0603_1608Metric
SW1	1	EVQQ2K03W	EVQQ2K03W	EVQQ2
D7	1	LED	FR1112H-TR	LED_SMD: LED_0805_2012Metric
D11	1	LED	VCDG1112H-4BY3C-TR	LED_SMD: LED_0805_2012Metric
C2, C3, C5, C13,C14,C15, C16, C35, C36	10	4.7uF	CGA4J1X7R1V475K125AC	Capacitor_SMD: C_0805_2012Metric
C10, C27, C28, C33, C40	5	0.1uF	CGA3E2X7R1E104K	Capacitor_SMD: C_0603_1608Metric
C8, C26, C34, C37, C39	5	1uF	CGJ3E1X7R1E105K080AC	Capacitor_SMD: C_0603_1608Metric

7. Conclusions

A battery supplied electrical system e.g. for LED lighting, requires a DC-to-DC converter to accommodate wide input voltage range. A Single-Ended Primary Inductance Converter (SEPIC) is suitable for this kind of application. In this application note, a general design approach of SEPIC DC-to-DC converter is presented. Mathematical equations should be used for initial components sizing. During this process, several iterations are required for optimal system performance. With aid of computer simulation tools and Nexperia device SPICE and RC thermal model, a more accurate initial estimation can be obtained.

8. References

1. Switching Power Supplies A-Z, Second Edition – Sanjaya Maniktala
2. RC Thermal Models – Nexperia

9. Revision history

Table 3. Revision history

Revision number	Date	Description
2.0	2021-05-10	Correction to Equation 6 and Equation 8.
1.0	2021-02-01	Initial version

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