AN50005

Paralleling power MOSFETs in high power applications

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Document information

Information	Content
Keywords	MOSFETs, paralleling, parameter spread, simulation
Abstract	This application note examines how current sharing imbalances between paralleled MOSFETs are affected by various parameters. Guidelines are given on taking these into account in designs. Realistic descriptions are provided to help designers to develop reliable and cost effective high power solutions.

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1. Introduction

In today's automotive and power industries, higher power requirements are leading to more designs that require lower R_{DSon}. Sometimes this is not achievable with a single packaged MOSFET and the design will need to make use of two or more devices in parallel. Higher power applications could also require the use of high performance substrates like heavy copper PCB, IMS (Insulated Metal Substrate) or DBC (Direct Bonded Copper) and even bare dies. By paralleling, the total current and thus dissipation is shared between each device. However, this is not as simple as applying Kirchhoff's current law: MOSFETs are not identical and thus they don't share equally.

This application note describes how sharing imbalances between paralleled MOSFETs form as well as guidelines and tools to take them into account. The final goal is to provide a set of best practices that can help to design circuits with standard paralleled MOSFETs.

2. Applications

Applications that require paralleled MOSFETs can be categorized into two main groups depending on the operation of the MOSFET: switch-mode and load switch.

The switch-mode types include motor drive applications, such as belt starter generators and superchargers, braking regeneration systems and switched mode power converters, such as regulators (DC/DC) and other types of inverters (DC/AC). Here the half-bridge represents the fundamental cell block that all the major circuit topologies are based upon. The MOSFETs are generally required to switch ON and OFF at a constant rate that can vary widely depending on the application, and are driven by a rectangular pulse with varying duty cycle (PWM). This is done with the intent of modulating the output power of the system to the load.

Load switching mainly refers to applications where MOSFETs are used in series with the battery such as in activation, safety switches and e-fuses, one example being battery isolation switches. The MOSFETs are required to switch ON once and will remain fully ON until the system is switched OFF. They might be swiftly switched OFF only in case some type of failure has been detected, for example in case of short circuit. Additionally, these switches may come in a back-to-back configuration in order to offer an additional reverse polarity protection.

This application note focuses on switch-mode applications and the half-bridge configuration.

3. Key specifications

The most important figure to monitor is the MOSFET junction temperature. This is a function of the power dissipated in each device which ideally should be uniform for all paralleled MOSFETs. Since $P = V \times I$ and the same voltage is applied across all the paralleled MOSFETs, it is clear that for ideal operation the current should be shared equally by each MOSFET and this is the simplest metric to quantify how well the MOSFETs perform. However, an equally valid approach is to consider the dissipated energy (or power), as done throughout the majority of this application note.

Current sharing in paralleled MOSFETs is mainly affected by the part to part variation of three data sheet parameters: R_{DSon}, $Q_{G(tot)}$, and $V_{GS(th)}$. This will be described further in the appropriate sections.

During the design phase, it is important to understand how to predict the worst case scenario in part to part variation in order to produce a reliable design. As with many other aspects of electronics, the designer will eventually decide how much of a headroom to adopt against the aforementioned worst case, maybe trading off some of the design robustness for improved performance. As better said in "*The Art of Electronics*":

> *"This example illustrates a frequent designer's quandary, namely a choice between a conservative circuit that meets the strict worst-case design criterion, and is therefore guaranteed to work, and a better-performing circuit design that does not meet worst-case specifications, but is overwhelmingly likely to function without problems. There are times when you will find yourself choosing the latter, ignoring the little voice whispering into your ear."* [1]

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Simulation setup

Disclaimer: this application note proposes the alteration of SPICE models. It is the user's responsibility to verify the model conformity to the data sheet, after any modification has been implemented. This can be done by following the guidelines described in the appendix.

The circuit used in the application note is composed of 3 MOSFETs in parallel both at the high and low side driving an inductive load, as shown in Fig. 1. The switching frequency is set at 20 kHz, duty cycle at 50 % and maximum V_{GS} is 15 V. Each MOSFET is conducting a current of 50 A, which is set by the constant current source of 150 A used in series with the load inductor. The SPICE simulation contains also three 0 V generators, one in each low side MOSFET source path, which are used to measure the low side drain current in order to calculate the dissipated energy and power. BUK7S1R0-40H is used throughout this document, unless stated otherwise. As shown in Fig. 1, parasitic inductance linked to the layout has been added to the simulation. There is no difference in terms of parasitics between the three branches (each branch corresponds to a single MOSFET and the path connecting it to the others in parallel through inlet and outlet: V_{SUPPLY} and phase for the high side, phase and GND for the low side).

This is an ideal scenario but achievable in practice within a reasonable margin. In this case any imbalance will only be determined by the intrinsic differences between the MOSFETs themselves. The importance of layout and influence of parasitics is discussed further in the corresponding chapter.

It is worth noting that the guidelines and observations made from now on do not depend on the battery voltage or other specifications, so they can be applied to a wide range of scenarios.

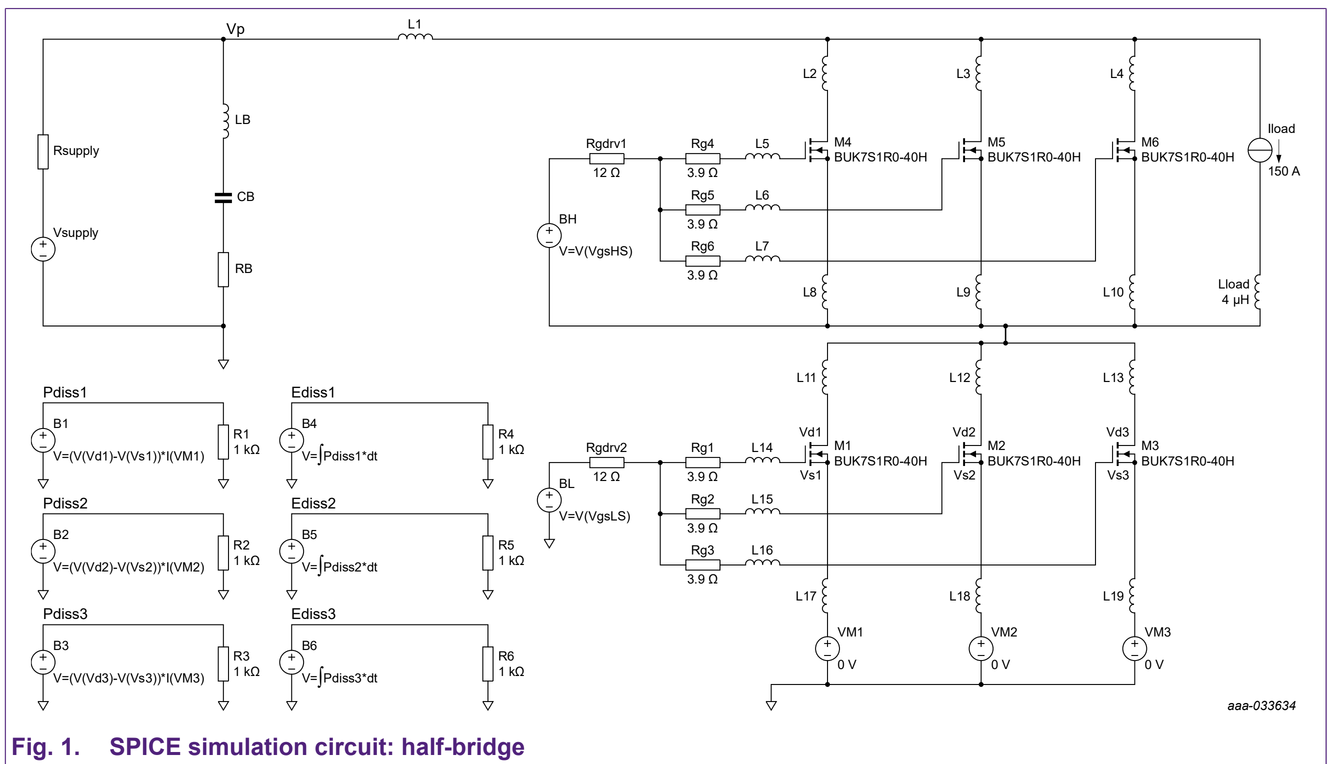

Fig. 1. SPICE simulation circuit: half-bridge

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4. MOSFET dissipation and parameters' influence on current sharing

By understanding how MOSFET dissipation works and highlighting which are the main parameters affecting it, it is possible to steer the worst case analysis towards a less burdensome but still realistic evaluation.

Power dissipation in a MOSFET employed in a half bridge is caused by two processes: conduction and switching. Fig. 2 shows the current flowing through the paralleled MOSFETs in case of ideal devices and the dissipated energy.

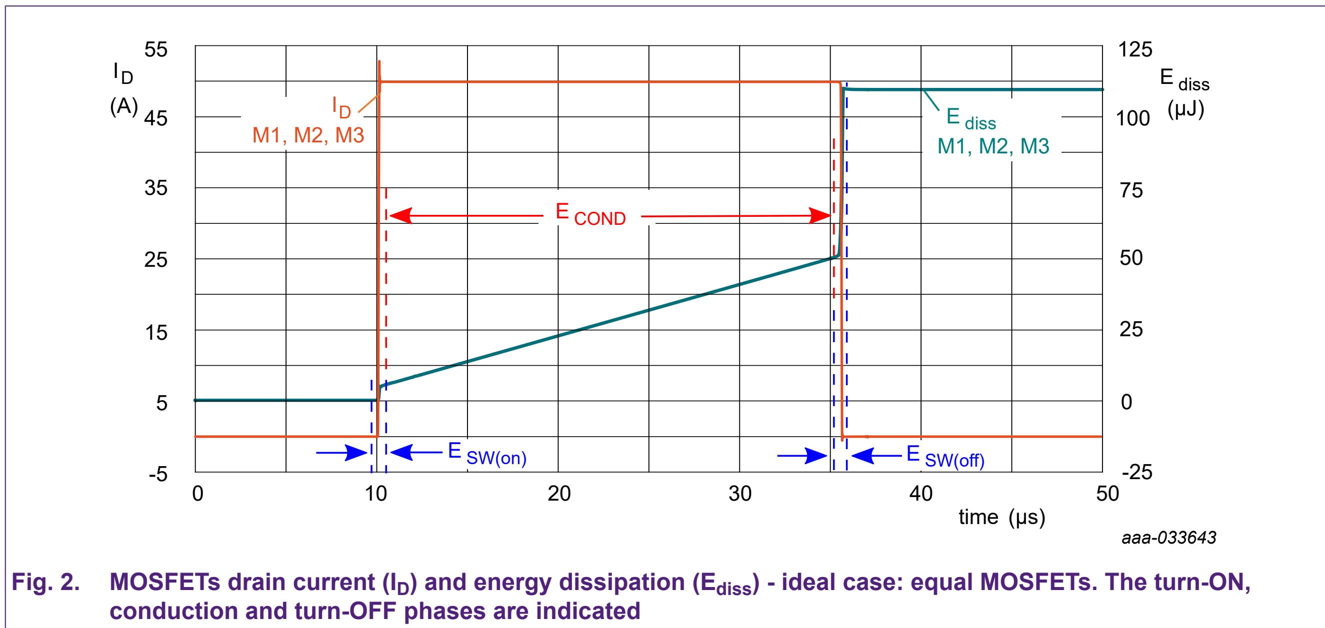

Fig. 2. MOSFETs drain current (I_D) and energy dissipation (E_{diss}) - ideal case: equal MOSFETs. The turn-ON, conduction and turn-OFF phases are indicated

The average power dissipated over a cycle can be found in a simulation environment or calculated, by taking into account each contribution separately. There is no hard separation between switching and conduction losses. However, in a simulation environment, the dissipated power can help in detecting this separation. Fig. 3 shows how the turn-ON phase has been found: the first point is set at around 9.9 μs where the power is 0 W, the second point is set at 10.4 μs where the dissipated power is almost constant at around 1.8 W (dissipated power during conduction - P_{cond}). While the drain current (I_D) flowing through MOSFET M1 is shown in Fig. 3, the drain-to-source voltage (V_{DS}) across it rises before the current falls, hence the valid loss recorded here. Moreover, the increase in dissipated power starting at 10 μs and lasting around 100 ns is due to the gate charge required to turn-ON the device.

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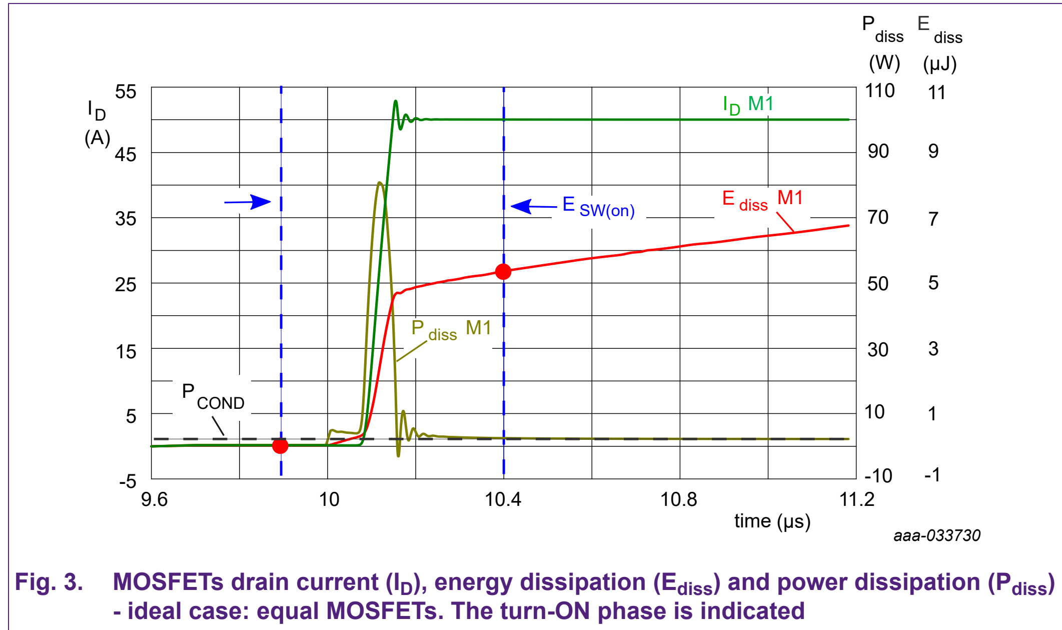

Fig. 3. MOSFETs drain current (I_D), energy dissipation (E_{diss}) and power dissipation (P_{diss}) - ideal case: equal MOSFETs. The turn-ON phase is indicated

Fig. 4 shows how the turn-OFF phase has been found: the first point is set at 36.2 µs where the power is 0 W, the second point is set at around 35.2 µs where the dissipated power starts to increase from 1.8 W.

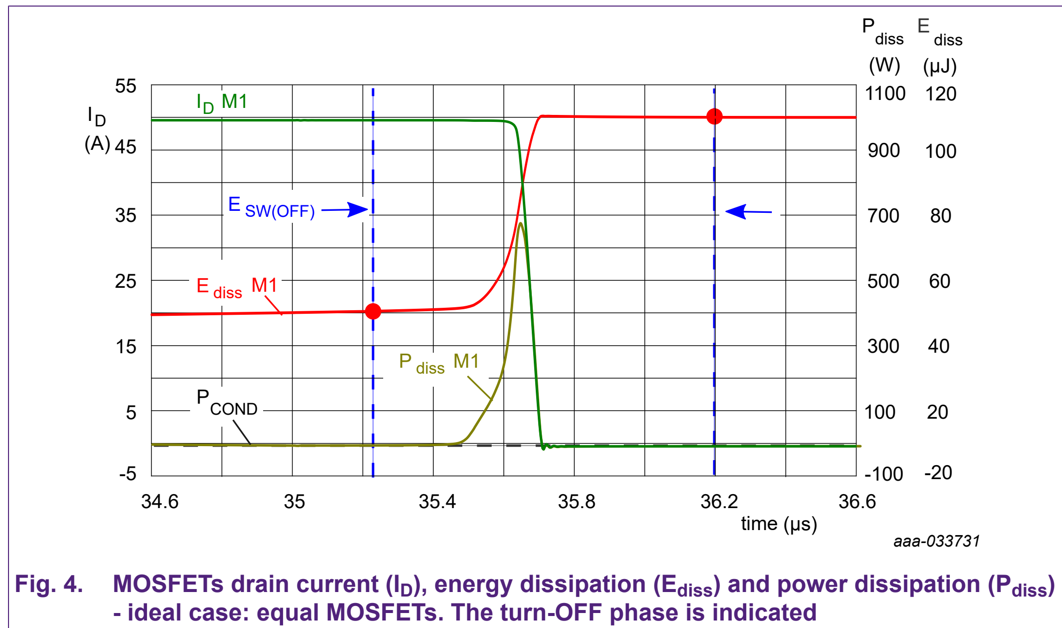

Fig. 4. MOSFETs drain current (I_D), energy dissipation (E_{diss}) and power dissipation (P_{diss}) - ideal case: equal MOSFETs. The turn-OFF phase is indicated

Equation 1 expresses the power dissipation in the MOSFET, while equations 2 and 3 show the individual contributions from switching and conduction.

$$P_{avg(tot)} = P_{sw} + P_{cond} \quad (1)$$

$$P_{sw} = (E_{sw(ON)} + E_{sw(OFF)}) \cdot f_{sw} \quad (2)$$

$$P_{cond} = E_{cond} \cdot f_{sw} \quad (3)$$

Where $E_{sw(ON)}$ and $E_{sw(OFF)}$ are the energy dissipation during turn-ON and turn-OFF, E_{cond} is the energy dissipation during a single conduction phase and f_{sw} the switching frequency. In this case, the total average power dissipated across each MOSFET over one cycle is around 2.1 W at 20 kHz.

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Table 1 shows the energy calculated during switching (divided into ON and OFF) and conduction. The degree of sharing of each MOSFET can be defined in several ways. Here it is defined as ratio between the energy dissipated in one MOSFET and the total energy dissipated in all of the paralleled devices, by using equation 4.

$$Total\ Energy\ Sharing = \frac{\left(E_{SW(ON)} + E_{SW(OFF)} + E_{SW(COND)}\right)_{(Mx)}}{\sum_{i=1}^{n\ FET}\left(E_{SW(ON)} + E_{SW(OFF)} + E_{SW(COND)}\right)_{(Mi)}} \cdot 100 \quad (4)$$

In this case, switching ($E_{sw(ON)}$ + $E_{sw(OFF)}$) accounts for around 55 % of the overall dissipation. However the switching:conduction dissipation ratio will depend on the switching frequency: a low frequency will lead to conduction losses dominating whereas switching losses will dominate at high frequency. Therefore, in order to simplify the evaluation, one might consider to take into account only parameters influencing the most important contribution.

With the MOSFET fully ON the only source of dissipation is given by its drain-to-source on state resistance (R_{DSon}). On the other hand, switching depends on threshold voltage ($V_{GS(th)}$) and input charge ($Q_{G(tot)}$).

Table 1. Summary - Ideal case: equal MOSFETs

Device	$E_{SW(ON)}$ [µJ]	$E_{SW(OFF)}$ [µJ]	E_{COND} [µJ]	Total Sharing
M1	5.1	52.8	46.1	33 %
M2	5.1	52.8	46.1	33 %
M3	5.1	52.8	46.1	33 %

5. Influence of parameter spread on current sharing performance

As previously mentioned, manufacturing spreads in data sheet parameters have a big impact on current sharing. Spread refers to the difference between maximum and minimum of a certain parameter. These spreads are unavoidable and caused by both intra- and inter- wafer variation during the silicon die fabrication. Every MOSFET produced by any manufacturer will carry these spreads. Nexperia’s power MOSFET fabrication processes are optimised to keep spreads as tight as possible in order to achieve good performance and reliability.

It is important to understand how each of the aforementioned parameters affect the current sharing among paralleled devices, before describing techniques and guidelines to counteract them. This can be done in a simulation environment. In the following section each parameter will be set at the outmost values of its data sheet spread. In addition to the simulations presented here, the Appendix contains experimental measurement data from an identical setup using MOSFETs with similar parameter spreads.

It is worth noting that spreads are measured and thus guaranteed only at certain electrical conditions. For instance, the threshold voltage spread is specified between 1 µA and 100 mA and at V_{DS} of 5 V, as shown in Fig. 5. However, this same behaviour is not guaranteed at higher currents.

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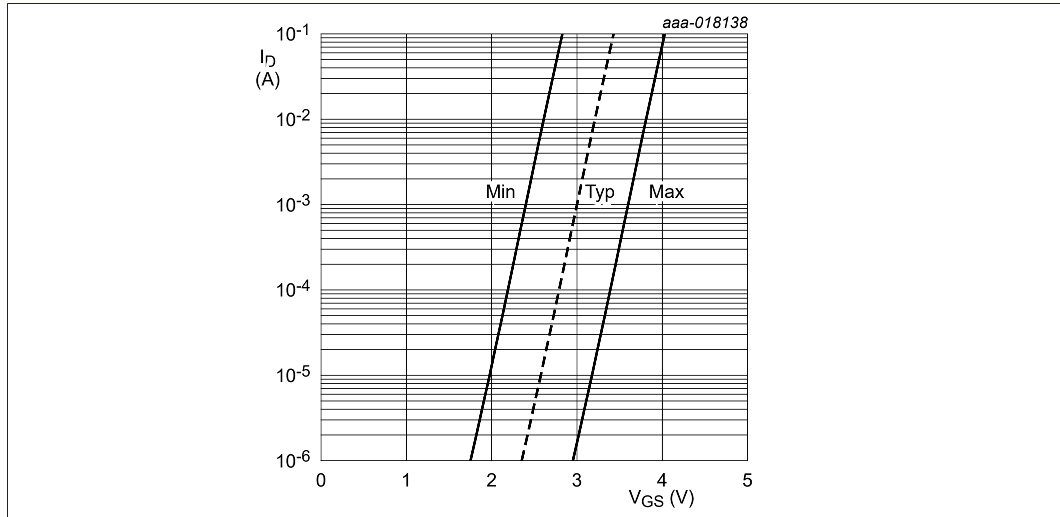

Fig. 5. BUK7S1R0-40H sub-threshold drain current as a function of gate-source voltage

5.1. Static operation (DC)

5.1.1. Drain-source on-state resistance – R_{DSon}

Table 2. BUK7S1R0-40H data sheet characteristics: R_{DSon}

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		0.62	0.88	1	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C		0.87	1.3	1.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C		0.97	1.4	1.75	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C		1.2	1.8	2.2	mΩ

The total spread, as per data sheet, is ΔR_{DSon} = 0.38 mΩ or $\Delta R_{DSon,rel}$ = ± 21.6 % (relative percentage with respect to the nominal value). The SPICE model of the device has been adjusted to account for the R_{DSon} spread. This is done by changing the value of the R_D parameter, located in the “Drain, gate and source resistances” section. The correct values can be found by sweeping the parameter after declaring a variable in the form of {variable}.

Table 3. SPICE model mod for R_{DSon} spread

SPICE parameter – *RD*	R_{DSon} [mΩ]	Conditions
316.247u	0.62	V_{GS} = 10 V, I_D = 25 A, T_j = 25 °C
576.260u	0.88	
695.949u	1.00	

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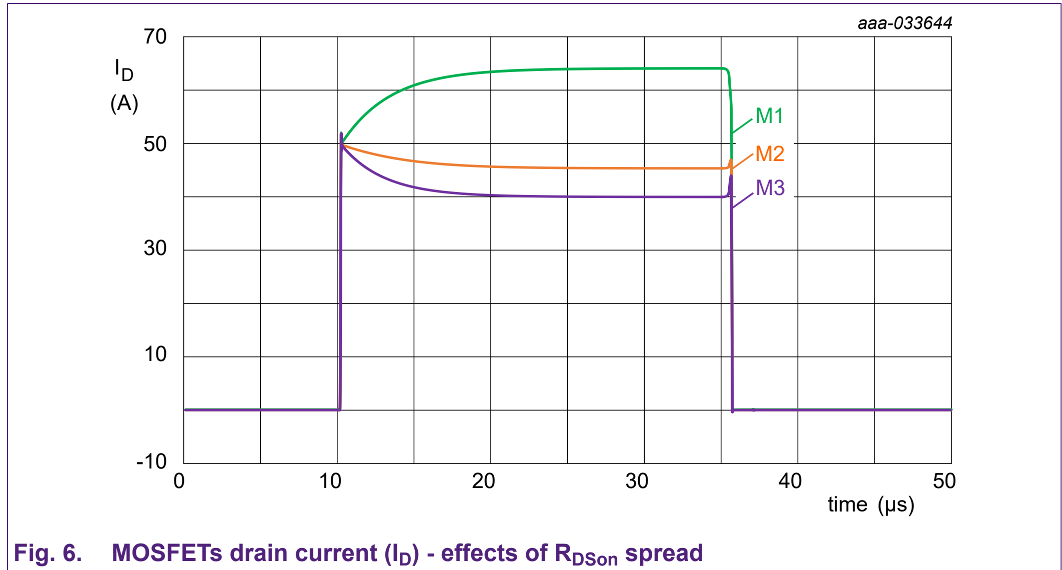

Fig. 6. MOSFETs drain current (I_D) - effects of R_{DSon} spread

The simulation setup and results are summarized in Table 4. The MOSFET having lower R_{DSon} (M1) will need to handle more energy, vice versa for M3. Both sharing during conduction and switching are impacted. M1 is now dissipating 2.5 W, around 20% more than the ideal case (2.1 W) while M3 is dissipating 1.7 W.

These results are valid only for the first cycles of operation, after which the temperature dependency of the R_{DSon} partly balance out the sharing, more information is provided in the corresponding section on temperature dependency.

Table 4. Summary - Effects of R_{DSon} spread

Device	R_{DSon} [mΩ]	$E_{SW(ON)}$ [µJ]	$E_{SW(OFF)}$ [µJ]	Energy Sharing Switching	E_{COND} [µJ]	Energy Sharing Conduction
M1	0.62	5.0	65.9	40.7 %	52.9	39.4 %
M2	0.88	5.1	48.8	30.9 %	42.5	31.6 %
M3	1	5.1	44.3	28.4 %	38.9	29.0 %

5.2. Dynamic operation

5.2.1. Total input charge – $Q_{G(tot)}$

Table 5 gives the typical and maximum values for gate charge parameters $Q_{G(tot)}$, Q_{GS} and Q_{GD}; refer to Fig. 7 for definitions of these parameters.

Table 5. BUK7S1R0-40H data sheet characteristics: gate charge

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V		-	98	137	nC
Q_{GS}	gate-source charge			-	27	40	nC
Q_{GD}	gate-drain charge			-	17	34	nC

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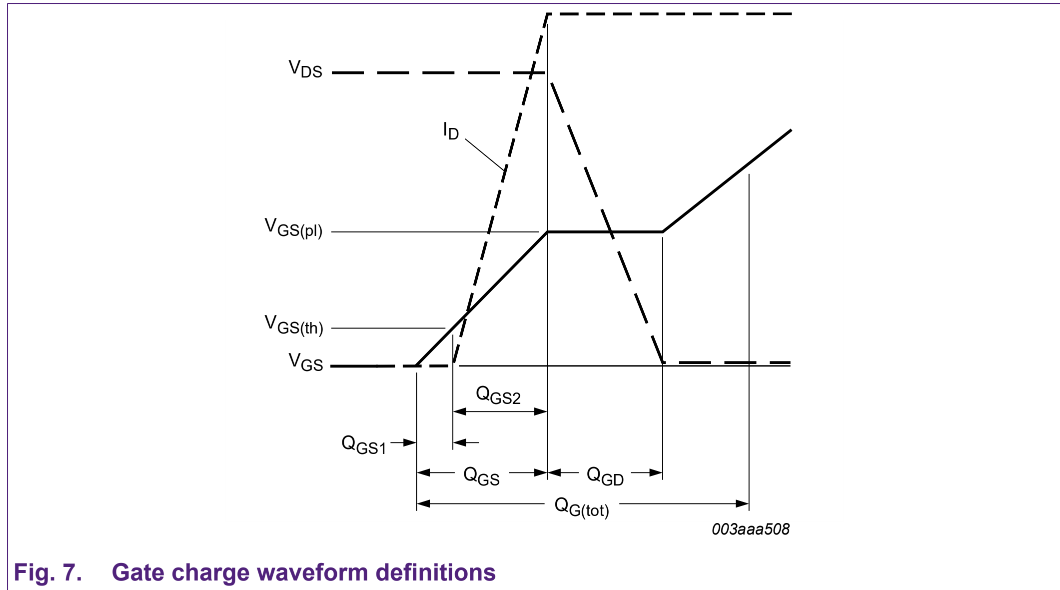

Fig. 7. Gate charge waveform definitions

The total spread, as per data sheet, is $\Delta Q_{G(tot)}$ = 39 nC or $\Delta Q_{G(tot),rel}$ = +40 %. In order to introduce this spread in the SPICE model, it is necessary to evaluate separately the contribution of Q_{GS} and Q_{GD} through C_{GS} and C_{GD}.

By doing so, the MOSFET will end up showing slightly higher maximum $Q_{G(tot)}$, since it is much harder to control the slope of the V_{GS} curve after the plateau voltage (refer to Fig. 7). Moreover, the two capacitances will not necessarily behave in the same way: being mostly independent, it could happen that a MOSFET shows, for instance, higher C_{GD} and lower C_{GS}, or any other combination in between. To facilitate the evaluation, the two have been considered both at their typical and maximum values only.

The SPICE model of the device has been adjusted to account for the C_{GD} and C_{GS} spread. This is done by changing the value of C_{GS} and multiplying the C_{GD} value by a specific coefficient *CGD_scale*. The former is defined as a constant value while C_{GD} as a voltage dependent value at the line “G11 3 2 VALUE …” in the corresponding section. The correct values can be found by sweeping the parameter after declaring a variable in the form of {*variable*}.

Table 6. SPICE model mod for $Q_{G(tot)}$ spread

SPICE parameter		Conditions
CGS	**Q_{GS} [nC]**	V_{DS} = 32 V; I_D = 25 A; V_{GS} = 10 V
6.1n	27.148	
9.24n	40.024	
CGD_scale	**Q_{GD} [nC]**	
0.84	17.008	
1.65	34.211	

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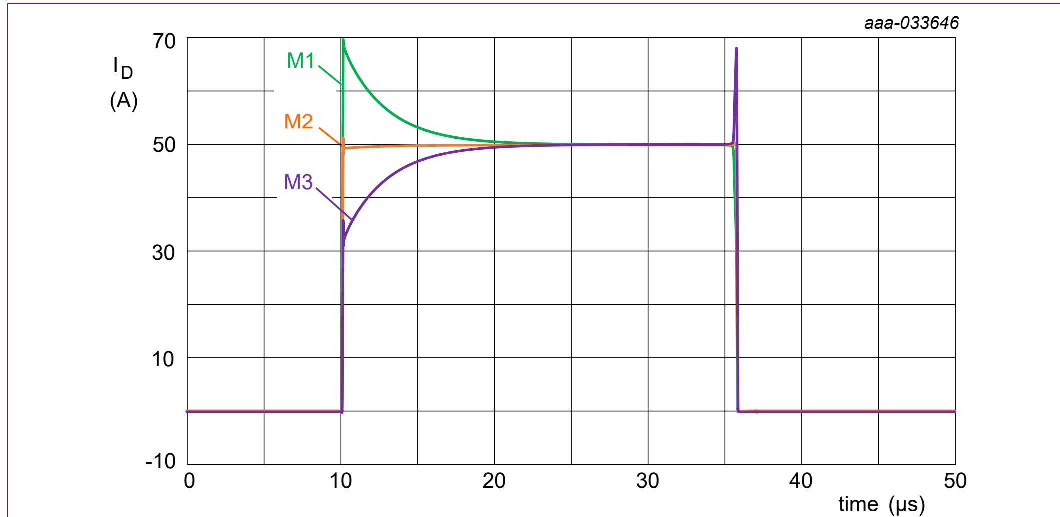

Fig. 8. MOSFETs drain current (I_D) - effects of $Q_{G(tot)}$ spread

The simulation setup and results are summarized in Table 7. The value of $Q_{G(tot)}$ has been calculated as the sum of the respective Q_{GS} and Q_{GD} (from Table 6). At turn-ON the device with lower input capacitance (M1) will switch ON first thus handling majority of the current. On the other hand, at turn-OFF the MOSFET with higher input capacitance (M3) will switch OFF last now handling most of the current. The sharing during switching is the most impacted, while conduction has changed only marginally. M3 is now dissipating 2.8 W (0.7 W more than the ideal case) while M1 is dissipating 1.9 W.

Table 7. Summary - Effects of $Q_{G(tot)}$ spread

Device	$Q_{G(tot)}$ [nC]	$E_{SW(ON)}$ [µJ]	$E_{SW(OFF)}$ [µJ]	Energy Sharing Switching	E_{COND} [µJ]	Energy Sharing Conduction
M1	94.4	9.4	35.7	21.4 %	49.9	35.8 %
M2	125.7	6.9	60.8	31.9 %	46.1	33.2 %
M3	158.0	4.7	94.4	46.7 %	43.2	31.0 %

5.2.2. Gate-source threshold voltage – $V_{GS(th)}$

Table 8. BUK7S1R0-40H data sheet characteristics: $V_{GS(th)}$

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		2.4	3	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		1	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	-	4.3	V

The total spread, as per data sheet, is $\Delta V_{GS(th)}$ = 1.2 V or $\Delta V_{GS(th),rel}$ = ± 20 %. The SPICE model of the device has been adjusted to account for the $V_{GS(th)}$ spread. This is done by changing the value of the Vto parameter located in the ".MODEL MINT NMOS" section. The correct values can be found by sweeping the parameter after declaring a variable in the form of {variable}.

Table 9. SPICE model mod for $V_{GS(th)}$ spread

SPICE parameter Vto	$V_{GS(th)}$ [V]	Conditions
3.243	2.400	V_{DS} = 12 V, I_D = 1 mA
3.843	3.000	
4.443	3.600	

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The MOSFETs drain current is shown in Fig. 9. After turn-ON, the loop inductance present in the circuit causes the current to stabilise only after 10 µs, further details in the Layout-dependent parasitics section.

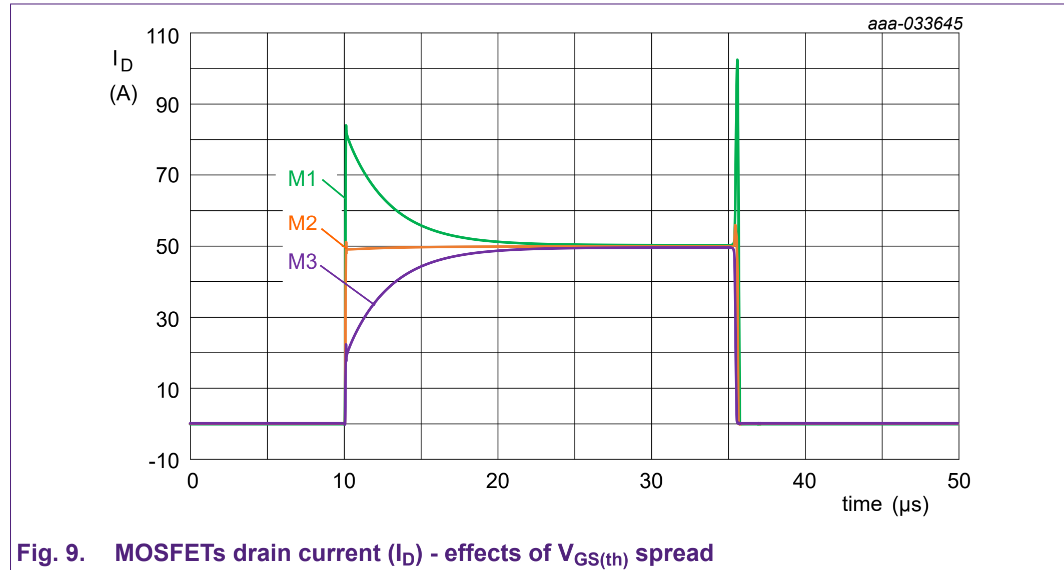

Fig. 9. MOSFETs drain current (I_D) - effects of $V_{GS(th)}$ spread

The simulation setup and results are summarized in Table 10. The MOSFET having lower $V_{GS(th)}$ will need to handle more energy overall. At turn-ON M1 will switch ON first thus handling majority of the current. Moreover, at turn-OFF the same MOSFET will switch OFF last, again, handling most of the current. The sharing during switching is the most impacted, with one MOSFET (M3) participating only minimally in the process, while conduction has changed only marginally. M1 is now dissipating 4.7 W (2.6 W more than the ideal case) while M3 only 1 W.

Table 10. Summary - Effects of $V_{GS(th)}$ spread

Device	$V_{GS(th)}$ [V]	$E_{SW(ON)}$ [µJ]	$E_{SW(OFF)}$ [µJ]	Energy Sharing Switching	E_{COND} [µJ]	Energy Sharing Conduction
M1	2.4	9.3	172.2	74.4 %	52.7	37.8 %
M2	3	5.1	48.7	22.1 %	45.7	32.8 %
M3	3.6	2.2	6.4	3.5 %	40.8	29.4 %

In conclusion, the MOSFET having lower $V_{GS(th)}$ will need to handle more energy both during turn-ON and turn-OFF, while with the capacitance spread the switching energy will be balanced between at least two devices. These results are valid only for the first cycles of operation, due to the temperature dependency of the $V_{GS(th)}$. More information is provided in the corresponding section on temperature dependency. Refer to Section 7.1 for an explanation of the shape of the current between switching and conduction, as shown in Fig. 6, Fig. 8 and Fig. 9.

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5.3. Paralleled MOSFETs and temperature dependency

Each MOSFET can be thought as a system composed of an electrical subsystem in a feedback loop with a thermal subsystem, as shown in Fig. 10.

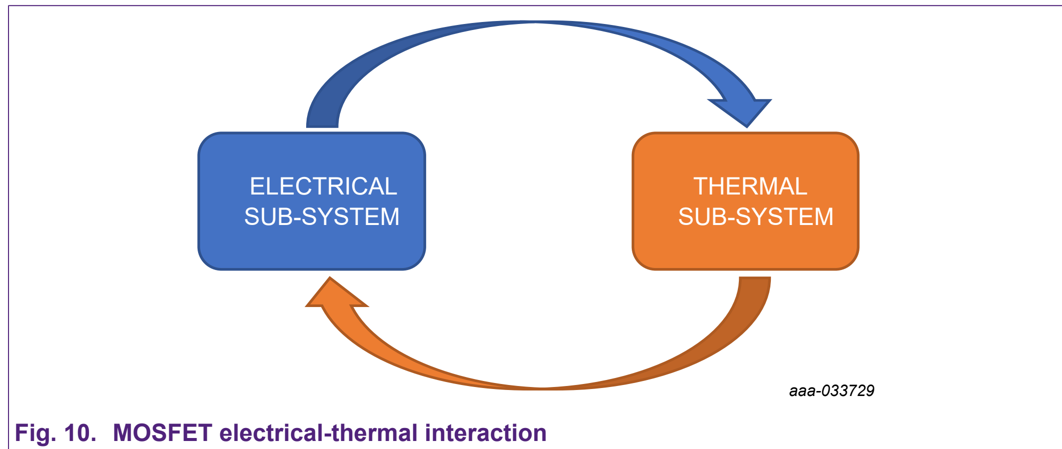

Fig. 10. MOSFET electrical-thermal interaction

Power MOSFETs are often considered to be immune to thermal runaway due to the R_{DSon} temperature coefficient. However, this is only true for MOSFETs that are fully ON. When a MOSFET is in the on-state, there are two competing effects that determine how its current behaves with increasing temperature. As the temperature rises, $V_{GS(th)}$ falls, thereby increasing the current. On the other hand, R_{DSon} increases with increasing temperature, thereby reducing the current. The resistance increase dominates at higher gate-source voltages (V_{GS}), while the threshold-voltage drop dominates at low V_{GS}. Consequently, for a given V_{DS}, there is a critical V_{GS} below which there is a positive feedback regime and above which there is a negative feedback and thermal stability. This critical point is known as the Zero Temperature Coefficient (ZTC) point, Fig. 11.

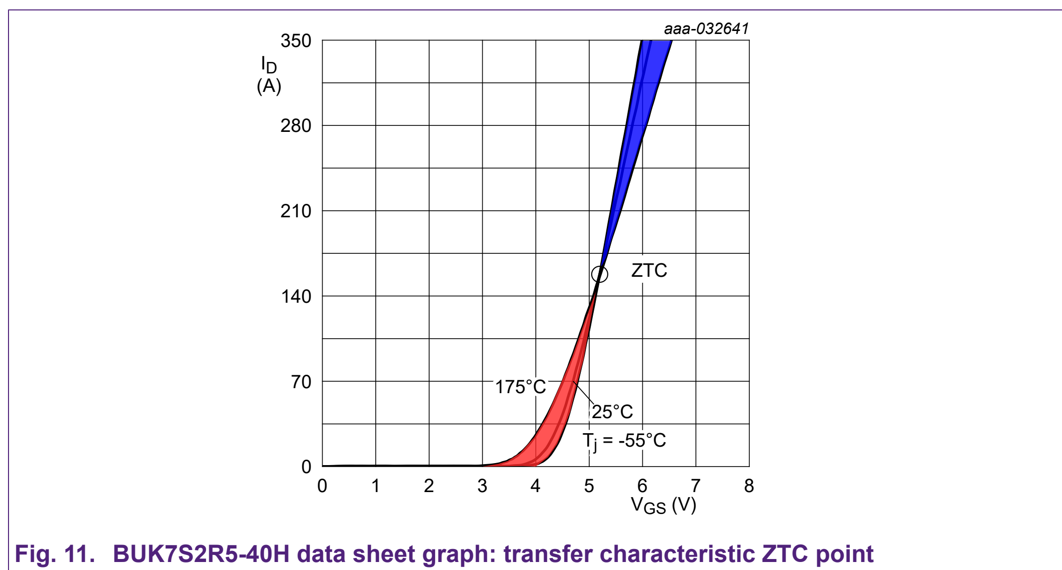

Fig. 11. BUK7S2R5-40H data sheet graph: transfer characteristic ZTC point

The interaction between thermal and electrical subsystems can be simulated using Nexperia advanced models[1] which make two additional thermal pins accessible: junction and case/mounting base. Within these models, parameters of interest for the paralleling are modelled with increased accuracy by including their temperature dependency. A circuit modelling the overall thermal system MOSFET-PCB-ambient to the drain tab must be connected to the mounting base pin of the model.

1 The advanced models will be released later in 2021

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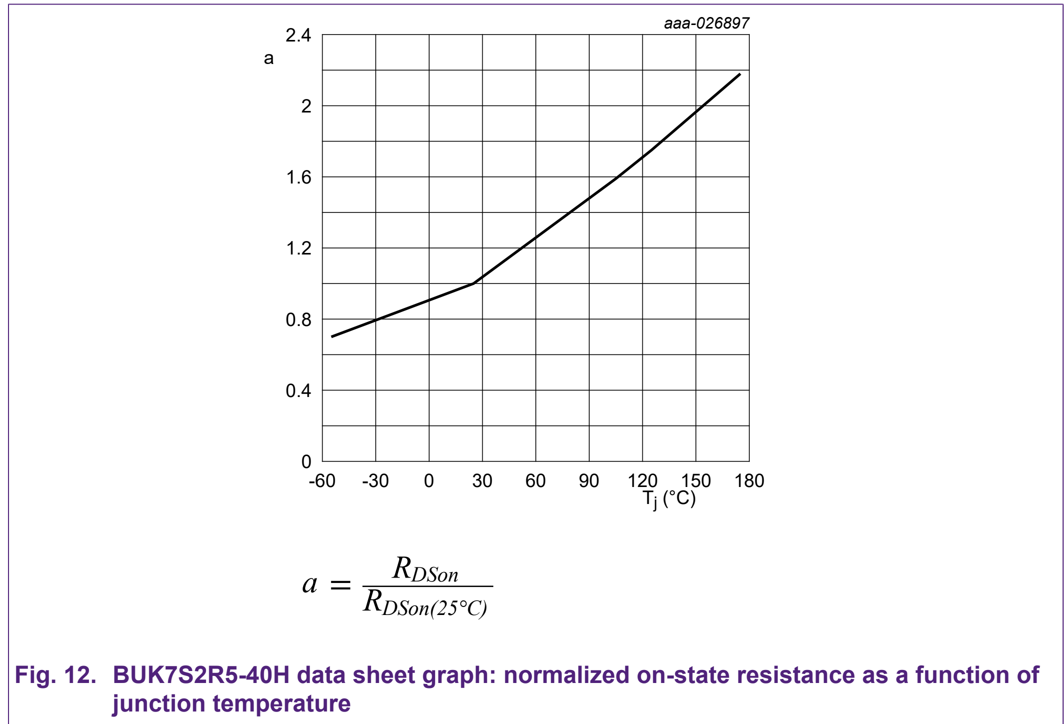
5.3.1. Temperature dependency during static operation (DC)

In a parallel configuration, R_{DSon} has the advantage of improving the sharing due to its positive temperature coefficient (PTC), Fig. 12. As one MOSFET conducts more current and dissipates more power, R_{DSon} increases and the conduction losses change improving the sharing.



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 12. BUK7S2R5-40H data sheet graph: normalized on-state resistance as a function of junction temperature

Ideally this phenomenon is maximized when the thermal coupling between paralleled MOSFETs is less effective, as each MOSFET is less influenced by the others around it. However, this leads to higher junction temperatures. This phenomenon can be described using the steady state simulation shown in Fig. 13. This time, to simplify the interaction, only two MOSFETs have been used in parallel. Additionally, a second circuit is used to model the thermal coupling between the two MOSFETs and their connection with the PCB.

The SPICE model of the devices have been adjusted in order for M1 to show lower R_{DSon} (0.62 mΩ) than M2 (1 mΩ).

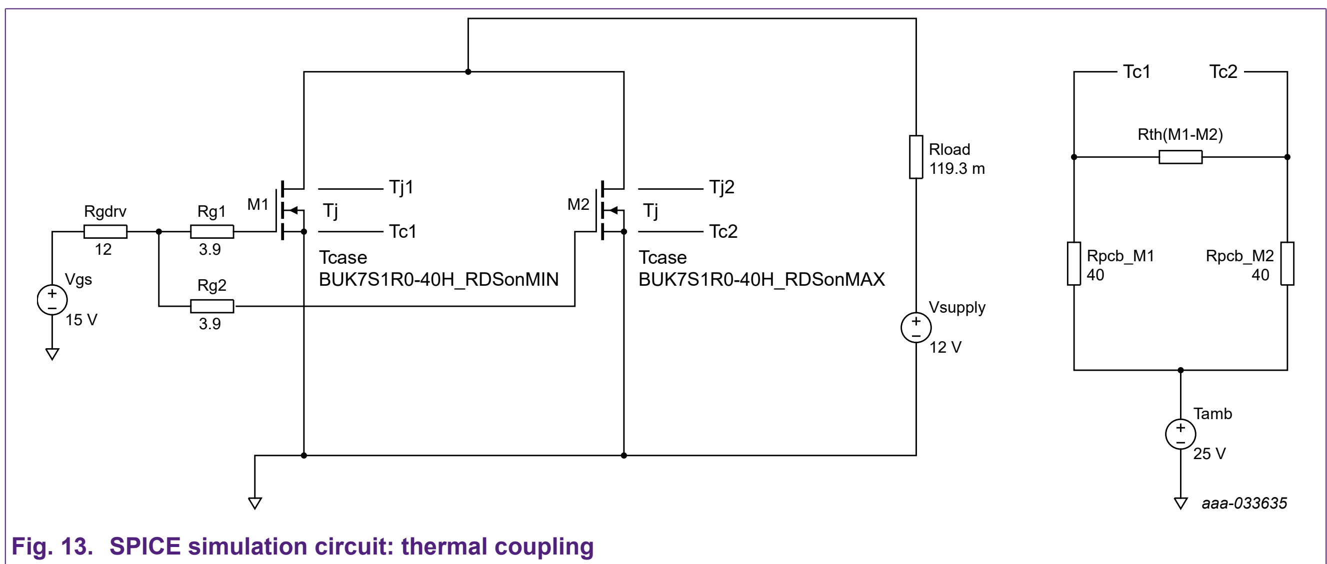


Fig. 13. SPICE simulation circuit: thermal coupling

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With reference to the graph in Fig. 14: the total current flowing through the devices is set at 100 A so that the leftmost y-axis shows current and sharing in percentage at the same time. In this case current has been used to calculate the degree of sharing between the MOSFETs as this example considers purely steady state conduction. As the thermal coupling between the two MOSFETs worsens (Rth(M1-M2) increases) the junction temperature of M1 increases while the current sharing in steady state improves (converges more towards 50 %). Moreover, even in case of high decoupling the R_{DSon} PTC will only improve the sharing by a maximum of around 2 % for each MOSFET.

Therefore good thermal coupling between paralleled MOSFETs is to be preferred as it allows for lower junction temperatures. More details on this are provided in the *PCB Layout influence: Circuit layout* section.

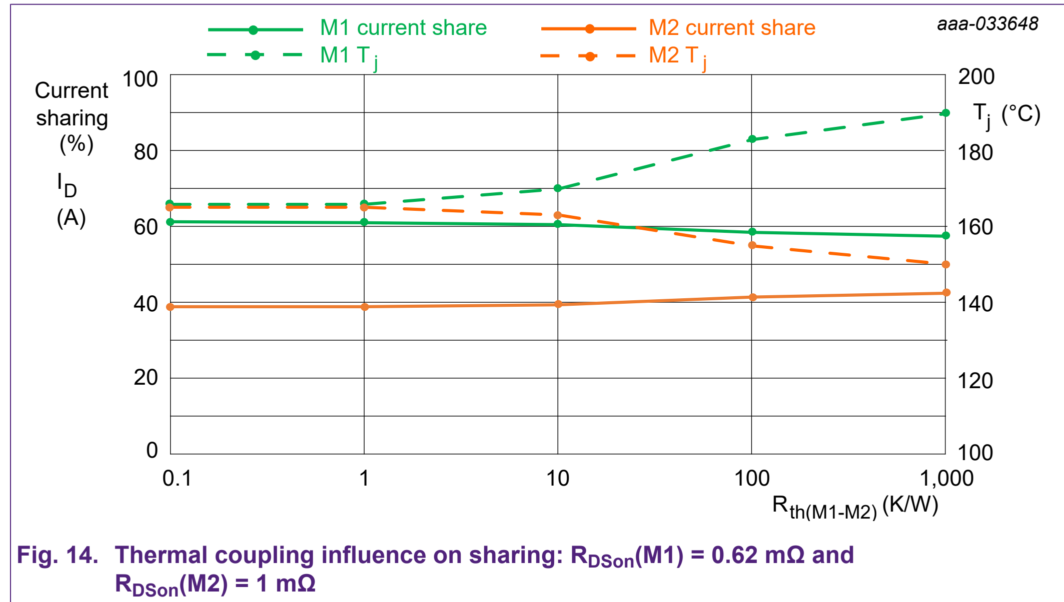

Fig. 14. Thermal coupling influence on sharing: R_{DSon}(M1) = 0.62 mΩ and R_{DSon}(M2) = 1 mΩ

5.3.2. Temperature dependency during dynamic operation

Threshold voltage is characterized by a negative temperature coefficient (NTC): it decreases as the junction temperature increases. This behaviour is more detrimental in case of paralleled MOSFETs. For instance, a device with an initial higher junction temperature will exhibit an even lower $V_{GS(th)}$ which increases the current flowing through the MOSFET and thus the power that it dissipates. As in the static case, good thermal coupling helps to keep the MOSFETs at similar temperatures. Other guidelines could be adopted to mitigate temperature gradient across paralleled MOSFETs, for more information refer to PCB Layout influence: Circuit layout.

Fig. 15 shows how the $V_{GS(th)}$ spread is almost constant with respect to the junction temperature, however this behaviour is guaranteed only at a drain current of 1 mA. For a temperature difference of 20 °C (from 25 to 45 °C) V_{GSth} reduces by about 0.2 V.

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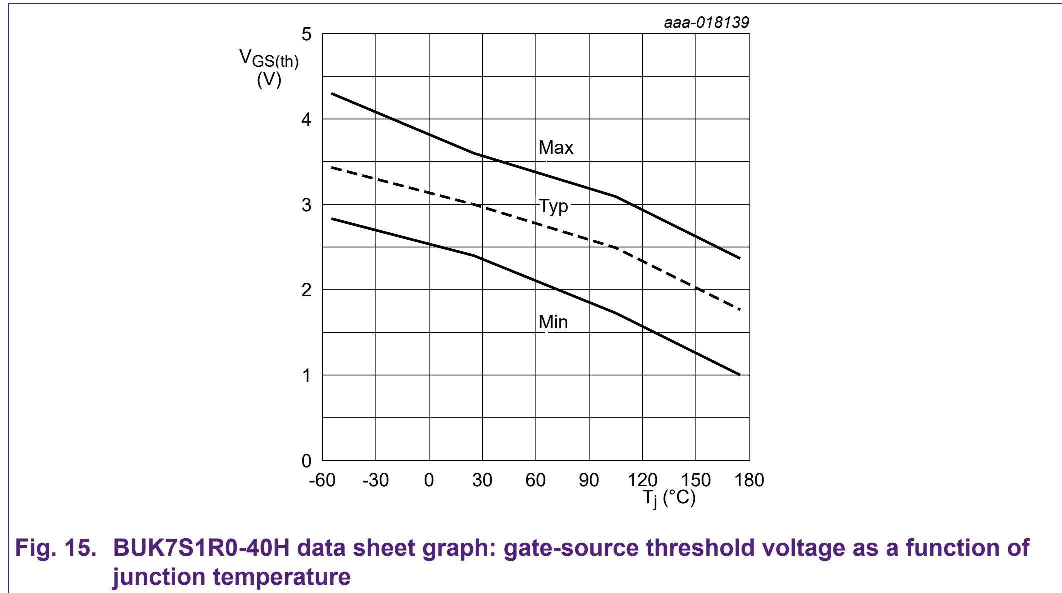

Fig. 15. BUK7S1R0-40H data sheet graph: gate-source threshold voltage as a function of junction temperature

Finally, unlike R_{DSon} and $V_{GS(th)}$, input charge is shown to only slightly vary with temperature.

5.4. Data sheet and batch spreads

If considering multiple MOSFETs in parallel, data sheet spreads may be too conservative. The design would certainly be reliable but the improved robustness to a wider worst case scenario could end up being more expensive. In this case then, the designer would prefer to evaluate a less stringent worst case scenario that, even if not guaranteed like the data sheet, can still be considered realistic. This is done by looking at batch spreads.

A batch refers to a group of devices that go through the whole manufacturing process at the same time. The number of dies in a batch can vary from a few thousands to over a few millions, depending on the size of the dies themselves. Within a set of paralleled MOSFETs, it is preferable to choose parts coming from the same reel in order to increase the possibility of using devices from the same batch. Furthermore, using MOSFETs with identical batch codes, which can be found on the package under the marking code, could be used to further narrow down the selection during PCB assembly.

Spreads within a batch are observed to be much lower than the corresponding data sheet ones. The same can be said even with those among different batches. Fig. 16 shows the spread of $V_{GS(th)}$ for the BUK7S1R5-40H for 10 different batches. In this case the 6-sigma spread is observed to be 0.42 V, from 2.86 V to 3.28 V. This value is calculated taking into account a small quantity of outliers (not shown in the plot of Fig. 16). Therefore, the observed worst case is given by a $\Delta V_{GS(th)}$ = 0.42 V or $\Delta V_{GS(th),rel}$ = ± 7 %, less than half of the guaranteed (data sheet) one.

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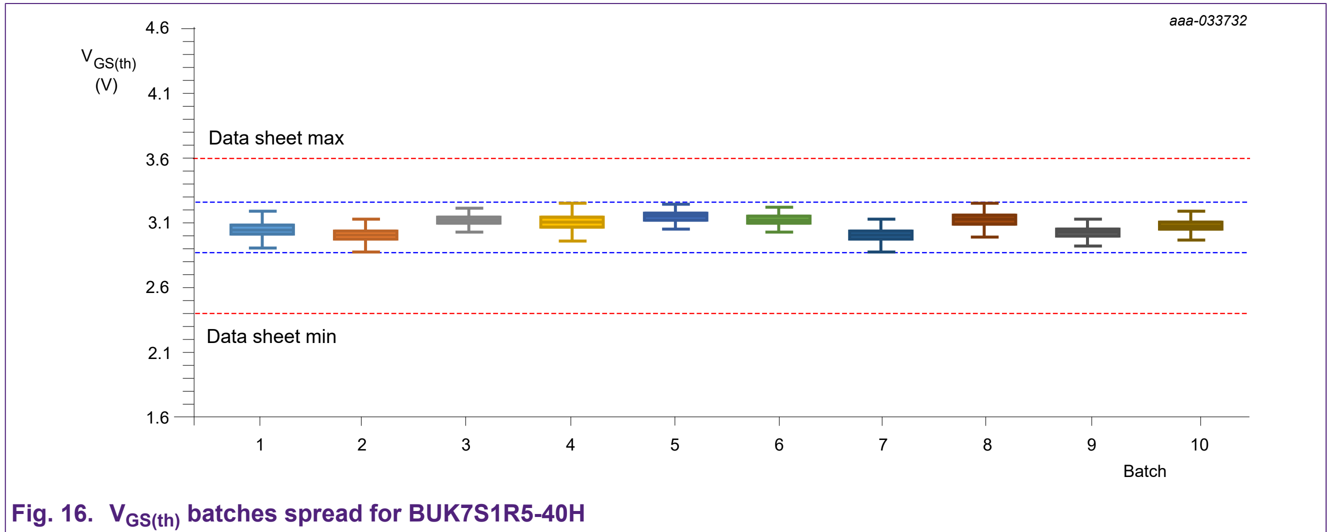

Fig. 16. $V_{GS(th)}$ batches spread for BUK7S1R5-40H

Fig. 17 shows the absolute value of the difference in $V_{GS(th)}$ ($|\Delta V_{GS(th)}|$) between two consecutive devices, within two different batches. In this case the 6-sigma spread is observed to be 0.25 V, or $\Delta V_{GS(th),rel}$ = ±4 %. Therefore, in case two consecutive MOSFETs coming from the same reel are used in parallel, the difference between their $V_{GS(th)}$ is observed to be even smaller than that between multiple batches.

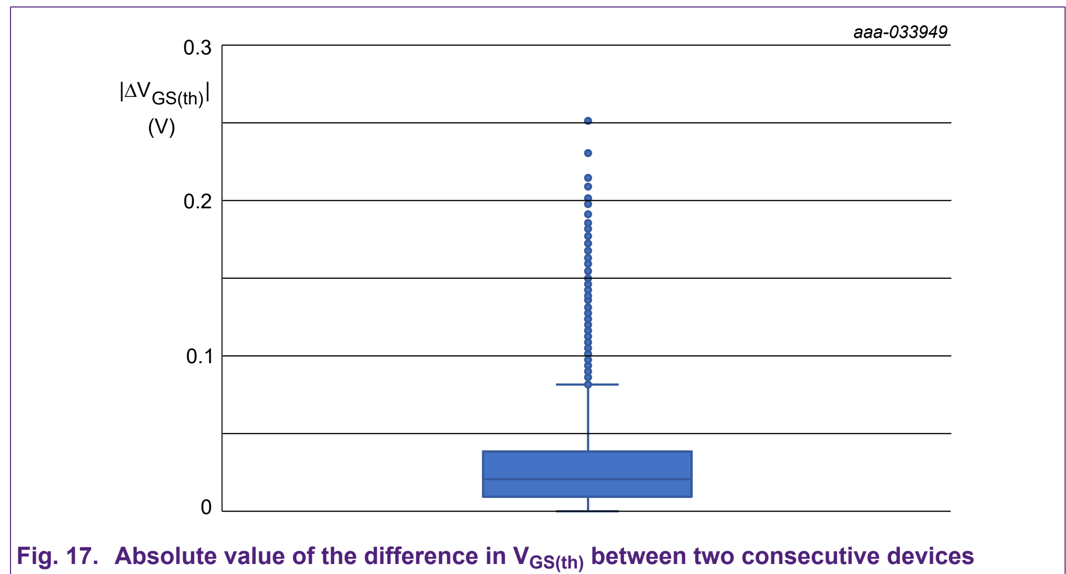

Fig. 17. Absolute value of the difference in $V_{GS(th)}$ between two consecutive devices

Fig. 18 compares the MOSFETs drain current in case of data sheet and batch spread, Table 11 quotes the energy shared by each MOSFET. M1 is now dissipating a total of 2.8 W and M3 1.5 W. Therefore, a difference of ±7 % in $V_{GS(th)}$ leads to a reduction of 1.9 W over a cycle of M1, reducing the ratio between these two MOSFETs dissipation from almost 5:1 down to 2.5:1.

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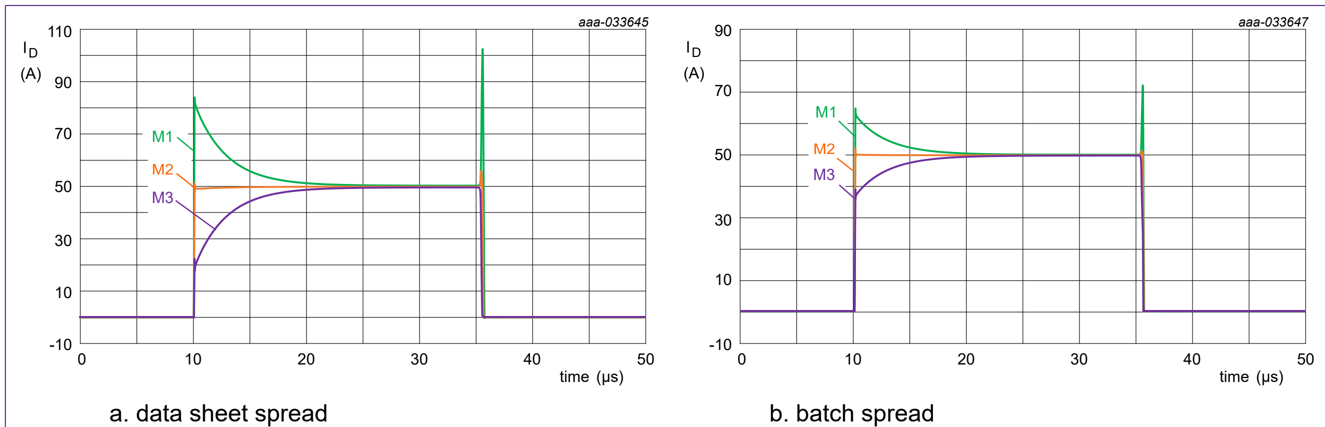

a. data sheet spread

b. batch spread

Fig. 18. MOSFETs drain current (I_D) – data sheet and batch $V_{GS(th)}$ spread comparison

Table 11. Summary - Effects of $V_{GS(th)}$ batch spread

Device	$V_{GS(th)}$ [V]	E_{SW} [µJ]	Energy Sharing Switching	E_{COND} [µJ]	Energy Sharing Conduction
M1	2.79	97.0	51.3 %	48.7	35.6 %
M2	3	59.4	31.4 %	45.4	33.2 %
M3	3.21	32.6	17.2 %	42.7	31.2 %

6. Circuit optimisation

There are two main types of circuit modifications, each has a different impact on the current sharing. These are: localized gate resistor and components in the MOSFETs source paths.

6.1. Localized gate resistor

The first type of circuit modification is also the most advantageous, it has no major drawbacks and it is the simplest to implement. The modification involves splitting the gate resistor between a localized one close to the gate of each MOSFET and a common resistor at the driver side, as shown in Fig. 18 b. Doing so will counteract the spreads and improve the sharing, mainly during switching with little impact during conduction.

It is important to keep the localized resistance as low as possible to give maximum coupling between the MOSFET gates, effectively allowing the input capacitances to be considered in parallel. A simple simulation can display this effect: two circuits modelling the driver and input impedance of each MOSFET are used as comparison. Fig. 19 a. shows the control voltage at each MOSFET gate, the voltage is slowed down in case of the MOSFET with higher C_{iss}, vice versa it is less filtered in case of lower capacitance.

By splitting the gate resistor the difference between the control voltages at each gate becomes negligible (Fig. 19 b). With reference to the naming adopted in the SPICE circuits of Fig. 19, the gate resistor at the driver can be calculated as:

$$R_{G,drv} = \frac{R_G}{nFET} - \frac{R_{G,split}}{nFET} \quad (5)$$

The value of $R_{G,drv}$ has been rounded to 12 Ω. A smaller $R_{G,drv}$ can be beneficial by reducing the switching time where the unequal sharing occurs. In a similar manner, the smaller $R_{G,split}$ the better coupled the MOSFETs gate, but it is recommended not to go below 2-3 Ω. In general, a gate resistor helps in dampening any oscillation in the gate-source loop that might compromise the EMC performance of the system. Therefore, given a lower resistance of the gate resistor, it is important to reduce as much as possible the loop inductance of the driver loop, for further information see section: PCB layout influence.

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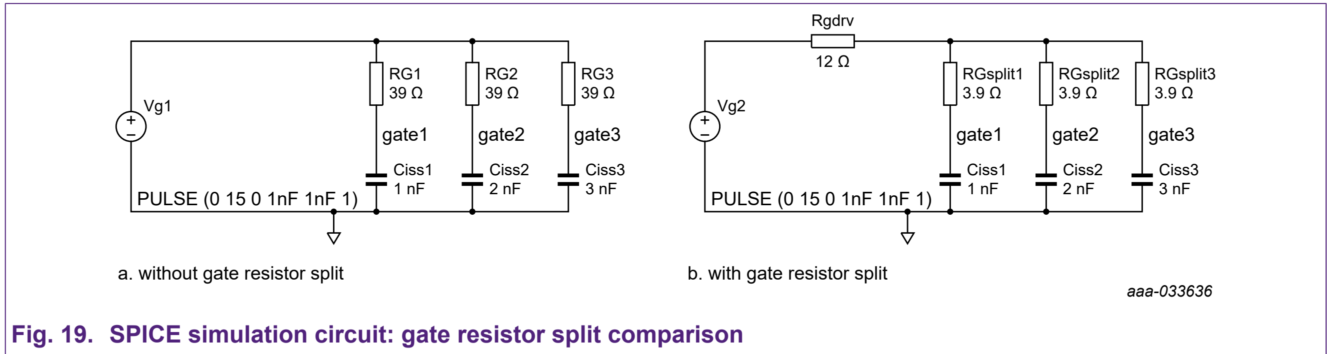

Fig. 19. SPICE simulation circuit: gate resistor split comparison

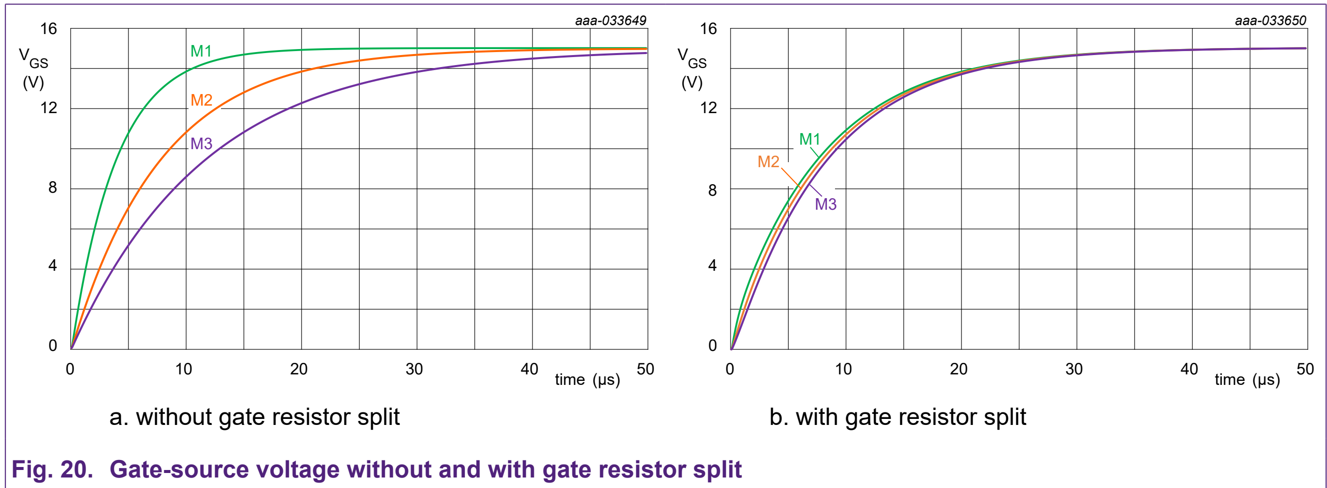

Fig. 20. Gate-source voltage without and with gate resistor split

The great improvement of the resistor split can be easily appreciated by simulating the same half-bridge circuit using two different gate resistors setups and introducing some spread. This time an arbitrary combination of all the spreads has been used. Fig. 21 shows the MOSFETs drain current without gate resistor split, while Fig. 22 shows the MOSFETs drain current with gate resistor split.

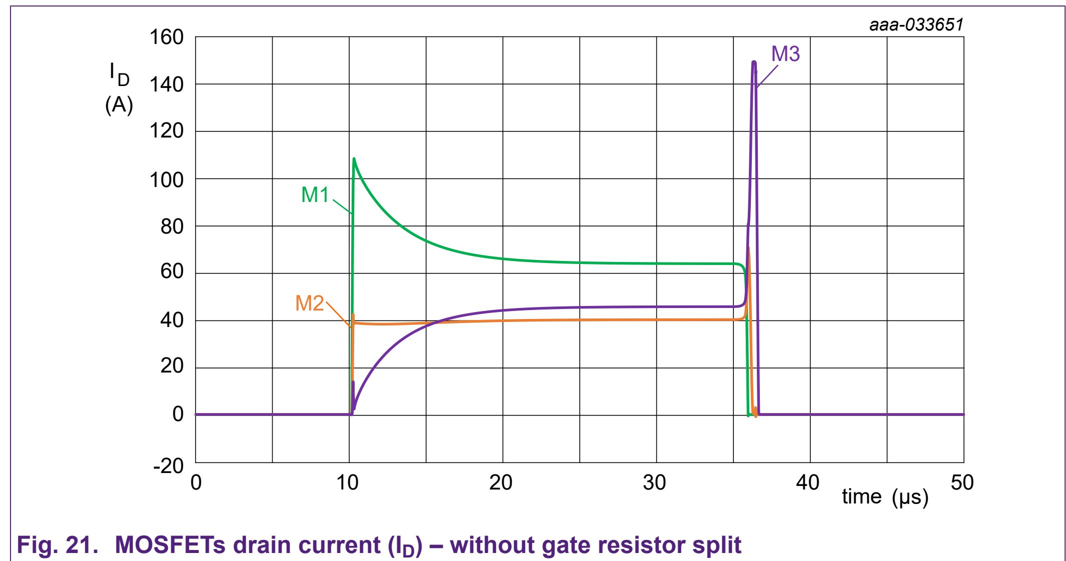

Fig. 21. MOSFETs drain current (I_D) – without gate resistor split

The simulations setup and results are summarized in Table 12 and Table 13, while a final comparison is given in Table 14. M3 is dissipating 8.2 W, M2 1.3 W and M1 2.0 W. At turn-ON M1 is switching first, due to having both lower $Q_{G(tot)}$ and $V_{GS(th)}$, thus handling the majority of the current. On the other hand, at turn-OFF the MOSFET with higher input charge (M3) will switch last and carry most of the current.

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Table 12. Summary - sharing without gate resistor split: R_G = 39 Ω

Device	R_{DSon} [mΩ]	$V_{GS(th)}$ [V]	$Q_{G(tot)}$ [nC]	E_{SW} [μJ]	Energy Sharing Switching	E_{COND} [μJ]	Energy Sharing Conduction
M1	0.62	3.21	94.4	42.7	9.6 %	62.2	47.0 %
M2	1	3	125.7	29.0	6.5 %	35.2	26.6 %
M3	0.88	2.79	158.0	373.0	83.9 %	34.9	26.4 %

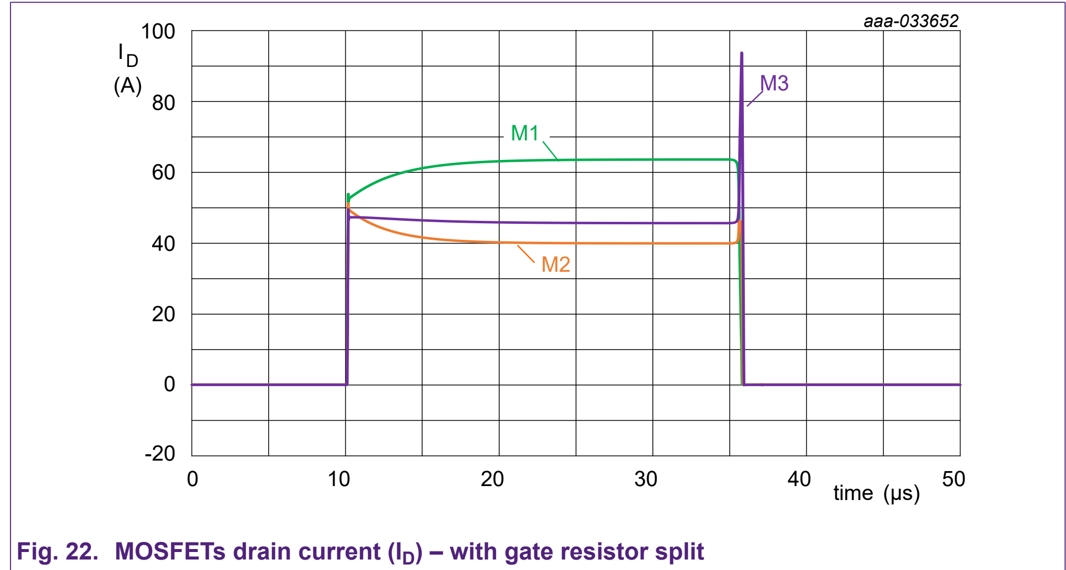

Fig. 22. MOSFETs drain current (I_D) – with gate resistor split

With the gate resistor split M3 is now dissipating 3.8 W, M2 2.0 W and M1 1.6 W. The improvements are noticeable both at turn-ON, where the peaks are now almost identical, and turn-OFF. During the latter the peak current through M3 has reduced from around 150 A down to almost 90 A. Sharing during conduction has improved as well, this is due to time it takes for the current to reach its conduction value following the turn-ON event. Overall, M3 is now dissipating 50 % less power.

Table 13. Summary - sharing with gate resistor split: $R_{G,drv}$ = 12 Ω and $R_{G,split}$ = 3.9 Ω

Device	R_{DSon} [mΩ]	$V_{GS(th)}$ [V]	$Q_{G(tot)}$ [nC]	E_{SW} [μJ]	Energy Sharing Switching	E_{COND} [μJ]	Energy Sharing Conduction
M1	0.62	3.21	94.4	30.0	12.4 %	52.3	39.6 %
M2	1	3	125.7	60.6	25.1 %	38.2	28.9 %
M3	0.88	2.79	158.0	150.5	62.4 %	41.4	31.5 %

Table 14. Summary – comparison of sharing with and without gate resistor split

Device	Total Energy Sharing	
	without gate resistor split	with gate resistor split
M1	18.1 %	22.1 %
M2	11.12 %	26.5 %
M3	70.7 %	51.4 %

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6.2. Components in the source path

Employing a resistor in series with each of the MOSFETs source path can lead to better sharing during conduction. The main disadvantage is that of an additional source of power dissipation which lowers the overall efficiency of the system and increases the burden on the cooling system. Given the relatively high value of resistance needed to be effective, this solution will not be ideal in all scenarios.

Certain designs might already include series resistors to monitor the current flowing through a half bridge. However, the only way for them to be effective in case of paralleled MOSFETs is if they are placed within the gate-source loop, as shown in Fig. 23. In case of current sensing, an additional small resistor may be added to decouple each loop in order to reduce potential crosstalk between each branch.

The resistor helps to counteract the spread of the R_{DSon}, thus leading to better sharing during conduction. Inductance located in the same place has a similar effect of slightly improving the sharing, this time during switching, by opposing quick changes in current (dI/dt) and thus lowering the current peaks. On the other hand, conduction losses would increase slightly due to the larger time constant of the current converging towards its conduction value (I_{tot} / $nFET$).

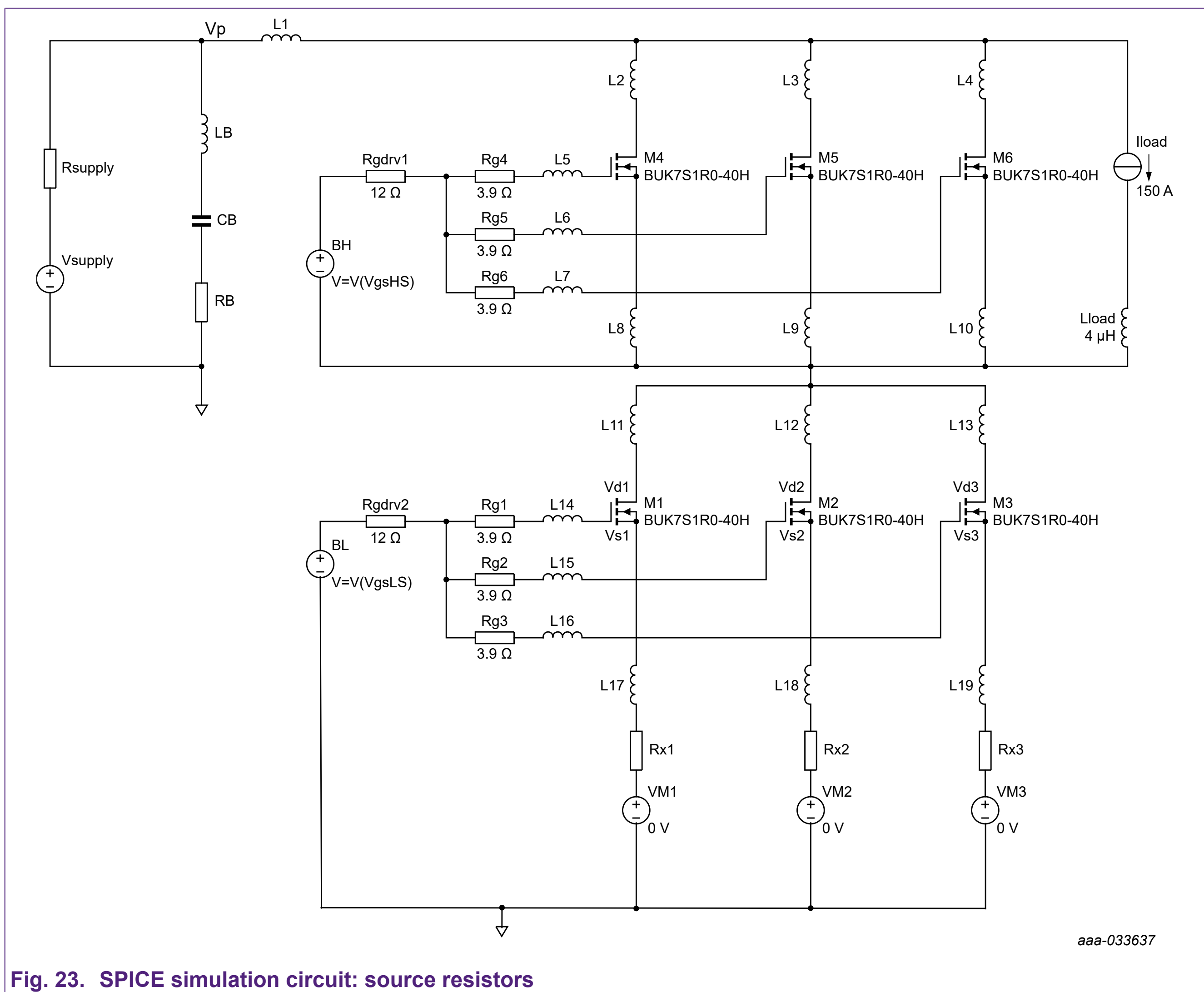

Fig. 23. SPICE simulation circuit: source resistors

The simulation setups and results are summarized in Table 15.

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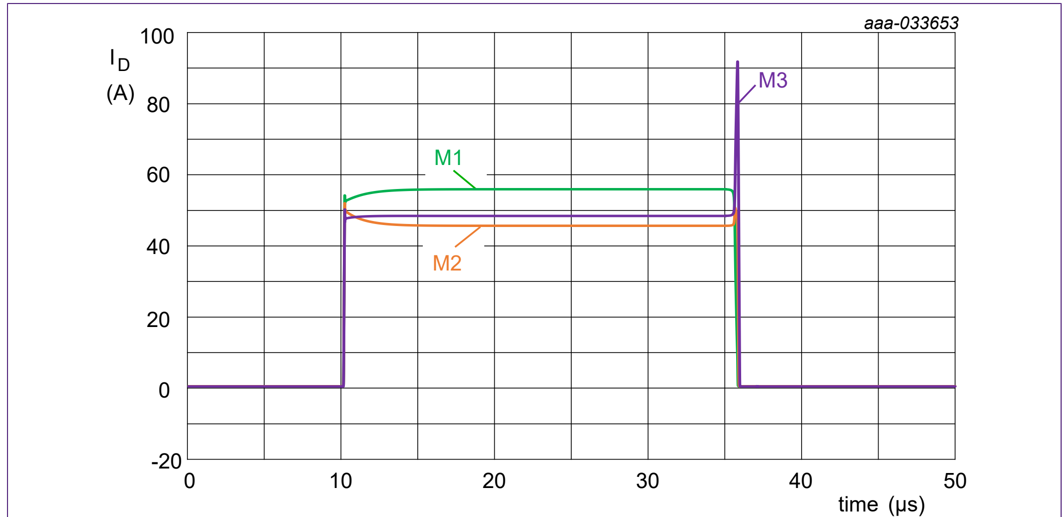

Fig. 24. MOSFETs drain current (I_D) – with a source resistor of 1 mΩ

Table 15. Summary – sharing with a source resistor of 1 mΩ

Device	R_{DSon} [mΩ]	$V_{GS(th)}$ [V]	$Q_{G(tot)}$ [nC]	E_{SW} [μJ]	Energy Sharing Switching	E_{COND} [μJ	Energy Sharing Conduction
M1	0.62	3.21	94.4	27.9	11.5 %	41.6	30.8 %
M2	1	3	125.7	66.5	27.4 %	47.3	35.1 %
M3	0.88	2.79	158.0	148.4	61.1 %	46.1	34.1 %

The efficacy of the resistor on the current sharing depends on its value. If the aim is to balance the current sharing, then the higher the resistance the better, as shown in Fig. 25. Naturally the dissipation will increase considerably with it. In order for it to be effective in counteracting the R_{DSon} spread it needs to be comparable with the actual R_{DSon} of the MOSFET.

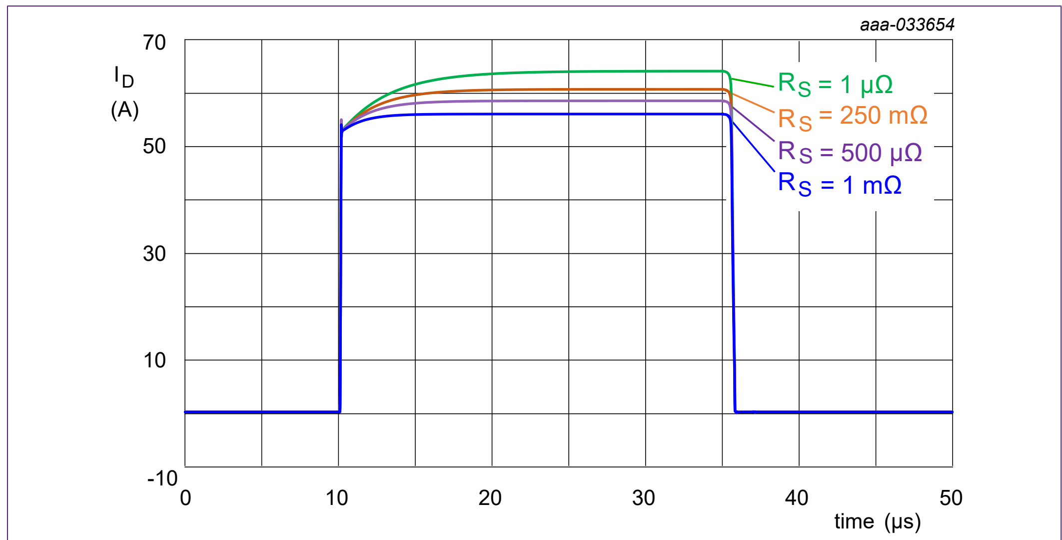

Fig. 25. MOSFETs drain current (I_D) – effects of source resistor value

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7. PCB layout influence

Tight spreads and a good layout are two important factors when designing an application with paralleled MOSFETs. This chapter describes guidelines to achieve a good layout and how parasitics influence the current sharing.

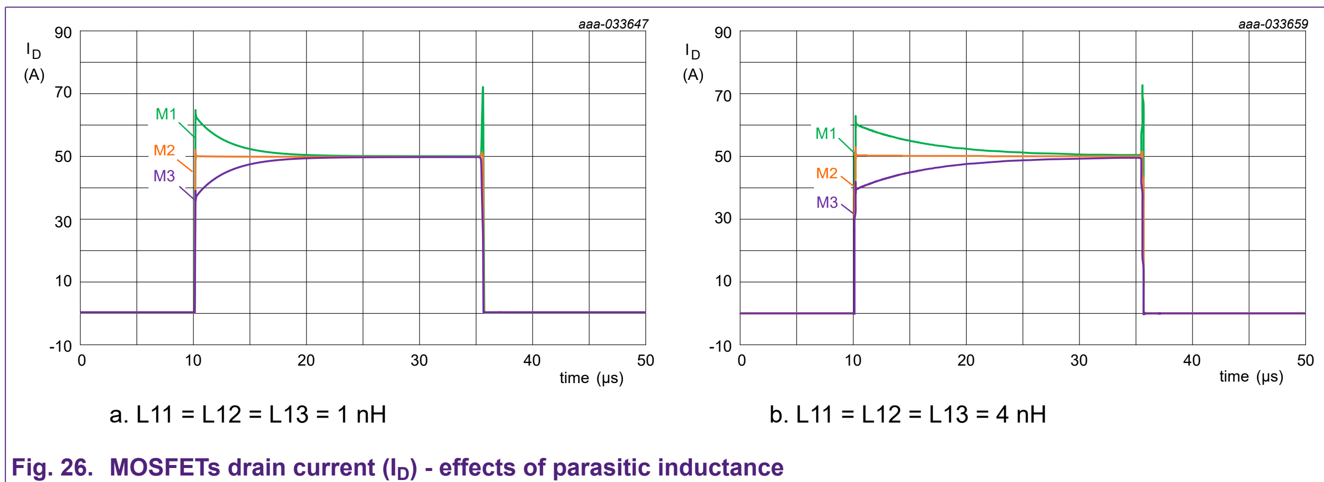
In a paralleled set of MOSFETs it is impossible to say beforehand where the device with lowest or highest spreads will be placed. Therefore, it is important to lay out each branch in the same way, failing to do so will result in the worsening of the worst case scenario.

7.1. Layout-dependent parasitics

In case of paralleled devices loop inductance and resistance in the path should be not only minimised but also equalised for each branch.

Higher inductance slows down the current reaching its steady state value due to the higher time constant of the circuit (τ = L/R), as shown in Fig. 26. The inductance decreases the peak current slightly but increases the overall sharing unbalance. Moreover, both high and low sides will experience larger voltage overshoots and oscillations in V_{DS} (and V_{GS}) due to resonance with the capacitances in the circuit (Fig. 27), often exceeding the supply voltage. This also leads to higher interference with nearby circuits and wiring.

In general, any rule that would be recommended for a single MOSFET can be applied here. For a more in depth explanation of the switching behaviour of a half-bridge and EMC consideration refer to "*AN90011: Half-bridge MOSFET switching and its impact on EMC*"[2]



a. L11 = L12 = L13 = 1 nH

b. L11 = L12 = L13 = 4 nH

Fig. 26. MOSFETs drain current (I_D) - effects of parasitic inductance

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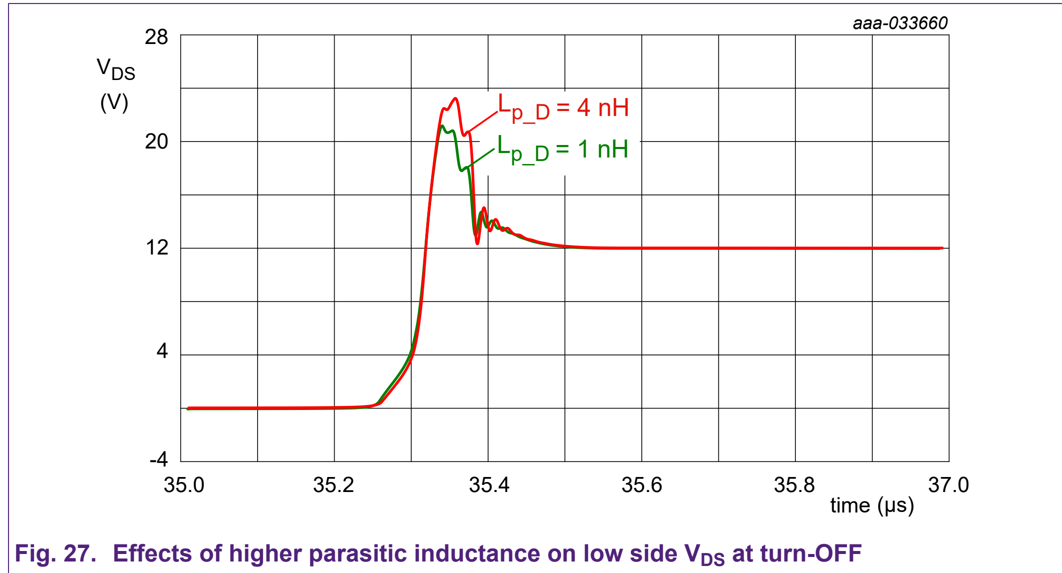
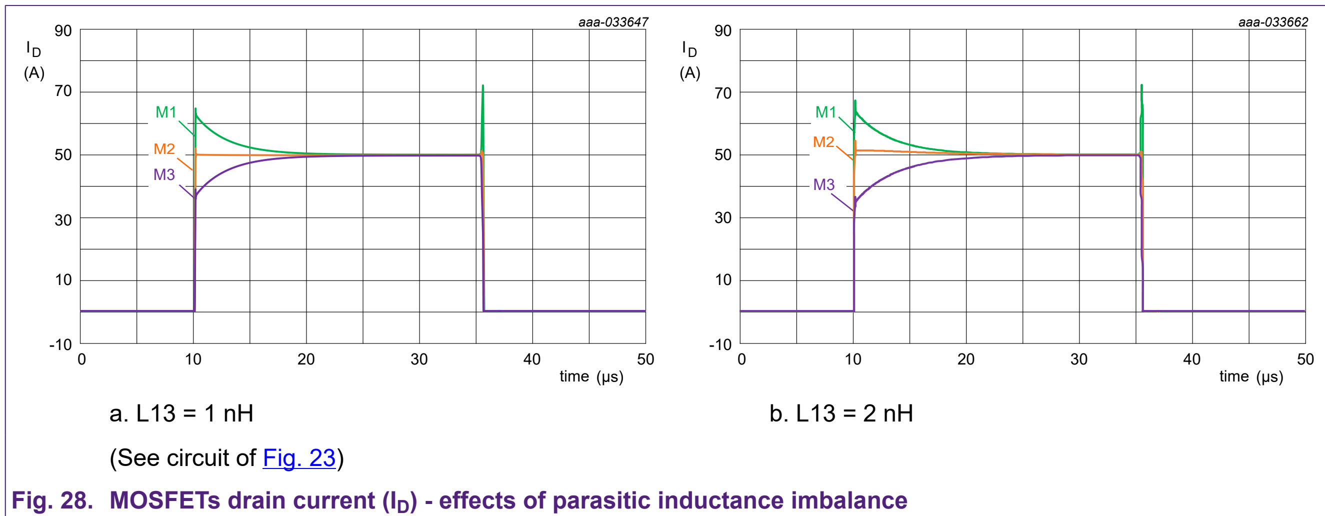


Fig. 27. Effects of higher parasitic inductance on low side V_{DS} at turn-OFF

Differences between loop inductances lead to worse current sharing, as shown in Fig. 28.



a. L13 = 1 nH

b. L13 = 2 nH

(See circuit of Fig. 23)

Fig. 28. MOSFETs drain current (I_D) - effects of parasitic inductance imbalance

7.2. Circuit layout

As in many other circumstances, the layout plays an important role in the final performance of an electronic system, almost as much as the quality of the parts. In case of paralleled MOSFETs the layout should be designed to provide: good thermal link between the devices, low and equal loop inductance in the gate-source and source-drain loops and low and equal resistance between the branches.

Good thermal coupling allows the devices to operate at similar lower temperatures. Furthermore, the designer should aim at obtaining similar $R_{th(mb-amb)}$ for each MOSFET. Multiple planes and thermal vias help in improving the heat exchange between devices and environment. Care should be taken in the placement of the MOSFETs: for instance by avoiding placing a subset of the MOSFETs near heat sinks, connectors or other components that may be keep them cooler than the other paralleled MOSFETs. For more information about this topic refer to "*AN90003: LFPAK MOSFET thermal design guide*" [3].

Low inductance in a loop can be achieved by reducing the area of the loop (thereby reducing the self-inductance) or by keeping the trace and its return path as close as possible to each other (thereby increasing the mutual inductance). Loop inductance in the gate-source loop can be reduced by keeping the driver as close as possible to the MOSFETs and by running gate and source traces parallel to each other, as shown in Fig. 29.

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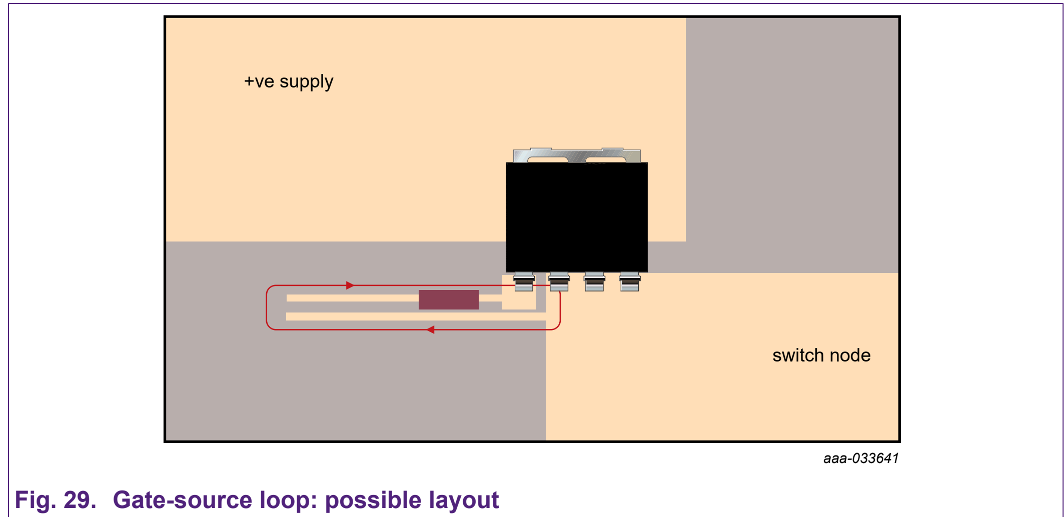

Fig. 29. Gate-source loop: possible layout

Inductance in the loop carrying the load current could be minimised, for instance, by employing the design in Fig. 30. For further details refer to “*AN90011: Half-bridge MOSFET switching and its impact on EMC*” [2].

Fig. 30. Half-bridge layout possibilities showing inductances

The placement of inlets and outlets plays another important role because it determines each branch parasitics. When using multiple devices in parallel, it could be helpful to use more than one inlet and outlet. Using multiple smaller cables can be actually beneficial for other reasons too. The positioning of these insertion points needs to be carefully planned. One possible way to facilitate

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this decision might be to use a CFD software and run a current density simulation. This type of simulation highlights the preferred path the current takes in a steady state condition (DC).

Fig. 31 shows the setup used for the simulations: 3 MOSFETs are placed in parallel both at high and low side. Each low side MOSFET is connected between phase (inlet), on the top layer, and ground (outlet) on the bottom one (not shown in the picture), through a number of filled vias. Each high side is instead connected between phase (outlet) and the positive supply (inlet) on the top layer. A total current of 150 A is set to flow through the paralleled devices. Two simulations are required, each with a single side active at a time.

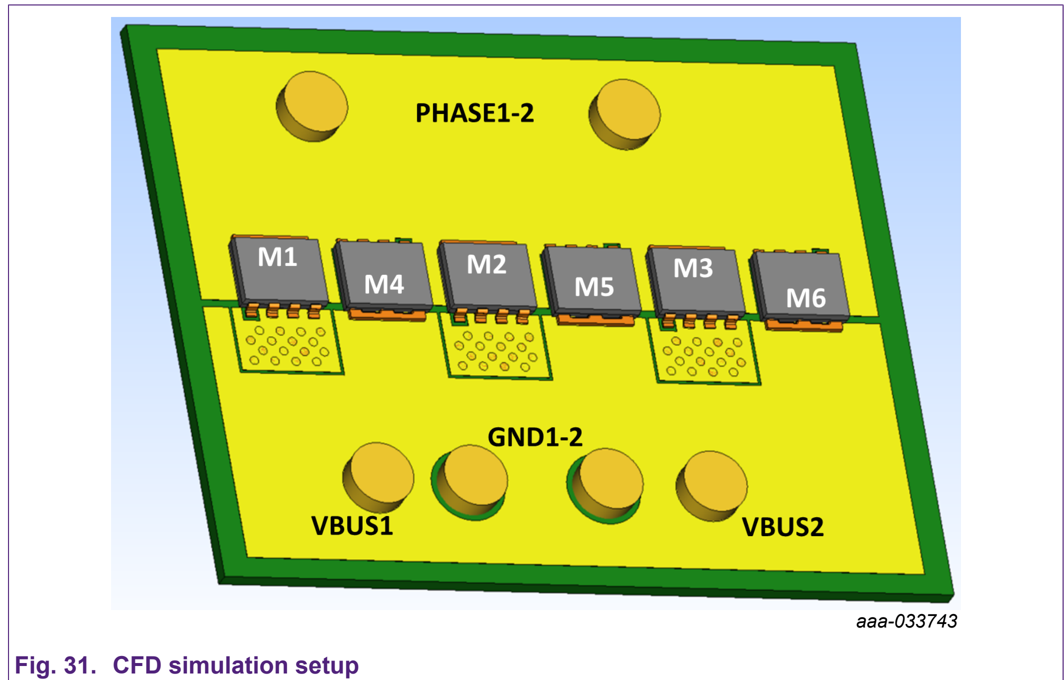

Fig. 31. CFD simulation setup

The results of the current density simulation for the low side and high side are shown in Fig. 32, Fig. 33 and Fig. 34. Higher current density is shown in red, while low or null in blue. For instance the high side simulation (Fig. 34) highlights a spot around M4 and inlet VBUS1 where current density is higher, due to the position of the latter. By integrating the current density over the entire surface of the die it is possible to calculate the sharing in steady state of the layout (between 30-40% in this particular case). These simulations have been obtained using scSTREAM.

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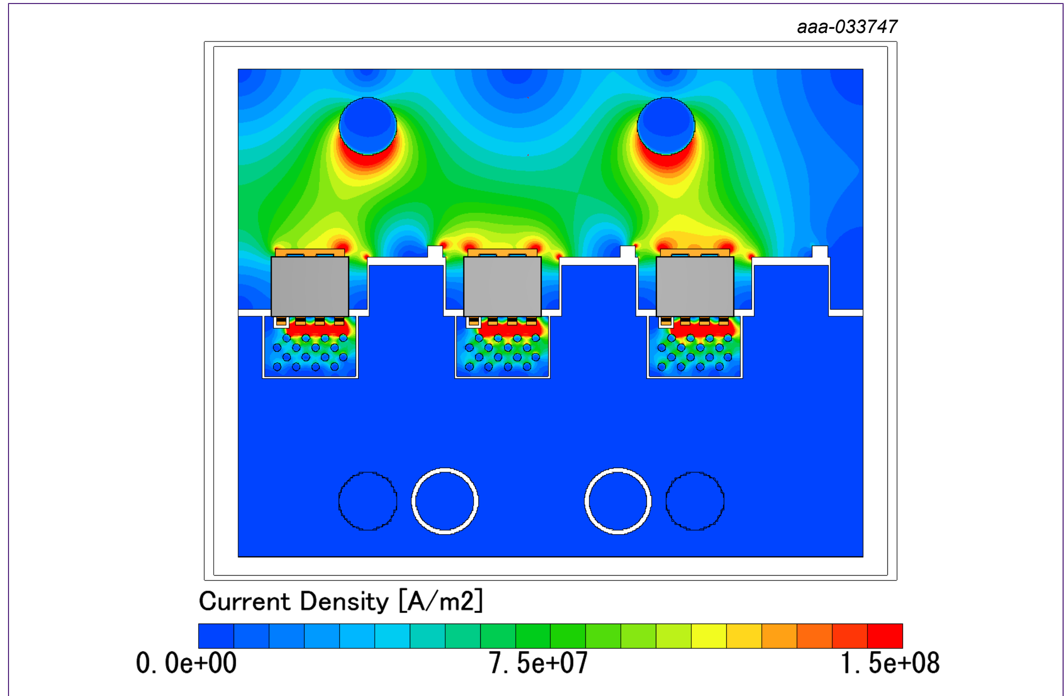

Fig. 32. CFD current density simulation: Low side MOSFETs ON – Top side

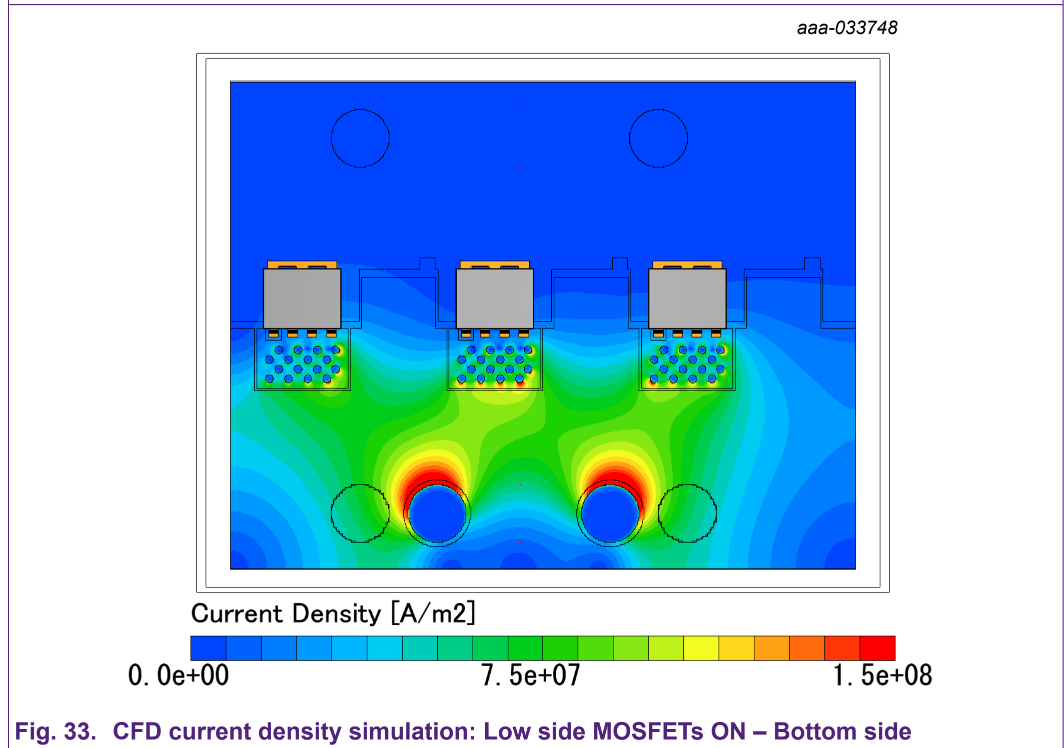

Fig. 33. CFD current density simulation: Low side MOSFETs ON – Bottom side

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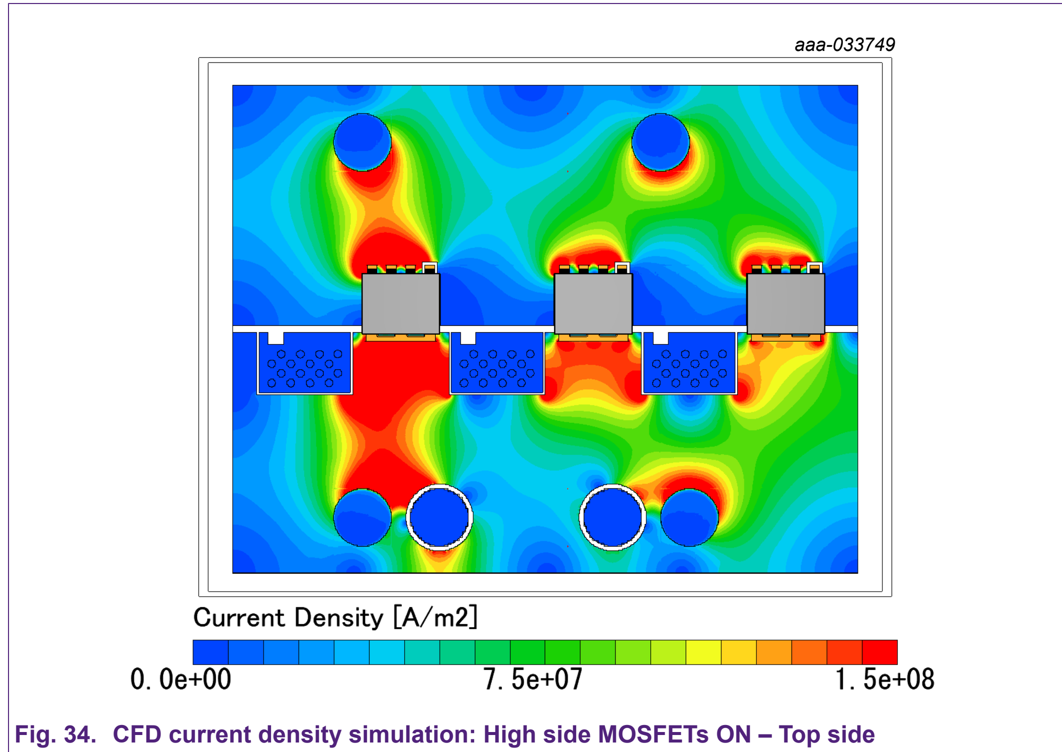

Fig. 34. CFD current density simulation: High side MOSFETs ON – Top side

8. Driving paralleled MOSFETs

When driving paralleled MOSFETs it is recommended to use one single gate driver. This is mainly done to synchronize the devices operation as much as possible.

The gate driver should have enough peak current capability to fully charge and discharge the total input capacitance of the paralleled MOSFETs. This requirement becomes more and more stringent as the number of MOSFETs increases, especially if the switching time is required to be low, as the total input capacitance is now $C_{iss,tot}$ = n.FETs × $C_{iss,max}$. Failing to do so means that the switching speed will be set by the gate driver itself and not by the gate resistor.

As shown by the previous simulations turn-OFF dissipates more energy than turn-ON. One simple way to reduce the switching losses is by decreasing the resistance of RG,drv only during the turn-OFF. This can be done by using a combination of a smaller resistor in series with a diode, placed in parallel with RG,drv, as shown in Fig. 35. However, before choosing the right value of RG,OFF it is recommended to take into account any parasitic inductance that may be present in the circuit: a combination of fast turn-OFF and high inductance could potentially induce avalanche, which, in a parallel configuration, could greatly stress the device with lower breakdown voltage.

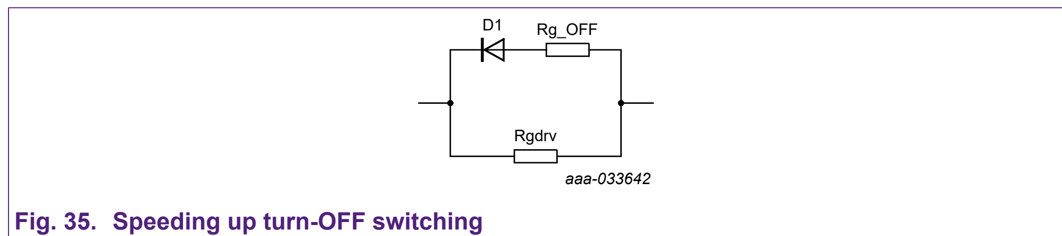

Fig. 35. Speeding up turn-OFF switching

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9. Simulation tools

This chapter describes how to set up a simulation aimed at finding the worst case scenario in a set of paralleled MOSFETs. In this case SPICE has been used, however, the same ideas can be applied to any other simulation tool that offers the same functionality.

The idea is to take into account MOSFET spreads in a simulation, in the same way of usual components tolerances. Two types of simulations are discussed: probability distribution and worst case scenario simulations.

Probability distribution simulation refers to a simulation where one or more parameters are defined by their probability distribution, generally shown to be approximately Gaussian (or Normal). This type of simulation would have the advantage of weighting each possible combination by the likelihood of it happening. In theory, this would yield a more realistic evaluation and the designer could run the simulation for a number of iterations corresponding to the design BOM (bill of materials). In practice this type of evaluation is impractical since the data corresponding to parameters distribution (mainly sigma value) would need to be measured for each specific part name, it would not be guaranteed and it would require additional expensive steps in the manufacturing process.

With respect to a distribution based simulation, the worst case scenario reduces the number of iterations by taking into account only the maximum distribution of a parameter around its typical value. The amount of runs is reduced to $2^N + 1$, where N is the number of indexed parameters and 1 is the nominal case, which is computed at the end. This type of evaluation is based on data sheet spreads, which are guaranteed. On the other hand, it might miss “local extrema”, i.e. points inside the spread at which the outcome is worse than the one resulting from considering only maximum, minimum and nominal.

The analysis requires four main figures:

- Spreads, namely typical value and Δ (tolerance)
- A function *binary(run, index)* that creates a set of indexes for the various combinations
- A function *wc(nominal, tol, index)* that reads these indexes and outputs the correct value for the parameter
- A function that automatically measures the average dissipated power over a cycle

Besides, the spreads need to be symmetrical so, in case of R_{DSon}, the evaluation will either use a higher minimum or maximum resistance than the data sheet one. Instead, in case the data sheet does not provide a minimum value, as for $Q_{G(tot)}$, then the middle point can be considered as nominal.

Prior to running the simulation the spice model of each MOSFET needs to be modified to replace the value of each parameter considered in the evaluation, with the output of the *wc(nom, tol, index)* function, as shown below:

- **R_{DSon} typical value 0.88 mΩ, tolerance ±0.12 mΩ**
  RD 3 4 {wc(576.2603u,tol_RD,3)} TC= 9.735m, 2.369u
- **Q_{GS} typical value 33.5 nC, tolerance ± 13 nC**
  CGS 2 6 {wc(7.67n,tol_CGS,6)}
- **Q_{GD} typical value 25.5 nC, tolerance ± 17 nC**
  .params CGD_scale = {wc(1.245,tol_CGD,9)}
  *…G11 3 2 VALUE {CGD_scale*V(13,0)*I(V11)}*
- **$V_{GS(th)}$ typical value 3 V, tolerance ±0.21 V**
  Vto= {wc(3.843,tol_VGSth,0)}

where: tol_RD = 119.68u, tolCGS = 1.57n, tol_CGD = 0.405 and tol_VGSth = 0.21.

In this particular case the number of parameters are 4, these change between the 3 paralleled MOSFETs so the total number of indexed parameters is 12. Consequently the amount of combinations will be $2^{12} + 1 = 4097$. Only one MOSFET can be considered for this evaluation. A slightly modified version of the circuit seen in Fig. 1 is used for this simulation. Furthermore, the small circuit of Fig. 36 is required in order to automatically compute the power dissipated by the MOSFET under investigation (the corresponding 0 V monitor generator is required too).

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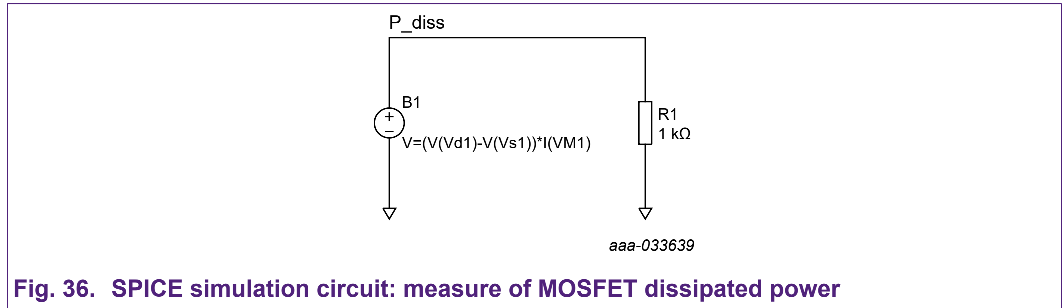

Fig. 36. SPICE simulation circuit: measure of MOSFET dissipated power

After the simulation is complete, the current through M1 can be displayed. The final result can be seen in Fig. 37, Fig. 38 and Fig. 39, which shows the first 20 iterations.

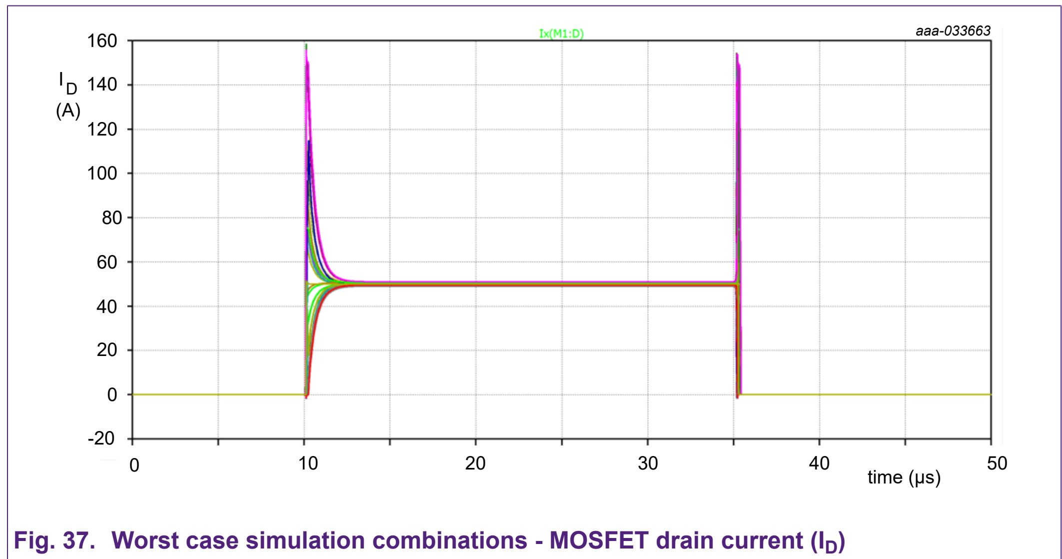

Fig. 37. Worst case simulation combinations - MOSFET drain current (I_D)

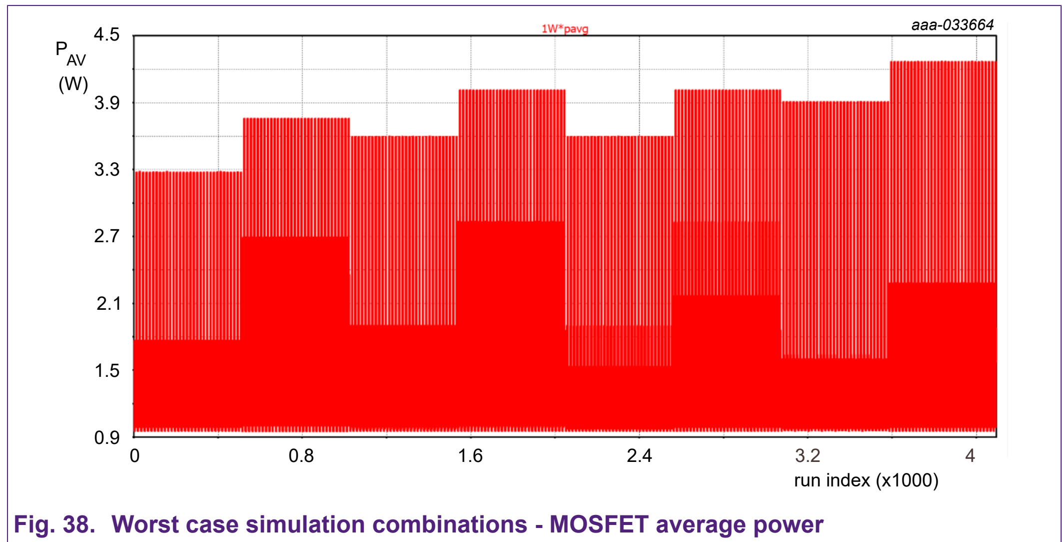

Fig. 38. Worst case simulation combinations - MOSFET average power

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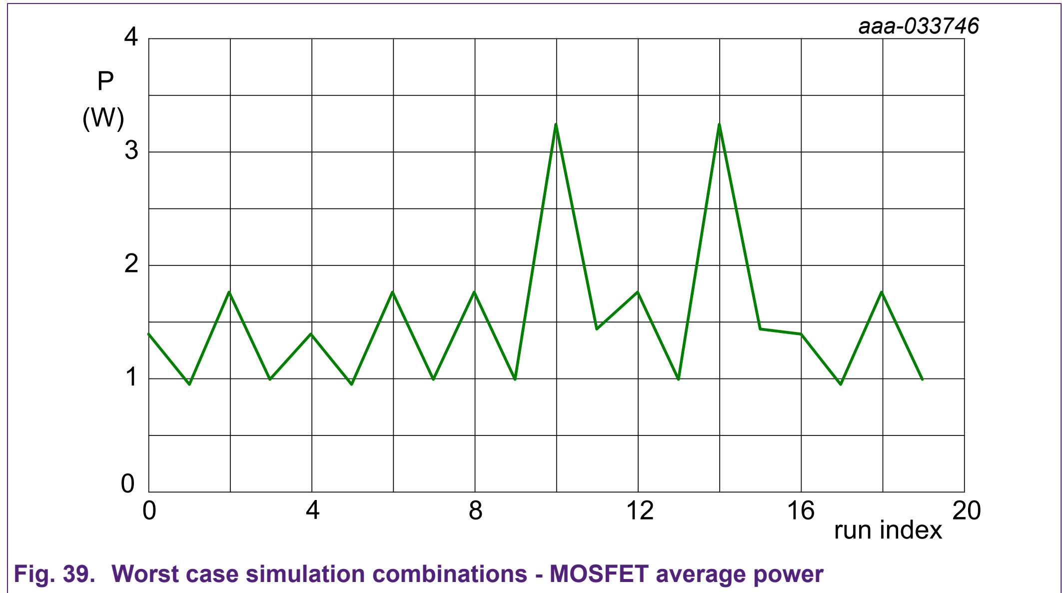

Fig. 39. Worst case simulation combinations - MOSFET average power

The worst case scenario is when a single MOSFET is dissipating around 4.2 W of power. In case only the $V_{GS(th)}$ spread is taken into account then the worst case scenario is when a single MOSFET is dissipating around 1.7 W of power. This result can be used in a simple network modelling the steady state temperature behaviour of the junction, as shown in Fig. 40. In this case a PCB thermal resistance of around 15 K/W is needed to guarantee the junction temperature to be lower than the maximum 175 °C. This would mean that an IMS or DBC board might be needed, as the temperature at the interface between MOSFET and PCB is higher than the rating of FR4. Alternatively, one might consider adding an additional MOSFET or selecting a lower R_{DSon} part.

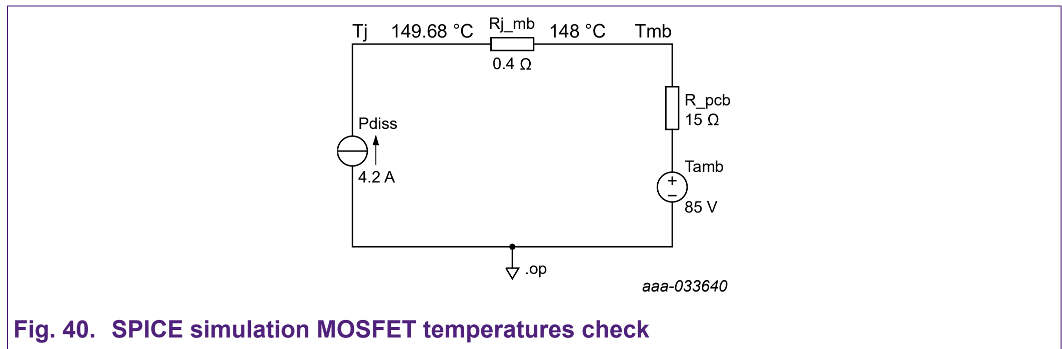

Fig. 40. SPICE simulation MOSFET temperatures check

This concept can be applied to a wide range of scenarios: for instance one could consider various duty cycles, evaluating each worst case scenario and then plugging these values into the current source of the circuit shown in Fig. 40. Furthermore the instantaneous power waveform of the worst case could be exported and used within an RC thermal network to verify that the instantaneous junction temperature is below 175 °C.

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10. Conclusion

This application note aims at giving the reader a description of how the sharing among paralleled MOSFETs is influenced by parameters spreads (e.g. R_{DSon}, $V_{GS(th)}$ and $Q_{G(tot)}$) and PCB layout. The analysis is conducted considering switch-mode (PWM) applications and thus the half-bridge topology.

During switching, $V_{GS(th)}$ spread contributes the most to current unbalances, affecting turn-ON and turn-OFF in the same way: the device with lower $V_{GS(th)}$ will turn-ON first and turn-OFF last, dissipating more power during both events. Additionally, the NTC of $V_{GS(th)}$ leads to increased dissipation as it further lowers the $V_{GS(th)}$ of the MOSFET that handles more power. The spread in $Q_{G(tot)}$ can be effectively counteracted by splitting the gate resistor between one close to the MOSFETs gate and a common one at the driver side. This modification will improve the sharing with huge benefits during switching.

The R_{DSon} is not as significant as $V_{GS(th)}$ when considering MOSFETs in parallel since its PTC improves the sharing during conduction and counteracts the imbalances caused by R_{DSon} spread. Additionally the losses during conduction ($I^2 \times R$) are generally lower than the switching losses therefore the imbalance will weigh less on the overall power sharing.

A worst case scenario simulation can be used to quantify and evaluate the performance of paralleled devices. It can be useful to understand which and how many devices to use in parallel. The worst case depends mainly on the spread of certain parameters. The $V_{GS(th)}$ batch variability is shown to be around half that indicated on the respective data sheet. Albeit not guaranteed, spread between batches is more realistic and leads to a design with improved performance.

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11. Appendix

11.1. Experimental measurements

The following data shows the first two pulses of current flowing through 3 low side MOSFETs used in parallel. The circuit topology employed is the half bridge driving a 4 μH inductive load. Four measurements are shown. M1, M2 and M3 R_{DSon}, $Q_{G(tot)}$ and $V_{GS(th)}$ (measured at both 1 mA and 1 A) are quoted in the tables for each measurement.

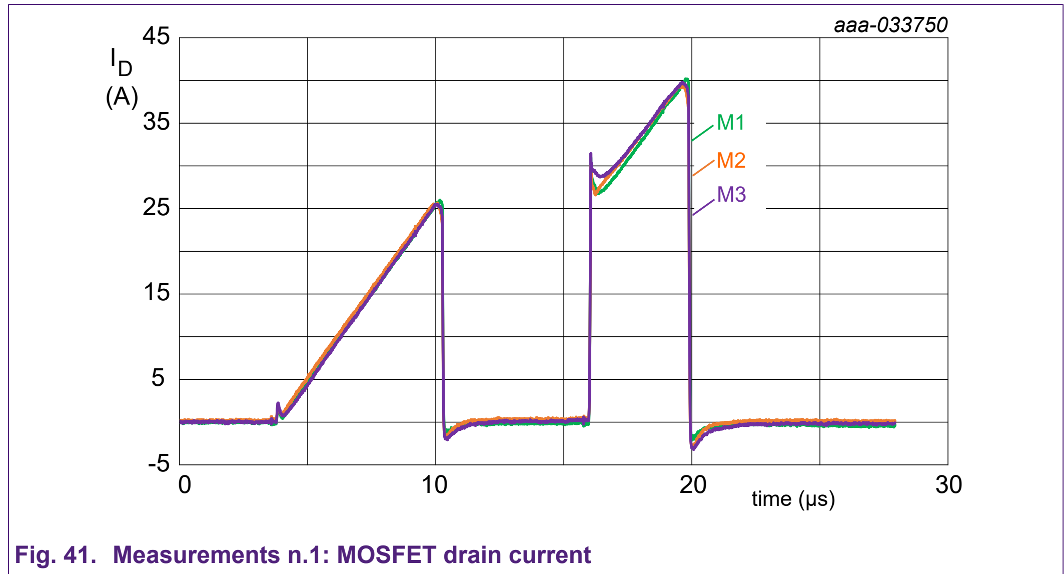

Fig. 41. Measurements n.1: MOSFET drain current

Table 16. Summary measurements n.1

Device	R_{DSon} [mΩ]	$Q_{G(tot)}$ [nC]	$V_{GS(th)}$ [V] @1 mA	$V_{GS(th)}$ [V]@ 1 A	Energy Sharing Switching	Energy Sharing Conduction
M1	3.16	35.57	3.02	3.62	33.7 %	33.1 %
M2	3.02	36.45	3.02	3.63	32.5 %	32.9 %
M3	2.94	35.64	3.02	3.62	33.8 %	34.0 %

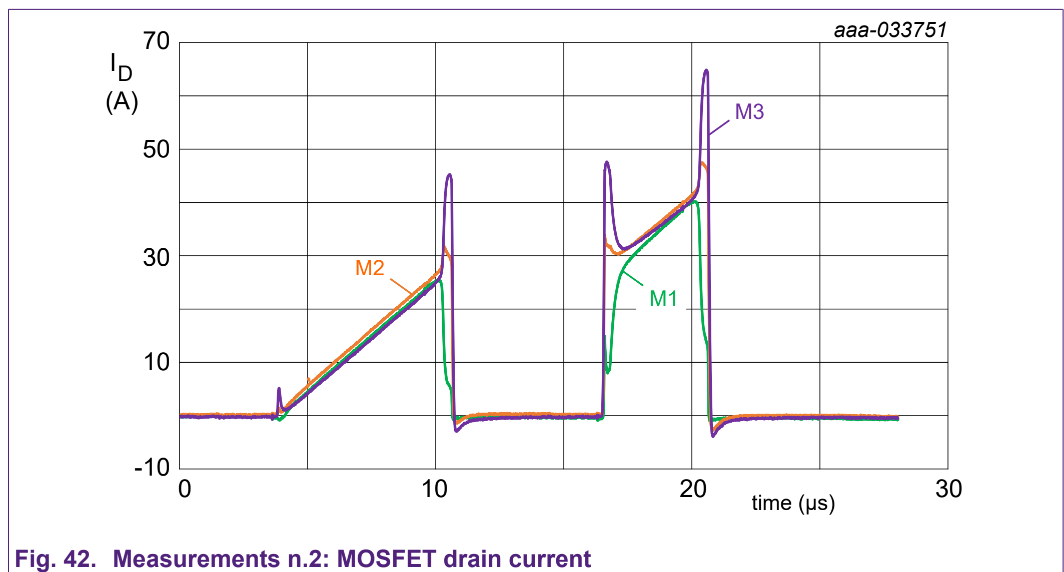

Fig. 42. Measurements n.2: MOSFET drain current

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Table 17. Summary measurements n.2

Device	R_{DSon} [mΩ]	$Q_{G(tot)}$ [nC]	$V_{GS(th)}$ [V] @1 mA	$V_{GS(th)}$ [V]@ 1 A	Energy Sharing Switching	Energy Sharing Conduction
M1	3.07	38.14	3.46	4.10	8.2 %	32.8 %
M2	2.94	35.64	3.02	3.62	36.1 %	33.7 %
M3	3.14	33.74	2.80	3.39	55.7 %	33.5 %

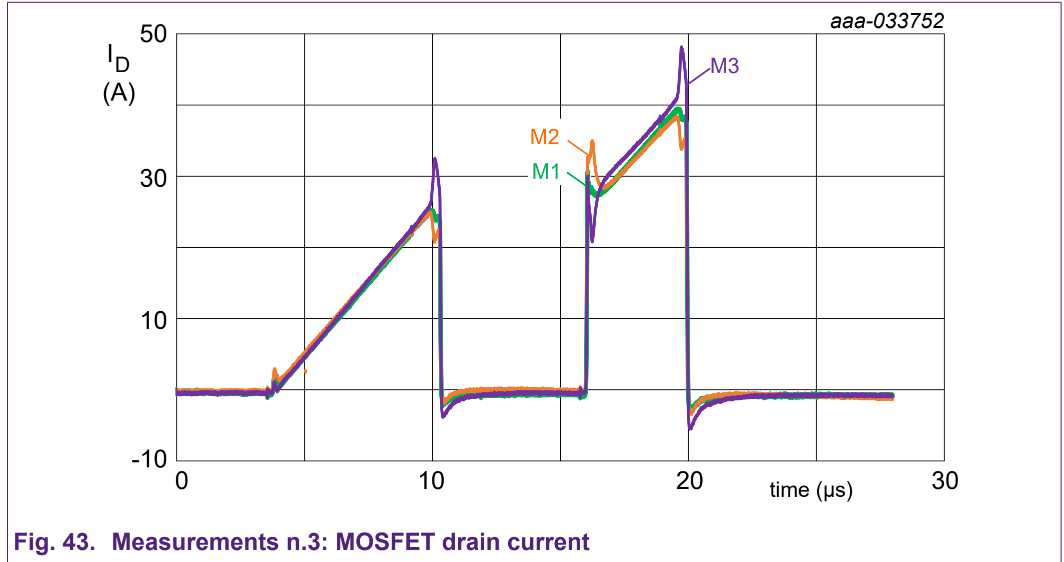

Fig. 43. Measurements n.3: MOSFET drain current

Table 18. Summary measurements n.3

Device	R_{DSon} [mΩ]	$Q_{G(tot)}$ [nC]	$V_{GS(th)}$ [V] @1 mA	$V_{GS(th)}$ [V]@ 1 A	Energy Sharing Switching	Energy Sharing Conduction
M1	3.16	35.57	3.02	3.62	32.0 %	32.9 %
M2	3.43	28.69	3.03	3.63	32.0 %	32.9 %
M3	3.05	44.50	3.02	3.62	36.0 %	34.2 %

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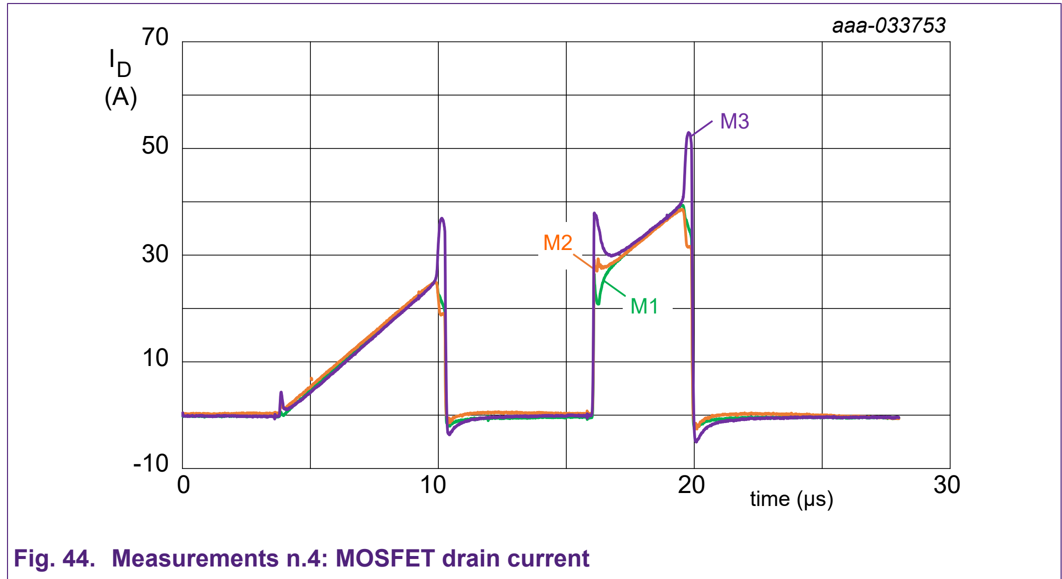

Fig. 44. Measurements n.4: MOSFET drain current

Table 19. Summary measurements n.4

Device	R_{DSon} [mΩ]	$Q_{G(tot)}$ [nC]	$V_{GS(th)}$ [V] @1 mA	$V_{GS(th)}$ [V]@ 1 A	Energy Sharing Switching	Energy Sharing Conduction
M1	3.16	35.57	3.02	3.62	25.5 %	33.2 %
M2	3.05	44.50	3.02	3.62	27.5 %	33.2 %
M3	3.14	33.74	2.80	3.39	45.3 %	33.6 %

11.2. Simulations

The following simulations can be used to verify a SPICE model conformity to data sheet.

R_{DSon} simulation

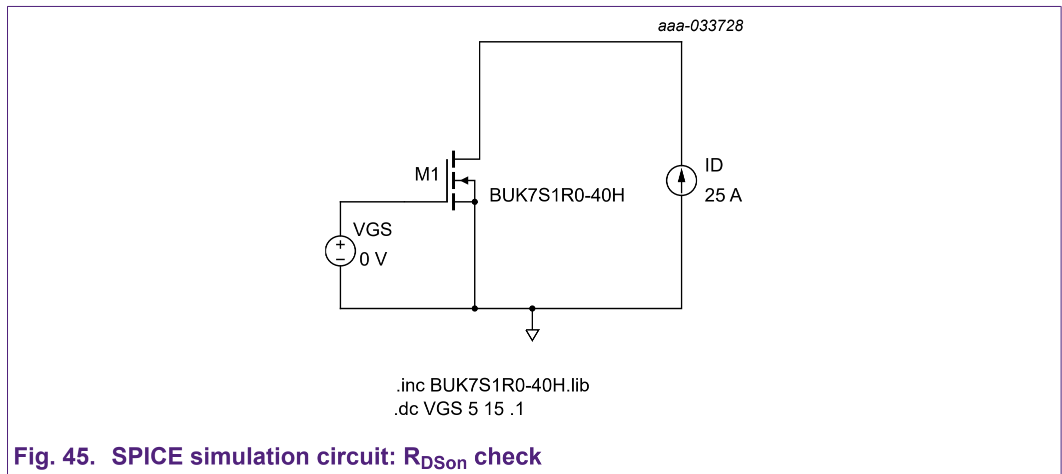

Fig. 45. SPICE simulation circuit: R_{DSon} check

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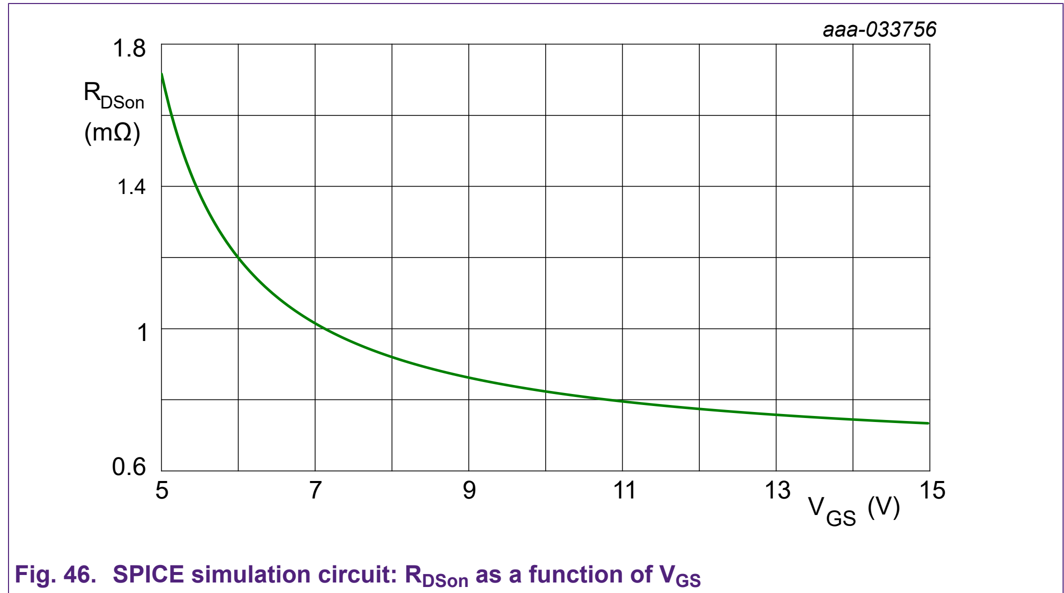

Fig. 46. SPICE simulation circuit: R_{DSon} as a function of V_{GS}

$Q_{G(tot)}$ simulation

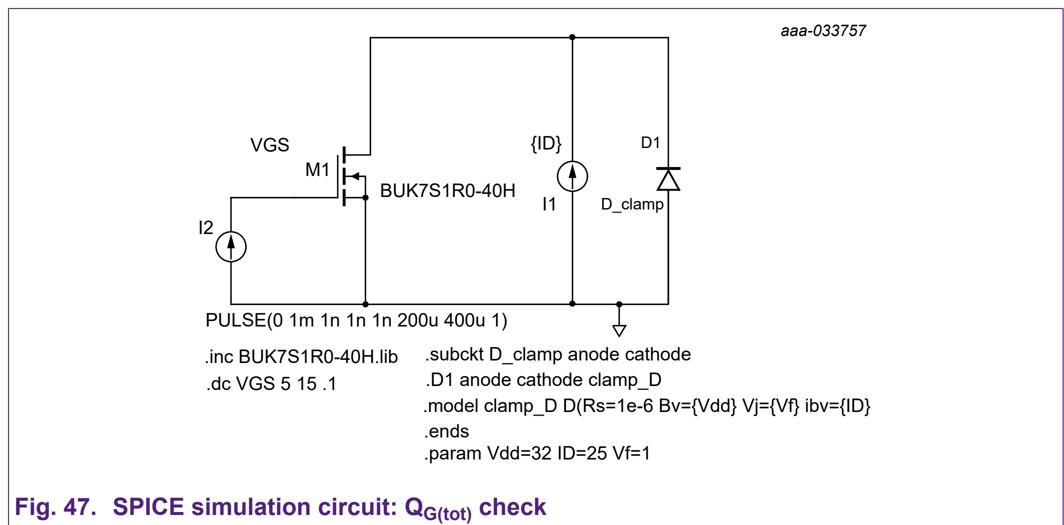

Fig. 47. SPICE simulation circuit: $Q_{G(tot)}$ check

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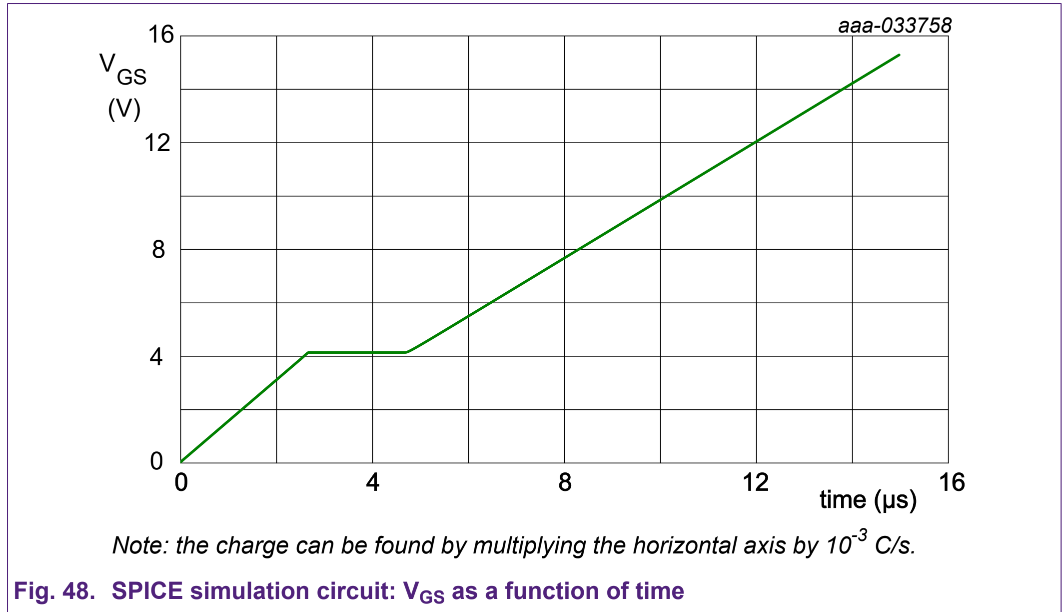

Note: the charge can be found by multiplying the horizontal axis by 10^{-3} C/s.

Fig. 48. SPICE simulation circuit: V_{GS} as a function of time

$V_{GS(th)}$ simulation

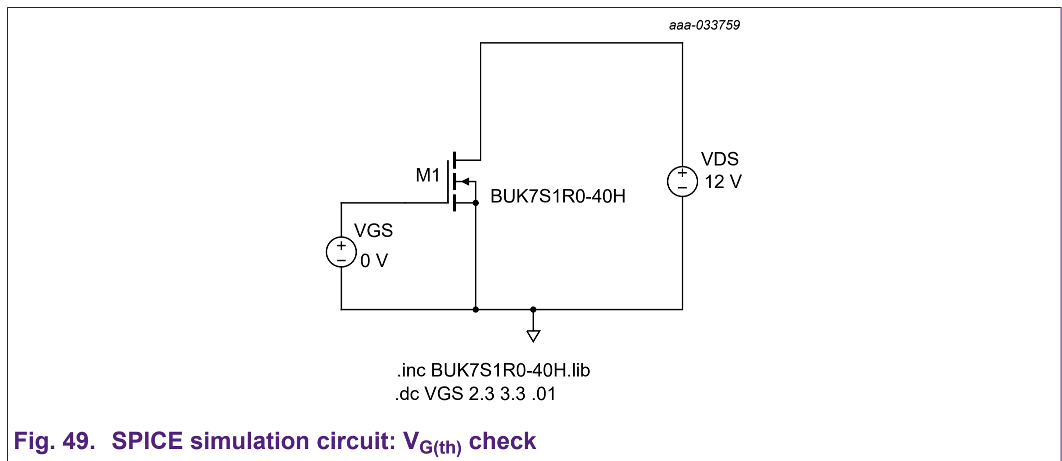

Fig. 49. SPICE simulation circuit: $V_{G(th)}$ check

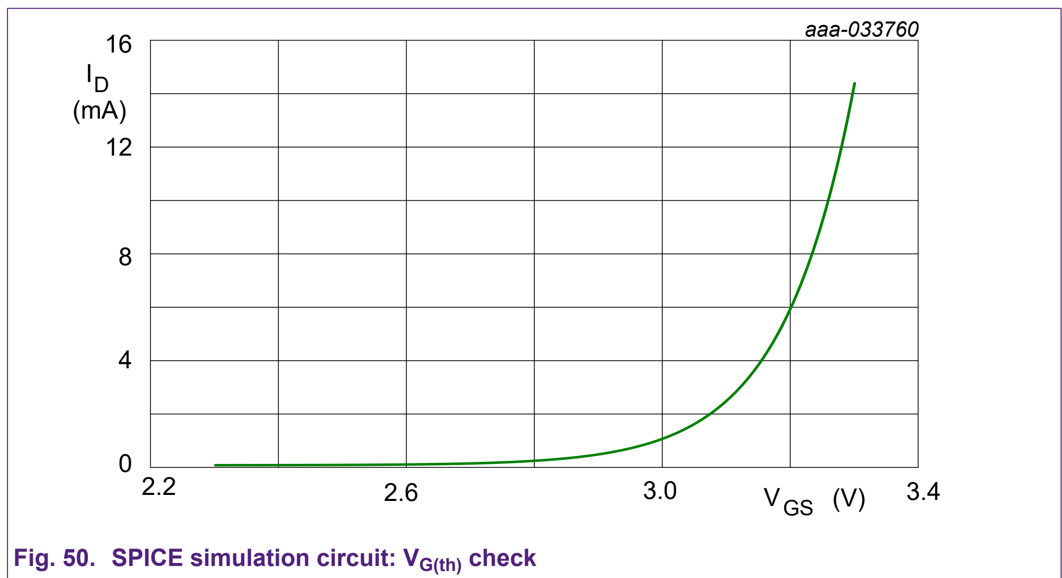

Fig. 50. SPICE simulation circuit: $V_{G(th)}$ check

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1. “The Art of Electronics”, by Paul Horowitz and Winfield Hill: §3.6.3. Paralleling MOSFETs, page. 213
2. AN90011: Half-bridge MOSFET switching and its impact on EMC
3. AN90003: LFPAK MOSFET thermal design guide”
4. BUK7S1R0-40H data sheet

13. Revision history

Table 20. Revision history

Revision number	Date	Description
1.1	2021-09-13	Minor update, values corrected in Table 12 and Table 14.
1.0	2021-09-07	Initial version.

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