AN90007

Pin FMEA for AVC family

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Document information

Information	Content
Keywords	FMEA, AVC, CMOS, 3.3 V systems
Abstract	This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of the Nexperia's AVC family under typical failure situations

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1. Introduction

Solution for low-voltage high-speed parallel interfaces.

The advanced very-low-voltage CMOS (AVC) logic family contains a feature rich logic portfolio providing a 1-bit, 2-bit, 4-bit up to 20-bit parallel interface products for use in 1.8 V, 2.5 V, 3.3 V and mixed 1.8 V/3.3 V systems, as well as dual supply transceivers for level shifting applications.

2. AVC family overview

AVC logic devices are specified over 1.2 V to 3.6 V (standard) or 0.8 V to 3.6 V (dual supply transceivers). With a typical propagation delay of 1.5 ns, AVC is one of the fastest families in the world. To reduce under and overshoot output options include source terminated balanced 12 mA drive and dynamically controlled outputs (DCO) that increase output impedance after the output transition is completed, to enable termination while maintaining a high signal rate.

Over voltage tolerant I/O, source termination resistor, bus hold, power OFF and DCO are some of the advanced features of these devices making them ideal for parallel interface applications.

AVC products are available in leaded package as SO, TSSOP and VSSOP. Innovative for PCB space saving are more the leadless packages as MicroPak and DQFN. Our AVC parallel interface products are fully specified from -40 °C to 85 °C, the dual supply level translating transceivers are fully specified from -40 °C to 125 °C.

3. Pin FMEA

This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia's AVC family under typical failure situations such as a short-circuit to V_{CC} or GND or to a neighboring pin, or if a pin is left open.

Some AVC family devices have special functions, such as translators and level-shifters, that can have different behaviors. A failure is classified according to its effect on the AVC device and the functionality of the application. (see Table 1)

Table 1. Classification of failure effects

Class	Failure effect
A	damage to device
	affects application functionality
B	no damage to device
	may affect application functionality
C	no damage to device
	no affect to application functionality

Table 2. FMEA matrix for pin short-circuit to V_{CC}

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined HIGH, no damage, no leakage, no output level change
Output	A	if output defined LOW, short-circuits and high currents can damage device, output level changes
GND	B	short-circuits and high currents can damage device, will affect functionality

Table 3. FMEA matrix for pin short-circuit to GND

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality
Output	C	if output defined LOW, no damage, no leakage, no output level change
Output	A	if output defined HIGH, short-circuits and high currents can damage device, output level changes
V_{CC}	B	no damage to device, will affect functionality

Table 4. FMEA matrix for pin left open

Pin	Class	Remarks
Input	B	undefined operating condition, no damage, increases leakage (except bus hold types), may affect functionality
Output	C	normal operating condition, no damage, no leakage
GND	B	undefined operating condition, no damage, increases leakage, will affect functionality
V_{CC}	B	undefined operating condition, no damage, increases leakage, will affect functionality

Table 5. FMEA matrix for pin short-circuits between neighbor pins

Pin	Class	Remarks
Input to input	C	if inputs have same voltage levels: no damage, no leakage
	B	if inputs have different voltage levels: leakage increases, will affect functionality
Input to output	A	if input and output have different voltage levels, can cause high current and can damage device, will affect functionality
	C	if input and output have same voltage levels, no damage, no leakage
Input to GND	-	see Table 3
Input to V_{CC}	-	see Table 2
Output to output	C	if outputs have same voltage levels, no damage, no leakage
	A	if outputs have different voltage levels, can cause high current and can damage device, will affect functionality
Output to input	-	same effect as ‘input to output’ condition
Output to GND	-	see Table 3
Output to V_{CC}	-	see Table 2
GND to V_{CC}	-	not applicable, these pins are not neighbors

4. Abbreviations

Table 6. Abbreviations

Acronym	Description
AVC	Advanced Very-low-voltage CMOS
CMOS	Complementary Metal-Oxide Semiconductor
DCO	Dynamic Controlled Outputs
FMEA	Failure Modes and Effects Analysis
PCB	Printed Circuit Board
TTL	Transistor-Transistor Logic

5. Revision history

Table 7. Revision history

Rev	Date	Description
v.1	20181130	AN90007

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