AN90016

Maximum continuous currents in NEXPERIA LFPAK power MOSFETs

Rev. 1.1 — 3 September 2020 application note

Document information

Information	Content
Keywords	LFPAK, MOSFET, ID, IS, continuous current
Abstract	This application note examines the factors that determine the maximum permissible current ratings for LFPAK (copper-clip package) MOSFETs.

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1. Introduction

Modern electronics using low-voltage (<100 V) MOSFETs has seen an increase in high-power demand in both automotive and industrial applications. Power output in kilowatt terms for applications such as motor drive is now a very common requirement. Combined with the existing space constraint in modules this means that the need to handle more power is being passed on to the components, particularly MOSFETs.

The current limit given in data sheets for power MOSFETs is one of the most important parameters in such high-power applications where the handling of very high currents is required.

As the MOSFET is a three terminal device – Gate, Source and Drain – current can flow through any of these terminals as I_G, I_S and I_D respectively. Only maximum continuous current I_D (drain-source) and continuous current I_S (source-drain/body diode) will be considered. Leakage currents (I_{GSS}, I_{DSS}) and pulsed currents such as I_{DM} are not in the scope of this document

This application note gives a comprehensive insight into the methodology in determining the maximum continuous current rating of NEXPERIA power MOSFETs.

It is critical to fully understand the capabilities, the boundaries and the relevant environmental conditions so that electronics engineers and designers select the right MOSFET for the right application - all of which will be discussed and addressed in this document.

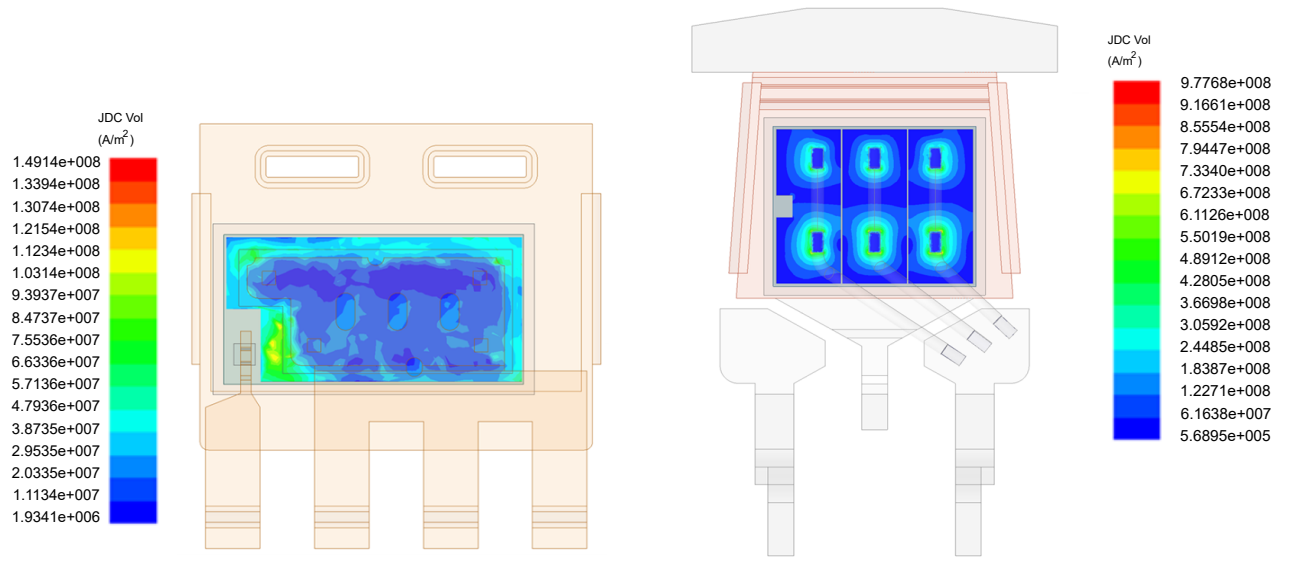
This application note is specific for LFPAK and its copper clip bond technology – NEXPERIA flagship package.

2. LFPAK, superior performance

LFPAK packages are compact in size, they offer much higher power density and reduced parasitic inductances compared with wire bond devices. Combined with their copper clip bond technology, they have played an important role in MOSFETs achieving a very high current capability.

As illustrated in Fig. 1 below, LFPAK copper clip bond packages have the following benefits:

- Prevents localised current crowding shown in Fig 1 b) D2PAK wire bond package
- Allows for a more uniform current spread
- Acts as a heat sink to the die



a) LFPAK88 b) D2PAK

Note: current density contour scaling is different for LFPAK88 and D2PAK, see accompanying colour scaling

Fig. 1. Current crowding contours for a) LFPAK88 and b) D2PAK packages

3. Key parameters that set out the boundaries

Before discussing what maximum current a MOSFET can achieve, it is important to highlight the parameters governing the boundaries of the environment within which the MOSFET must operate. These boundaries are mainly set by the thermal environment, but also by the conditions that impact the MOSFET data sheet parameters; both have a direct effect on the performance and the capabilities of the MOSFET.

Thermal environment and thermal parameters

This section discusses the thermal parameters and explains their direct impact on the maximum current in a MOSFET.

Temperature Range and the 175 °C limit

-55 °C is the lowest temperature given in the data sheet. Although normally this is associated with storage temperature, MOSFETs' characteristics in NEXPERIA data sheet are given against this value. Note - the lowest temperature associated with real life application is usually **-40 °C**

25 °C (unless otherwise stated) is the reference temperature that all maximum capabilities of MOSFETs are based upon. In NEXPERIA MOSFET data sheets, this is given as a mounting base temperature parameter – $\mathbf{T_{mb}}$ – referring to the central point of the MOSFET drain tab. Note - other MOSFET venders commonly use T_c (case temperature), which refers to the same point, i.e. drain tab and not to the plastic part of the MOSFET.

175 °C refers to the junction, i.e. the silicon die, temperature of the MOSFET and the parameter for this is given as $\mathbf{T_j}$. All MOSFETs must operate below this temperature – more details are given later.

The 175 °C limit explained

With high temperatures, it is understandable to think that the plastic mould should be the first cause of concern.

Historically plastic moulds have caused issues and although improvements have been made in this industry, if the right compound is not properly selected it can still cause issues and leads to device failures. However, plastic mould compound alone does not give the full story nor is it the source of setting the 175 °C limit, as will be discussed in the next section.

4. MOSFET structure

This section briefly discusses the main components in the internal structure of LFPAK MOSFETs and their temperature properties:

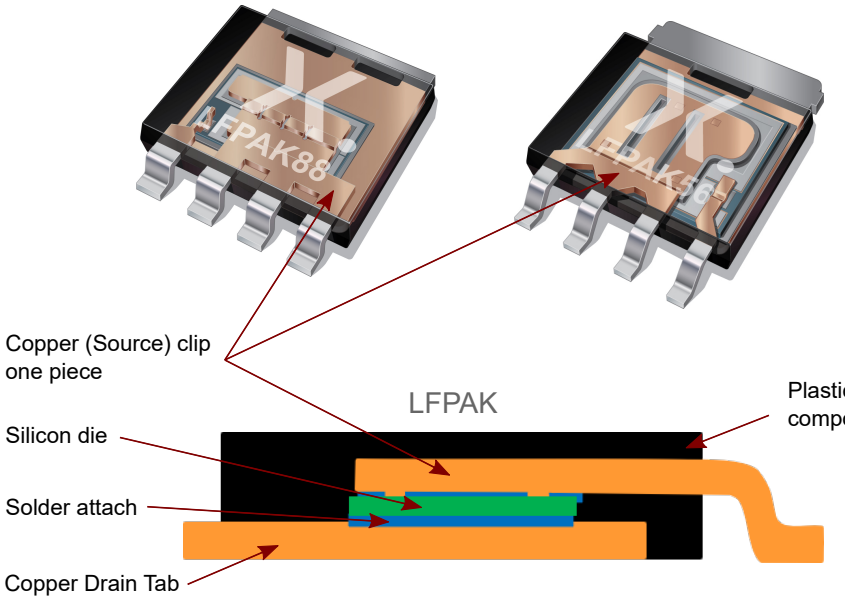


Fig. 2. LFPAK internal structure

Silicon / die: 250 °C. Pure silicon melting temperature is 1,414 °C. However, silicon in the MOSFET is doped and at ~250ºC there will be thermal activation where current will flow across the PN junction and the MOSFET no longer acts as a switching device – i.e. there is no control over turn-on / turn-off.

Copper clip: melting temperature of copper is 900 °C. This is to highlight the fact that it can handle very high temperature and not used for any calculation purposes. The criteria used to make sure that the copper in the MOSFET is capable for current handling is explained later in the note.

Solder attach: melting point >300 °C.

Plastic mould compound: Can potentially harden and becomes brittle around 190 °C and above. The composition of the plastic mould compound is carefully selected to withstand high temperature specification.

As shown above, the internal components of the MOSFET are either naturally capable of withstanding temperatures >175 °C or specifically selected to do so.

Limiting the MOSFETs maximum junction temperature T_j to 175 °C is driven by the reliability requirements MOSFETs need to meet. And thus, 175 °C is the temperature limit used by NEXPERIA for qualification and life test of MOSFETs in line with industry standard.

All automotive power MOSFETs must meet the 175 °C junction temperature specification. Although this requirement is not applicable to non-automotive devices which meet T_j of 150 °C, most of NEXPERIA industrial MOSFETs are life tested and qualified to 175 °C.

5. Maximum power and maximum current

5.1. Maximum power

With the junction temperature limit set to a maximum of 175 °C, the maximum amount of power allowed in the MOSFET can then be determined.

The key parameters needed to calculate this maximum power allowance are the thermal impedance between the die and the mounting base; $Z_{th(j\text{-}mb)}$ and thermal resistance between the die and the mounting base $R_{th(j\text{-}mb)}$.

$R_{th(j\text{-}mb)}$ is the thermal resistance which means that the thermal response has reached steady state conditions (also referred to as DC conditions).

$Z_{th(j\text{-}mb)}$ is the term used to represent thermal impedance in its entirety, steady state as well as transient conditions (more details are given later).

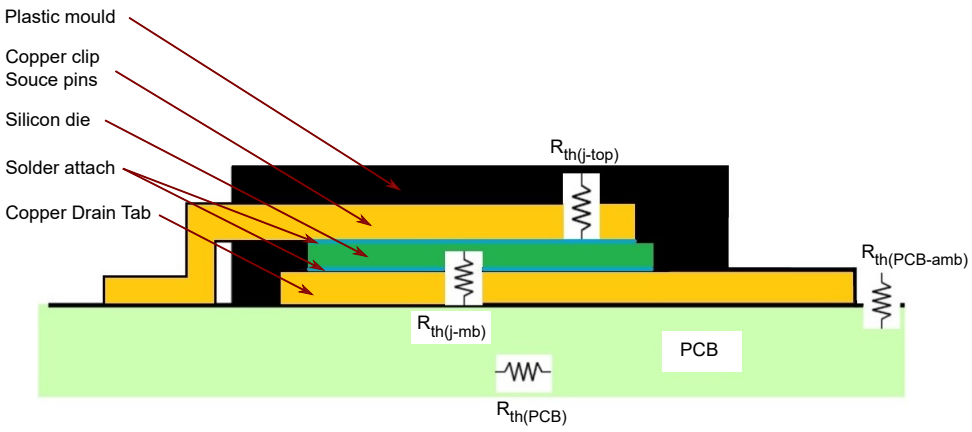


Fig. 3. Thermal resistances inside and outside the MOSFET

Fig. 3 illustrates the main thermal paths that exist from the MOSFET silicon die to the external surroundings and ambient environment. The dominant path in dissipating heat from the die is through the MOSFET drain tab and therefore the thermal impedance of most relevance is $Z_{th(j\text{-}mb)}$ (also referred to as $R_{th(j\text{-}mb)}$).

It is worth pointing out that the source clip in the LFPAK package also provides an important thermal path. Having the right amount of copper in the PCB layout for the source pins is beneficial and should be considered in the design.

The LFPAK thin plastic mould adds another option of dissipating heat from the top of the device should the design consider a heat sink at the top. For more details about thermal performance and recommendations please refer to the NEXPERIA thermal guide *AN90003*.

As previously mentioned all maximum capabilities of the MOSFET are given in reference to T_{mb} = 25 °C.

The maximum power allowance can then be derived from the following formula:

$$P_{(max)} = \frac{T_{j(max)} - T_{(mb)}}{R_{th(j\text{-}mb)}} \quad (1)$$

The junction to mounting base thermal impedance values can be obtained from the graph provided in the data sheet; the parameter used is transient thermal impedance $Z_{th(j\text{-}mb)}$.

For references the device used in the application note is PSMNR70-40SSH (LFPAK88 0.7 mΩ, 40 V, standard level) qualified to 175 °C.

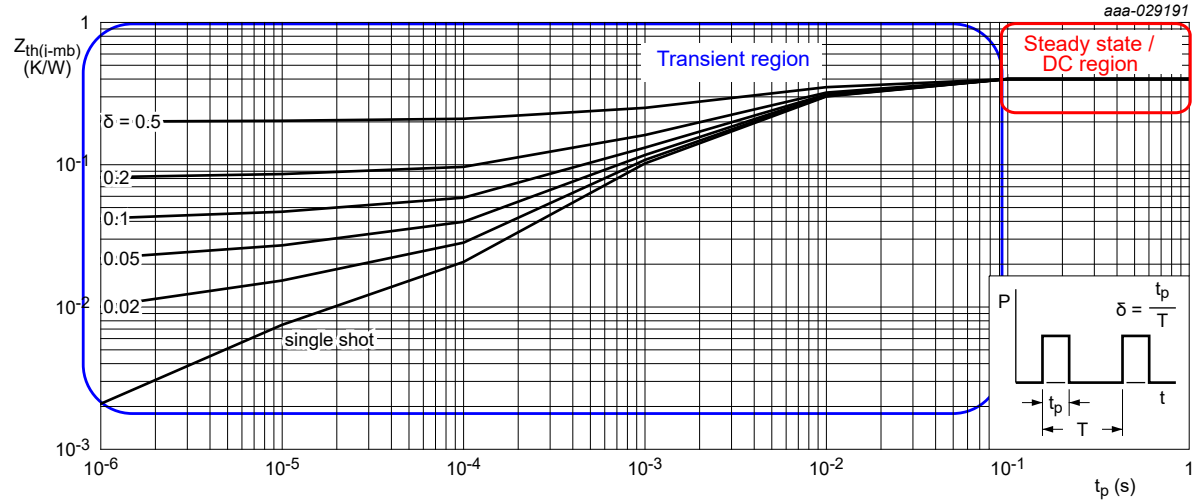


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

As can be seen from the graph in Fig. 4 the MOSFET thermal response is similar to an RC network electrical response – hence the thermal models provided on NEXPERIA support page representing this response are referred to as RC thermals – see the Support TAB of the PSMNR70-40SSH product information page. For detailed information about RC thermal models see application note *AN11261*.

The curve in the graph showing pulses up to 100 ms is known as the transient condition section (transient region) and the parameter used is $Z_{th(j\text{-}mb)}$. It is given in single shot pulse or repeated PWM pulses with various duty cycles. The transient region is relevant to situations such as short circuits, power surges or switching transitions, they tend to be high power for short periods of time. Larger devices normally perform better in this region due to their bigger drain tab areas.

For pulses above 10 ms, as can be seen from the graph the curves start to plateau and will flatten after 100 ms. This section of the graph is referred to as steady state and is given as thermal resistance parameter $R_{th(j\text{-}mb)}$.

From 100 ms onwards the MOSFET will transition into thermal stability and is considered in DC state. In this region the thermal impedance reaches its maximum value and the steady state capabilities of the MOSFETs are given against this maximum value.

Note: the time it takes the MOSFET to reach steady state is not necessarily the same for the PCB where the MOSFET is mounted on as the PCB thermal response is slower. Therefore it is important to use the right thermal impedance for each the PCB and the MOSFET when running thermal analysis for a given condition. RC Cauer models found in NEXPERIA support page allow for PCB RC network to be added if known.

5.2. Maximum continuous drain current

The maximum current a MOSFET can achieve is primarily derived from the maximum power allowance in the MOSFET. When calculating maximum continuous current, the maximum steady state power must be used.

Example:

Device Name: PSMNR70-40SSH

T_{mb} = 25 °C

$T_{j(max)}$ = 175 °C

$R_{th(j\text{-}mb)}$ = (0.4 K/W max)

Table 1. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.35	0.4	K/W

$$P_{(max)} = \frac{T_{j(max)} - T_{(mb)}}{R_{th(j\text{-}mb)}} = \frac{175 - 25}{0.4} = 375\ W \quad (2)$$

This value for maximum power can be found in data sheet limiting values table:

Table 2. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	T_{mb} = 25 °C		-	375	W

Using the power formulae:

$$P = I^2 \times R \quad (3)$$

Where *I* is the drain current (I_D) and *R* is the on-state resistance of the MOSFET (R_{DSon}).

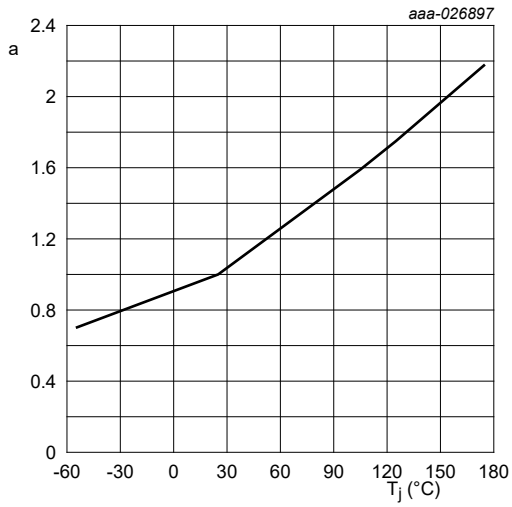
I_D can then be calculated as:

$$I_D = \sqrt{\frac{P}{R_{DSon}}} \quad (4)$$

The on-state resistance value that must be used to calculate $I_{D(max)}$, is the MOSFET R_{DSon} at T_j max – in this case R_{DSon} at T_j = 175 °C.

$$I_{D(max)} = \sqrt{\frac{P_{(max)}}{R_{DSon}\,@175\ °C}} \quad (5)$$

A factorisation graph is provided in the data sheet for R_{DSon} as a function of junction temperature, (see Fig. 5). This can be useful to calculate the current for a specific temperature requirement. For PSMNR70-40SSH the R_{DSon} multiplication factor for T_j = 175 °C is 2.19. Note: this graph is based on measured values.



$$a = \frac{R_{DSon}}{R_{DSon\ 25\ °C}}$$

Fig. 5. Normalized drain-source on-state resistance factor as a function of junction temperature

From the data sheet characteristics table, Max R_{DSon} = 0.7 mΩ (V_{GS} = 10 V, T_j = 25 °C):

Table 3. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		0.43	0.62	0.7	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C		0.85	1.23	1.53	mΩ

The resulting R_{DSon} at V_{GS} = 10 V, T_j = 175 °C = 1.53 mΩ, (2.19 x 0.7 mΩ). This value is also included in the data sheet characteristic table. For further details about MOSFET data sheet parameters please refer to application note *AN11158*.

$$I_{D(max)} = \sqrt{\frac{P}{R_{DSon}}} = \sqrt{\frac{375}{0.00153}} = 495\ A \quad (6)$$

495 A is considered to be the theoretical capability at T_j = 175 °C. Another term commonly used is silicon capability.

Once the theoretical maximum I_D is established, the next stage is to validate this value through test and verification. This will allow for other limiting factors to be highlighted and considered in finalising and protecting the $I_{D(max)}$ given in the data sheets.

In the case of PSMN70-40SSH, the validated $I_{D(max)}$ @ T_{mb} = 25 °C is 425 A.

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C	[1]	-	425	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	350	A

[1] 425A. Continuous current has been successfully demonstrated during application. Practically, the current will be limited by the PCB, thermal design and operating temperature.

The formulae:

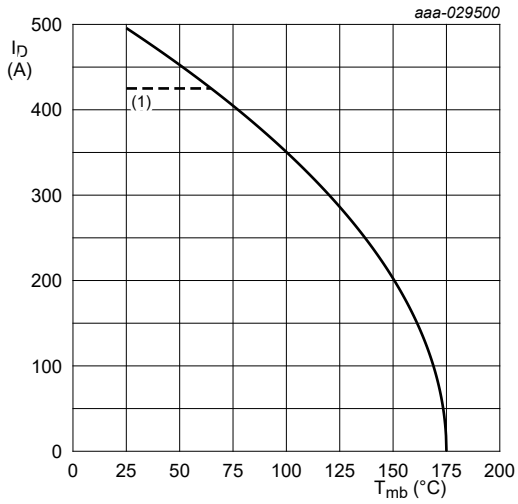
$$I_{D(max)} = \sqrt{\frac{P_{(max)}}{R_{DSon}\,@175\ °C}}$$

can also be used for different temperatures. For example $I_{D(max)}$ at 100 °C can be calculated as follows:

$$P_{(max)} = \frac{T_{j(max)} - T_{(mb)}}{R_{th(j\text{-}mb)}} = \frac{175 - 100}{0.4} = 187.5\ W \quad (7)$$

$$I_{D(max)} = \sqrt{\frac{187}{0.00153}} = 350\ A \quad (8)$$

The same principle applies across the full operating temperature range. MOSFET data sheets contain a drain current de-rating graph in the limiting values section, see Fig. 6 below.



$V_{GS} \geq 10$ V
(1) 425 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 6. Continuous drain current as a function of mounting base temperature

Fig. 6 shows:

- $I_{D(max)}$ for silicon capability @ 175 °C (solid curve)
- $I_{D(max)}$ capped value (dashed line)

As stated in NEXPRIA data sheets the continuous $I_{D(max)}$ value in the limiting table is not given as a figure verified by design i.e. theoretical, but rather demonstrated through testing. Some of the reasons for capping the continuous $I_{D(max)}$ value at lower limits than the solid curve given in the graph are as follows:

Package limit

- This is normally associated with wire bond MOSFETs.
- Historically old parts (10 years or older) experienced issues with the package – this was due to a combination of:
  1. Wire bond fuse – being a major reason for lowering the current rating
  2. Plastic mould compound.

- This limited $I_{D(max)}$ to 100 A – 120 A, and this legacy approach had been carried on for some devices even if they were clip bond LFPAK and less than 10 years old.
- As MOSFETs capabilities have reached a much higher level than has been possible in the past, it is only appropriate to select the right plastic compound and adapt a more accurate approach so that these new limits are achieved.
- By making the package not the limiting factor NEXPERIA MOSFETs can operate to their optimum level, giving the designer full advantage of these capabilities.

Test boards

- Test boards are important part in verifying the $I_{D(max)}$ capabilities more so at NEXPERIA as they may be the limiting factor – as mentioned previously only $I_{D(max)}$ values that are verified through test are used.
- Improvement have been made in recent years so the right test boards are used to maintain T_{mb} at 25 °C.
  - Note that some MOSFETs vendors state continuous max current as verified by design and some limit the rating to a one second test. Although for R_{th} thermal stability is considered to be reached at one second, (represented by the flat line in Z_{th} graph) and for the MOSFET this is steady state condition. The length of time for max I_D test at NEXPERIA exceeds 30 seconds continuous.

$T_{j(max)}$ exceeded

- Junction temperature T_j is monitored during continuous I_D testing. Higher I_D values resulting in T_j exceeding 175 °C are not considered.

Silicon limit

- The silicon capability at 175 °C given in the data sheet as the solid curve is the absolute limit. Meaning only the I_D values that PASS the test at the curve level or below are validated. Instances where MOSFETs I_D measure values above the curve can be explained by the fact that most MOSFETs operate at their typical R_{DSon} values while the curve only considers the $R_{DSon(max)}$ values.

Source pins

- Calculations based on the source pins dimensions i.e. length, width, cross-section area, size, etc., as well as the alloy/copper property are used to make sure the current density and capability of the pins meet the I_D rating.

In summary the final maximum continuous I_D rating is based on the lowest limit met by any of the above criteria.

5.3. Maximum continuous source current

Although I_S has always been given as a separate parameter, its value had historically been linked to I_D. The value of I_S was based on calculation and was either lower than I_D or made the same even if it was calculated to be a higher value. A more accurate approach is to rate the current capabilities for both I_D and I_S separately. This approach is now standard and verification through testing in the same way as explained previously is applied.

Determining the I_S limiting value

As far as the maximum power in the MOSFET is concerned, it is the same power allowance whether it is applied through the MOSFET channels (I_D) or the MOSFET body diode (I_S). Therefore the simple power formulae to use is P = V × I, where V is the body diode voltage drop (V_{SD}) and I is the source-drain current I_S. Therefore the power calculated in the previous sections still applies, and in the case of the device example given, P = 375 W.

- The power through the MOSFET channel is $P = I^2 \times R$
- Power through the MOSFET body diode is P = V × I, where V is the diode voltage drop (V_{SD}) and I is the source-drain current I_S

The V_{SD} maximum value given in the data sheet characteristics table is 1 V, (see Table 5 below).

Table 5. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	0.75	1	V

In theory I_S should be = 375 A, (I = P/V, P = 375 W, V = 1). In reality though V_{SD} is typically around 0.75 V and this would be the case for more than 90% of all devices.

Furthermore, V_{SD} is temperature dependant and the voltage will drop as temperature goes up. It is also true to say that the voltage V_{SD} goes up when current increases, but the heating element (induced by the current as self-heating) has a bigger impact.

The continuous source current that has been measured and is validated in the data sheet for PSMNR70-40SSH is 500 A, see Table 6 below.

Table 6. Limiting values

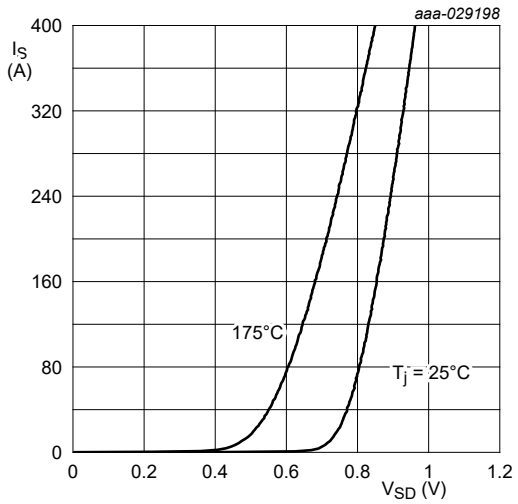
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	500	A

[1] 500A. Continuous current has been successfully demonstrated during application. Practically, the current will be limited by the PCB, thermal design and operating temperature.

Source-drain characteristic

MOSFET data sheets include a V_{SD} characteristic graph, see Fig. 7 below.



V_{GS} = 0 V

Fig. 7. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical value

The above graph is obtained by testing the device with pulsed current to avoid self-heating, (which would result in higher values for V_{SD}). In real applications self-heating will most likely occur, as currents lasting more than 100 ms will be sufficient to get R_{th} in steady state region and allow the device to heat up.

To help determine V_{SD} values at higher temperatures Fig. 7 includes curves for T_j = 25 °C and for T_j = 175 °C. This shows that the V_{SD} value reduces with increased junction temperature. As can be seen from Fig. 7 (T_j = 175 °C curve), with I_S = 400 A, V_{SD} is just over 0.8 V and with power = 375 W this will result in I_S = 440 A. The rating for I_S given in data sheet is = 500 A, this difference can be explained by the following: power of 375 W is based on max R_{th} of 0.4 K/W. However, a typical R_{th} is = 0.35 K/W resulting in power = 428 W. With I_S = 500 A, V_{SD} = 0.85 V.

Note: the I_S value given in the data sheet (in this case 500 A) has been proven through testing and the value is validated .

6. Practical application examples

This section details the function and configuration of power MOSFETs in a basic application circuit. Three key application stages will be discussed - RPP (Reverse Polarity Protection), isolation and load drive. Fig. 8 below shows a simplified circuit capturing some basic operations of the different MOSFET configurations.

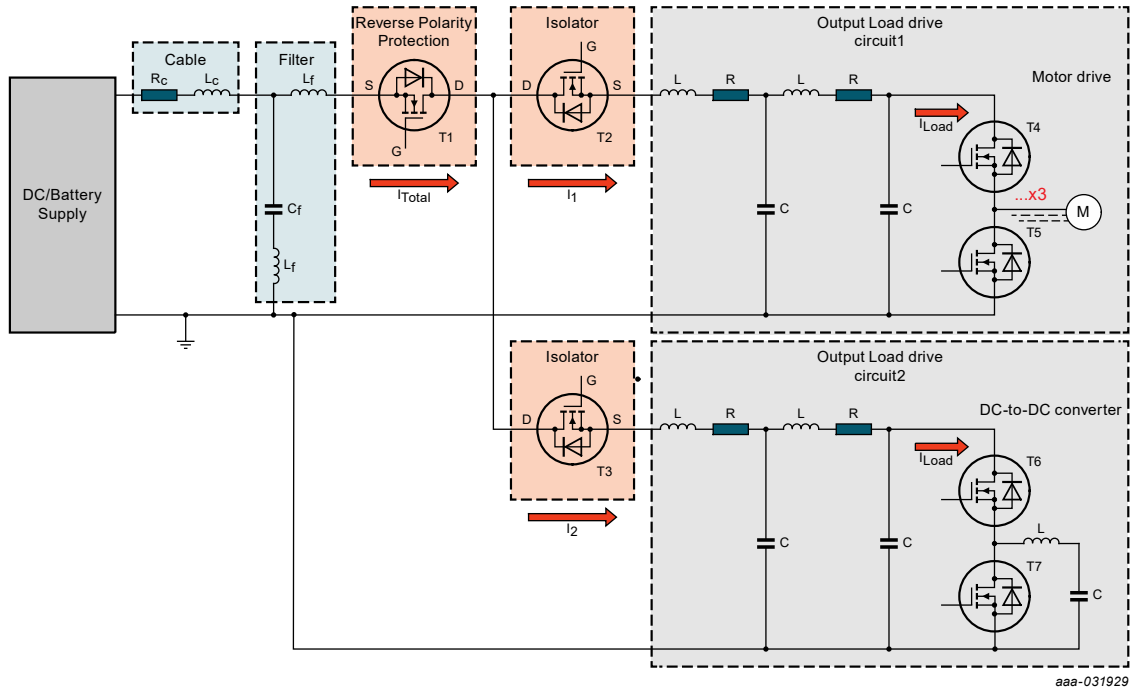


Fig. 8. Simplified motor drive and DC-to-DC converter application diagram

6.1. Output load drive MOSFETs T4, T5, T6 and T7

The circuits shown in Fig. 9 and Fig. 10 both show a pair of power MOSFETs implemented as a half-bridge, a common configuration for motor drive (T4 and T5 see Fig. 9) and DC-to-DC converters (T6 and T7, see Fig. 10) – for details on half-bridge MOSFET switching parameters and performance refer to NEXPERIA application note *AN90011*.

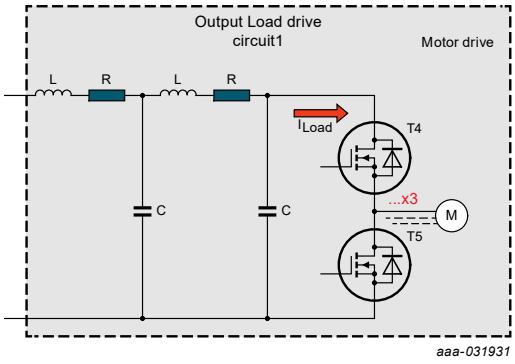


Fig. 9. Output load drive circuit 1 (motor drive)

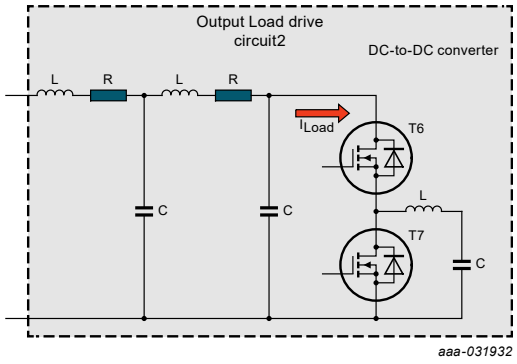


Fig. 10. Output load drive circuit 2 (DC-to-DC)

In this example we look at output load drive circuit 1, T4 and T5 in relation to current demand which will be gated by the type of motors driven and the power requirement of the application.

Motor drive application

Parameters profiling a motor can be summarised in Fig. 11 below:

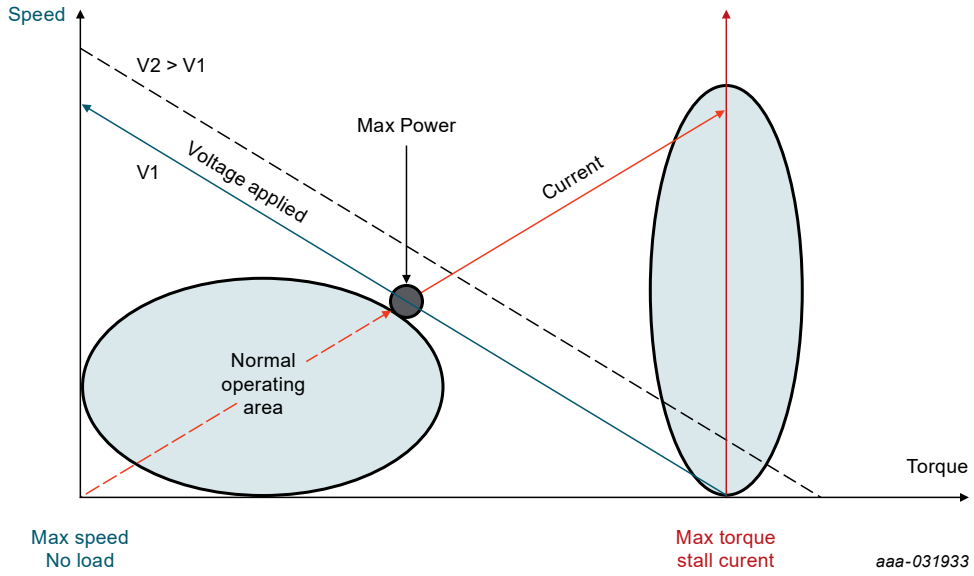


Fig. 11. Motor operation parameters

Normal operating area is where a motor is designed and specified to spend most of its working life. However, it is expected that motors will go through situations of stalled rotation a number of times in their operating life. These stalled motor situations, albeit don't happen on a prolonged periods, are considered part of the a normal operation. Adding to this profile, fault conditions situation such as short circuit where motor drive circuit are expected to recover from, one can appreciate the type of power capabilities that need to be considered in selecting a power MOSFET driving such application. Note: although stall conditions may last few tens or hundreds milliseconds, as explained previously this will be enough to make the MOSFET operate in DC conditions and therefore continuous current capability is key.

6.2. Output isolator MOSFETs T2 and T3

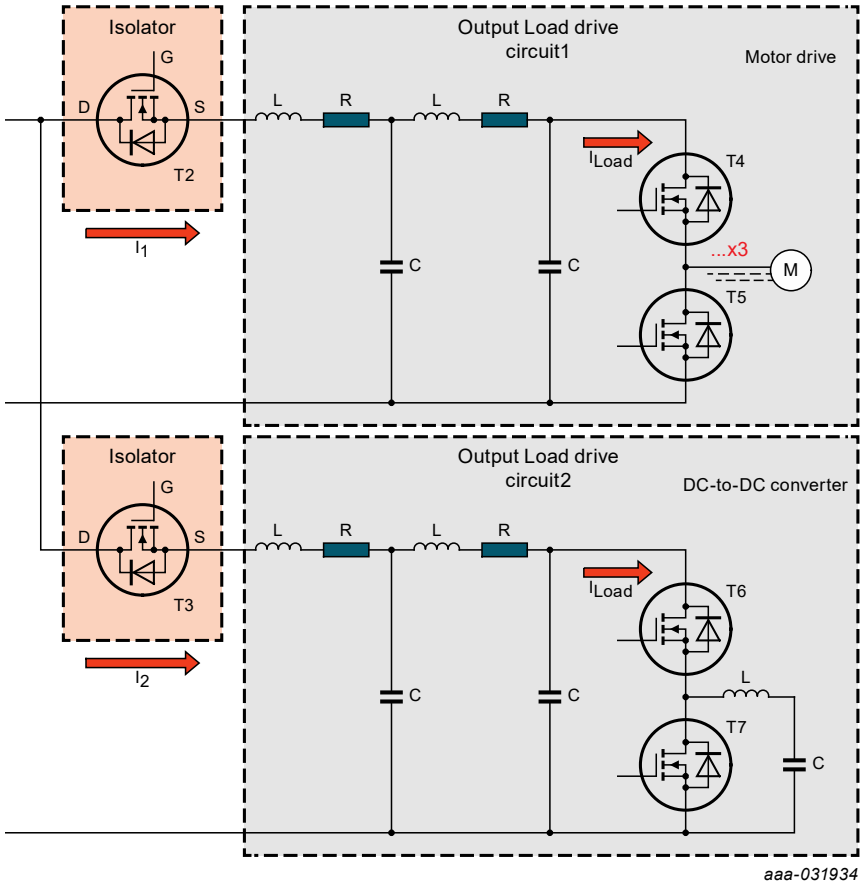


Fig. 12. MOSFETs used as isolators T2 and T3

Some designs may drive two different output loads. A representation of such circuits is given in Fig. 12 above. MOSFETs T2 and T3 are used to isolate their respective circuits as they may not need to operate at the same time.

MOSFETs are also used as isolators is designs using the same circuit duplicated to drive one common output. This may be due to redundancy requirement in order to meet a safety standard (usually associated with automotive application to allow continuous operation even in cases of failure – such redundancy circuit is not part of this example here, but the same principle applies).

In such applications particular attention should be given to:

- Current capability in MOSFETs. T2 and T3 need to cater not only for the current needed to drive the loads, but also for the immediate drive circuits current drawn (Fig. 12 circuit 1 & circuit 2 respectively).
- Some designs require large capacitors in the drive circuit. The drive circuit itself can be treated as a capacitive load and therefore high inrush current or soft start capabilities are important in the selection of MOSFETs – soft start mode is applied to MOSFET's turn on so that high inrush currents are brought under control and this type of operation requires a MOSFET with strong SOA performance. For SOA related details please see NEXPERIA application note *AN11158*.
- Another issue that might result from such large capacitors used in the drive circuits is the current they supply in a case of a fault incident explained as follows:
  In a case where T3 is off (circuit 2 is disabled) and T2 is ON, if a short circuit occurs in drive circuit1, charged capacitors from drive circuit 2 can supply very high current to drive circuit 1 through the MOSFET body diode of T3 and through T2 (the same can occur in the opposite direction). In this example it is important to pay attention to I_S capability in a MOSFET

MOSFETs T2 and T3 require strong capabilities in continuous I_D, I_S and depending on implementation of soft start, strong SOA.

6.3. Reverse polarity protection MOSFET T1

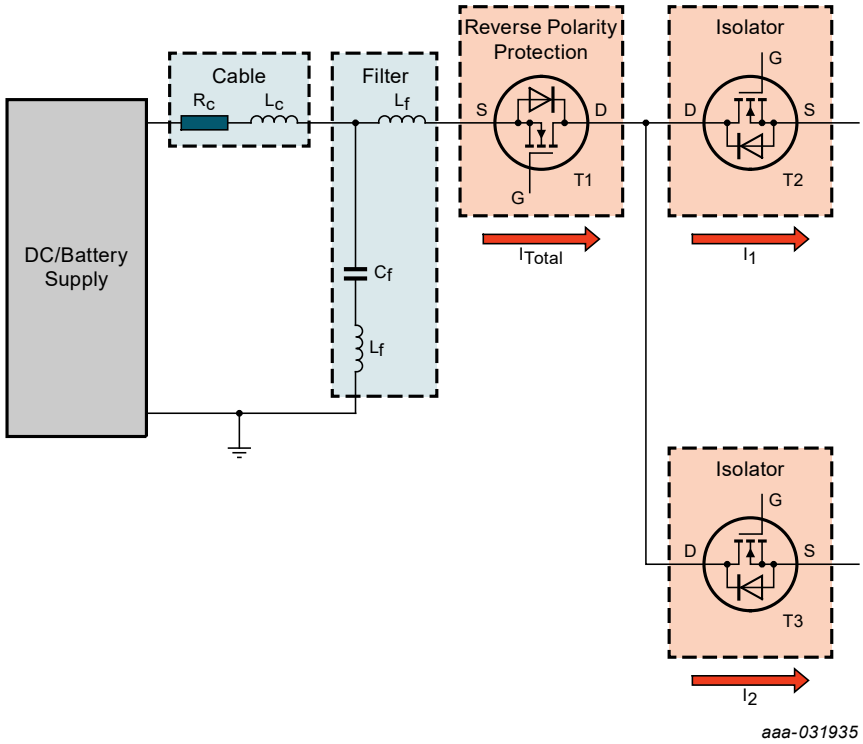


Fig. 13. Reverse polarity protection MOSFET T1

See Fig. 13 continuous current capability is of most relevance here as the MOSFET T1 is implemented on the supply line which allows the flow of all the current needed for the whole module on a continuous basis.

It can also be seen that current flows through T1 from the supply regardless of whether the MOSFET is ON or OFF – when MOSFET is OFF it will still conduct through its body diode. As such it is important to pay attention to I_S capability.

To avoid current flowing through MOSFET body diode some designs implement two MOSFETs back to back for reverse polarity protection, see Fig. 14.

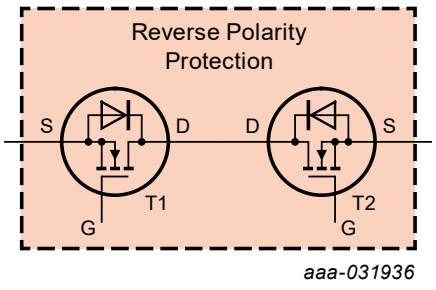


Fig. 14. Reverse polarity protection using back-to-back MOSFETs

In a back-to-back configuration the other parameter that becomes of relevance is the avalanche performance of the MOSFETs. A situation where a fault condition occurs and T2 turns off as part of a protection mechanism. Due to inductances in the cable and/or the circuit a build-up of a voltage at the drain of T2 might occur and potentially lead to an avalanche event. For details on avalanche topic see NEXPERIA application note *AN10273*.

Multiple MOSFET parameters are highlighted in the application examples given above, all showing the importance of, and the need to use a MOSFET that is capable of handling high continuous current.

7. Revision history

Table 7. Revision history

Revision number	Date	Description
1.1	2020-09-03	Typo corrected in Fig. 11.
1.0	2020-06-29	Initial version.

8. Legal information

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Date of release: 3 September 2020