AN90029

Pin FMEA for AXPnT family

Rev. 1 — 13 July 2021 application note

Document information

Information	Content
Keywords	FMEA, AXPnT, CMOS, 2.5 V/5 V systems
Abstract	This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia's AXPnT family under typical failure situations

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1. Introduction

The AXP translator family, is an Advanced eXtremely Low Voltage family, for high-performance low-voltage applications. Lowest power voltage translator solution offering the widest range of voltage translation from 0.7 V to 5.5 V. The AXP translators (AXPnT) are ideal for high performance applications with Microprocessors / Microcontrollers / ASICs operating at ultra-low voltages below 1.8 V that still need to interface with I/O peripheral solutions typically operating at 2.5 V, 3.3 V, or even 5.5 V.

2. AXPnT family overview

The AXPnT comprises two categories, one for standard buffers, inverters, gates and configurable functions and another category for transceiver part. Below are listed the key-features.

Features of AXPnT

Available in buffers, inverters, gates and configurable function

- Wide supply voltage range:
  - V_{CCI}: 0.7 V to 2.75 V
  - V_{CCO}: 1.2 V to 5.5 V
- Fully specified from -40 °C to +85 °C
- Very low static and dynamic power consumption
- Low noise overshoot and undershoot:
  - < 10% of V_{CCO}
- I_{OFF} circuitry provides partial power-down mode operation
- Inputs accept voltages up to 2.75 V
- High noise immunity
- Low input (C_I) and output (C_O) capacitance
- Fully specified at 0.7 V supply range
- Schmitt-trigger action on all inputs
- 8.0 mA balanced output drive
- Over-voltage tolerant I/Os up to 2.75 V
- Suspend mode
- t_{pd} of 2.6 ns at V_{CC} of 1.8 V
- Available in small footprint packages

Available in transceiver function

- Wide supply voltage range:
  - $V_{CC(A)}$: 0.9 V to 5.5 V
  - $V_{CC(B)}$: 0.9 V to 5.5 V
- Fully specified from -40 °C to +125 °C
- Low static and dynamic power consumption
- Low noise overshoot and undershoot:
  - < 10% of V_{CCO}
- I_{OFF} circuitry provides partial power-down mode operation
- Inputs accept voltages up to 5 V
- High noise immunity
- Low input (C_I) and output (C_O) capacitance
- Fully specified at 0.9 V supply range
- Schmitt-trigger action on all inputs
- 8.0 mA balanced output drive
- Over-voltage tolerant I/Os up to 5.5 V
- Suspend mode
- t_{pd} of 8.5 ns at V_{CC} of 1.8 V
- Available in small footprint packages

3. Pin FMEA

This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia's AXPnT family under typical failure situations such as a short-circuit to V_{CC} or GND or to a neighboring pin, or if a pin is left open.

A failure is classified according to its effect on the AXPnT device and the functionality of the application; see Table 1.

Table 1. Classification of failure effects

Class	Failure effect
A	damage to device
	affects application functionality
B	no damage to device
	may affect application functionality
C	no damage to device
	no affect to application functionality

Table 2. FMEA matrix for pin short-circuit to V_{CCI}

V_{CCI} is the supply voltage associated with the input port.

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality.
Output	A	if output defined LOW, short-circuits and high currents can damage device, output level changes.
Output	A	if output defined HIGH, short-circuits and high currents can damage device, output level changes.
GND	A	short-circuits and high currents can damage device, will affect functionality.

Table 3. FMEA matrix for pin short-circuit to V_{CCO}

V_{CCO} is the supply voltage associated with the output port.

Pin	Class	Remarks
Input	A	damage to device, no leakage, may affect functionality.
Output	C	if output defined HIGH, no damage, no leakage, no output level change.
Output	A	if output defined LOW, short-circuits and high currents can damage device, output level changes.
GND	A	short-circuits and high currents can damage device, will affect functionality.

Table 4. FMEA matrix for pin short-circuit to GND

V_{CCI} is the supply voltage associated with the input port.
V_{CCO} is the supply voltage associated with the output port.

Pin	Class	Remarks
Input	B	normal operating condition, no damage, no leakage, may affect functionality.
Output	C	if output defined LOW, no damage, no leakage, no output level change.
Output	A	if output defined HIGH, short-circuits and high currents can damage device, output level changes.
V_{CCI}	A	short-circuits and high currents can damage device, will affect functionality.
V_{CCO}	A	short-circuits and high currents can damage device, will affect functionality.

Table 5. FMEA matrix for pin left open

V_{CCI} is the supply voltage associated with the input port.
V_{CCO} is the supply voltage associated with the output port.

Pin	Class	Remarks
Input	B	undefined operating condition, no damage, increases leakage, may affect functionality.
Output	C	normal operating condition, no damage, no leakage.
GND	A	undefined operating condition, can damage device, increases leakage, will affect functionality.
V_{CCI}	B	undefined operating condition, no damage, increases leakage, will affect functionality.
V_{CCO}	B	undefined operating condition, no damage, will affect functionality.

Table 6. FMEA matrix for pin short-circuits between neighbor pins

V_{CCI} is the supply voltage associated with the input port.

V_{CCO} is the supply voltage associated with the output port.

Pin	Class	Remarks
Input to input	C	if inputs have same voltage levels: no damage, no leakage.
	B	if inputs have different voltage levels: leakage increases, will affect functionality.
Input to output	A	if input and output have different voltage levels, can cause high current and can damage device, will affect functionality.
	C	if input and output have same voltage levels, no damage, no leakage.
Input to GND	-	see Table 4
Input to V_{CCI}	-	see Table 2
Input to V_{CCO}	-	see Table 3
Output to output	C	if outputs have same voltage levels, no damage, no leakage.
	A	if outputs have different voltage levels, can cause high current and can damage device, will affect functionality.
Output to input	-	same effect as 'Input to output' condition.
Output to GND	-	see Table 4
Output to V_{CCI}	-	see Table 2
Output to V_{CCO}	-	see Table 3
GND to V_{CCI}	-	see Table 2
GND to V_{CCO}	-	see Table 3

4. Revision history

Table 7. Revision history

Rev	Date	Description
AN90029 v.1	20210713	AN90029 initial version

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